

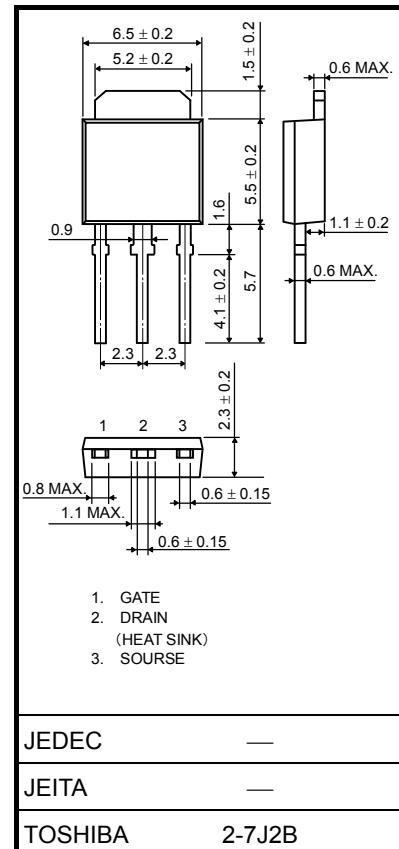
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSVII)

TK2Q60D

Switching Regulator Applications

Unit: mm

- Low drain-source ON-resistance: $R_{DS(ON)} = 3.2 \Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 1.0 \text{ S}$ (typ.)
- Low leakage current: $I_{DSS} = 10 \mu\text{A}$ (max) ($V_{DS} = 600 \text{ V}$)
- Enhancement mode: $V_{th} = 2.4$ to 4.4 V ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)



Weight: 0.36 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Thermal Characteristics

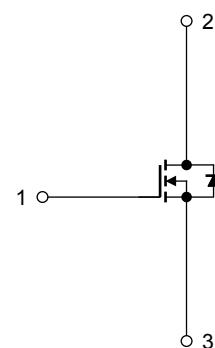
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	R_{th} (ch-c)	2.08	$^{\circ}\text{C/W}$
Thermal resistance, channel to ambient	R_{th} (ch-a)	125	$^{\circ}\text{C/W}$

Note 1: Ensure that the channel temperature does not exceed 150°C .

Note 2: $V_{DD} = 90 \text{ V}$, $T_{ch} = 25^{\circ}\text{C}$ (initial), $L = 44.1 \text{ mH}$, $R_G = 25\Omega$, $I_{AR} = 2 \text{ A}$

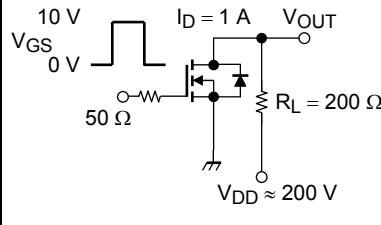
Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.



Start of commercial production
2009-03

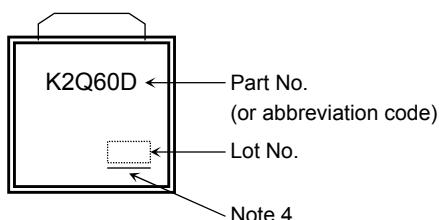
Electrical Characteristics ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Gate leakage current	I_{GSS}	$V_{GS} = \pm 30\text{ V}$, $V_{DS} = 0\text{ V}$	—	—	± 1	μA	
Drain cut-off current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$	—	—	10	μA	
Drain-source breakdown voltage	$V_{(BR) DSS}$	$I_D = 10\text{ mA}$, $V_{GS} = 0\text{ V}$	600	—	—	V	
Gate threshold voltage	V_{th}	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$	2.4	—	4.4	V	
Drain-source ON resistance	$R_{DS (\text{ON})}$	$V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$	—	3.2	4.3	Ω	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ A}$	0.3	1.0	—	S	
Input capacitance	C_{iss}	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	—	280	—	pF	
Reverse transfer capacitance	C_{rss}		—	1.5	—		
Output capacitance	C_{oss}		—	30	—		
Switching time	Rise time	t_r	 V_{GS} 10 V V_{GS} 0 V 50 Ω $I_D = 1\text{ A}$ V_{OUT} $V_{DD} \approx 200\text{ V}$ Duty $\leq 1\%$, $t_w = 10\text{ }\mu\text{s}$	—	15	—	ns
	Turn-on time	t_{on}		—	35	—	
	Fall time	t_f		—	7	—	
	Turn-off time	t_{off}		—	55	—	
Total gate charge	Q_g	$V_{DD} \approx 400\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 2\text{ A}$	—	7	—	nC	
Gate-source charge	Q_{gs}		—	4	—		
Gate-drain charge	Q_{gd}		—	3	—		

Source-Drain Ratings and Characteristics ($T_a = 25^\circ\text{C}$)

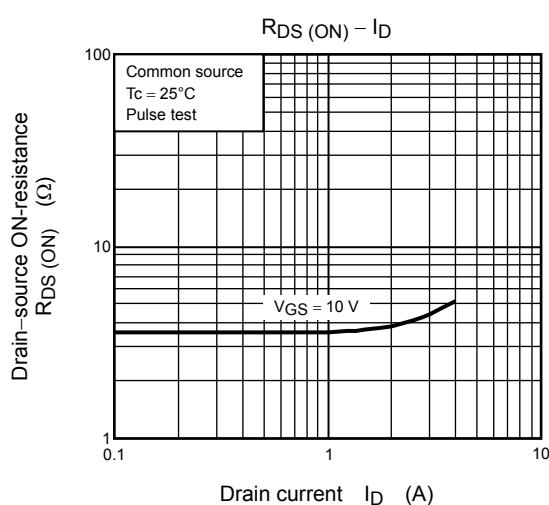
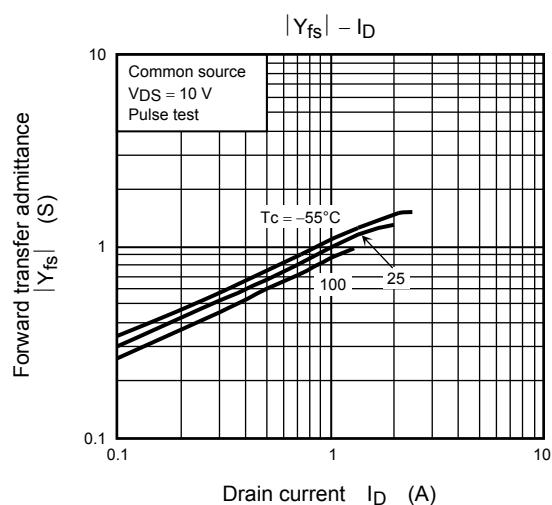
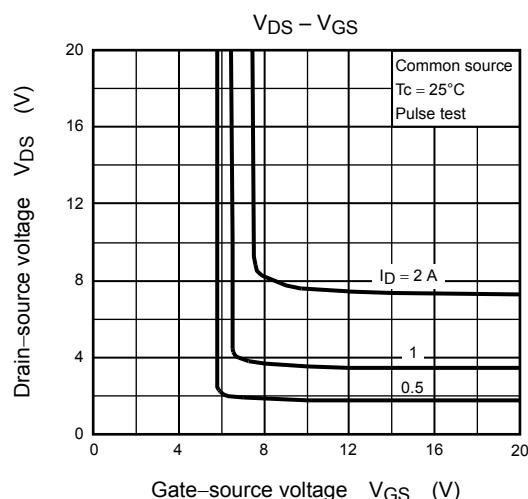
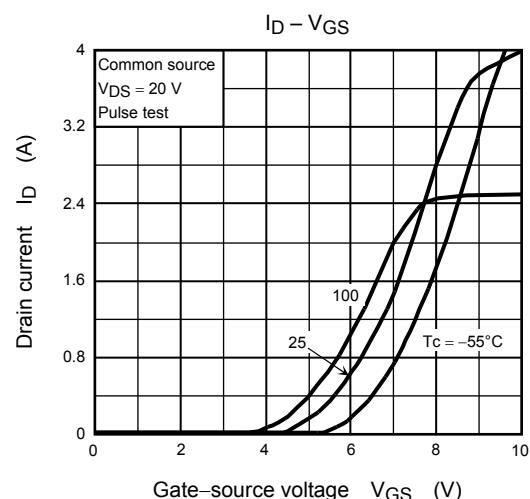
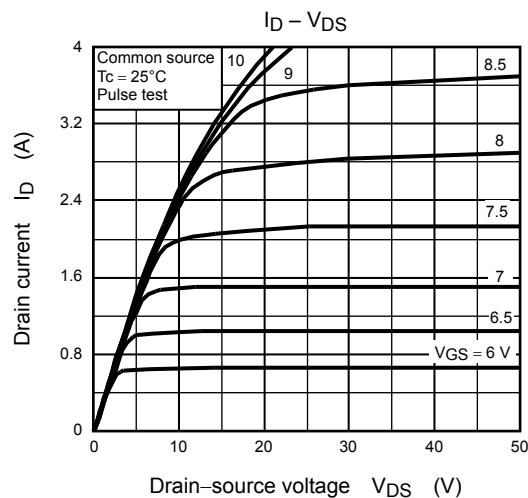
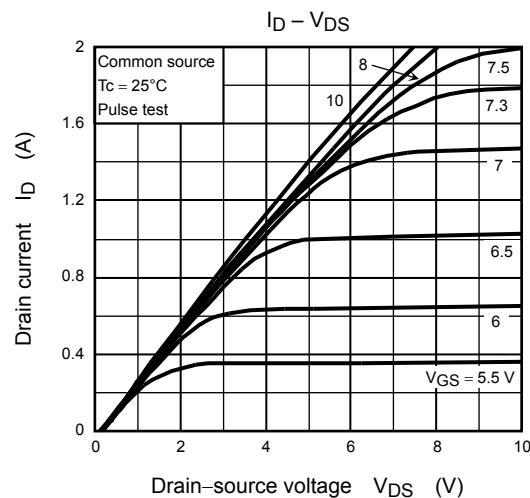
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	2	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	8	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 2\text{ A}$, $V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 2\text{ A}$, $V_{GS} = 0\text{ V}$, $dI_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	550	—	ns
Reverse recovery charge	Q_{rr}		—	2.2	—	μC

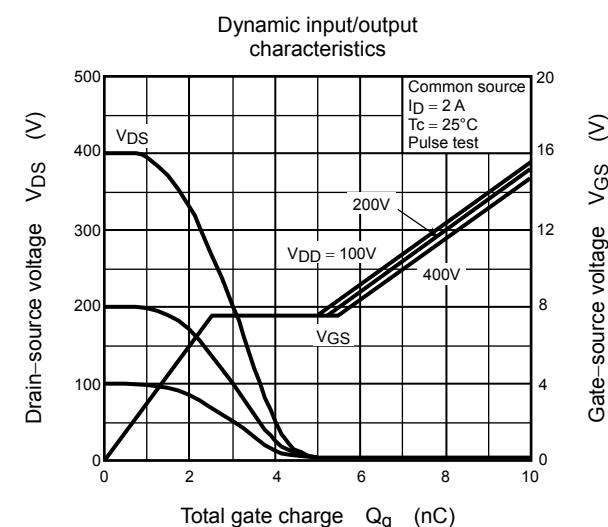
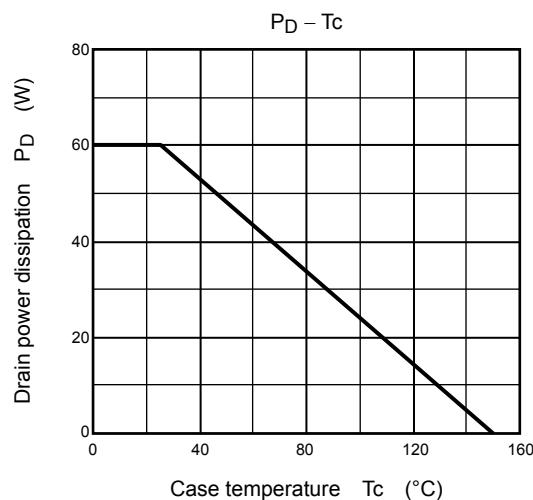
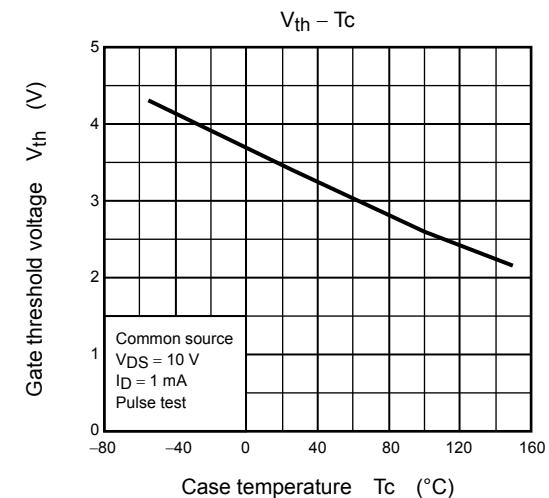
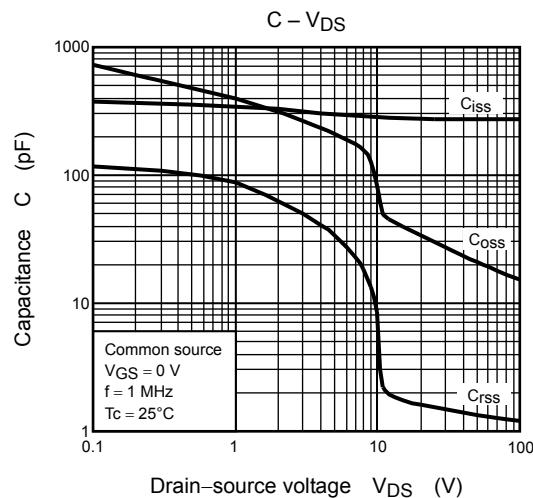
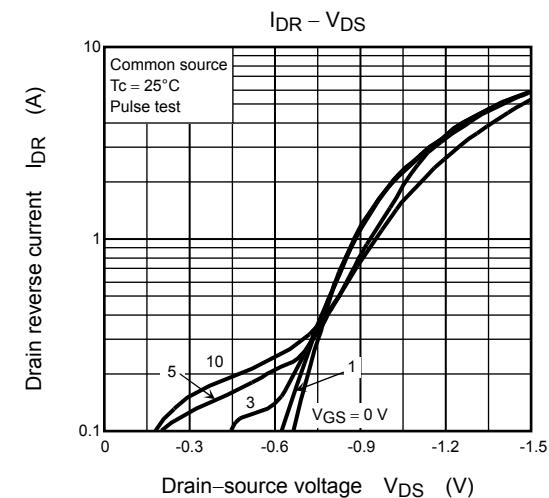
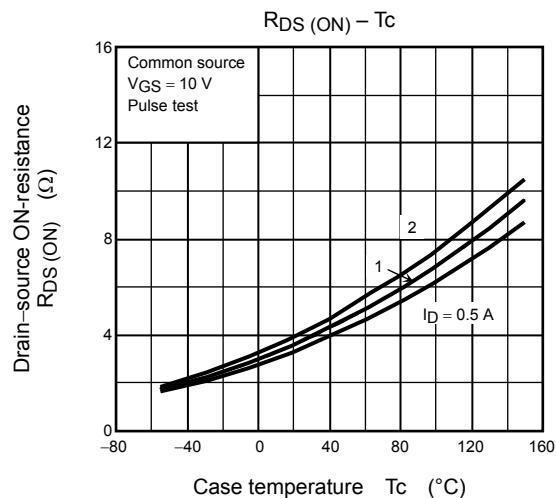
Marking

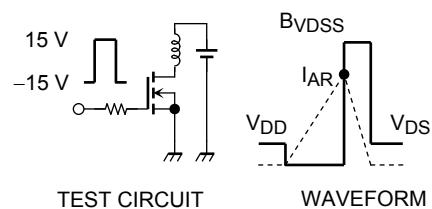
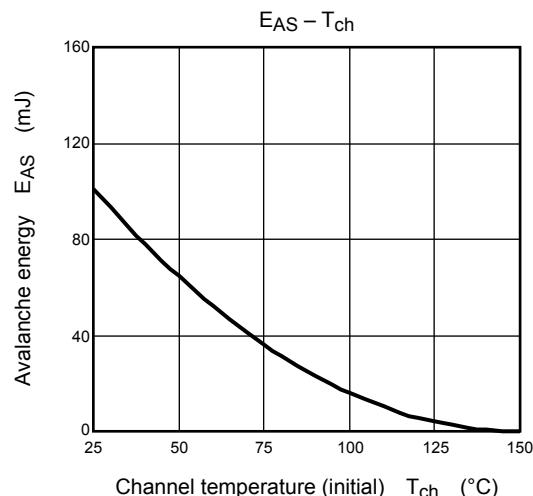
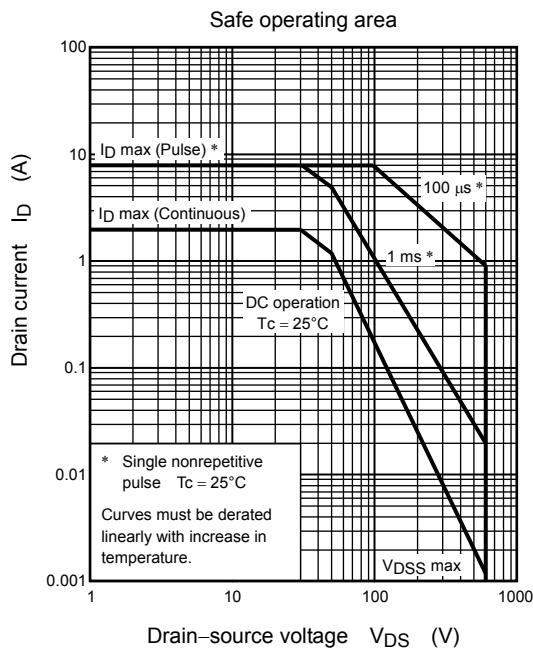
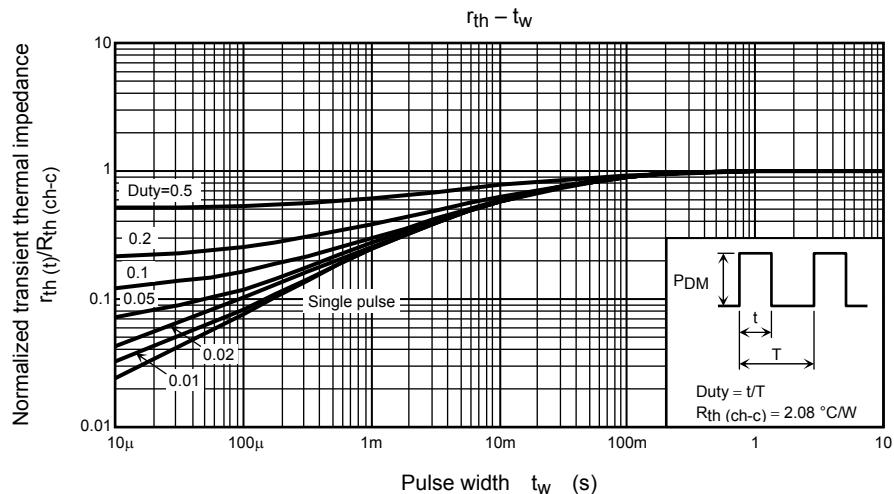


Note 4 : A line under a Lot No. identifies the indication of product Labels
[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

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$$R_G = 25 \Omega$$

$$V_{DD} = 90 \text{ V}, L = 44.1 \text{ mH}$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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