



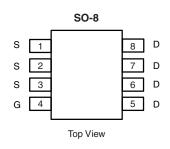
# N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)			
30	0.011 at V <sub>GS</sub> = 10 V	12			
	0.016 at V <sub>GS</sub> = 4.5 V	9.8			

### **FEATURES**

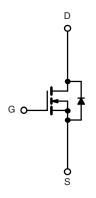
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> Tested





Ordering Information: Si4894BDY-T1-E3 (Lead (Pb)-free)

Si4894BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T <sub>A</sub> = 25 °C, unle	ss otherwise r	noted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		$V_{DS}$	30		V
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Comment /T 150 90\8	T <sub>A</sub> = 25 °C	I <sub>D</sub> 12 9.5	8.9		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C		9.5	7.1	l
Pulsed Drain Current		I <sub>DM</sub>	40		Α
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	2.3	1.3	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	I <sub>AS</sub> 20 E <sub>AS</sub> 20		
Avalanche Energy	L = 0.1 IIII	E <sub>AS</sub>			mJ
M	T <sub>A</sub> = 25 °C	В	2.5 1.4		W
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	$P_{D}$	1.6	0.9	VV
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Mariana la Ambianta	t ≤ 10 s	R <sub>thJA</sub>	43	50		
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	□thJA	73	90	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	19	25		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

## Vishay Siliconix



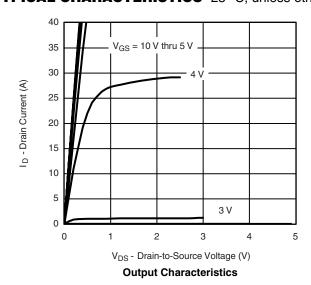
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$			3.0	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtaga Drain Current	1	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
	В	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A	0.009 0.011		0.011		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 9.8 \text{ A}$		0.013	0.016	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 12 A		32		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = 2.3 A, V <sub>GS</sub> = 0 V		0.76	1.1	V	
Dynamic <sup>b</sup>			<u>'</u>				
Input Capacitance	C <sub>iss</sub>			1580		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		295			
Reverse Transfer Capacitance	C <sub>rss</sub>			140			
Total Gate Charge	Q <sub>q</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 12 \text{ A}$		13.2	20	nC	
Total Gate Charge	<b>∢</b> g			25.4	38		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 12 \text{ A}$		5.3			
Gate-Drain Charge	$Q_{gd}$			4.3			
Gate Resistance	$R_{g}$		0.9	1.8	2.7	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			13	20		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$		10	15		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong$ 1 A, $V_{GEN}$ = 10 V, $R_g$ = 6 $\Omega$		33	50	ns	
Fall Time	t <sub>f</sub>			10	15		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.3 A, dI/dt = 100 A/μs		25	40		

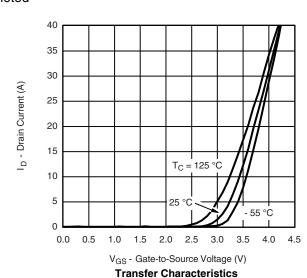
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

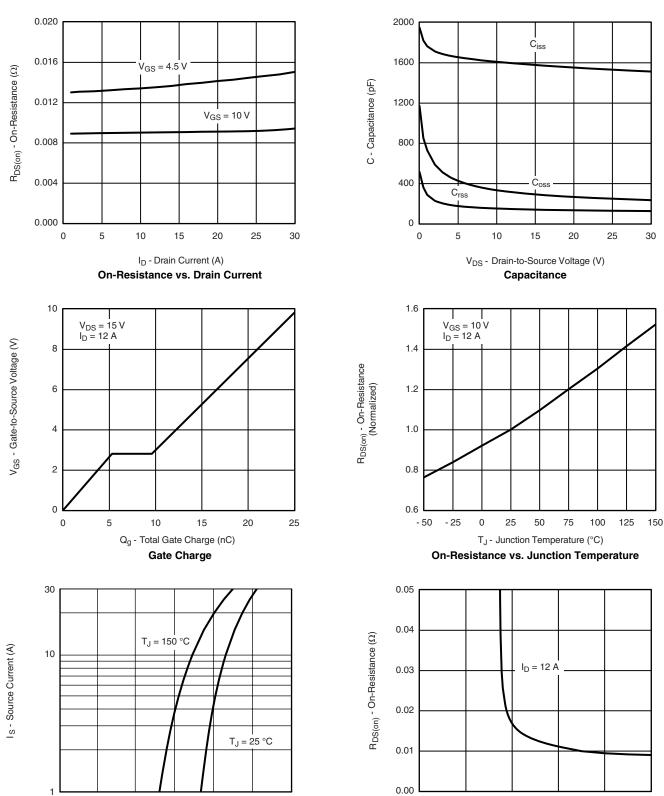








### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



0.0

0.2

0.4

0.6

 $V_{SD}$  - Source-to-Drain Voltage (V)

Source-Drain Diode Forward Voltage

0.8

1.0

1.2

0

2

8

6

V<sub>GS</sub> - Gate-to-Source Voltage (V)

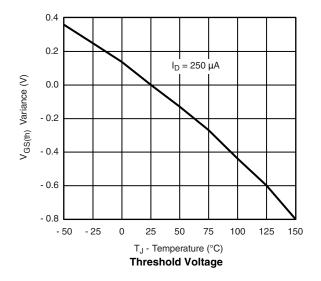
On-Resistance vs. Gate-to-Source Voltage

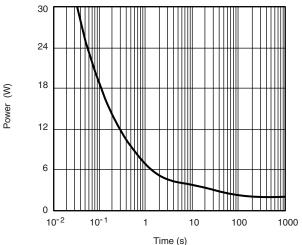
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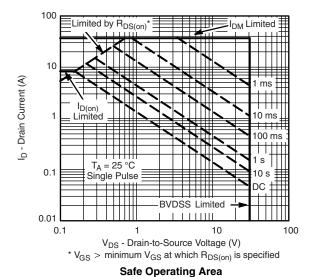
# VISHAY

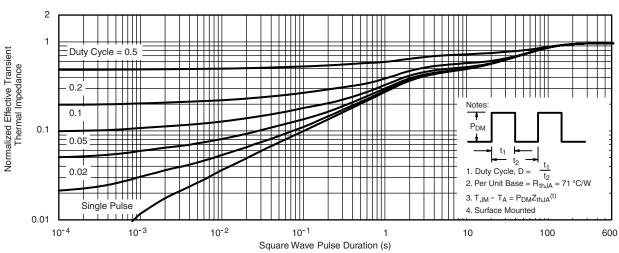
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





Single Pulse Power, Junction-to-Ambient

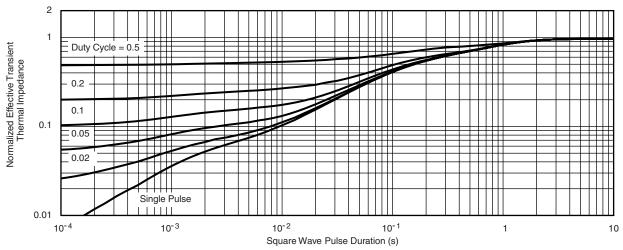




Normalized Thermal Transient Impedance, Junction-to-Ambient



### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

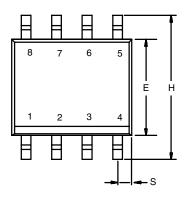


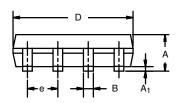
Normalized Thermal Transient Impedance, Junction-to-Foot

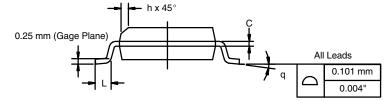
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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







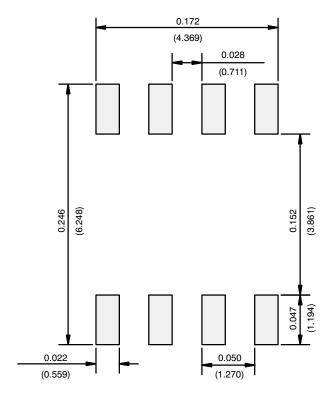
	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
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DWG: 5498

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### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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