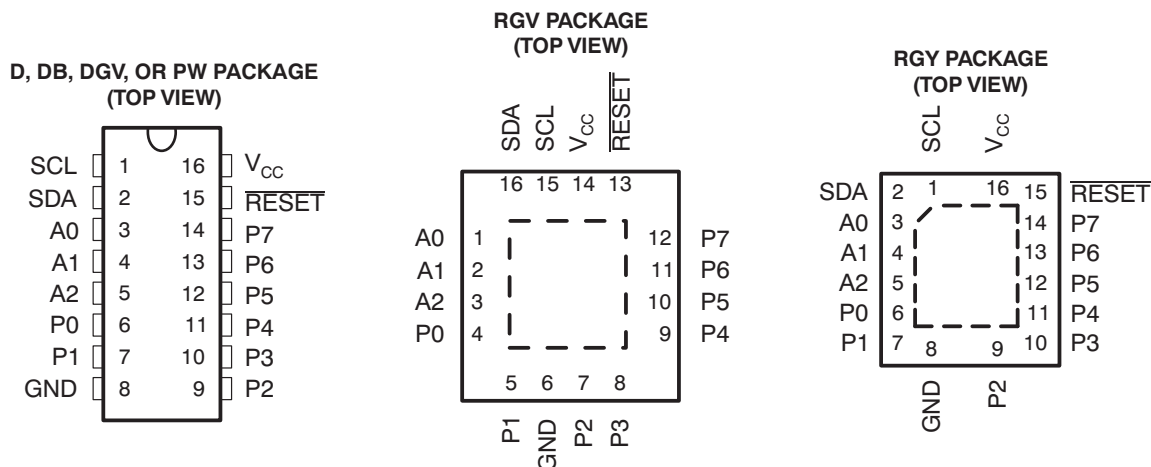


REMOTE 8-BIT I²C AND SMBus LOW-POWER I/O EXPANDER WITH RESET AND CONFIGURATION REGISTERS

FEATURES

- Low Standby Current Consumption of 1 μ A Max
- I²C to Parallel Port Expander
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I²C Bus
- Three Hardware Address Pins Allow for Use of up to Eight Devices on I²C/SMBus
- Lower-Voltage Higher-Performance Migration Path for PCA9556
- Input/Output Configuration Register
- Polarity Inversion Register
- Active-Low Reset Input
- Internal Power-On Reset
- High-Impedance Open Drain on P0
- Power Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This 8-bit I/O expander for the two-line bidirectional bus (I²C) is designed for 2.3-V to 5.5-V V_{CC} operation. The device provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface [serial clock (SCL) and serial data (SDA)].

The PCA9557 consists of one 8-bit configuration (input or output selection), input port, output port, and polarity inversion (active-high) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the input port register can be inverted with the polarity inversion register. All registers can be read by the system master.

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The system master can reset the PCA9557 in the event of a timeout or other improper operation by asserting a low in the active-low reset ($\overline{\text{RESET}}$) input. The power-on reset puts the registers in their default state and initializes the I²C/SMBus state machine. Asserting $\overline{\text{RESET}}$ causes the same reset/initialization to occur without depowering the part.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I²C address, allowing up to eight devices to share the same I²C bus or SMBus.

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGV | Reel of 2000 | PCA9557RGVR | PD557 |
| | QFN – RGY | Reel of 1000 | PCA9557RGYR | PD557 |
| | SOIC – D | Reel of 2500 | PCA9557DR | PCA9557 |
| | | Reel of 250 | PCA9557DT | |
| | | Tube of 40 | PCA9557D | |
| | SSOP – DB | Reel of 2000 | PCA9557DBR | PD557 |
| | | Tube of 80 | PCA9557DB | |
| | TSSOP – PW | Reel of 2000 | PCA9557PWR | PD557 |
| | | Reel of 250 | PCA9557PWT | |
| | | Tube of 90 | PCA9557PW | |
| | TVSOP – DGV | Reel of 2000 | PCA9557DGV | PD557 |

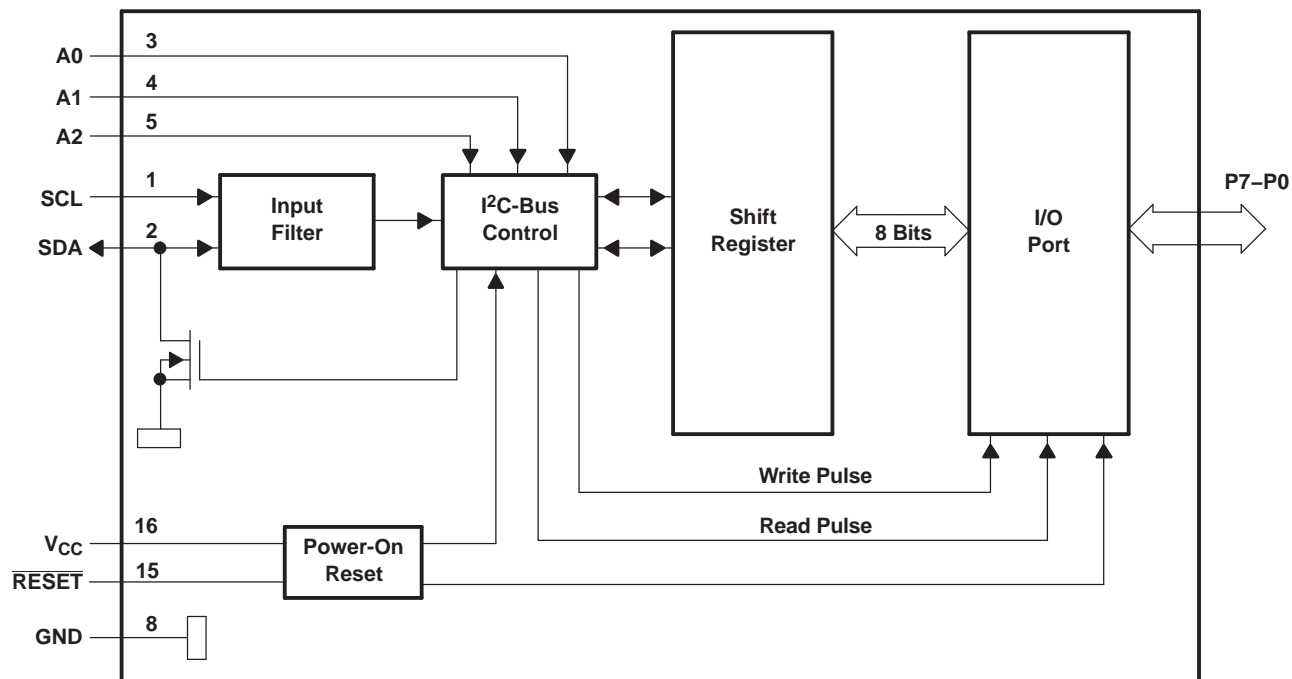
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TERMINAL FUNCTIONS

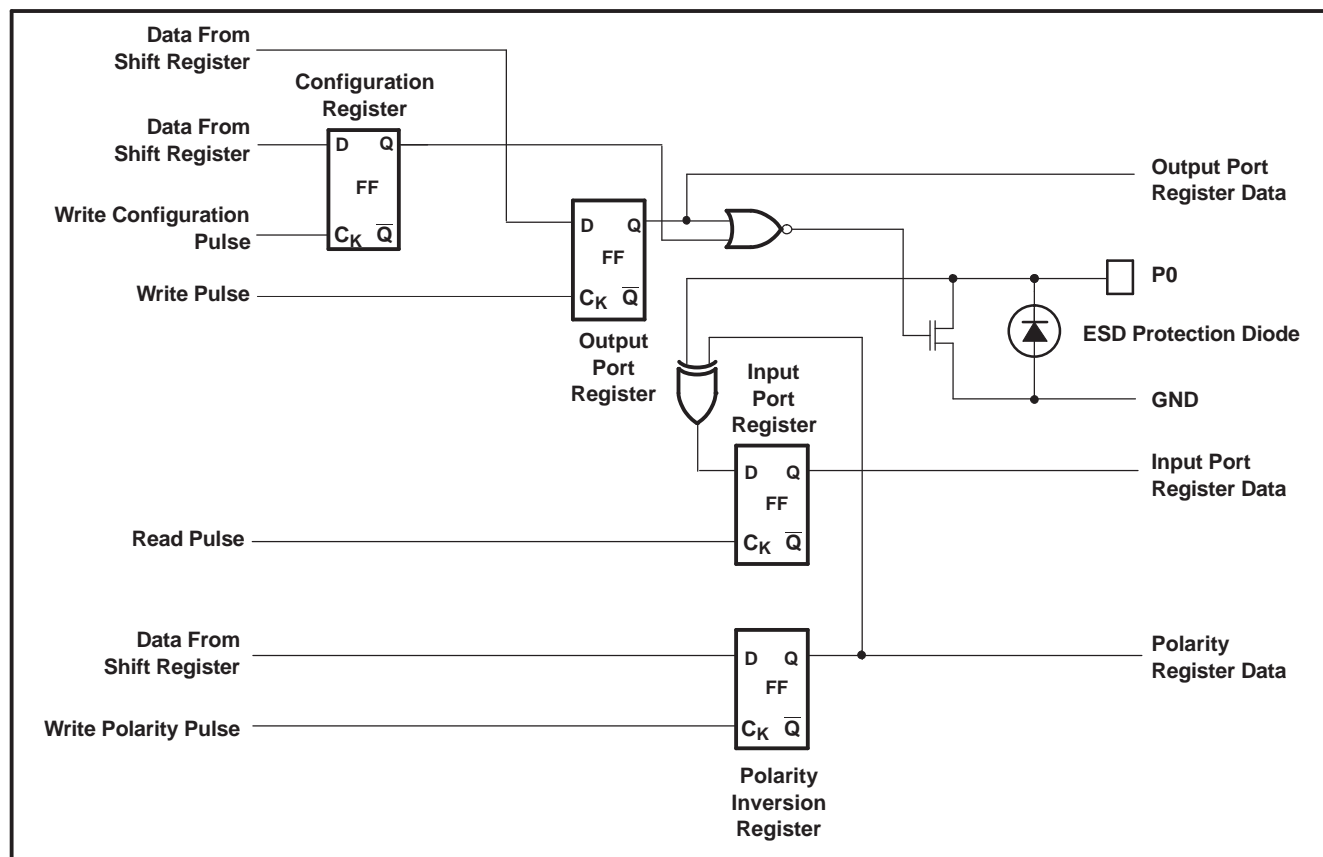
| NO. | | NAME | DESCRIPTION |
|--|-----------|---------------------------|--|
| QFN (RGY), SOIC (D), SSOP (DB), TSSOP (PW), AND TVSOP (DGV) | QFN (RGV) | | |
| 1 | 15 | SCL | Serial clock bus. Connect to V _{CC} through a pullup resistor. |
| 2 | 16 | SDA | Serial data bus. Connect to V _{CC} through a pullup resistor. |
| 3 | 1 | A0 | Address input. Connect directly to V _{CC} or ground. |
| 4 | 2 | A1 | Address input. Connect directly to V _{CC} or ground. |
| 5 | 3 | A2 | Address input. Connect directly to V _{CC} or ground. |
| 6 | 4 | P0 | P-port input/output. High impedance open-drain design structure. Connect to V _{CC} through a pullup resistor. |
| 7 | 5 | P1 | P-port input/output. Push-pull design structure. |
| 8 | 6 | GND | Ground |
| 9 | 7 | P2 | P-port input/output. Push-pull design structure. |
| 10 | 8 | P3 | P-port input/output. Push-pull design structure. |
| 11 | 9 | P4 | P-port input/output. Push-pull design structure. |
| 12 | 10 | P5 | P-port input/output. Push-pull design structure. |
| 13 | 11 | P6 | P-port input/output. Push-pull design structure. |
| 14 | 12 | P7 | P-port input/output. Push-pull design structure. |
| 15 | 13 | $\overline{\text{RESET}}$ | Active-low reset input. Connect to V _{CC} through a pullup resistor if no active connection is used. |
| 16 | 14 | V _{CC} | Supply voltage |

LOGIC DIAGRAM (POSITIVE LOGIC)



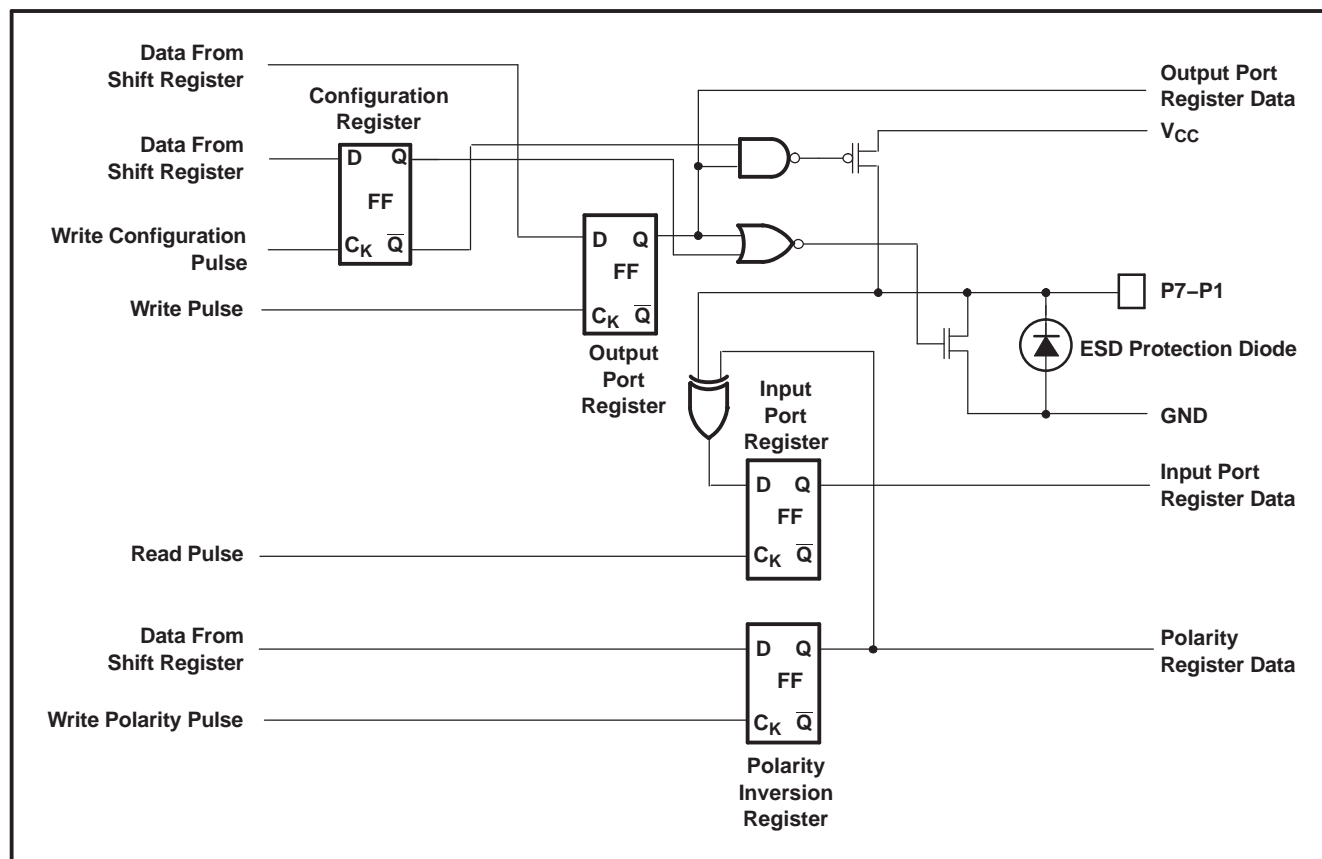
- A. Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.
- B. All I/Os are set to inputs at reset.

SIMPLIFIED SCHEMATIC DIAGRAM OF P0



A. On power up or reset, all registers return to default values.

SIMPLIFIED SCHEMATIC DIAGRAM OF P7–P1



A. On power up or reset, all registers return to default values.

I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (A2–A0) inputs of the slave device must not be changed between the start and the stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 2).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

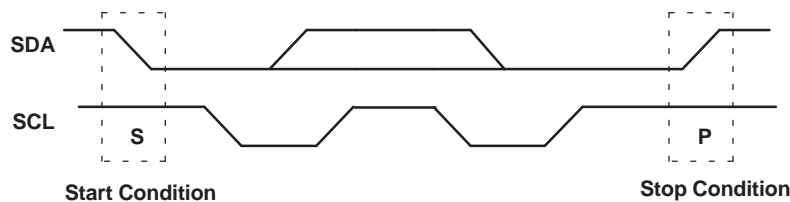


Figure 1. Definition of Start and Stop Conditions

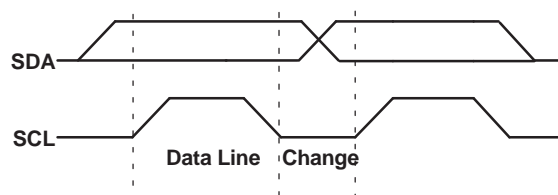


Figure 2. Bit Transfer

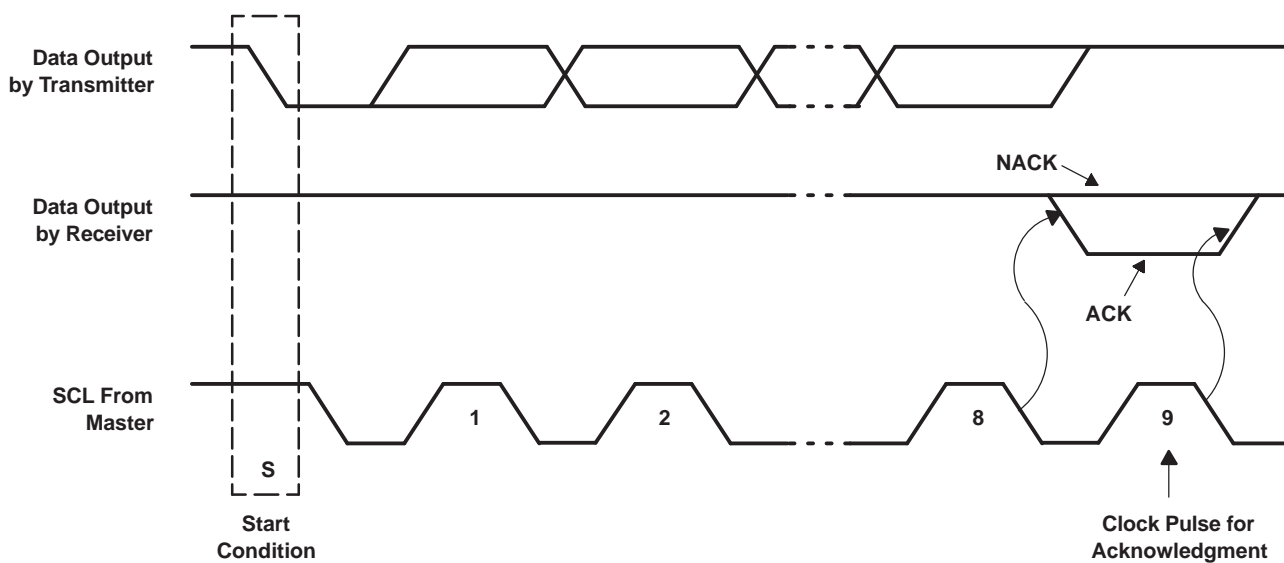


Figure 3. Acknowledgment on the I²C Bus

Interface Definition

| BYTE | BIT | | | | | | | |
|-------------------|---------|----|----|----|----|----|----|---------|
| | 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
| I²C slave address | L | L | H | H | A2 | A1 | A0 | R/W |
| Px I/O data bus | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Device Address

The address of the PCA9557 is shown in [Figure 4](#).

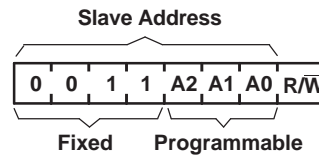


Figure 4. PCA9557 Address

Address Reference

| INPUTS | | | I ² C BUS SLAVE ADDRESS |
|--------|----|----|------------------------------------|
| A2 | A1 | A0 | |
| L | L | L | 24 (decimal), 18 (hexadecimal) |
| L | L | H | 25 (decimal), 19 (hexadecimal) |
| L | H | L | 26 (decimal), 1A (hexadecimal) |
| L | H | H | 27 (decimal), 1B (hexadecimal) |
| H | L | L | 28 (decimal), 1C (hexadecimal) |
| H | L | H | 29 (decimal), 1D (hexadecimal) |
| H | H | L | 30 (decimal), 1E (hexadecimal) |
| H | H | H | 31 (decimal), 1F (hexadecimal) |

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9557. Two bits of this data byte state the operation (read or write) and the internal registers (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a new command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

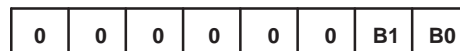


Figure 5. Control Register Bits

Command Byte

| CONTROL REGISTER BITS | | COMMAND BYTE (HEX) | REGISTER | PROTOCOL | POWER-UP DEFAULT |
|-----------------------|----|-----------------------|--------------------|-----------------|---------------------|
| B1 | B0 | | | | |
| 0 | 0 | 0x00 | Input Port | Read byte | xxxx xxxx |
| 0 | 1 | 0x01 | Output Port | Read/write byte | 0000 0000 |
| 1 | 0 | 0x02 | Polarity Inversion | Read/write byte | 1111 0000 |
| 1 | 1 | 0x03 | Configuration | Read/write byte | 1111 1111 |

Register Descriptions

The input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to signal the I²C device that the input port register will be accessed next.

Register 0 (Input Port Register)

| BIT | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | X | X | X | X | X | X | X | X |

The output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Register 1 (Output Port Register)

| BIT | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Register 2 (Polarity Inversion Register)

| BIT | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

The configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Register 3 (Configuration Register)

| BIT | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Power-On Reset

When power (from 0 V) is applied to V_{CC} , an internal power-on reset holds the PCA9557 in a reset condition until V_{CC} has reached V_{POR} . At that time, the reset condition is released, and the PCA9557 registers and I²C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle. The \overline{RESET} input can be asserted to reset the system, while keeping the V_{CC} at its operating level.

RESET

A reset can be accomplished by holding the \overline{RESET} pin low for a minimum of t_W . The PCA9557 registers and I²C/SMBus state machine are held in their default states until \overline{RESET} again is high. This input requires a pullup resistor to V_{CC} if no active connection is used.

Bus Transactions

Data is exchanged between the master and PCA9557 through write and read commands.

Writes

Data is transmitted to the PCA9557 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see [Figure 4](#) for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission (see [Figure 6](#) and [Figure 7](#)).

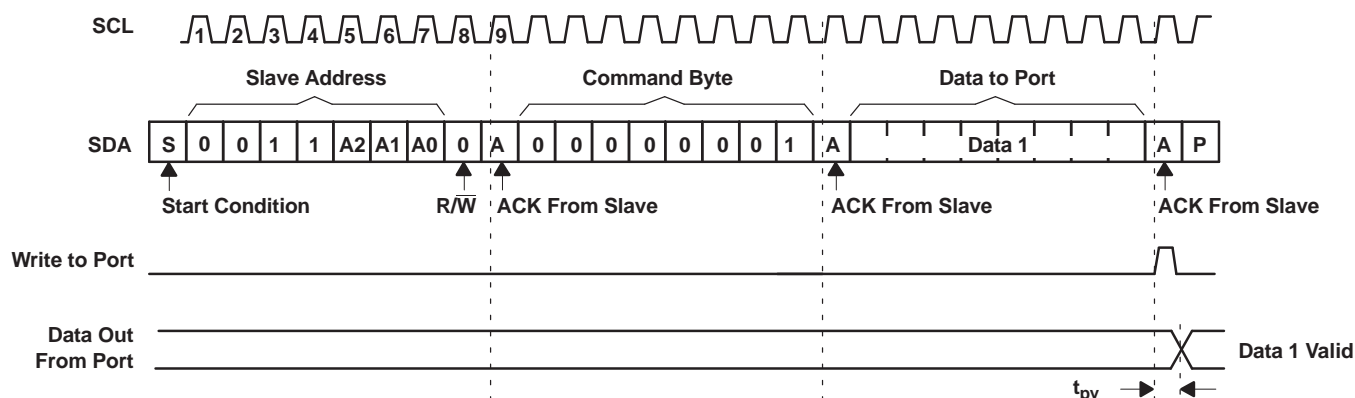


Figure 6. Write to Output Port Register

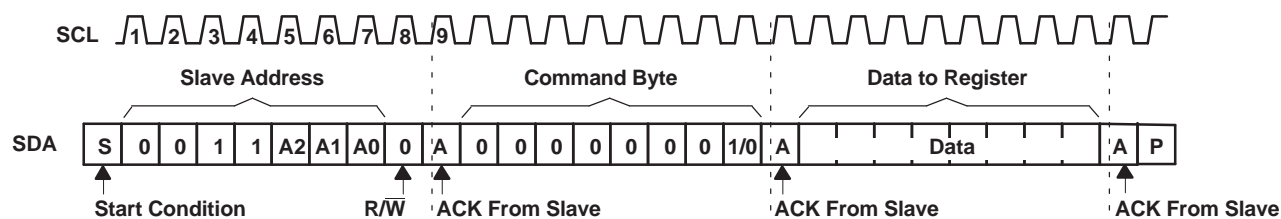


Figure 7. Write to Configuration or Polarity Inversion Registers

Reads

The bus master first must send the PCA9557 address with the LSB set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9557 (see Figure 8 and Figure 9). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

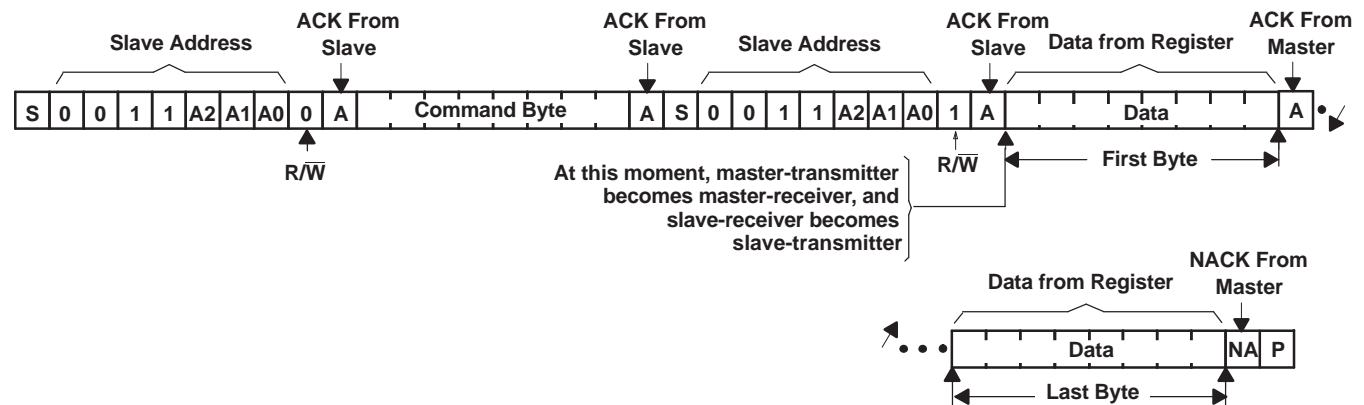
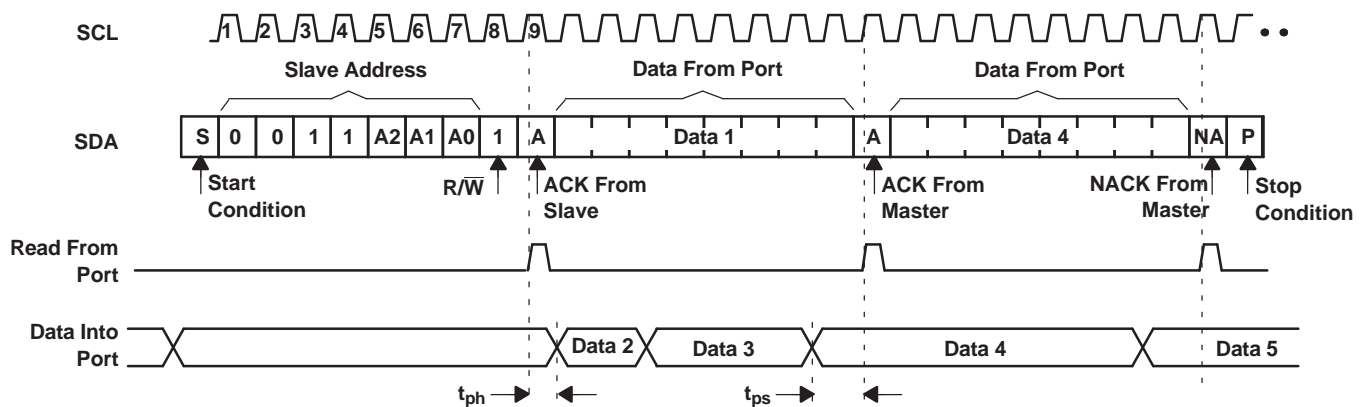


Figure 8. Read From Register



- This figure assumes the command byte has been previously programmed with 00h.
- Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.
- This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 8).

Figure 9. Read Input Port Register

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|--|-----------------------------|------|------|
| V_{CC} | Supply voltage range | –0.5 | 6 | V |
| V_I | Input voltage range ⁽²⁾ | –0.5 | 6 | V |
| V_O | Output voltage range ⁽²⁾ | –0.5 | 6 | V |
| I_{IK} | Input clamp current | $V_I < 0$ | –20 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | –20 | mA |
| I_{IOK} | Input/output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | –20 | μA |
| I_{OL} | Continuous output low current | $V_O = 0$ to V_{CC} | 50 | mA |
| I_{OH} | Continuous output high current | $V_O = 0$ to V_{CC} | –50 | mA |
| I_{CC} | Continuous current through GND | | –250 | mA |
| | Continuous current through V_{CC} | | 160 | |
| θ_{JA} | Package thermal impedance ⁽³⁾ | D package | 73 | °C/W |
| | | DB package | 82 | |
| | | DGV package | 120 | |
| | | PW package | 108 | |
| | | RGV package | 51 | |
| | | RGY package | 47 | |
| T_{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JEDEC 51-7.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|----------|--------------------------------|----------------------------------|----------------------------|------|
| V_{CC} | Supply voltage | 2.3 | 5.5 | V |
| V_{IH} | High-level input voltage | SCL, SDA | $0.7 \times V_{CC}$ | V |
| | | A2–A0, P7–P0, \overline{RESET} | 2 | |
| V_{IL} | Low-level input voltage | SCL, SDA | -0.5 $0.3 \times V_{CC}$ | V |
| | | A2–A0, P7–P0, \overline{RESET} | –0.5 | |
| I_{OH} | High-level output current | P7–P1 | –10 | mA |
| I_{OL} | Low-level output current | P7–P0 | 25 | mA |
| T_A | Operating free-air temperature | –40 | 85 | °C |

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|---|--|------------------|------|--------------------|-----|------|
| V _{IK} | Input diode clamp voltage | I _I = –18 mA | 2.3 V to 5.5 V | –1.2 | | | V |
| V _{POR} | Power-on reset voltage | V _I = V _{CC} or GND, I _O = 0 | V _{POR} | | 1.65 | 2.1 | V |
| V _{OH} | P-port high-level output voltage ⁽²⁾ | I _{OH} = –8 mA | 2.3 V | 1.8 | | | V |
| | | | 3 V | 2.6 | | | |
| | | | 4.5 V | 3 | | | |
| | | | 4.75 V | 4.1 | | | |
| | | I _{OH} = –10 mA | 2.3 V | 1.5 | | | |
| | | | 3 V | 2.5 | | | |
| | | | 4.5 V | 3 | | | |
| | | | 4.75 V | 4 | | | |
| I _{OL} | SDA | V _{OL} = 0.4 V | 2.3 V to 5.5 V | 3 | | | mA |
| | P port ⁽³⁾ | V _{OL} = 0.5 V | | 8 | 20 | | |
| | | V _{OL} = 0.55 V | 2.3 V to 5.5 V | 8 | 20 | | |
| | | V _{OL} = 0.7 V | | 10 | 24 | | |
| I _{OH} | P port, except for P0 ⁽³⁾ | V _{OH} = 2.3 V | 2.3 V to 5.5 V | –4 | | | mA |
| | P0 ⁽³⁾ | V _{OH} = 4.6 V | 4.6 V to 5.5 V | | | 1 | μA |
| | | V _{OH} = 3.3 V | 3.3 V to 5.5 V | | | 1 | |
| I _I | SCL, SDA | V _I = V _{CC} or GND | 2.3 V to 5.5 V | | | ±1 | μA |
| | A2–A0, RESET | | | | | ±1 | |
| I _{IH} | P port | V _I = V _{CC} | 2.3 V to 5.5 V | | | 1 | μA |
| I _{IL} | P port | V _I = GND | 2.3 V to 5.5 V | | | 1 | μA |
| I _{CC} | Operating mode | V _I = V _{CC} or GND, I _O = 0, I/O = inputs, f _{SCL} = 400 kHz | 5.5 V | | 19 | 25 | μA |
| | | | 3.6 V | | 12 | 22 | |
| | | | 2.7 V | | 8 | 20 | |
| | | V _I = V _{CC} or GND, I _O = 0, I/O = inputs, f _{SCL} = 100 kHz | 5.5 V | | 1.5 | 5 | |
| | | | 3.6 V | | 1 | 4 | |
| | | | 2.7 V | | 0.6 | 3 | |
| | Standby mode | V _I = V _{CC} or GND, I _O = 0, I/O = inputs, f _{SCL} = 0 kHz | 5.5 V | | 0.25 | 1 | |
| | | | 3.6 V | | 0.25 | 0.9 | |
| | | | 2.7 V | | 0.2 | 0.8 | |
| ΔI _{CC} | Additional current in Standby mode | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 2.3 V to 5.5 V | | | 0.2 | mA |
| | | Every LED I/O at V _I = 4.3 V, f _{SCL} = 0 kHz | 5.5 V | | | 0.4 | |
| C _I | SCL | V _I = V _{CC} or GND | 2.3 V to 5.5 V | | 4 | 6 | pF |
| C _{io} | SDA | V _{IO} = V _{CC} or GND | 2.3 V to 5.5 V | | 5.5 | 8 | pF |
| | P port | | | | 7.5 | 9.5 | |

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.

(2) The total current sourced by all I/Os must be limited to 85 mA per bit.

(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P7–P0) must be limited to a maximum current of 200 mA.

I²C INTERFACE TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 10](#))

| | | STANDARD MODE I ² C BUS | | FAST MODE I ² C BUS | | UNIT |
|-----------------------|--|---------------------------------------|------|---------------------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t _{scl} | I ² C clock frequency | 0 | 100 | 0 | 400 | kHz |
| t _{sch} | I ² C clock high time | 4 | | 0.6 | | μs |
| t _{scl} | I ² C clock low time | 4.7 | | 1.3 | | μs |
| t _{sp} | I ² C spike time | | 50 | | 50 | ns |
| t _{sds} | I ² C serial data setup time | 250 | | 100 | | ns |
| t _{sdh} | I ² C serial data hold time | 0 | | 0 | | ns |
| t _{icr} | I ² C input rise time | | 1000 | 20 + 0.1C _b ⁽¹⁾ | 300 | ns |
| t _{icf} | I ² C input fall time | | 300 | 20 + 0.1C _b ⁽¹⁾ | 300 | ns |
| t _{ocf} | I ² C output fall time, 10-pF to 400-pF bus | | 300 | 20 + 0.1C _b ⁽¹⁾ | 300 | ns |
| t _{buf} | I ² C bus free time between Stop and Start | 4.7 | | 1.3 | | μs |
| t _{sts} | I ² C Start or repeated Start condition setup time | 4.7 | | 0.6 | | μs |
| t _{sth} | I ² C Start or repeated Start condition hold time | 4 | | 0.6 | | μs |
| t _{sps} | I ² C Stop condition setup time | 4 | | 0.6 | | μs |
| t _{vd(data)} | Valid data time, SCL low to SDA output valid | | 1 | | 0.9 | μs |
| t _{vd(ack)} | Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low | | 1 | | 0.9 | μs |
| C _b | I ² C bus capacitive load | | 400 | | 400 | pF |

(1) C_b = total capacitance of one bus line in pF

RESET TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 13](#))

| | | STANDARD MODE I ² C BUS | | FAST MODE I ² C BUS | | UNIT |
|--------------------|-------------------------------------|---------------------------------------|-----|-----------------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t _W | Reset pulse duration ⁽¹⁾ | 16 | | 16 | | ns |
| t _{REC} | Reset recovery time | 0 | | 0 | | ns |
| t _{RESET} | Time to reset ⁽²⁾ | 400 | | 400 | | ns |

(1) A pulse duration of 16 ns minimum must be applied to $\overline{\text{RESET}}$ to return the PCA9557 to its default state.

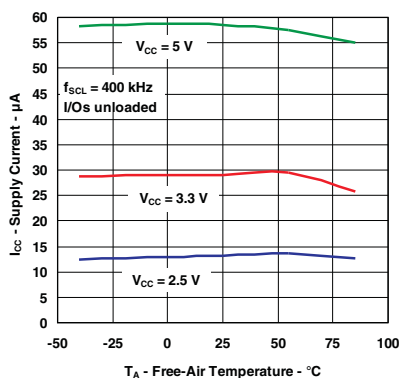
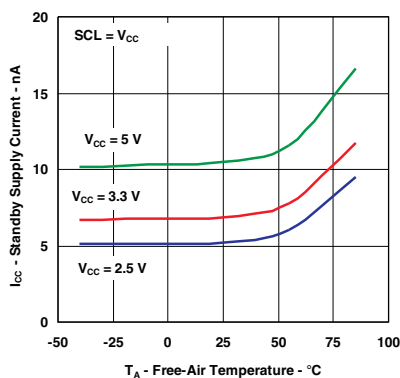
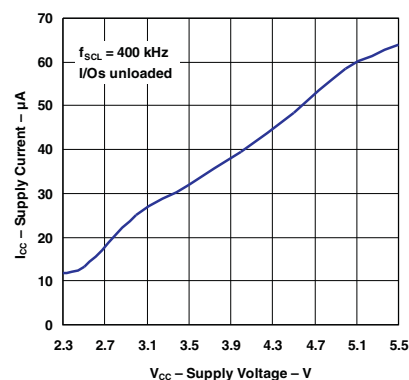
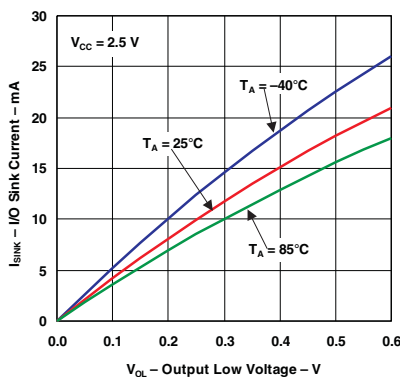
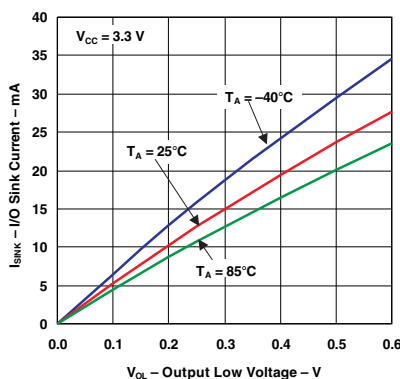
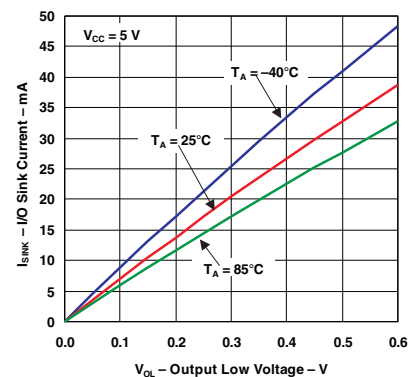
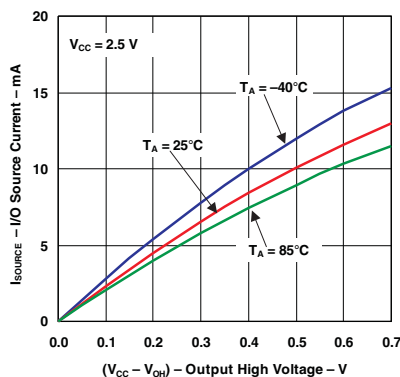
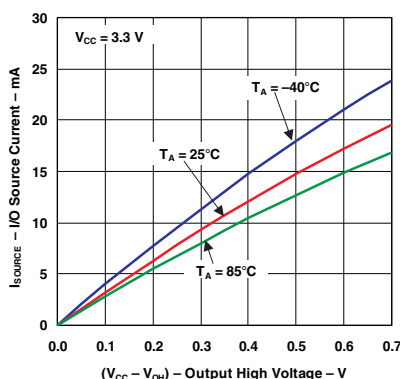
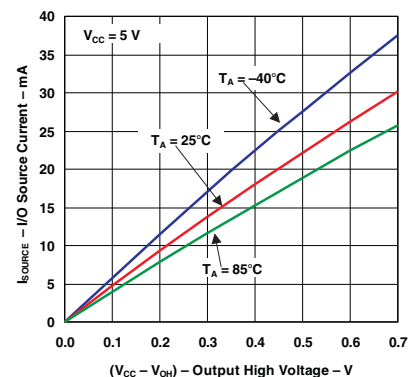
(2) The PCA9557 requires a minimum of 400 ns to be reset.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 10](#))

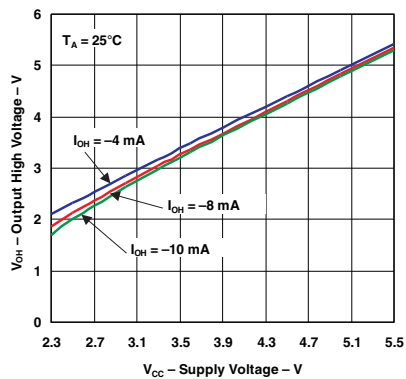
| PARAMETER | FROM | TO | STANDARD MODE I ² C BUS | | FAST MODE I ² C BUS | | UNIT |
|---------------------------------------|--------|-------|---------------------------------------|-----|-----------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{pv} Output data valid | SCL | P0 | | 250 | | 250 | ns |
| | SCL | P1–P7 | | 200 | | 200 | |
| t _{ps} Input data setup time | P port | SCL | 0 | | 0 | | ns |
| t _{ph} Input data hold time | P port | SCL | 200 | | 200 | | ns |

TYPICAL CHARACTERISTICS

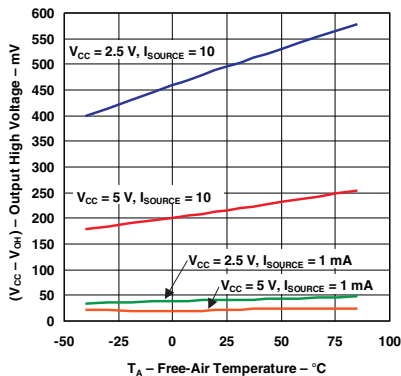
**SUPPLY CURRENT
VS
TEMPERATURE**

**STANDBY SUPPLY CURRENT
VS
TEMPERATURE**

**SUPPLY CURRENT
VS
SUPPLY VOLTAGE**

**I/O SINK CURRENT
VS
OUTPUT LOW VOLTAGE**

**I/O SINK CURRENT
VS
OUTPUT LOW VOLTAGE**

**I/O SINK CURRENT
VS
OUTPUT LOW VOLTAGE**

**I/O SOURCE CURRENT
VS
OUTPUT HIGH VOLTAGE
(P7–P1)**

**I/O SOURCE CURRENT
VS
OUTPUT HIGH VOLTAGE
(P7–P1)**

**I/O SOURCE CURRENT
VS
OUTPUT HIGH VOLTAGE
(P7–P1)**


TYPICAL CHARACTERISTICS (continued)

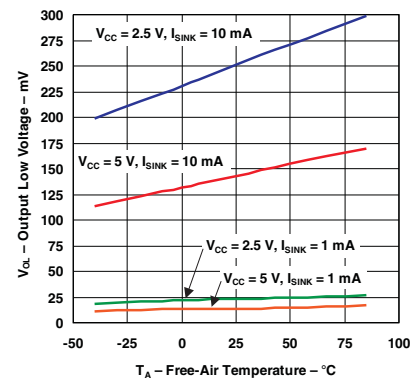
**OUTPUT HIGH VOLTAGE
vs
SUPPLY VOLTAGE
(P7–P1)**



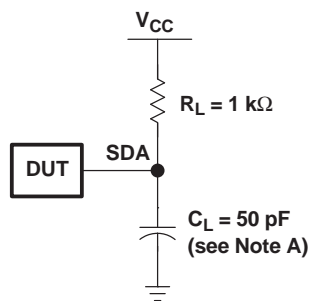
**OUTPUT HIGH VOLTAGE
vs
TEMPERATURE
(P7–P1)**



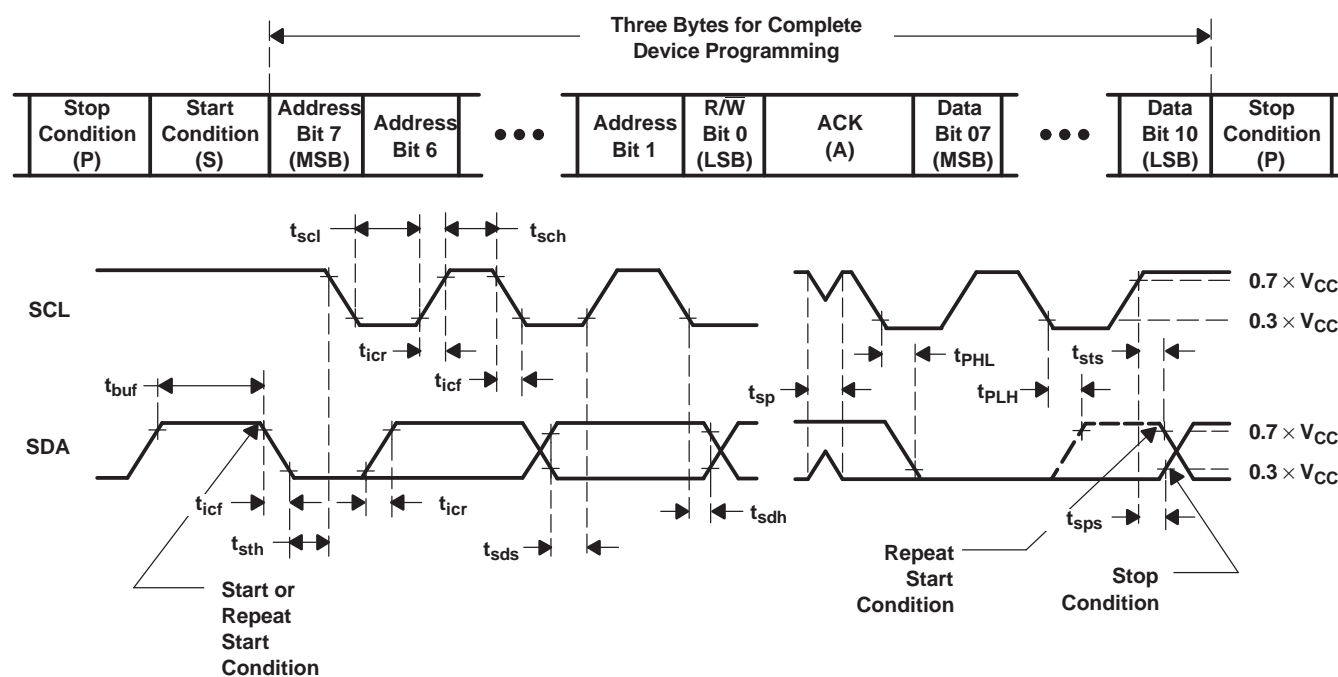
**OUTPUT LOW VOLTAGE
vs
TEMPERATURE**



PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



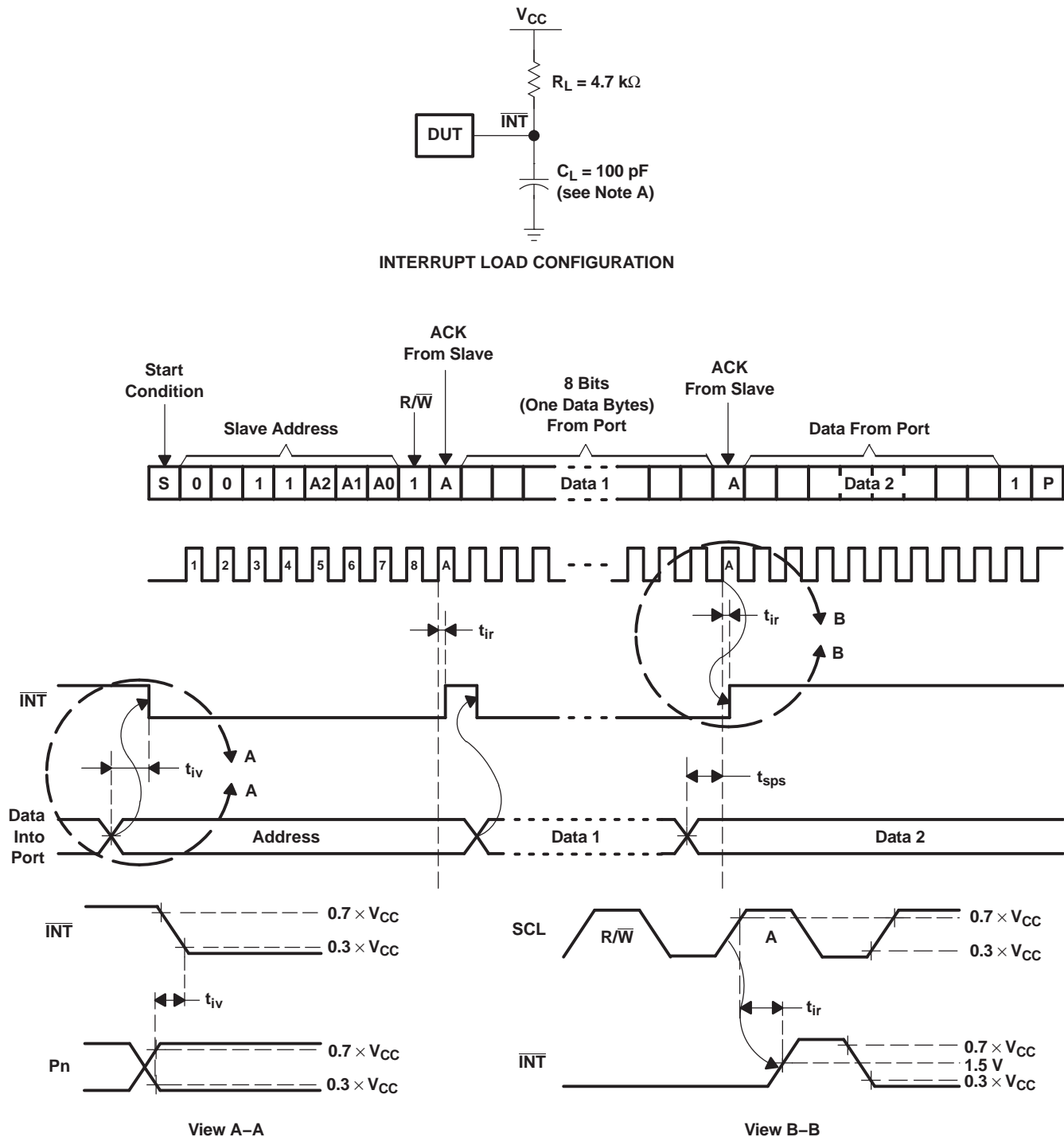
VOLTAGE WAVEFORMS

| BYTE | DESCRIPTION |
|------|--------------------------|
| 1 | I ² C address |
| 2, 3 | P-port data |

- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f \leq 30\text{ ns}$.
- C. All parameters and waveforms are not applicable to all devices.

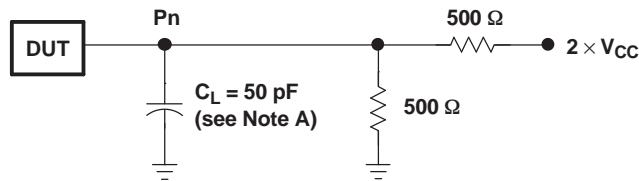
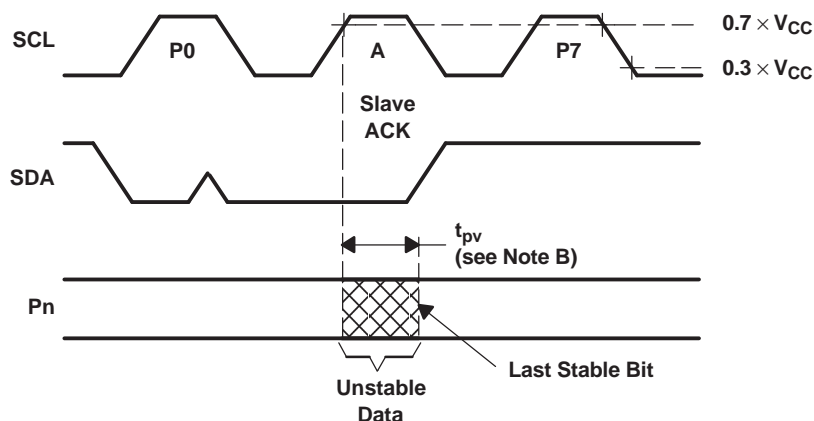
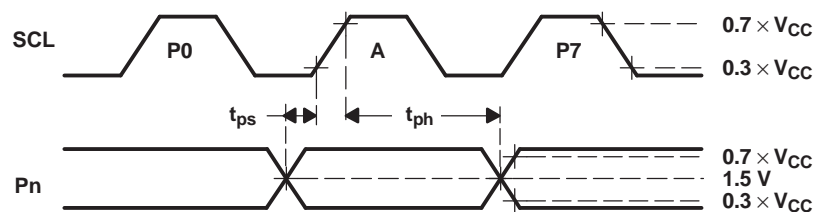
Figure 10. I²C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- C. All parameters and waveforms are not applicable to all devices.

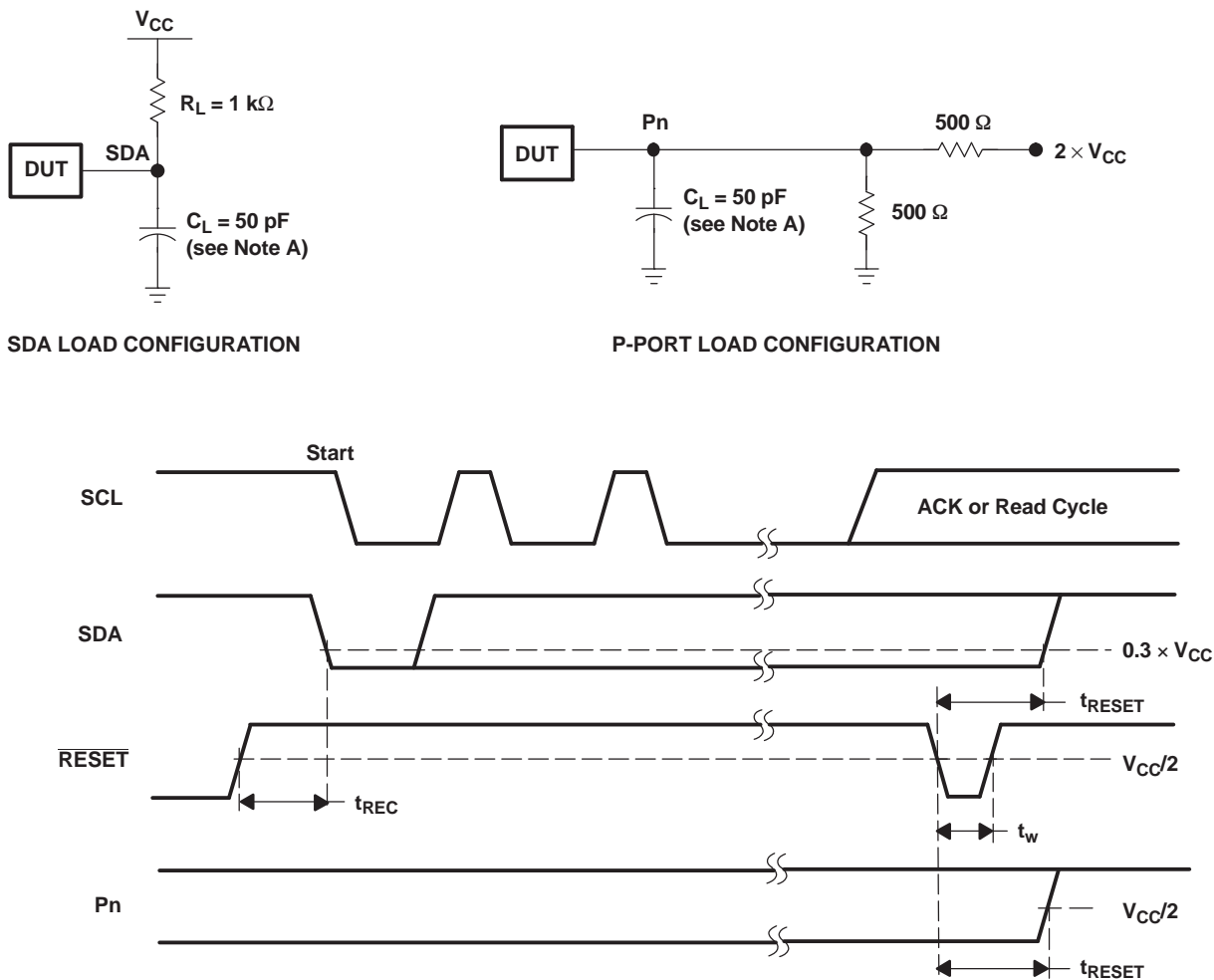
Figure 11. Interrupt Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)**P-PORT LOAD CONFIGURATION****WRITE MODE ($R/\bar{W} = 0$)****READ MODE ($R/\bar{W} = 1$)**

- A. C_L includes probe and jig capacitance.
- B. t_{pv} is measured from $0.7 \times V_{CC}$ on SCL to 50% I/O (P_n) output.
- C. All inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 12. P-Port Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

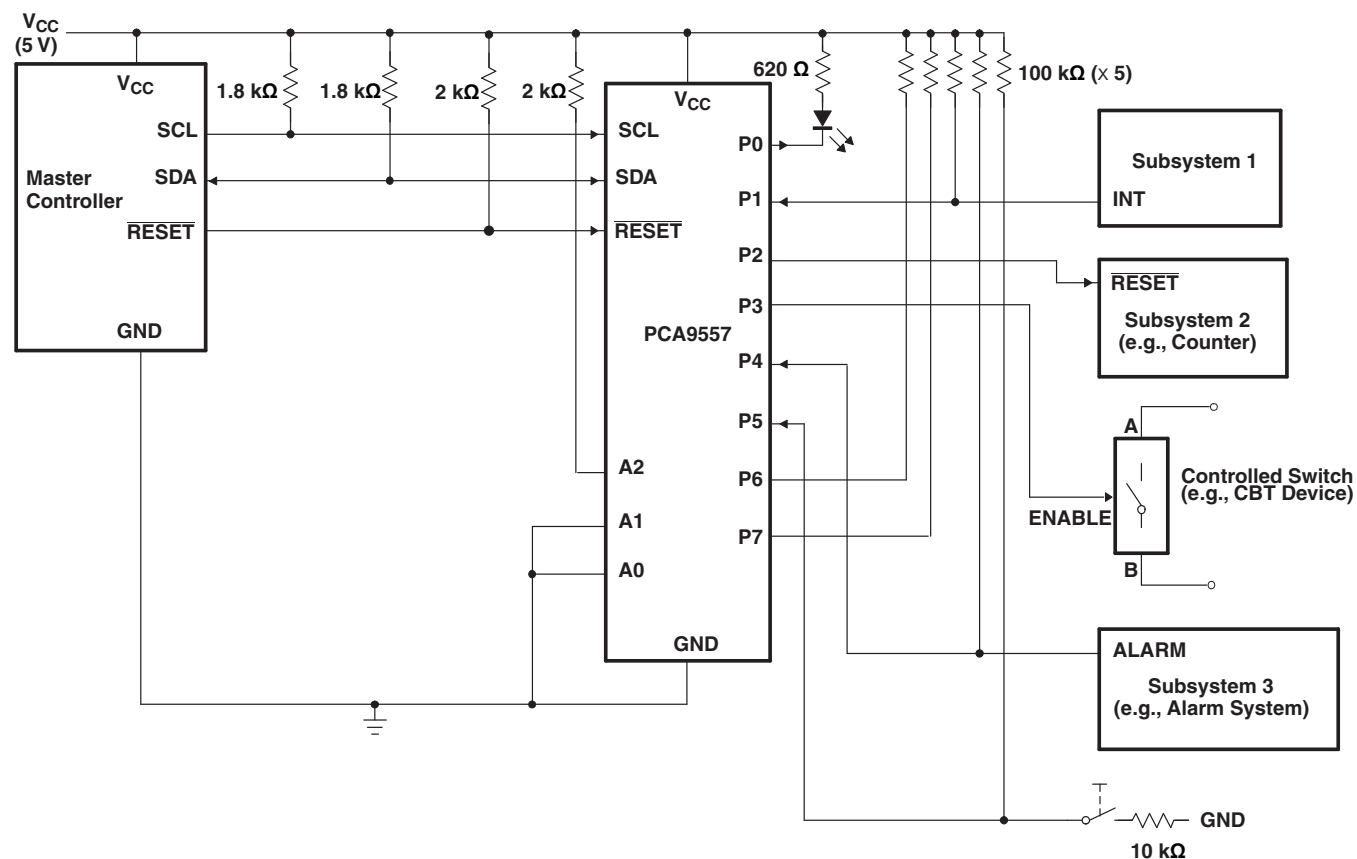


- C_L includes probe and jig capacitance.
- All inputs are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r/t_f \leq 30$ ns.
- I/Os are configured as inputs.
- All parameters and waveforms are not applicable to all devices.

Figure 13. Reset Load Circuits and Voltage Waveforms

APPLICATION INFORMATION

Figure 14 shows an application in which the PCA9557 can be used.



- A. Device address is configured as 0011100 for this example.
- B. P1, P4, and P5 are configured as inputs.
- C. P0, P2, and P3 are configured as outputs.
- D. P6 and P7 are not used and must be configured as outputs.

Figure 14. Typical Application

Minimizing I_{CC} When I/O Is Used to Control LED

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in Figure 14. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC} . The ΔI_{CC} parameter in *Electrical Characteristics* shows how I_{CC} increases as V_{IN} becomes lower than V_{CC} . Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off.

Figure 15 shows a high-value resistor in parallel with the LED. Figure 16 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

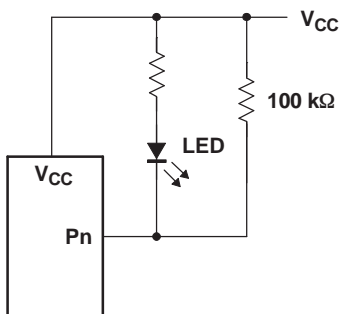


Figure 15. High-Value Resistor in Parallel With the LED

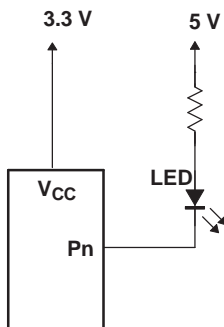


Figure 16. Device Supplied by a Low Voltage

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|-------------------------|-------------------------|
| PCA9557D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9557 | Samples |
| PCA9557DB | ACTIVE | SSOP | DB | 16 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557DBG4 | ACTIVE | SSOP | DB | 16 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557DBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557DBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9557 | Samples |
| PCA9557DGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557DGVRG4G4 | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9557 | Samples |
| PCA9557DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9557 | Samples |
| PCA9557DT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9557 | Samples |
| PCA9557DTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCA9557 | Samples |
| PCA9557PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|-------------------------|-------------------------|
| PCA9557PWTG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PD557 | Samples |
| PCA9557RGVR | ACTIVE | VQFN | RGV | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PD557 | Samples |
| PCA9557RGVRG4 | ACTIVE | VQFN | RGV | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PD557 | Samples |
| PCA9557RGYR | ACTIVE | VQFN | RGY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PD557 | Samples |
| PCA9557RGYRG4 | ACTIVE | VQFN | RGY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PD557 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCA9557DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| PCA9557DGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| PCA9557DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| PCA9557DT | SOIC | D | 16 | 250 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| PCA9557PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| PCA9557PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| PCA9557RGVR | VQFN | RGV | 16 | 2500 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCA9557DBR | SSOP | DB | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| PCA9557DGVR | TVSOP | DGV | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| PCA9557DR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| PCA9557DT | SOIC | D | 16 | 250 | 367.0 | 367.0 | 38.0 |
| PCA9557PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| PCA9557PWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |
| PCA9557RGVR | VQFN | RGV | 16 | 2500 | 367.0 | 367.0 | 35.0 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

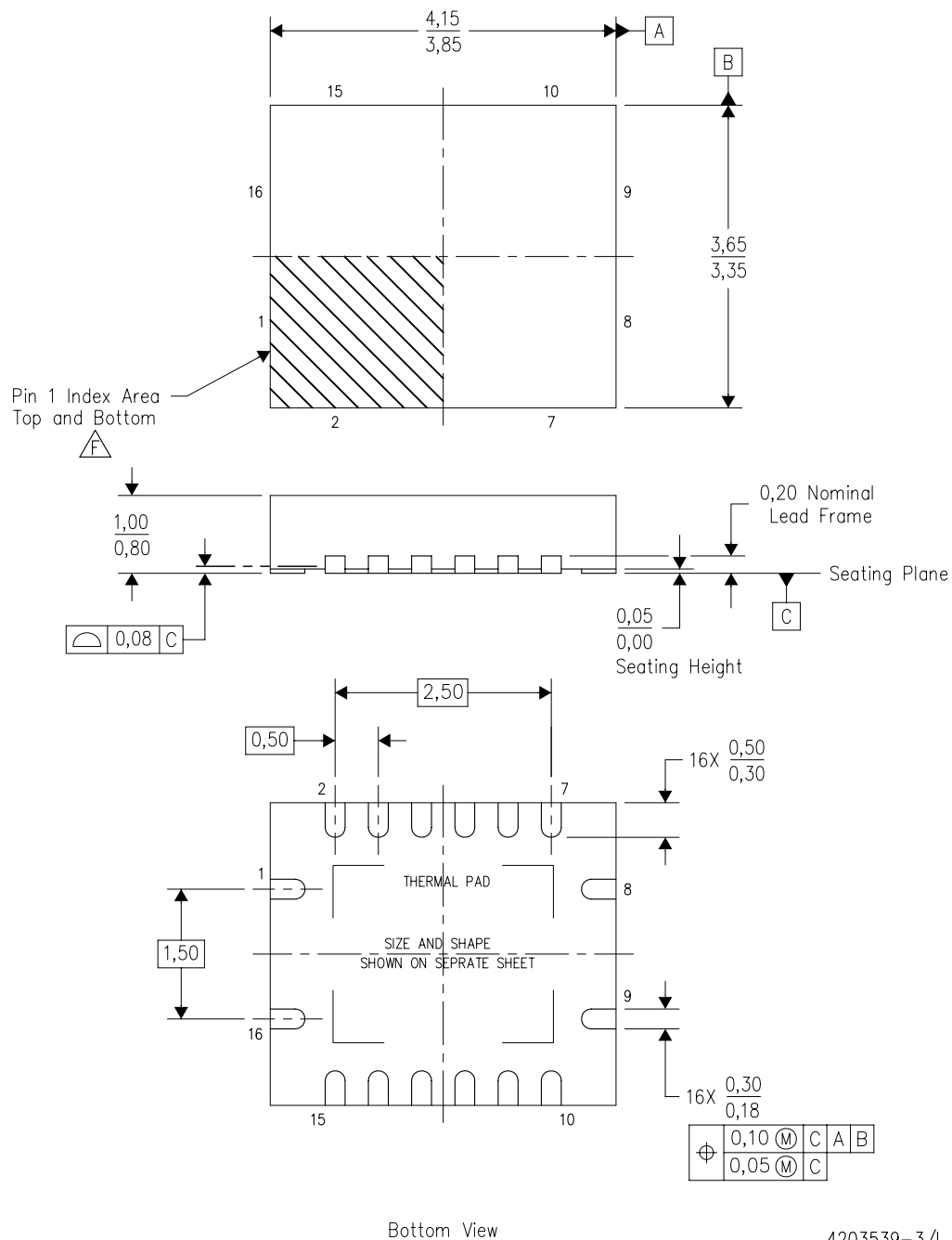


4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

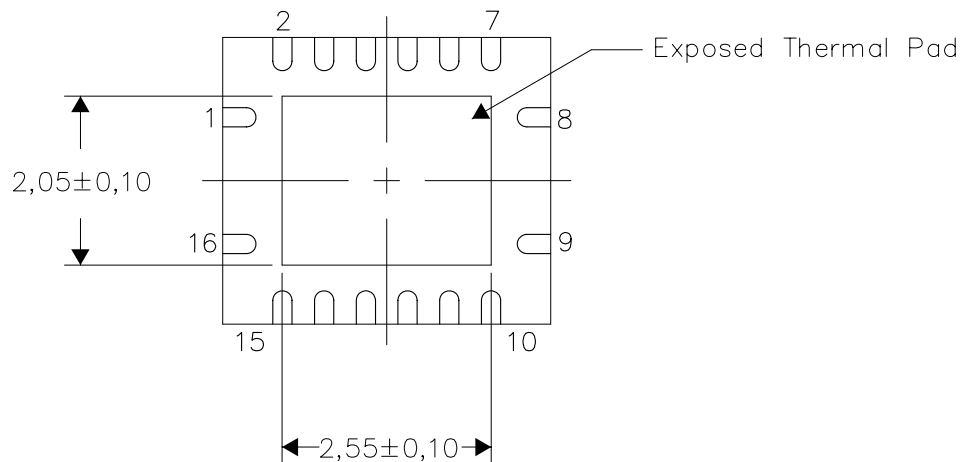
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

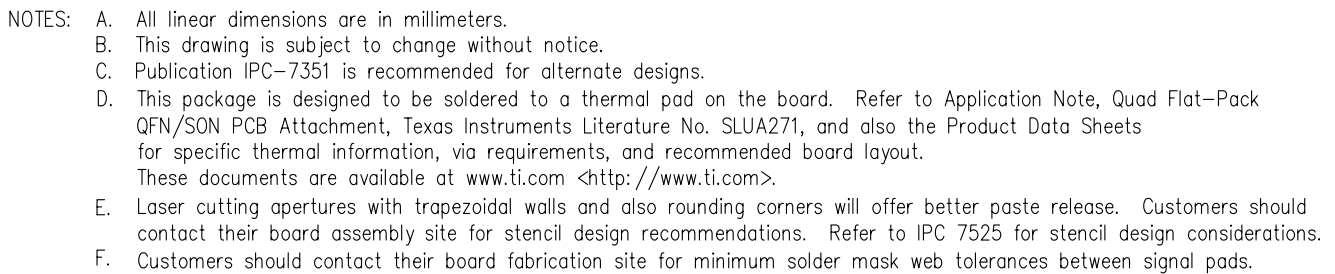


Bottom View

Exposed Thermal Pad Dimensions

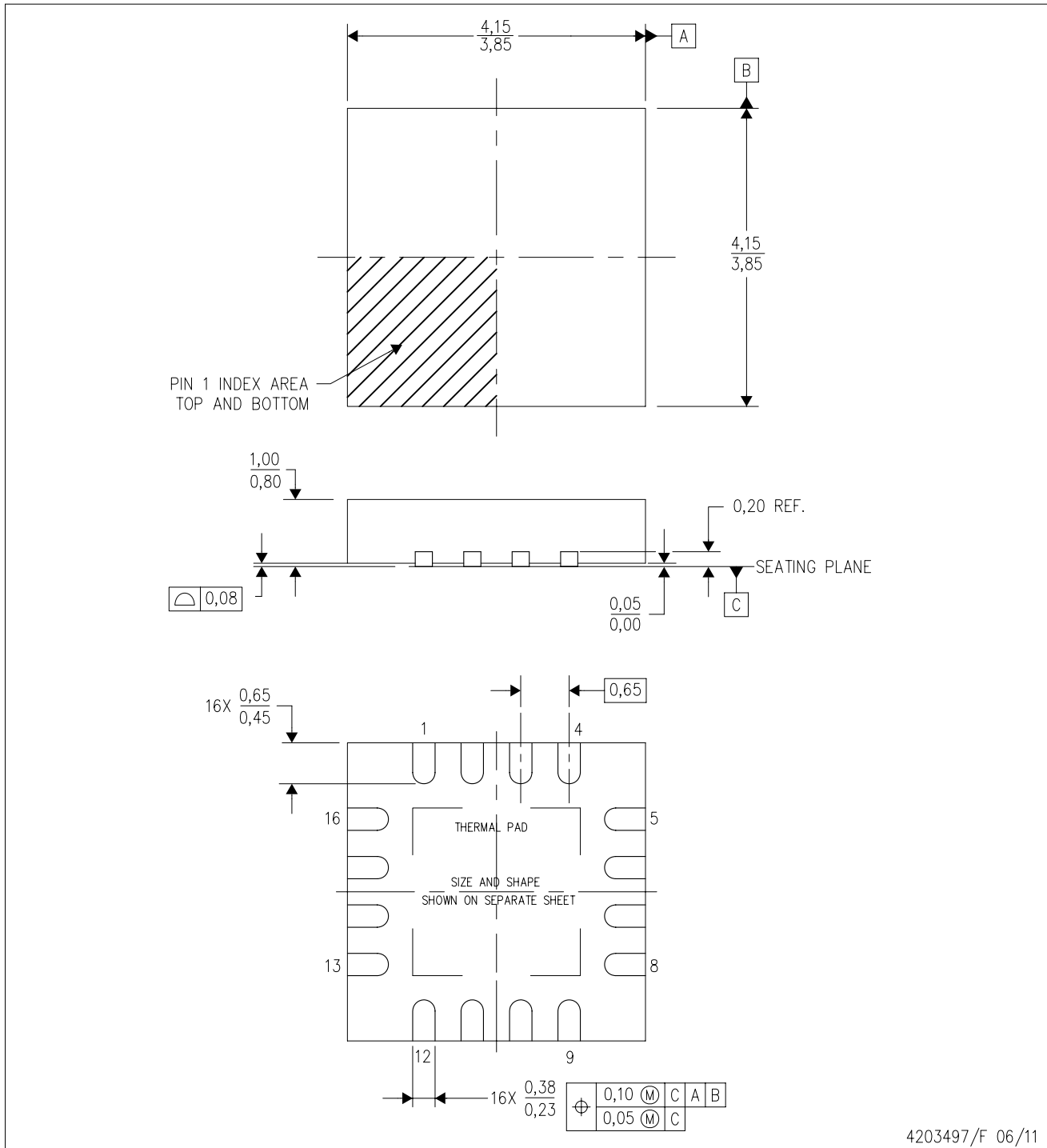
4206353-3/0 11/11

NOTE: All linear dimensions are in millimeters



RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

RGV (S-PVQFN-N16)

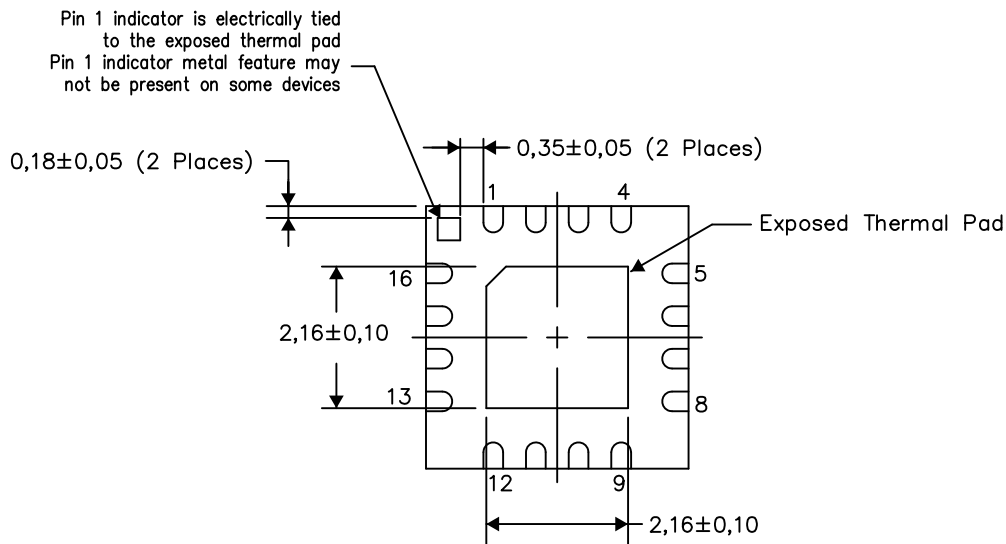
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

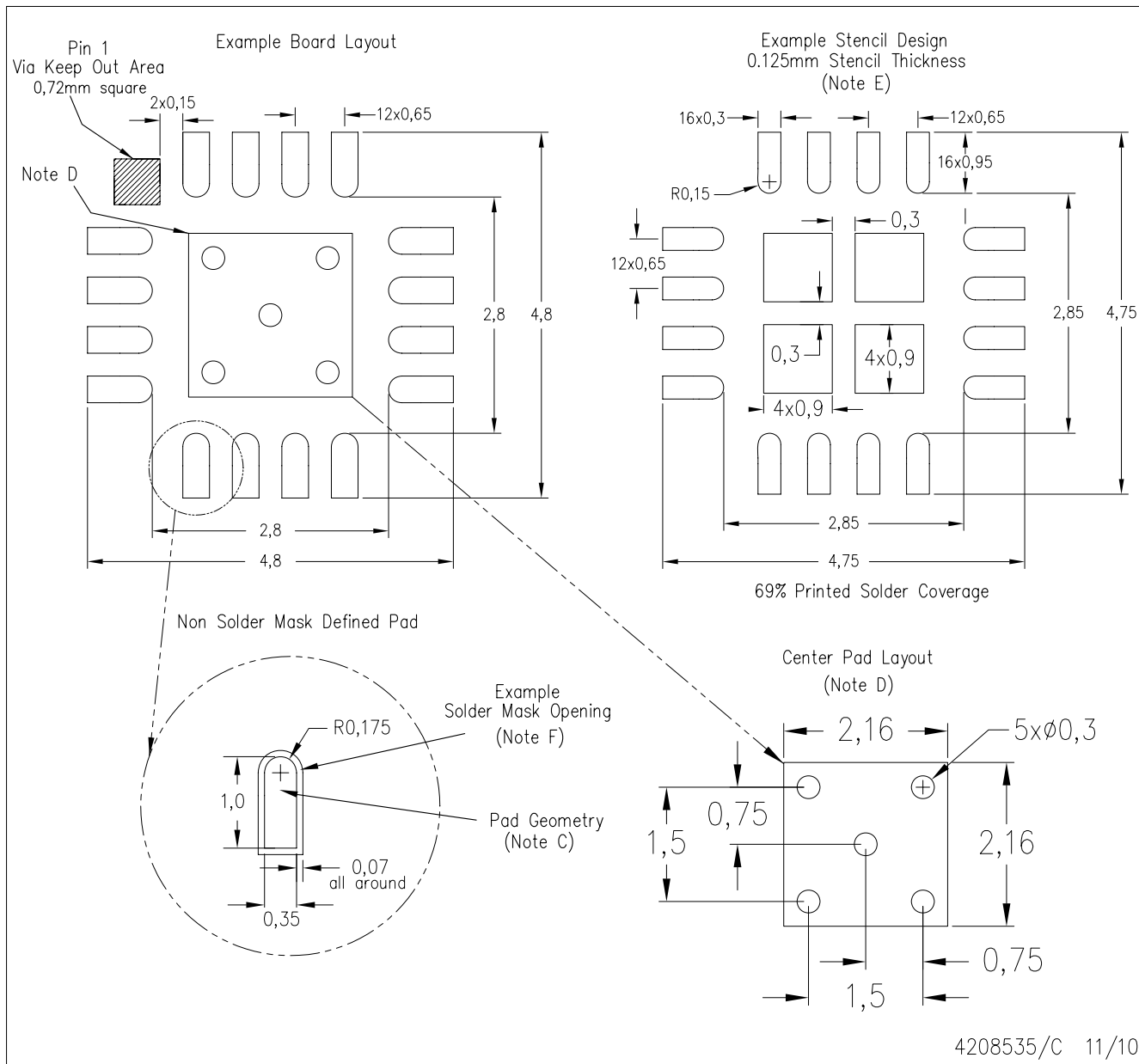
Exposed Thermal Pad Dimensions

4206351-2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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