MACH110-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 38 Inputs
- 32 Outputs
- 32 Flip-Flops
- 2 "PAL22V16" Blocks

GENERAL DESCRIPTION

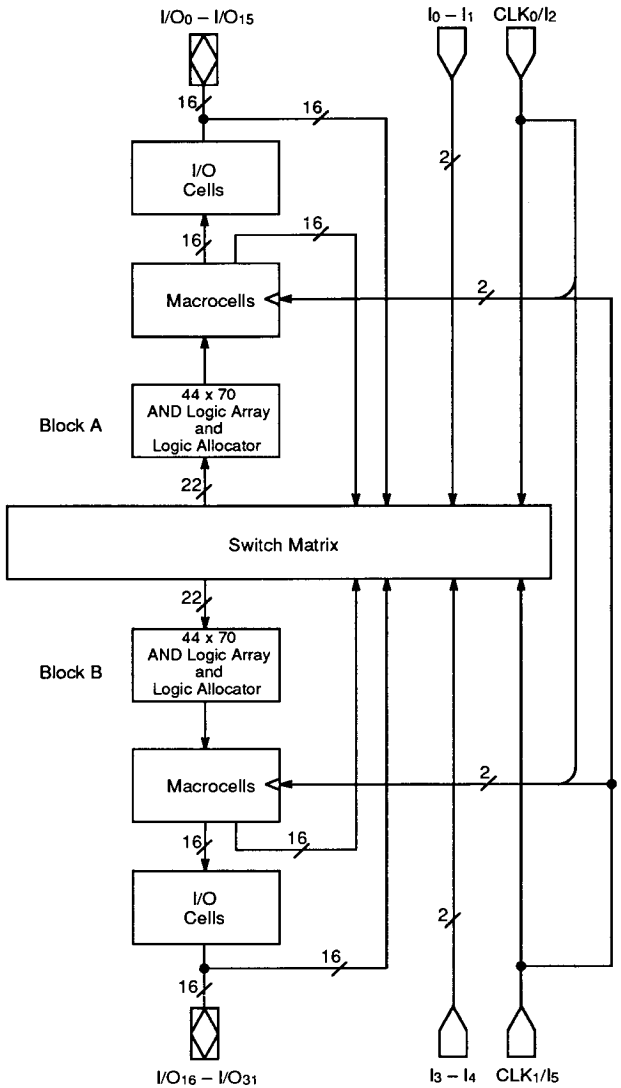
The MACH110 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately three times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

The MACH110 consists of two PAL blocks interconnected by a programmable switch matrix. The two PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH110 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

Publication # 14127 Rev. B Amendment /0
Issue Date: October 1990

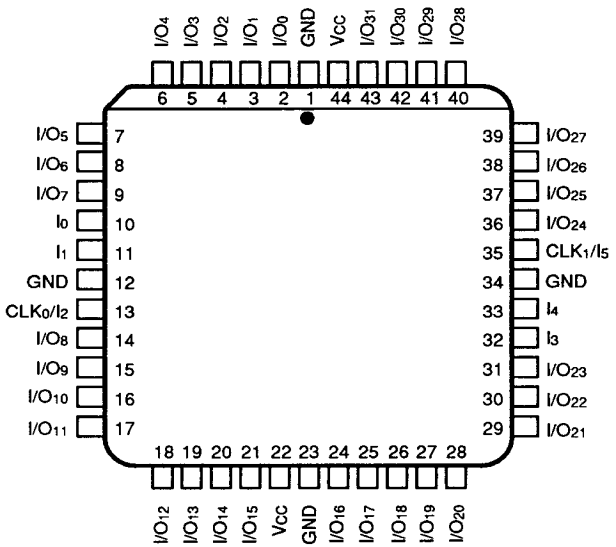
BLOCK DIAGRAM



14127-001B

CONNECTION DIAGRAM
Top View

PLCC/CQFP



Pin Designations

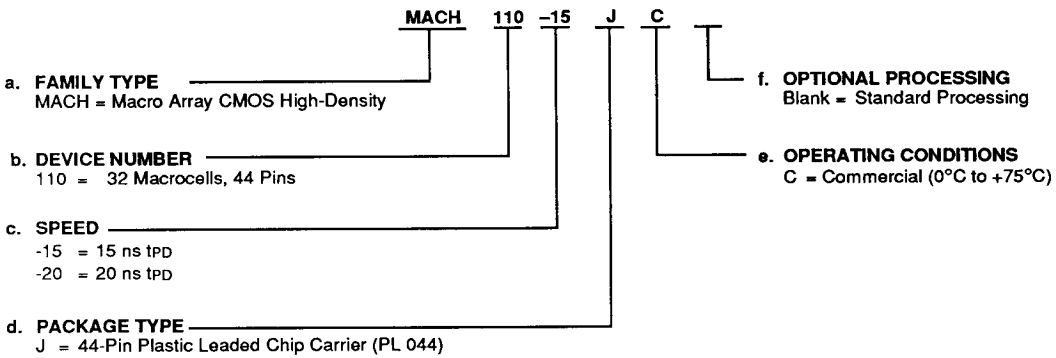
CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
VCC	Supply Voltage

14127-002A

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Device Number**
c. **Speed**
d. **Package Type**
e. **Operating Conditions**
f. **Optional Processing**



Valid Combinations
MACH110-15JC
MACH110-20JC

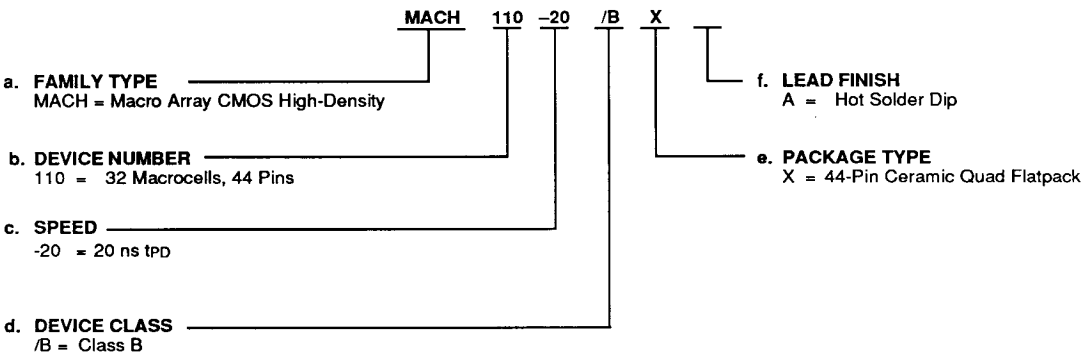
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Product List) products are fully compliant with MIL–STD–883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Device Number
c. Speed
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations
MACH110-20/BXA

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

The MACH110 consists of two PAL blocks connected by a switch matrix. There are 32 I/O pins and 6 dedicated input pins feeding the switch matrix. These signals are distributed to the two PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH110 (figure 8) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the three-state product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH110 switch matrix is fed by the 6 dedicated inputs and all of the feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH110 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the extra product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the three-state product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH110 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

The Macrocell

The MACH110 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH110 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

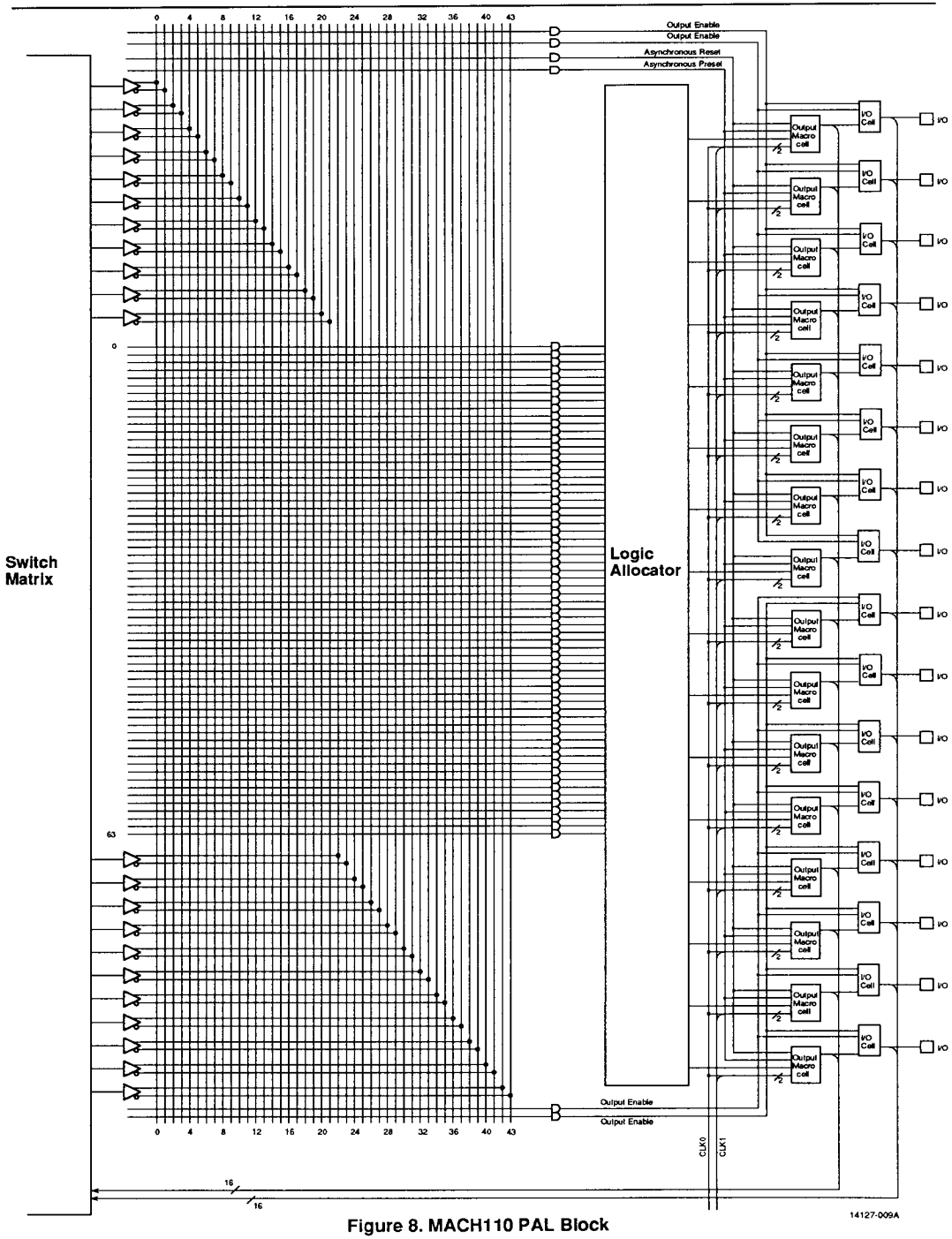


Figure 8. MACH110 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		150	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	12		15		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{CF}	Clock to Feedback (Note 4)					6		8	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$	D-type	50		40		MHz
				T-type	45.5		37		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					20		25	ns
t_{ARW}	Asynchronous Reset Width				15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time				10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					20		25	ns
t_{APW}	Asynchronous Preset Width				15		20		ns
t_{APR}	Asynchronous Preset Recovery Time				10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					15		20	ns

Notes:

2. See Switching Test Circuit, page 53, for test conditions.
3. Parameters measured with 16 outputs switching.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		200	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	9	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

PRELIMINARY

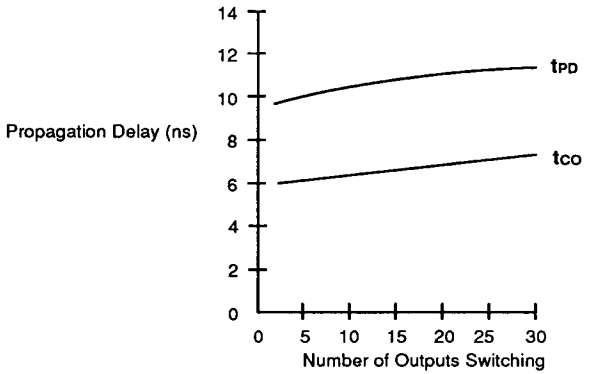
Parameter Symbol	Parameter Description				-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{CF}	Clock to Feedback (Note 4)					8	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 6)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		MHz
				T-type	37		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					25	ns
t_{ARW}	Asynchronous Reset Width (Note 5)				20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 5)				15		ns
t_{AP}	Asynchronous Preset to Registered Output					25	ns
t_{APW}	Asynchronous Preset Width (Note 5)				20		ns
t_{APR}	Asynchronous Reset Recovery Time (Note 5)				15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 5)					20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 5)					20	ns

Notes:

2. See Switching Test Circuit, page 53, for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Parameters measured with 16 outputs switching.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

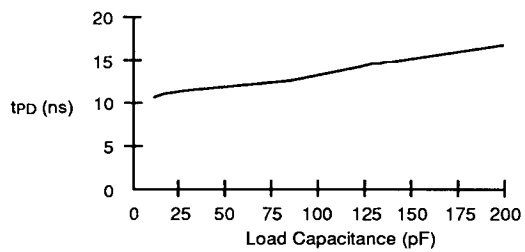
TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



t_{PD}, t_{CO} vs Number of Outputs Switching

14127-005A



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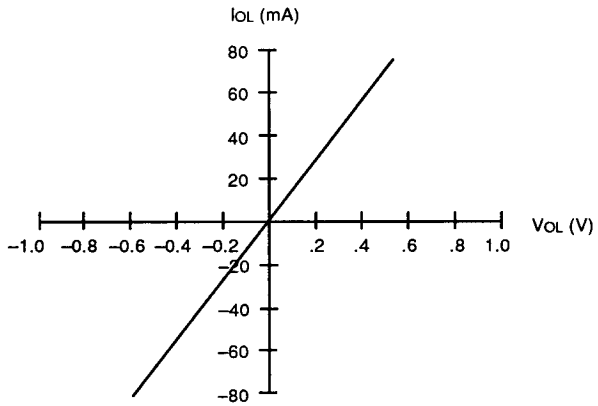
t_{PD} vs Load Capacitance

TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



Output, LOW

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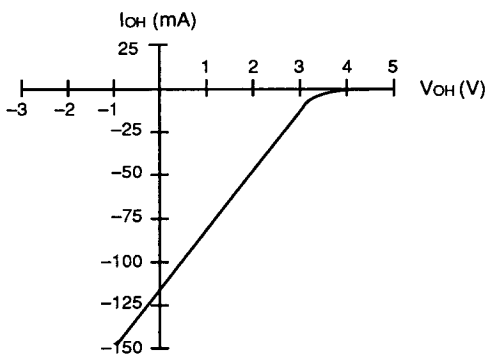
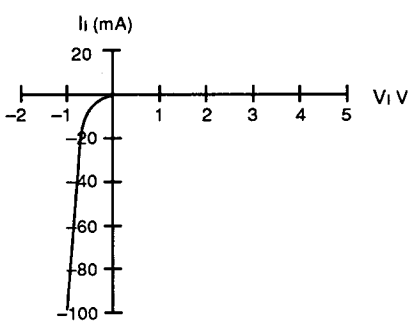


Output, HIGH

14127-008A

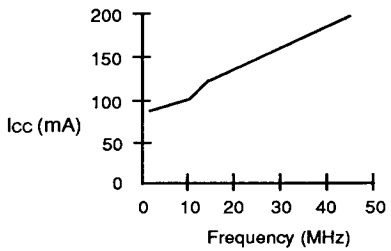


14127-009A

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C, frequency = 0 MHz unless otherwise specified



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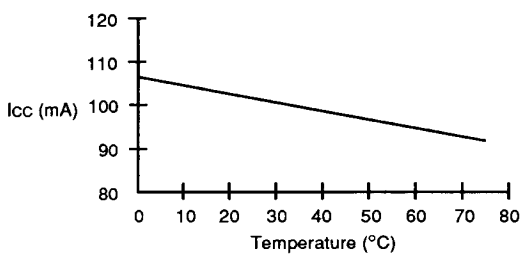
I_{CC} vs. Operating Frequency



14127-011A

I_{CC} vs. Operating Temperature

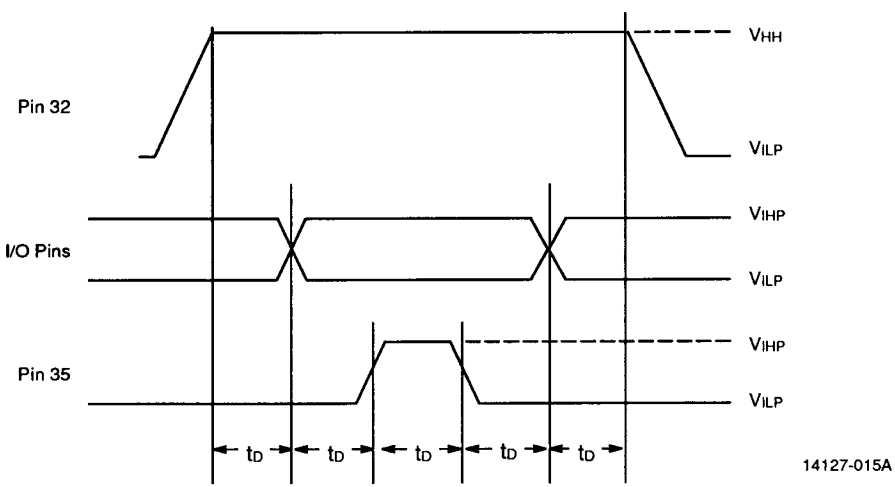
REGISTER PRELOAD

The Preload function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. Before ending the preload operation, simple combinatorial values should be restored by reapplying the input values that were present at the start of the preload operation. These values should be applied before pin 32 is lowered. Data in combinatorial latches may be lost.

The procedure for preloading follows.

1. Raise V_{CC} to 5.0 V ± 0.25 V.
2. If asynchronous reset or preset is used in the design, place inputs in a state that keeps the reset and preset inactive for a delay t_D.
3. Raise pin 32 to V_{HH} to disable outputs.
4. Apply the desired value (V_{ILP}/V_{IHP}) to outputs. Note that a preloaded HIGH will set the flip-flop HIGH.
5. Pulse pin 35 from V_{ILP} to V_{IHP} to V_{ILP}.
6. Remove V_{ILP}/V_{IHP} from all outputs.
7. Reapply the input values of step 2.
8. Lower pin 32 to V_{ILP}.
9. Verify for V_{OL}/V_{OH} at all output pins as per programmed pattern.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	9	9.25	9.5	V
V_{ILP}	Low-level input voltage	0	0.2	0.4	V
V_{IHP}	High-level input voltage	2.8	5.0	5.5	V
V_{CCH}	Supply voltage during preload	4.5	5.0	5.5	V
t_D	Delay time	10	20	50	µs



Preload Waveform

REGISTER OBSERVABILITY

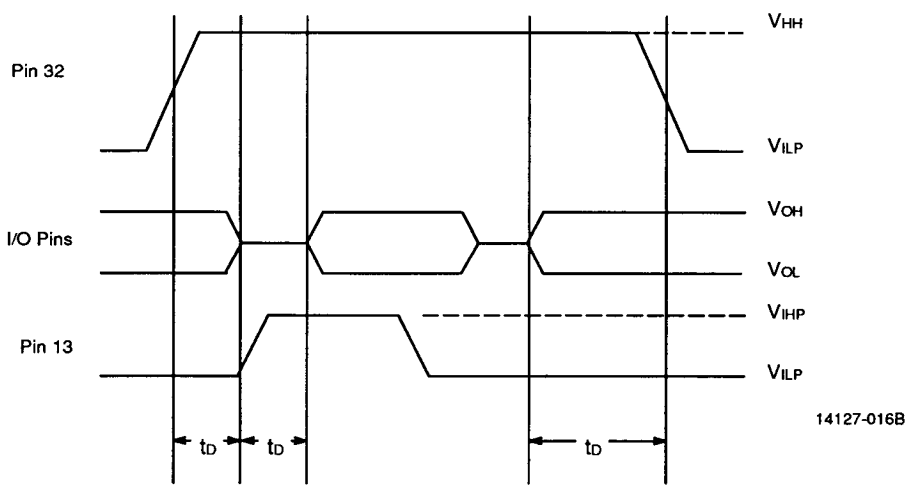
The Observability function allows the registers to be viewed at the output pins. This feature aids functional testing of sequential designs by allowing direct observation of register states.

The value of outputs corresponding to combinatorial macrocells should be ignored. Before ending the observe operation, simple combinatorial logic values can be restored by reapplying the input values that were present at the start of the observe operation. These values should be applied before pin 32 is lowered. Data in combinatorial latches may be lost.

The procedure for observability follows.

1. If asynchronous reset or preset is used in the design, place inputs in a state that keeps the reset and preset inactive for a delay t_D.
2. Raise pin 32 to V_{HH}.
3. Remove input values.
4. Raise pin 13 to V_{IHP}.
5. Register values will be sent to I/O pins.
6. Lower pin 13 to V_{ILP}.
7. Reapply the input values of step 1.
8. Lower pin 32 to V_{ILP}.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	9	9.25	9.5	V
V_{ILP}	Low-level input voltage	0	0.2	0.4	V
V_{IHP}	High-level input voltage	2.8	5.0	5.5	V
t_D	Delay time	10	20	50	µs



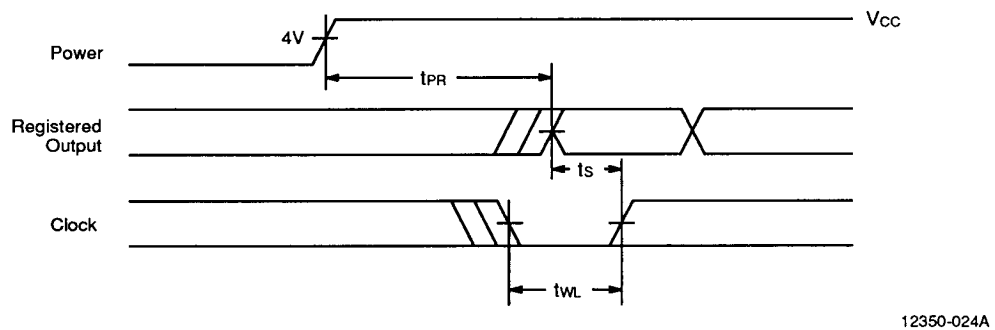
Observability Waveform

POWER-UP RESET

The MACH110 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max.	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform