



Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821A/B/C
IDT54/74FCT823A/B/C
IDT54/74FCT824A/B/C
IDT54/74FCT825A/B/C

FEATURES:

- Equivalent to AMD's Am29821-25 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT821A/823A/824A/825A equivalent to FAST™ speed
- **IDT54/74FCT821B/823B/824B/825B 25% faster than FAST**
- **IDT54/74FCT821C/823C/824C/825C 40% faster than FAST**
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input (CLR)
- $I_{OL} = 48\text{mA}$ (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output compatibility
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series ($5\mu\text{A}$ max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

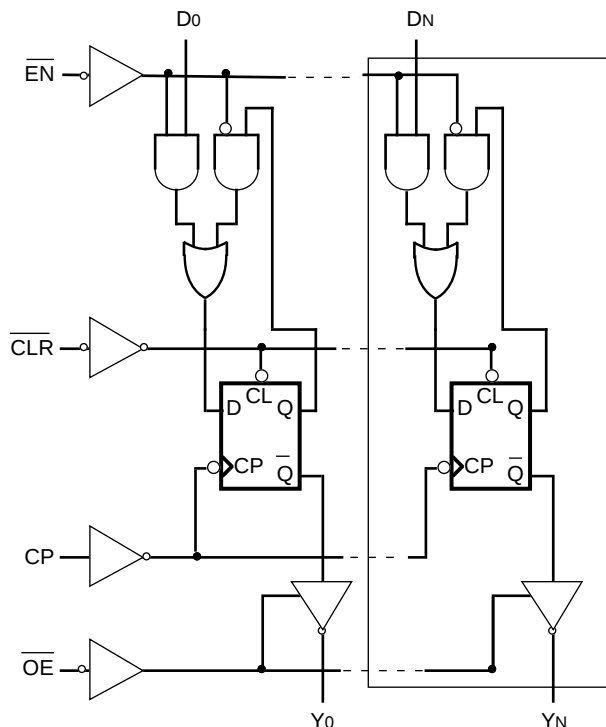
The IDT54/74FCT800 series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821 are buffered, 10-bit wide versions of the popular '374 function. The IDT54/74FCT823 and IDT54/74FCT824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825 are 8-bit buffered registers with all the '823 controls plus multiple enables ($\overline{OE1}$, $\overline{OE2}$, $\overline{OE3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and $\overline{RD}/\overline{WR}$. They are ideal for use as an output port requiring HIGH I_{OL}/I_{OH} .

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAMS

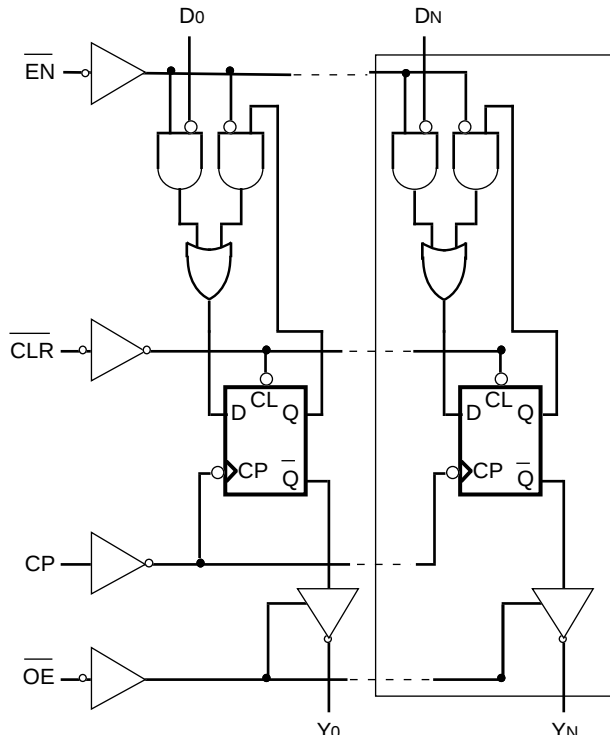
IDT54/74FCT821/823/825



The IDT logo is a registered trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

2608 cnv* 01

IDT54/74FCT824



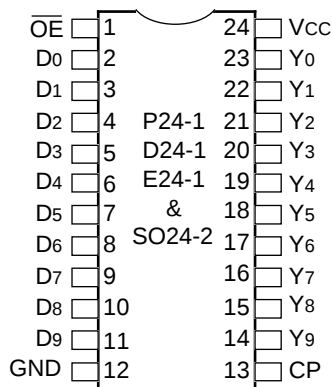
2608 cnv* 02

MILITARY AND COMMERCIAL TEMPERATURE RANGES

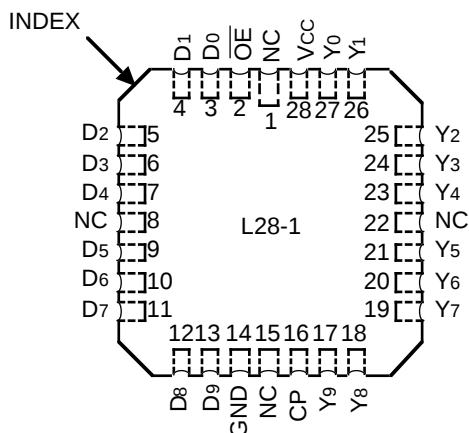
MAY 1992

PIN CONFIGURATIONS

IDT54/74FCT821 10-BIT REGISTER

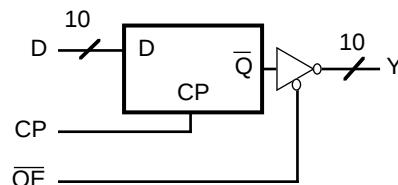


DIP/SOIC/CERPACK
TOP VIEW



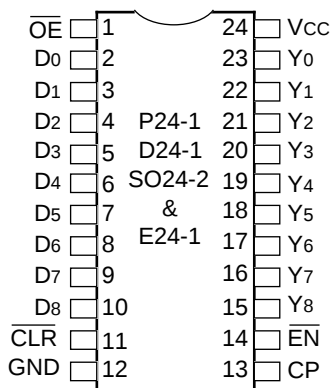
LCC
TOP VIEW

LOGIC SYMBOLS

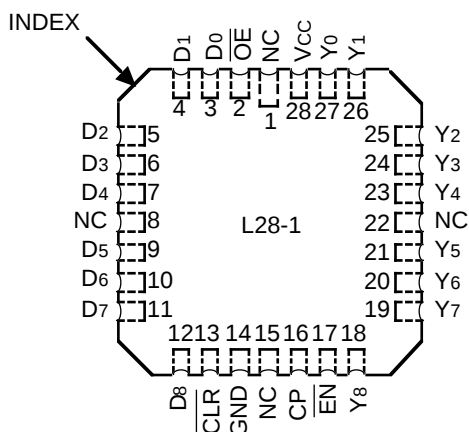


2608 cnv* 03

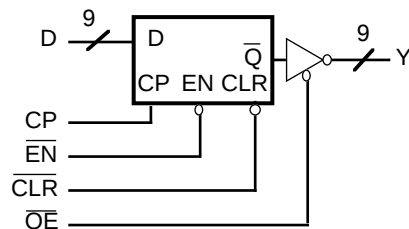
IDT54/74FCT823/824 9-BIT REGISTERS



DIP/SOIC/CERPACK
TOP VIEW

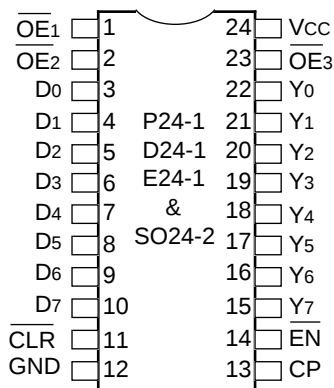


LCC
TOP VIEW

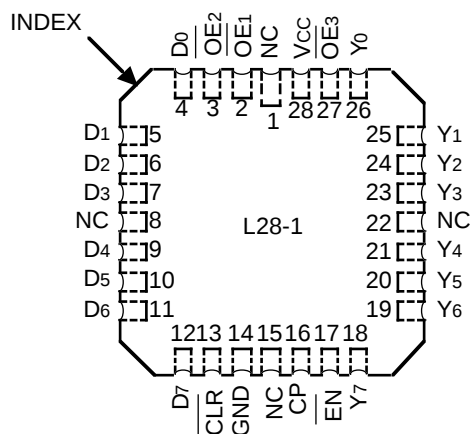


2608 cnv* 04

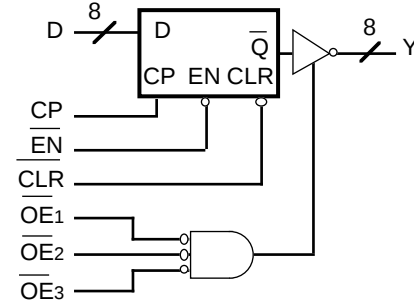
IDT54/74FCT825 8-BIT REGISTER



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW



2608 cnv* 05

PRODUCT SELECTOR GUIDE

	Device		
	10-Bit	9-Bit	8-Bit
Non-inverting	54/74FCT821A/B/C	54/74FCT823A/B/C	54/74FCT825A/B/C
Inverting		54/74FCT824A/B/C	

2608 tbl 01

PIN DESCRIPTION

Name	I/O	Description
D _I	I	The D flip-flop data inputs.
$\overline{\text{CLR}}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{\text{OE}}$ is LOW, the Q _I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y _I , $\overline{\text{Y}}$ _I	O	The register three-state outputs.
$\overline{\text{EN}}$	I	Clock Enable. When the clock enable is LOW, data on the D _I input is transferred to the Q _I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q _I outputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output Control. When the $\overline{\text{OE}}$ input is HIGH, the Y _I outputs are in the high impedance state. When the $\overline{\text{OE}}$ input is LOW, the TRUE register data is present at the Y _I outputs.

2608 tbl 10

FUNCTION TABLE⁽¹⁾

IDT54/74FCT821/823/825

Inputs					Internal/Outputs		Function
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{EN}}$	D _I	CP	Q _I	Y _I	
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

2608 tbl 02

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

FUNCTION TABLE⁽¹⁾

IDT54/74FCT824

Inputs					Internal/Outputs		Function
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{EN}}$	D _I	CP	Q _I	Y _I	
H	H	L	L	↑	H	Z	High Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

NOTE:

2608 tbl 03

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC}	−0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	−55 to +125	°C
T _{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T _{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

2608 tbl 04

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} − 0.2V

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _I = V _{CC}	—	—	5	μA
I _{IL}	Input LOW Current		V _I = 2.7V	—	—	5 ⁽⁴⁾	
			V _I = 0.5V	—	—	−5 ⁽⁴⁾	
			V _I = GND	—	—	−5	
I _{OZH}	Off State (High Impedance) Output Current	V _{CC} = Max.	V _O = V _{CC}	—	—	10	μA
I _{OZL}			V _O = 2.7V	—	—	10 ⁽⁴⁾	
			V _O = 0.5V	—	—	−10 ⁽⁴⁾	
			V _O = GND	—	—	−10	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _N = −18mA		—	−0.7	−1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _O = GND		−75	−120	—	mA
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OH} = −32μA		V _{HC}	V _{CC}	—	V
		V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = −300μA	V _{HC}	V _{CC}	—	
			I _{OH} = −15mA MIL.	2.4	4.3	—	
			I _{OH} = −24mA COM'L.	2.4	4.3	—	
V _{OL}	Output LOW Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OL} = 300μA		—	GND	V _{LC}	V
		V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 300μA	—	GND	V _{LC} ⁽⁴⁾	
			I _{OL} = 32mA MIL.	—	0.3	0.5	
			I _{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:

2608 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \overline{EN} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \overline{EN} = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.2	6.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \overline{EN} = \text{GND}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.2	16.8 ⁽⁵⁾	

NOTES:

2608 tbl 07

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions ⁽¹⁾	IDT54/74FCT821A/ 823A/824A/825A				IDT54/74FCT821B/ 823B/824B/825B				IDT54/74FCT821C/ 823C/824C/825C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to Y _i ($\overline{OE}$ = LOW)	CL = 50pF RL = 500Ω	—	10.0	—	11.5	—	7.5	—	8.5	—	6.0	—	7.0	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	—	20.0	—	20.0	—	15.0	—	16.0	—	12.5	—	13.5	
tsU	Set-up Time HIGH or LOW D _i to CP	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW D _i to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tsU	Set-up Time HIGH or LOW $\overline{EN}$ to CP		4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{EN}$ to CP		2.0	—	2.0	—	0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{CLR}$ to Y _i		—	14.0	—	15.0	—	9.0	—	9.5	—	8.0	—	8.5	ns
tREM	Recovery Time $\overline{CLR}$ to CP		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tw	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tw	$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tpZH tpZL	Output Enable Time $\overline{OE}$ to Y _i	CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	9.0	—	7.0	—	8.0	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	—	23.0	—	25.0	—	15.0	—	16.0	—	12.5	—	13.5	
tpHZ tplZ	Output Disable Time $\overline{OE}$ to Y _i	CL = 5pF ⁽³⁾ RL = 500Ω	—	7.0	—	8.0	—	6.5	—	7.0	—	6.2	—	6.2	ns
		CL = 50pF RL = 500Ω	—	8.0	—	9.0	—	7.5	—	8.0	—	6.5	—	6.5	

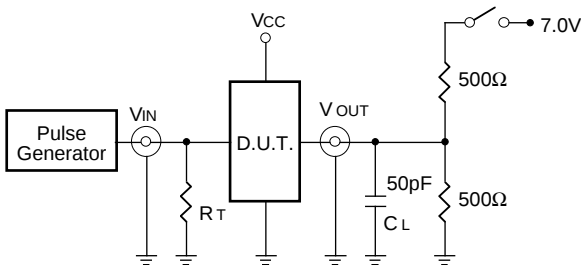
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2608 tbl* 08

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



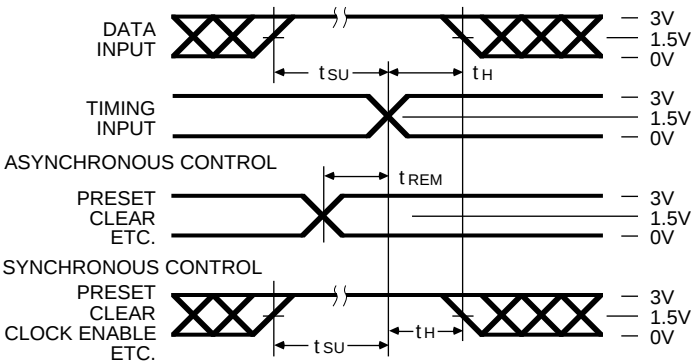
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

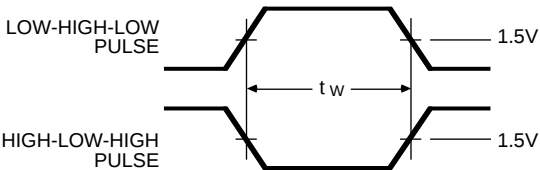
DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2608 tbl 09

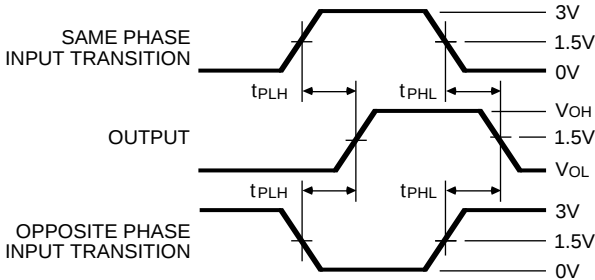
SET-UP, HOLD AND RELEASE TIMES



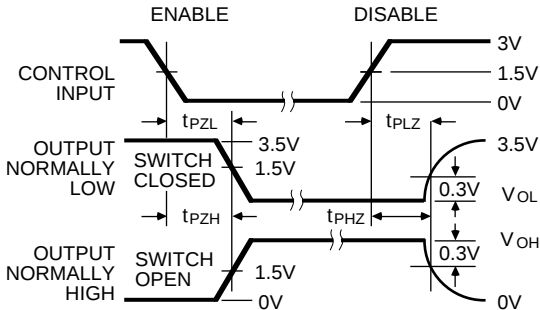
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.

2608 drw 01

ORDERING INFORMATION

2523

cnv* 11

FCT

XXXX

X

X

Temp. Range

Device Type

Package

Process

Blank

B

Commercial

MIL-STD-883, Class B

P

D

E

L

SO

Plastic DIP

CERDIP

CERPACK

Leadless Chip Carrier

Small Outline IC

821A

821B

821C

823A

823B

823C

824A

824B

824C

825A

825B

825C

10-Bit Non-Inverting Register

Fast 10-Bit Non-Inverting Register

Super Fast 10-Bit Non-Inverting Register

9-Bit Non-Inverting Register

Fast 9-Bit Non-Inverting Register

Super Fast 9-Bit Non-Inverting Register

9-Bit Inverting Register

Fast 9-Bit Inverting Register

Super Fast 9-Bit Inverting Register

8-Bit Non-Inverting Register

Fast 8-Bit Non-Inverting Register

Super Fast 8-Bit Non-Inverting Register

54

74

–55°C to +125°C

0°C to +70°C

2608 cnv* 11

2608 cnv* 11