

74F113

Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 74F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is

transferred to the outputs on the falling edge of the clock pulse.

Asynchronous input:

LOW input to \bar{S}_D sets Q to HIGH level

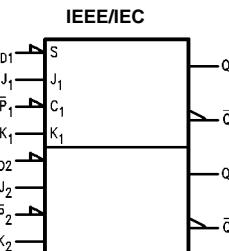
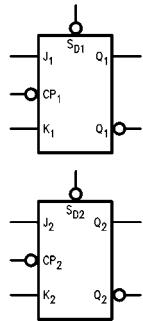
Set is independent of clock

Ordering Code:

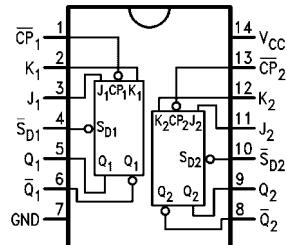
Order Number	Package Number	Package Description
74F113SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F113SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F113PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	20 μ A/-0.6 mA
$\overline{CP}_1, \overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20 μ A/-2.4 mA
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/5.0	20 μ A/-3.0 mA
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs	50/33.3	-1 mA/20 mA

Truth Table

Inputs				Outputs	
\overline{S}_D	\overline{CP}	J	K	Q	\overline{Q}
L	X	X	X	H	L
H	\sim	h	h	\overline{Q}_0	Q_0
H	\sim	l	h	L	H
H	\sim	h	l	H	L
H	\sim	l	l	Q_0	\overline{Q}_0

H (h) = HIGH Voltage Level

L (l) = LOW Voltage level

\sim = HIGH-to-LOW Clock Transition

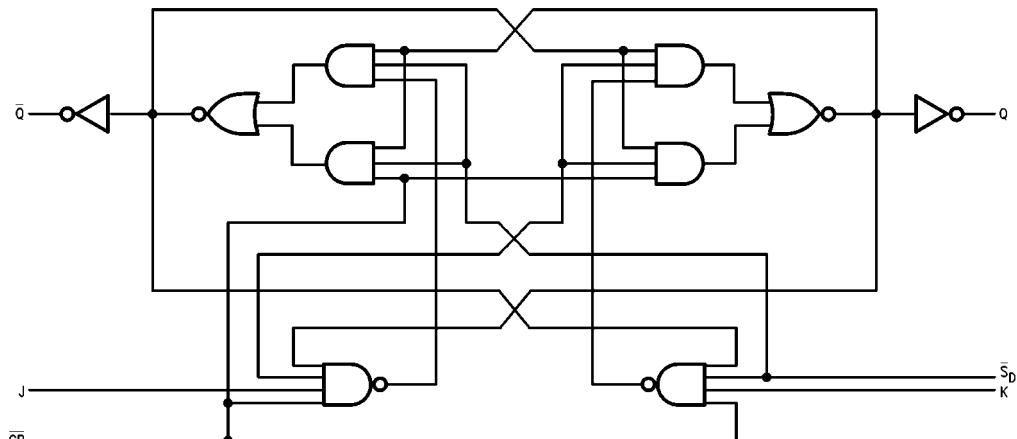
X = Immaterial

Q_0 (\overline{Q}_0) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output prior to the HIGH-to-LOW clock transition.

Logic Diagram

(One Half Shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings ^(Note 1)		Recommended Operating Conditions				
Storage Temperature	-65°C to +150°C					
Ambient Temperature under Bias	-55°C to +125°C					
Junction Temperature under Bias	-55°C to +150°C					
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V					
Input Voltage (Note 2)	-0.5V to +7.0V					
Input Current (Note 2)	-30 mA to +5.0 mA					
Voltage Applied to Output						
in HIGH State (with $V_{CC} = 0V$)						
Standard Output	-0.5V to V_{CC}					
3-STATE Output	-0.5V to +5.5V					
Current Applied to Output						
in LOW State (Max)	twice the rated I_{OL} (mA)					
DC Electrical Characteristics						
Symbol	Parameter	Min	Typ	Max	Units	V_{CC}
V_{IH}	Input HIGH Voltage	2.0			V	
V_{IL}	Input LOW Voltage		0.8		V	
V_{CD}	Input Clamp Diode Voltage		-1.2		V	Min
V_{OH}	Output HIGH Voltage 10% V_{CC} 5% V_{CC}	2.5 2.7			V	Min
V_{OL}	Output LOW Voltage 10% V_{CC}		0.5		V	Min
I_{IH}	Input HIGH Current		5.0		μA	Max
I_{BVI}	Input HIGH Current Breakdown Test		7.0		μA	Max
I_{CEX}	Output HIGH Leakage Current		50		μA	Max
V_{ID}	Input Leakage Test	4.75			V	0.0
I_{OD}	Output Leakage Circuit Current		3.75		μA	0.0
I_{IL}	Input LOW Current		-0.6 -2.4 -3.0		mA	Max
I_{OZH}	Output Leakage Current		50		μA	Max
I_{OZL}	Output Leakage Current		-50		μA	Max
I_{OS}	Output Short-Circuit Current	-60	-150		mA	Max
I_{CC}	Power Supply Current	12	19		mA	Max

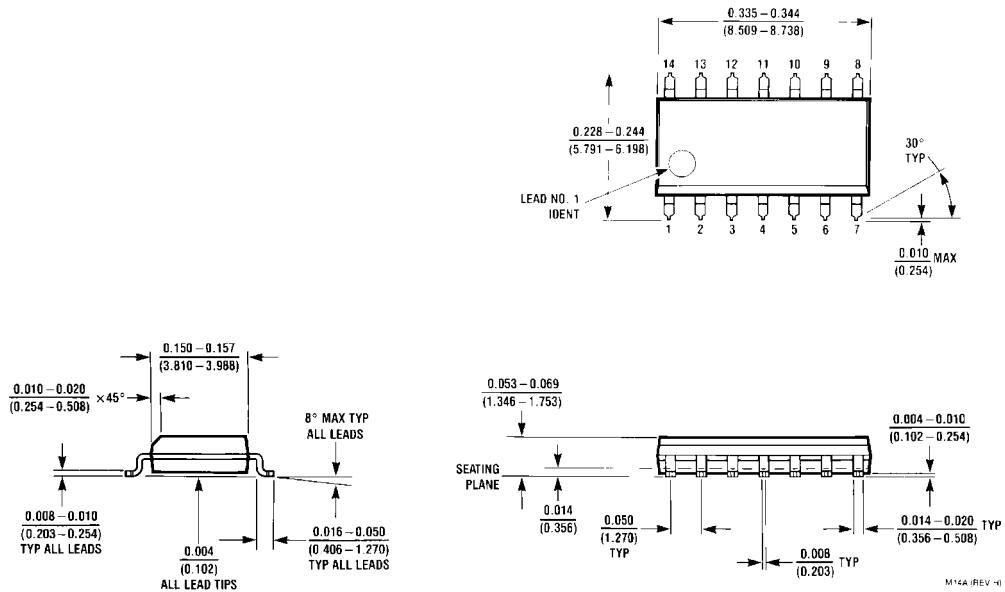
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$			$T_A = 0^\circ C$ to $+70^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	85	105		80		MHz
t_{PLH}	Propagation Delay \overline{CP}_n to Q_n or \overline{Q}_n	2.0	4.0	6.0	2.0	7.0	ns
t_{PLH}	Propagation Delay \overline{S}_{Dn} to Q_n or \overline{Q}_n	2.0	4.5	6.5	2.0	7.5	ns
t_{PHL}		2.0	4.5	6.5	2.0	7.5	ns

AC Operating Requirements

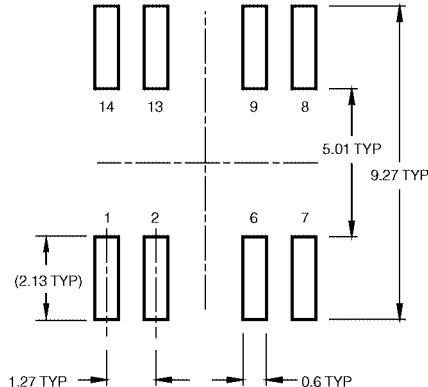
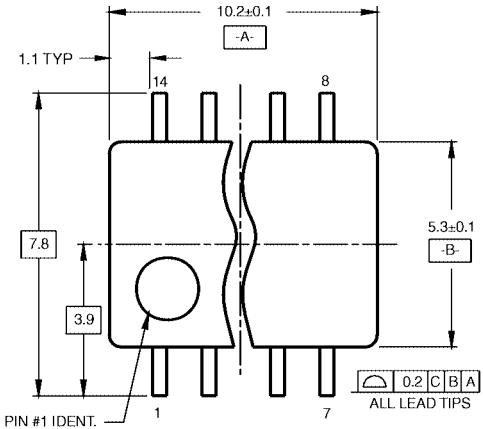
Symbol	Parameter	$T_A = +25^\circ C$ $V_{CC} = +5.0V$		$T_A = 0^\circ C$ to $+70^\circ C$ $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.0		5.0		
$t_S(L)$	J_n or K_n to \overline{CP}_n	3.0		3.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	J_n or K_n to \overline{CP}_n	0		0		
$t_W(H)$	\overline{CP}_n Pulse Width HIGH or LOW	4.5		5.0		
$t_W(L)$	\overline{S}_{Dn} Pulse Width, LOW	4.5		5.0		
t_{REC}	\overline{S}_{Dn} to \overline{CP}_n Recovery Time	4.0		5.0		

Physical Dimensions inches (millimeters) unless otherwise noted

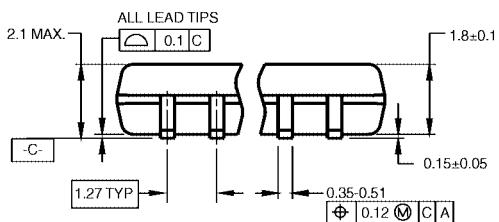


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

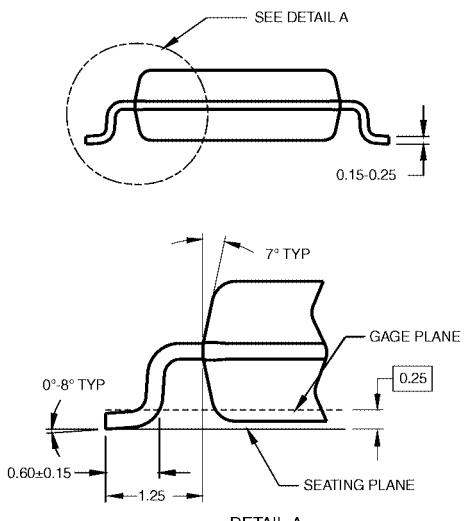


DIMENSIONS ARE IN MILLIMETERS

NOTES:

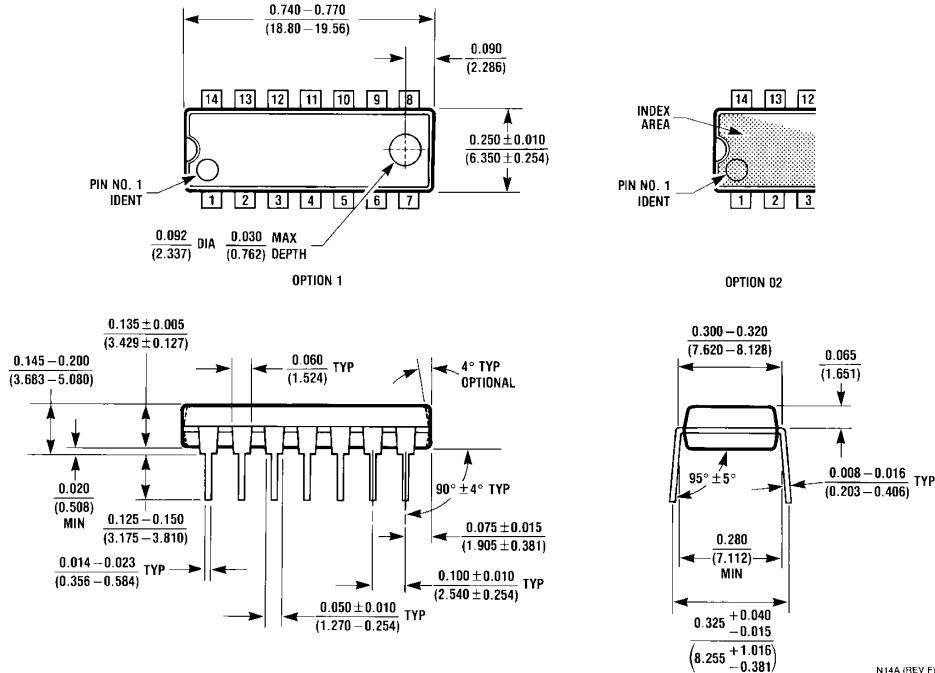
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

N14A (REV F)

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