

Feb.28,2002 Ver.1
Under Development

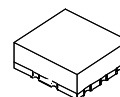
SPDT SWITCH GaAs MMIC

■GENERAL DESCRIPTION

The NJG1543HB3 is a GaAs SPDT switch MMIC which features low loss, high isolation and low control current and ideally suitable for switching the RF receiving circuit of cellular phone.

This switch is operated in the wide frequency range from 100MHz to 3GHz at low voltage from 2.5V.

■PACKAGE OUTLINE



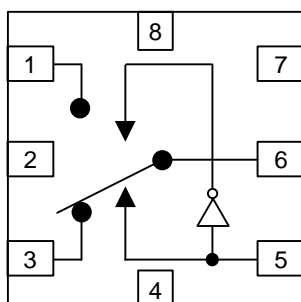
NJG1543HB3

■FEATURES

- Low voltage operation +2.7V typ.
- Low insertion loss 0.5dB typ. @f=2.0GHz, $P_{IN}=22\text{dBm}$
0.6dB typ. @f=2.5GHz, $P_{IN}=22\text{dBm}$
- High isolation 26dB typ. @f=2.0GHz, $P_{IN}=22\text{dBm}$
25dB typ. @f=2.5GHz, $P_{IN}=22\text{dBm}$
- Low current consumption 30uA typ. @2.5GHz, $P_{IN}=22\text{dBm}$
- Low control current 15uA typ. @2.5GHz
- Package USB8-B3 (Package size: 1.5x1.5x0.8mm)

■PIN CONFIGURATION

Top view



Pin Connection

- 1.P1
- 2.GND
- 3.P2
- 4.GND
- 5.VCTL
- 6.PC
- 7.VDD
- 8.GND

■TRUTH TABLE

Control Voltage: "H"= $V_{CTL(H)}$, "L"= $V_{CTL(L)}$

VCTL	H	L
PC-P1	ON	OFF
PC-P2	OFF	ON

■ABSOLUTE MAXIMUM RATINGS

($T_a=25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
Input Power	P_{IN}	$V_{DD}=2.7\text{V}$, $V_{CTL}=0\text{V}/2.7\text{V}$	32	dBm
Supply Voltage	V_{DD}	VDD terminal	7.5	V
Control Voltage	V_{CTL}	VCTL terminal	7.5	V
Power Dissipation	P_D		450	mW
Operating Temp.	T_{opr}		-40~+85	$^{\circ}\text{C}$
Storage Temp.	T_{stg}		-55~+125	$^{\circ}\text{C}$

■ELECTRICAL CHARACTERISTICS

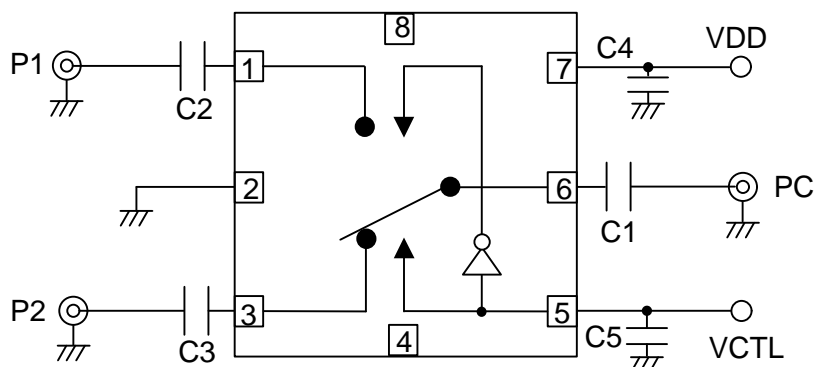
(General conditions: $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=2.7\text{V}$, $Z_s=Z_l=50\Omega$, $T_a=25^{\circ}\text{C}$)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		2.5	2.7	6.5	V
Operating Current	I_{DD}	$f=2.5\text{GHz}$, $P_{IN}=22\text{dBm}$	-	30	50	μA
Control Voltage (LOW)	$V_{CTL(L)}$		0.0	-	0.8	V
Control Voltage (HIGH)	$V_{CTL(H)}$		2.0	-	V_{DD}	V
Control Current	I_{CTL}	$f=2.5\text{GHz}$, $P_{IN}=22\text{dBm}$	-	15	30	μA
Insertion Loss 1	Loss1	$f=2.0\text{GHz}$, $P_{IN}=22\text{dBm}$	-	0.5	0.7	dB
Insertion Loss 2	Loss2	$f=2.5\text{GHz}$, $P_{IN}=22\text{dBm}$	-	0.6	0.8	dB
Isolation 1	ISL1	$f=2.0\text{GHz}$, $P_{IN}=22\text{dBm}$	24	26	-	dB
Isolation 2	ISL2	$f=2.5\text{GHz}$, $P_{IN}=22\text{dBm}$	22	25	-	dB
Pout at 1dB compression point	$P_{-1\text{dB}}$	$f=2.5\text{GHz}$	27	30	-	dBm
VSWR	VSWR	$f=0.1\sim 2.5\text{GHz}$, ON state	-	1.4	1.6	
Switching Time	T_{SW}	$f=0.1\sim 2.5\text{GHz}$	-	1	-	μs

■ TERMINAL INFORMATION

Pin	Symbol	Description
1	P1	RF port. This port is connected with PC port by controlling 5 pin (VCTL) to 2.0V~V _{DD} . An external capacitor is required to block the DC bias voltage of internal circuit.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	P2	RF port. This port is connected with PC port by controlling 5 pin (VCTL) to 0V~+0.8V. An external capacitor is required to block the DC bias voltage of internal circuit.
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
5	VCTL	Control port. This terminal is set to High-Level by 2V~V _{DD} , and Low-Level by +0.8~0V.
6	PC	Common RF port. In order to block the DC bias voltage of internal circuit, an external capacitor is required.
7	VDD	Positive voltage supply terminal. The positive voltage (+2.5~+6.5V) have to be supplied. The bypass capacitor should be connected with GND as close as possible for excellent RF performance.
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.

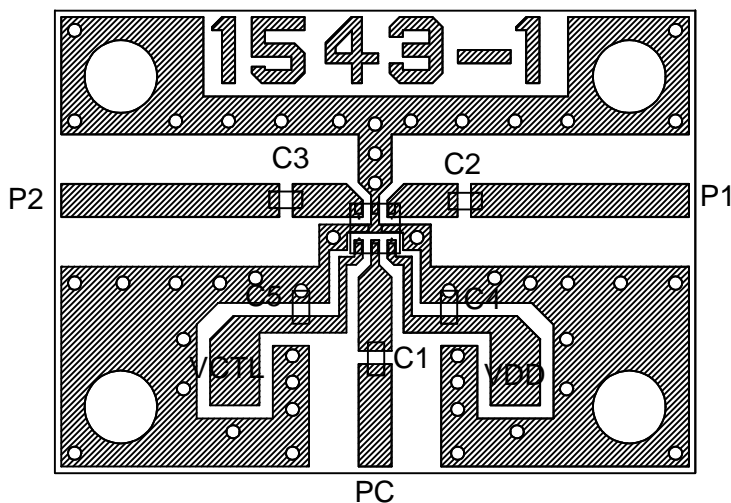
APPLICATION CIRCUIT



Parts list

Parts ID	CONSTANT	COMMENT
C1~C3	56pF	MURATA (GRM36, 1005size)
C4, C5	10pF	MURATA (GRM36, 1005size)

RECOMMENDED PCB DESIGN



PCB:FR-4, t=0.5mm
 Capacitor: Size 1005
 Strip Line Width=1.0mm
 PCB Size: 19.4x14.0mm

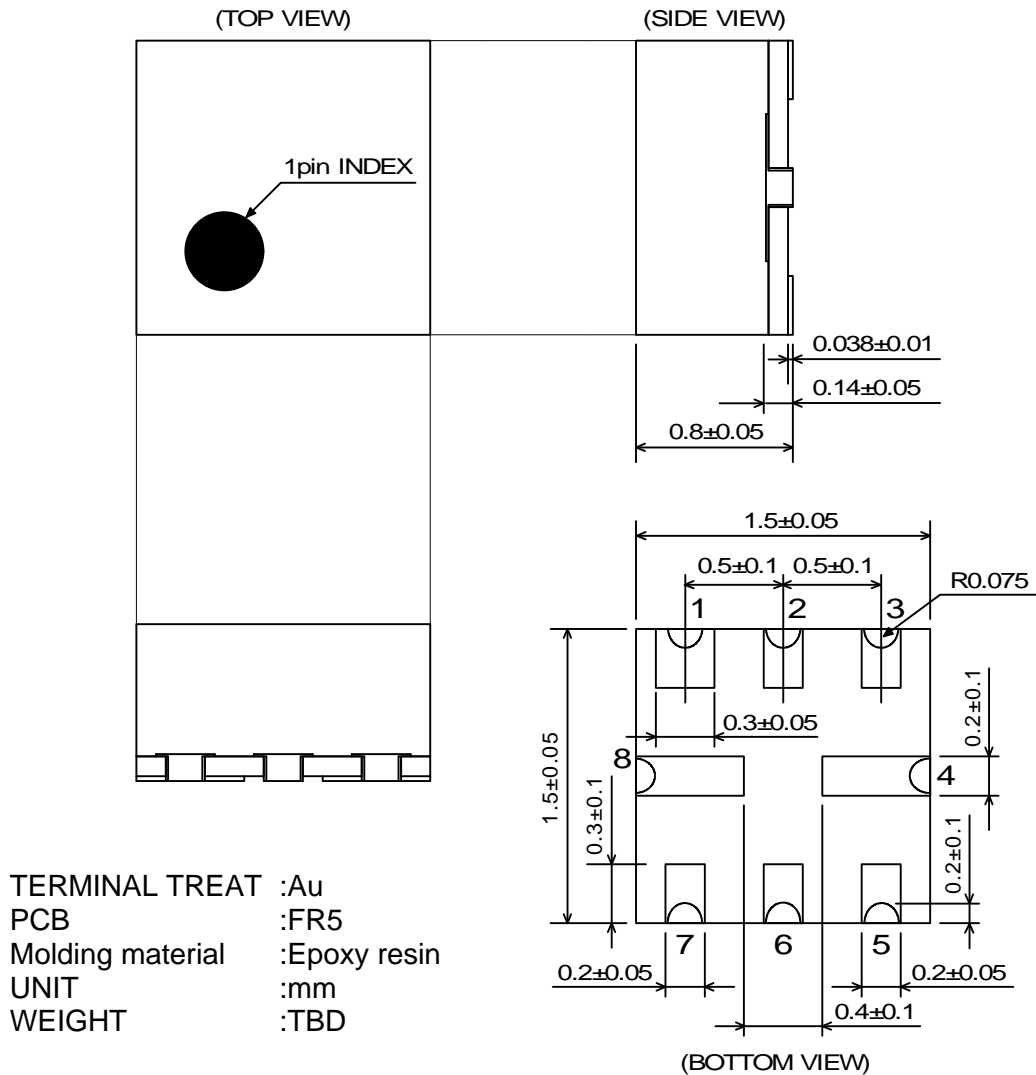
Circuit losses including losses
 of capacitors and connectors

freq (GHz)	Loss (dB)
0.8	0.11
1.0	0.12
1.5	0.16
1.8	0.19
2.0	0.21
2.5	0.27

PRECAUTIONS

- [1] The DC blocking capacitor have to be placed at RF terminal of PC1, PC2, PC.
- [2] To reduce stripline influence on RF characteristics, please locate bypass capacitors (C4, C5) close to each terminal.
- [3] To avoid degradation of isolation or high power characteristics, please layout ground pattern right under this IC.

■PACKAGE OUTLINE (USB8-B3)



Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle