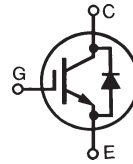


High Voltage, High Gain BiMOSFET™

IXBL64N250

Monolithic Bipolar MOS Transistor

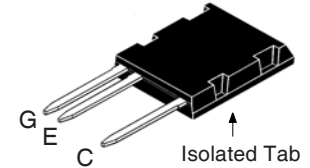
(Electrically Isolated Tab)



$$\begin{aligned} V_{CES} &= 2500V \\ I_{C110} &= 46A \\ V_{CE(sat)} &\leq 3.0V \end{aligned}$$

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	2500	V
V_{CGR}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}, R_{GE} = 1M\Omega$	2500	V
V_{GES}	Continuous	± 25	V
V_{GEM}	Transient	± 35	V
I_{C25}	$T_C = 25^\circ\text{C}$	116	A
I_{C110}	$T_C = 110^\circ\text{C}$	46	A
I_{CM}	$T_C = 25^\circ\text{C}, 1\text{ms}$	750	A
SSOA	$V_{GE} = 15V, T_{VJ} = 125^\circ\text{C}, R_G = 1\Omega$	$I_{CM} = 160$	A
(RBSOA)	Clamped Inductive Load	$V_{CE} \leq 0.8 \cdot V_{CES}$	
T_{SC} (SCSOA)	$V_{GE} = 15V, T_J = 125^\circ\text{C}$ $R_G = 5\Omega, V_{CE} = 1250V, \text{Non-Repetitive}$	10	μs
P_C	$T_C = 25^\circ\text{C}$	500	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	$^\circ\text{C}$
V_{ISOL}	50/60Hz, 1 minute	2500	V~
F_C	Mounting Force with Clip	30..170 / 7..36	Nm/lb-in.
Weight		8	g

ISOPLUS i5-Pak™



G = Gate C = Collector
E = Emitter

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- High Blocking Voltage
- Low Switching Losses
- High Current Handling Capability
- Anti-Parallel Diode

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterrupted Power Supplies (UPS)
- Capacitor Discharge Circuits
- Laser Generators

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 1\text{mA}, V_{GE} = 0V$	2500		V
$V_{GE(th)}$	$I_C = 4\text{mA}, V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = 0.8 \cdot V_{CES}, V_{GE} = 0V$ Note 2, $T_J = 125^\circ\text{C}$			50 μA 6 mA
I_{GES}	$V_{CE} = 0V, V_{GE} = \pm 25V$			± 200 nA
$V_{CE(sat)}$	$I_C = 64A, V_{GE} = 15V$, Note 1 $T_J = 125^\circ\text{C}$		2.5 3.1	V V

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Characteristic Values

Min. Typ. Max.

g_{fs}	$I_C = 64\text{A}, V_{CE} = 10\text{V}, \text{Note 1}$	40	72	S
C_{ies}	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		8900	pF
C_{oes}			345	pF
C_{res}			118	pF
Q_g	$I_C = 64\text{A}, V_{GE} = 15\text{V}, V_{CE} = 600\text{V}$		400	nC
Q_{ge}			46	nC
Q_{gc}			155	nC
$t_{d(on)}$	Resistive Switching Times, $T_J = 25^\circ\text{C}$ $I_C = 128\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1250\text{V}, R_G = 1\Omega$		49	ns
t_r			318	ns
$t_{d(off)}$			232	ns
t_f			170	ns
$t_{d(on)}$	Resistive Switching Times, $T_J = 125^\circ\text{C}$ $I_C = 128\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1250\text{V}, R_G = 1\Omega$		54	ns
t_r			578	ns
$t_{d(off)}$			222	ns
t_f			175	ns
R_{thJC}				0.25 $^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$

Reverse Diode

Symbol Test Conditions

($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Characteristic Values

Min. Typ. Max

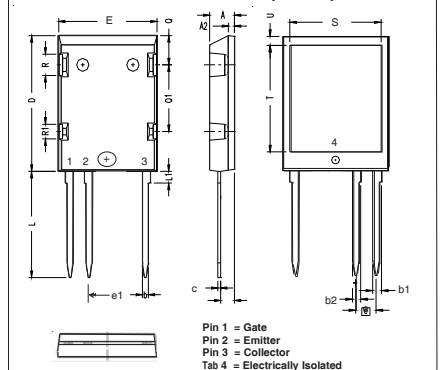
V_F	$I_F = 64\text{A}, V_{GE} = 0\text{V}, \text{Note 1}$		3.0	V
t_{rr}	$I_F = 64\text{A}, V_{GE} = 0\text{V}, -di_F/dt = 650\text{A}/\mu\text{s}$ $V_R = 600\text{V}, V_{GE} = 0\text{V}$		160	ns
I_{RM}			480	A

Notes:

1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. Part must be heatsunk for high-temp I_{ces} measurement.

Additional provisions for lead-to-lead isolation are required at $V_{CE} > 1200\text{V}$

ISOPLUS i5-Pak™ HV (IXBL) Outline



SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	0.190	0.205	4.83	5.21
A1	0.102	0.118	2.59	3.00
A2	0.046	0.055	1.17	1.40
b	0.045	0.055	1.14	1.40
b1	0.063	0.072	1.60	1.83
b2	0.058	0.068	1.47	1.73
c	0.020	0.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	0.770	0.799	19.56	20.29
e	0.150 BSC		3.81 BSC	
e1	0.450 BSC		11.43 BSC	
L	0.780	0.820	19.81	20.83
L1	0.080	0.102	2.03	2.59
Q	0.210	0.235	5.33	5.97
Q1	0.490	0.513	12.45	13.03
R	0.150	0.180	3.81	4.57
R1	0.100	0.130	2.54	3.30
S	0.668	0.690	16.97	17.53
T	0.801	0.821	20.34	20.85
U	0.065	0.080	1.65	2.03

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

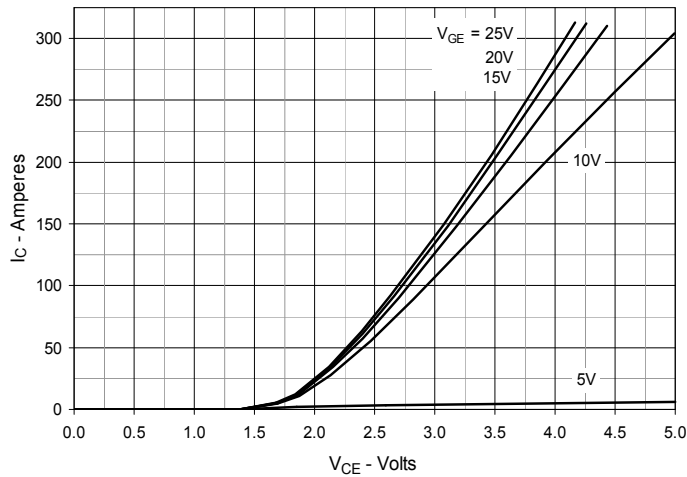


Fig. 2. Output Characteristics @ $T_J = 125^\circ\text{C}$

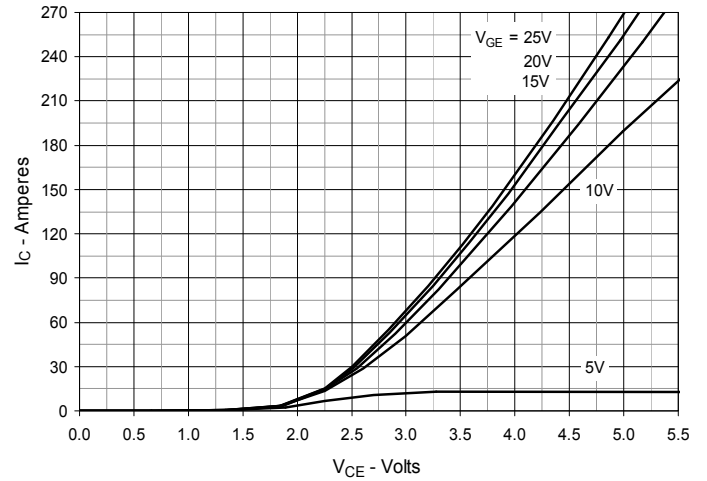


Fig. 3. Dependence of $V_{CE(sat)}$ on Junction Temperature

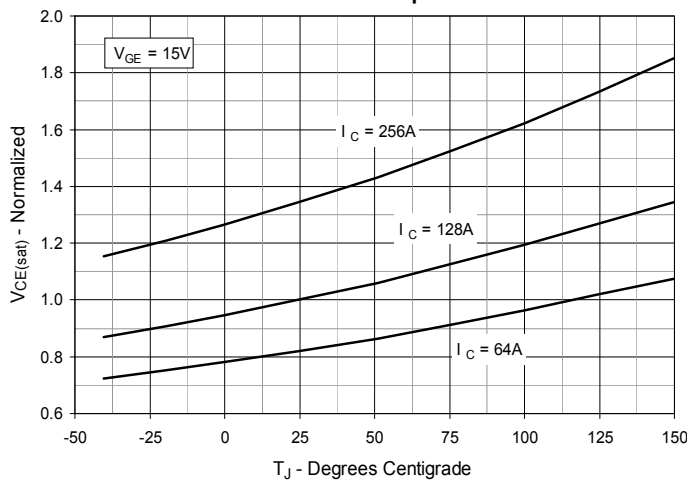


Fig. 4. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

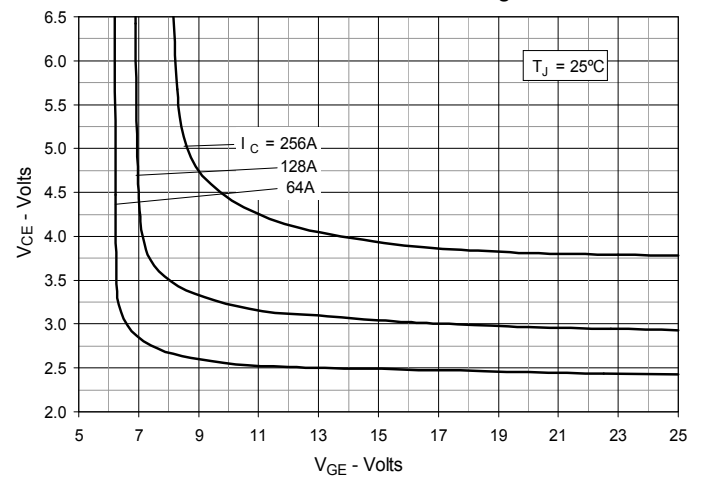


Fig. 5. Breakdown & Threshold Voltages vs. Junction Temperature

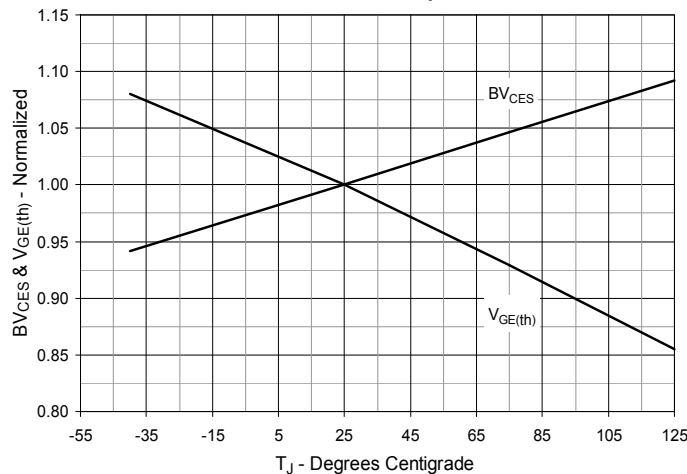


Fig. 6. Input Admittance

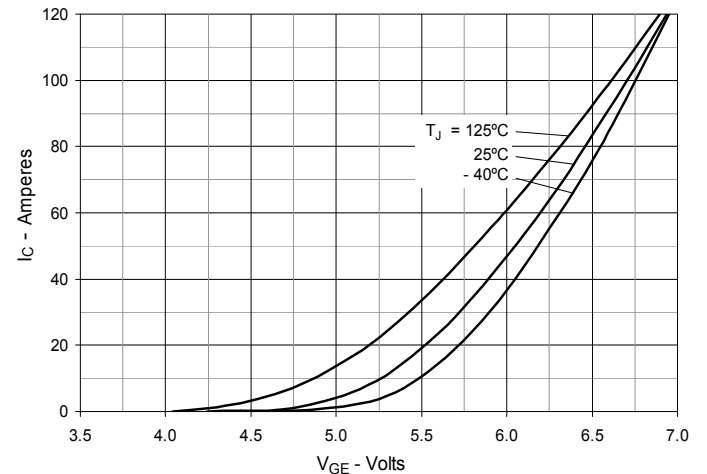


Fig. 7. Transconductance

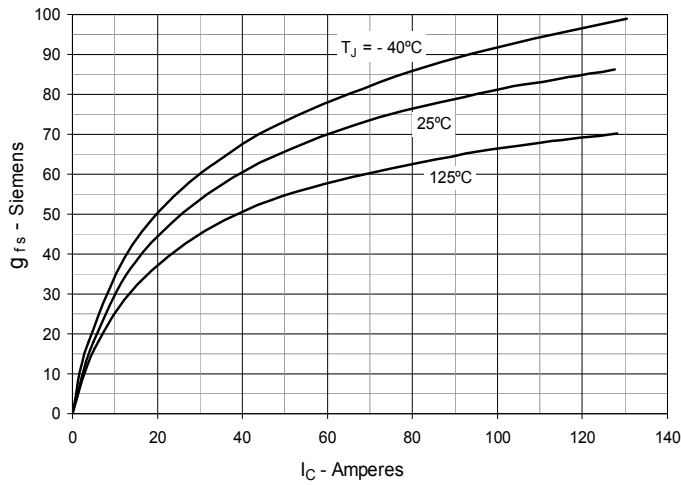


Fig. 8. Forward Voltage Drop of Intrinsic Diode

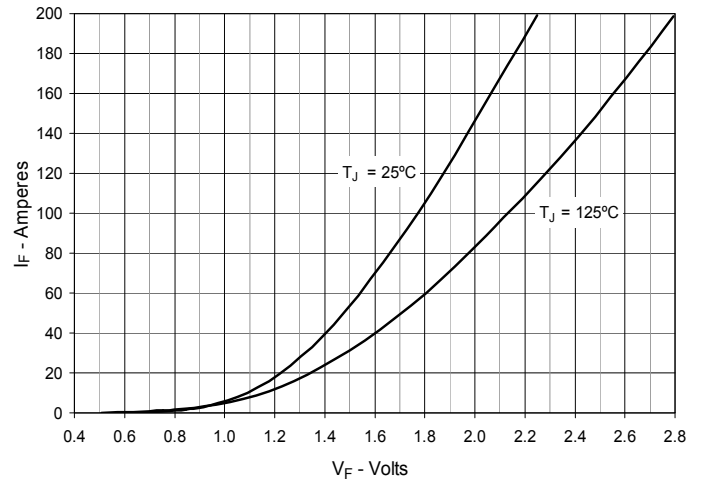


Fig. 9. Gate Charge

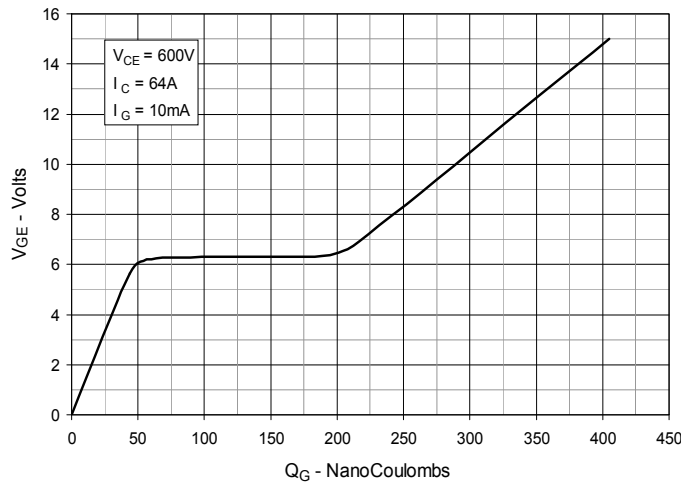


Fig. 10. Capacitance

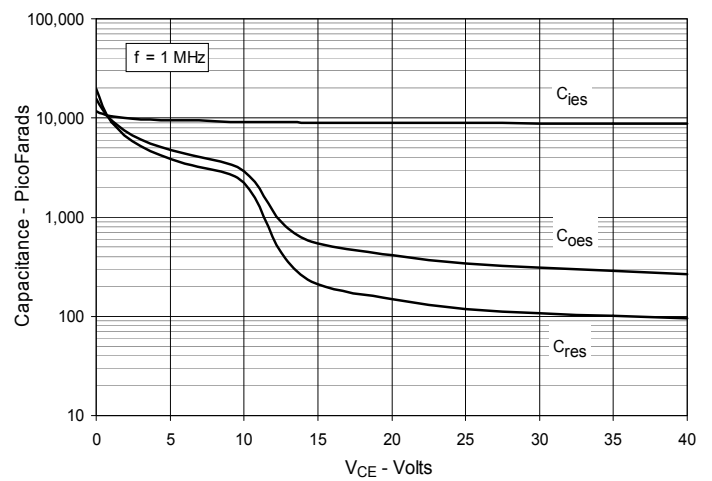


Fig. 11. Reverse-Bias Safe Operating Area

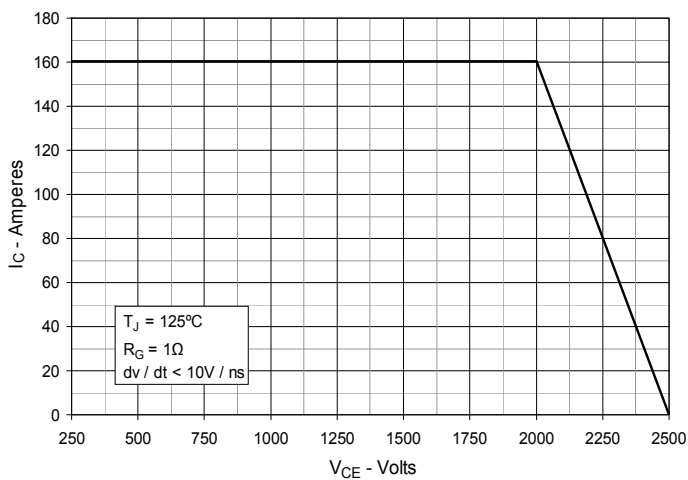


Fig. 12. Maximum Transient Thermal Impedance

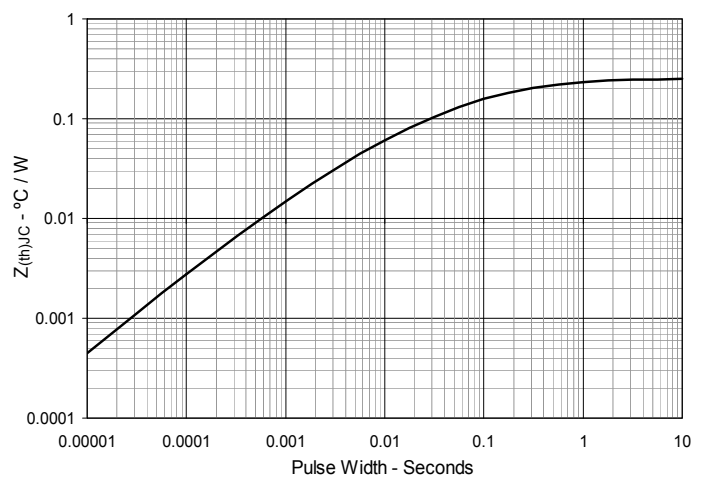


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

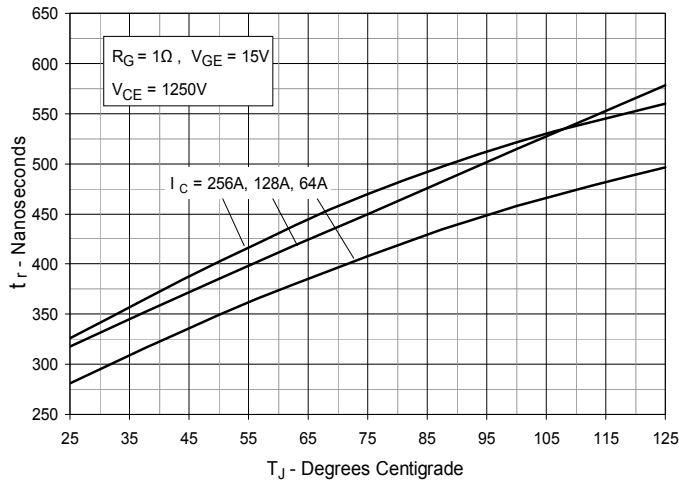


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

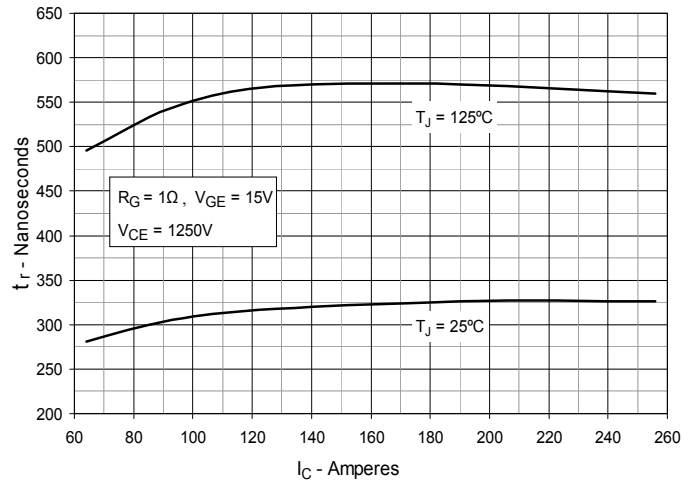


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

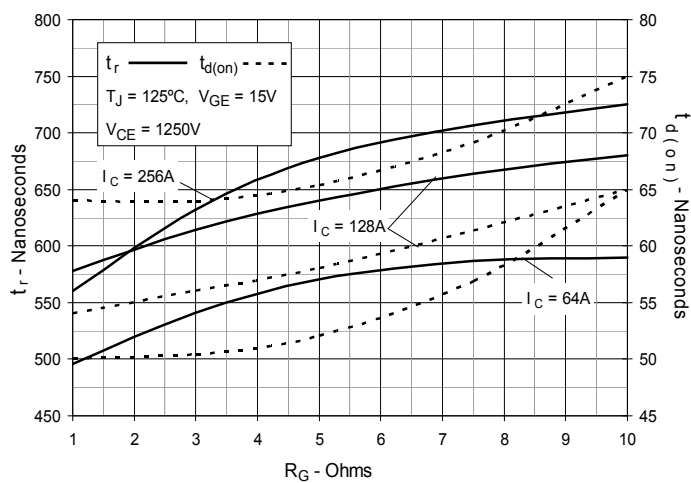


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

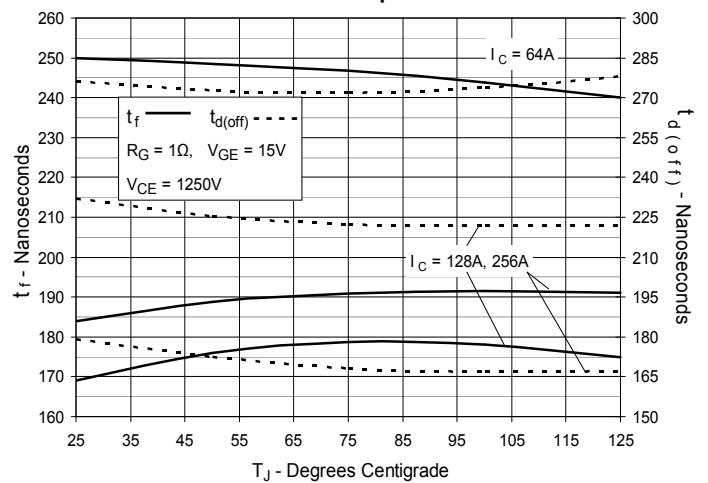


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

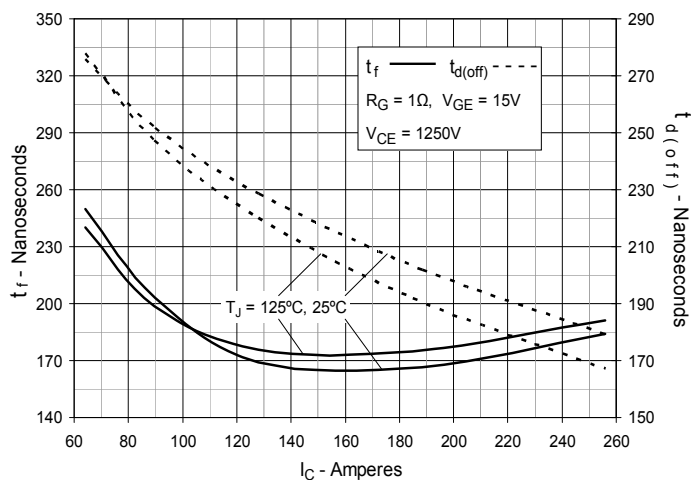


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

