R2J20604NP

Integrated Driver – MOS FET (DrMOS)

REJ03G1605-0200
Rev.2.00
Jun 30, 2008

Description

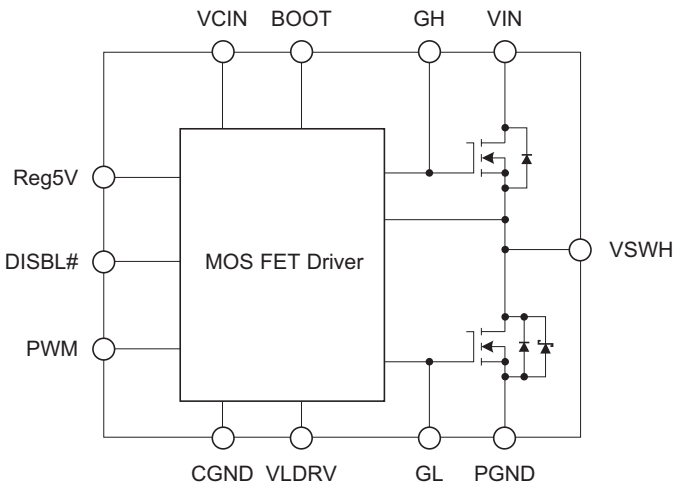
The R2J20604NP multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. The on and off timing of the power MOS FET is optimized by the built-in driver, making this device suitable for large-current buck converters. The chip also incorporates a high-side bootstrap Schottky barrier diode (SBD), eliminating the need for an external SBD for this purpose.

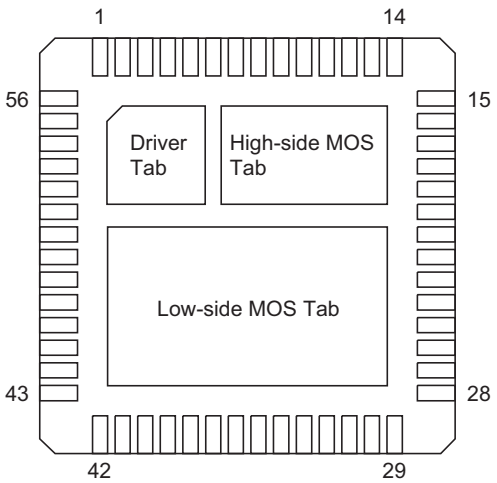
Integrating a driver and both high-side and low-side power MOS FETs, the new device is also compliant with the package standard "Integrated Driver – MOS FET (DrMOS)" proposed by Intel Corporation.

Features

- Built-in power MOS FET suitable for applications with 12 V input and low output voltage
- Built-in driver circuit which matches the power MOS FET
- Built-in tri-state input function which can support a number of PWM controllers
- Capable of 3.3 V PWM signal
- VIN operating-voltage range: 16 V max
- High-frequency operation (above 1 MHz) possible
- Large average output current (Max. 40 A)
- Achieve low power dissipation (About 4.4 W at 1 MHz, 25 A)
- Controllable driver: Remote on/off
- Built-in Schottky diode for bootstrapping
- Low-side drive voltage can be independently set
- Small package: QFN56 (8 mm × 8 mm × 0.95 mm)
- Terminal Pb-free

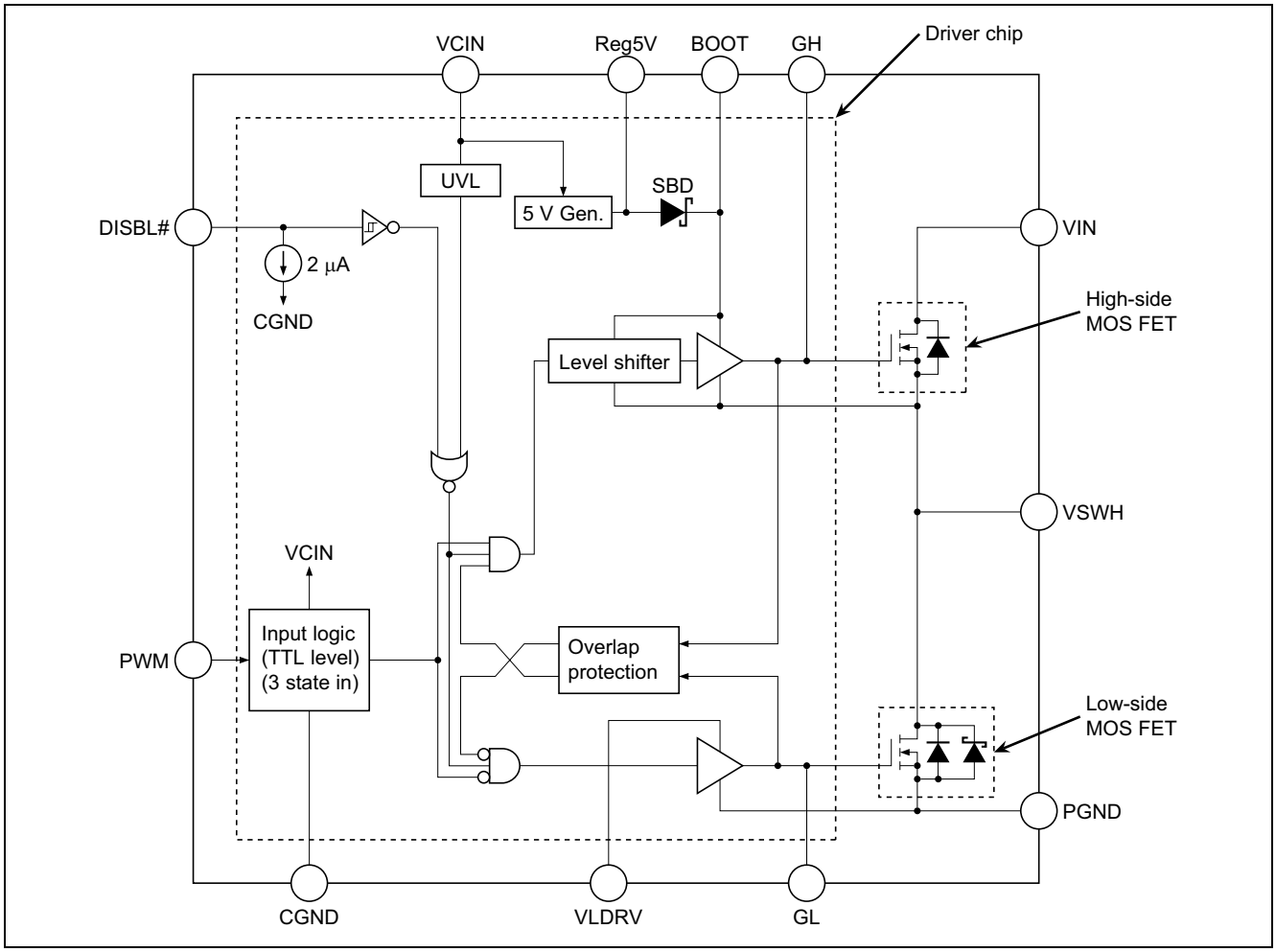
Outline





(Bottom view)
QFN56 package 8 mm × 8 mm

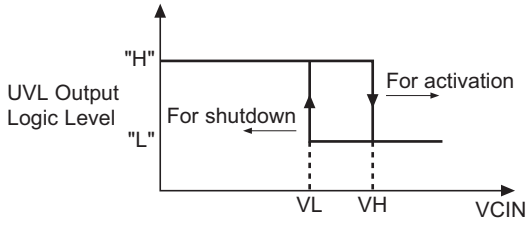
Block Diagram



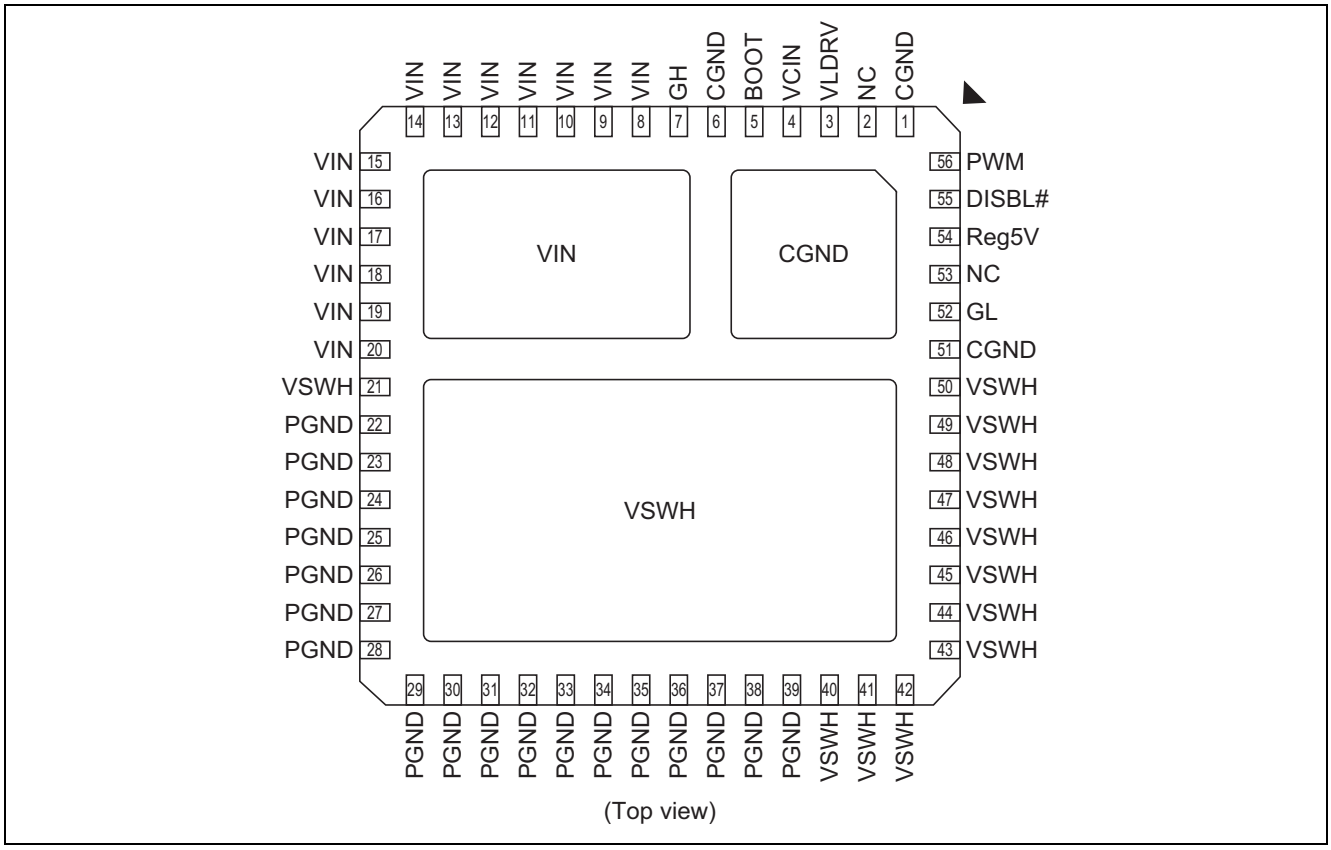
Notes: 1. Truth table for the DISBL# pin.

DISBL# Input	Driver Chip Status
“L”	Shutdown (GL, GH = “L”)
“Open”	Shutdown (GL, GH = “L”)
“H”	Enable (GL, GH = “Active”)

2. Output signal from the UVL block



Pin Arrangement



Note: All die-pads (three pads in total) should be soldered to PCB.

Pin Description

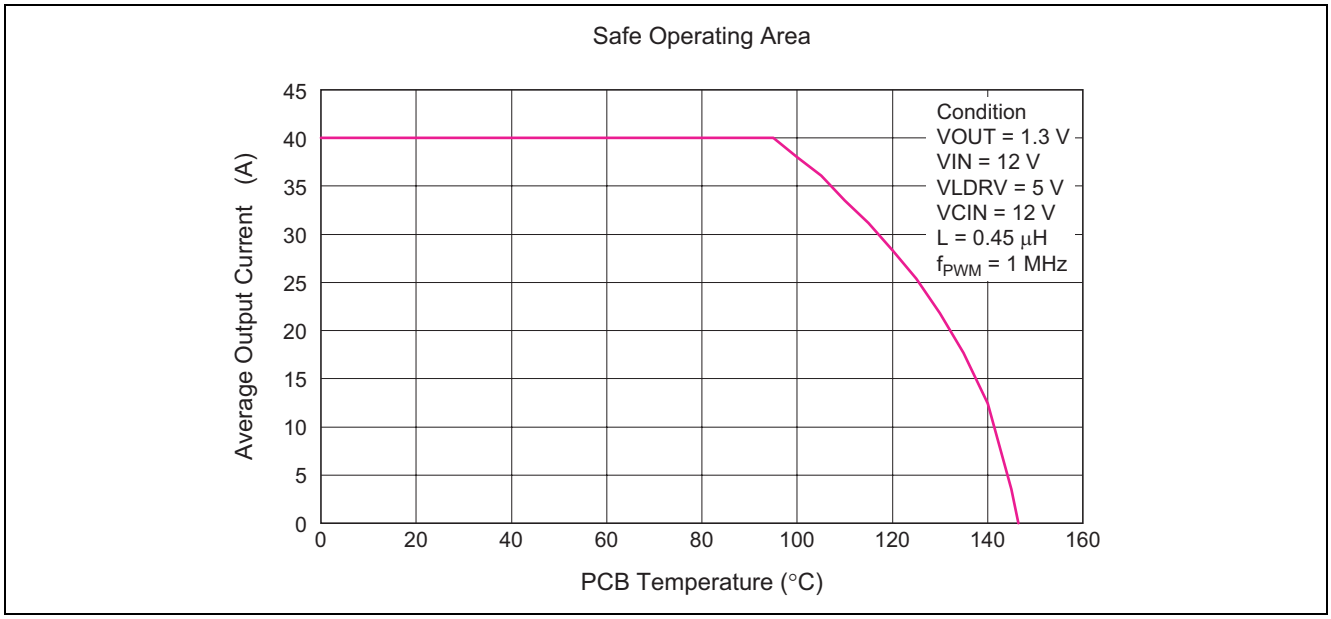
Pin Name	Pin No.	Description	Remarks
CGND	1, 6, 51, Tab	Control signal ground	Should be connected to PGND externally
NC	2, 53	No connect	
VLDRV	3	Low side gate supply voltage	For 5 V to 12 V gate drive voltage for Low side gate driver
VCIN	4	Control input voltage (+12 V input)	Driver Vcc input
BOOT	5	Bootstrap voltage pin	To be supplied +5 V through internal SBD
GH	7	High side gate signal	Pin for Monitor
VIN	8 to 20, Tab	Input voltage	
VSWH	21, 40 to 50, Tab	Phase output/Switch output	
PGND	22 to 39	Power ground	
GL	52	Low side gate signal	Pin for Monitor
Reg5V	54	+5 V logic power supply output	
DISBL#	55	Signal disable	Disabled when DISBL# is “L”
PWM	56	PWM drive logic input	

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Units	Note
Power dissipation	Pt(25)	25	W	1
	Pt(110)	8	W	1
Average output current	Iout	40	A	
Input voltage	VIN (DC)	–0.3 to +16	V	2
	VIN (AC)	20		2, 6
Supply voltage	VCIN (DC)	–0.3 to +16	V	2
	VCIN (AC)	20		2, 6
Low side driver voltage	VLDRV (DC)	–0.3 to +16	V	2
	VLDRV (AC)	20		2, 6
Switch node voltage	VSWH (DC)	16	V	2
	VSWH (AC)	20		2, 6
BOOT voltage	VBOOT (DC)	22	V	2
	VBOOT (AC)	25		2, 6
DISBL# voltage	Vdisble	–0.3 to VCIN	V	2
PWM voltage	Vpwm	–0.3 to +5.5	V	2, 4
		–0.3 to +0.3	V	2, 5
Reg5V current	Ireg5V	–10 to +0.1	mA	3
Operating junction temperature	Tj-opr	–40 to +150	°C	
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Pt(25) represents a PCB temperature of 25°C, and Pt(110) represents 110°C.
2. Rated voltages are relative to voltages on the CGND and PGND pins.
3. For rated current, (+) indicates inflow to the chip and (–) indicates outflow.
4. This rating is when UVL (Under Voltage Lock out) is ineffective (normal operation mode).
5. This rating is when UVL (Under Voltage Lock out) is effective (lock out mode).
6. The specification values indicated “AC” are limited within 100 ns.



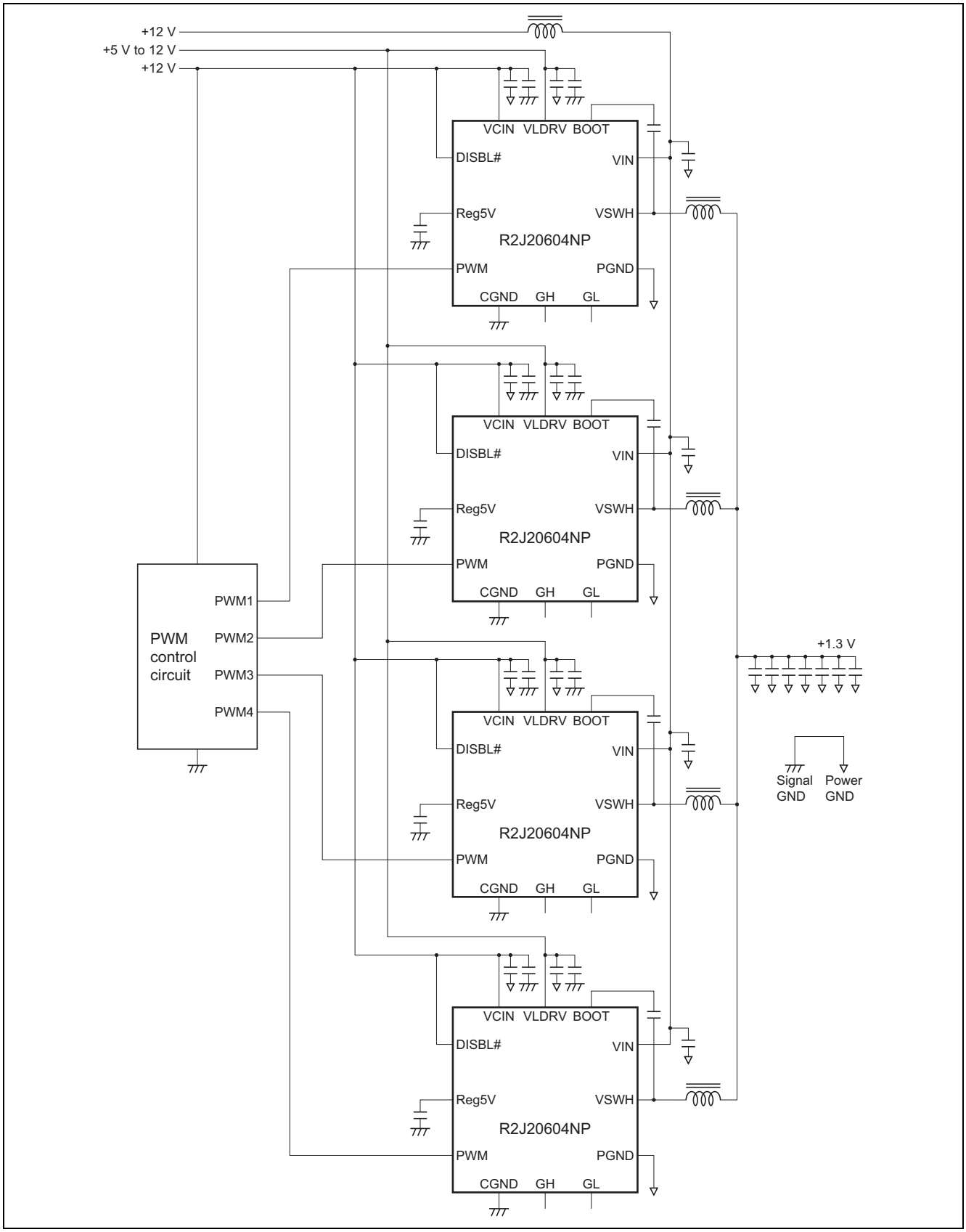
Electrical Characteristics

(Ta = 25°C, VCIN = 12 V, VLDRV = 5 V, VSWH = 0 V, unless otherwise specified)

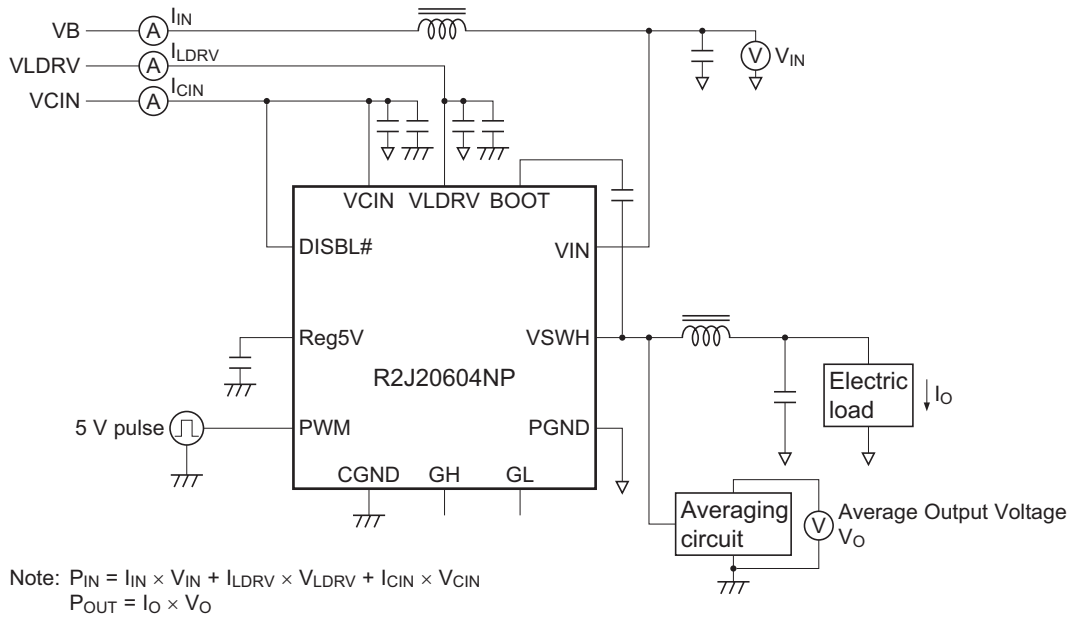
Item		Symbol	Min	Typ	Max	Units	Test Conditions
Supply	VCIN start threshold	V_H	7.0	7.4	7.8	V	
	VCIN shutdown threshold	V_L	6.6	7.0	7.4	V	
	UVLO hysteresis	dUVL	—	0.4 *1	—	V	$V_H - V_L$
	VCIN bias current	I_{CIN}	10.5	14.0	18.5	mA	f_{PWM} = 1 MHz, $t_{on\text{-}PWM}$ = 125 ns
	VLDRV bias current	I_{LDRV}	35.5	44.0	52.5	mA	f_{PWM} = 1 MHz, $t_{on\text{-}PWM}$ = 125 ns
PWM Input	PWM rising threshold	$V_{H\text{-}PWM}$	1.7	2.1	2.5	V	
	PWM falling threshold	$V_{L\text{-}PWM}$	0.9	1.2	1.5	V	
	PWM input resistance	$R_{IN\text{-}PWM}$	11	22	33	kΩ	$\frac{4\text{ V} - 1\text{ V}}{I_{PWM}(V_{PWM} = 4\text{ V}) - I_{PWM}(V_{PWM} = 1\text{ V})}$
	Tri-state shutdown window	$V_{IN\text{-}SD}$	$V_{L\text{-}PWM}$	—	$V_{H\text{-}PWM}$	V	
	Shutdown hold-off time	$t_{HOLD\text{-}OFF}$	—	240 *1	—	ns	
5V Regulator	Output voltage	Vreg	4.95	5.2	5.45	V	
	Line regulation	Vreg-line	–10	0	10	mV	VCIN = 12 V to 16 V
	Load regulation	Vreg-load	–10	0	10	mV	Ireg = 0 to 10 mA
DISBL# Input	Disable threshold	V_{DISBL}	0.9	1.2	1.5	V	
	Enable threshold	V_{ENBL}	1.9	2.4	2.9	V	
	Input current	I_{DISBL}	0.5	2.0	5.0	μA	DISBL# = 1 V

Note: 1. Reference values for design. Not 100% tested in production.

Typical Application

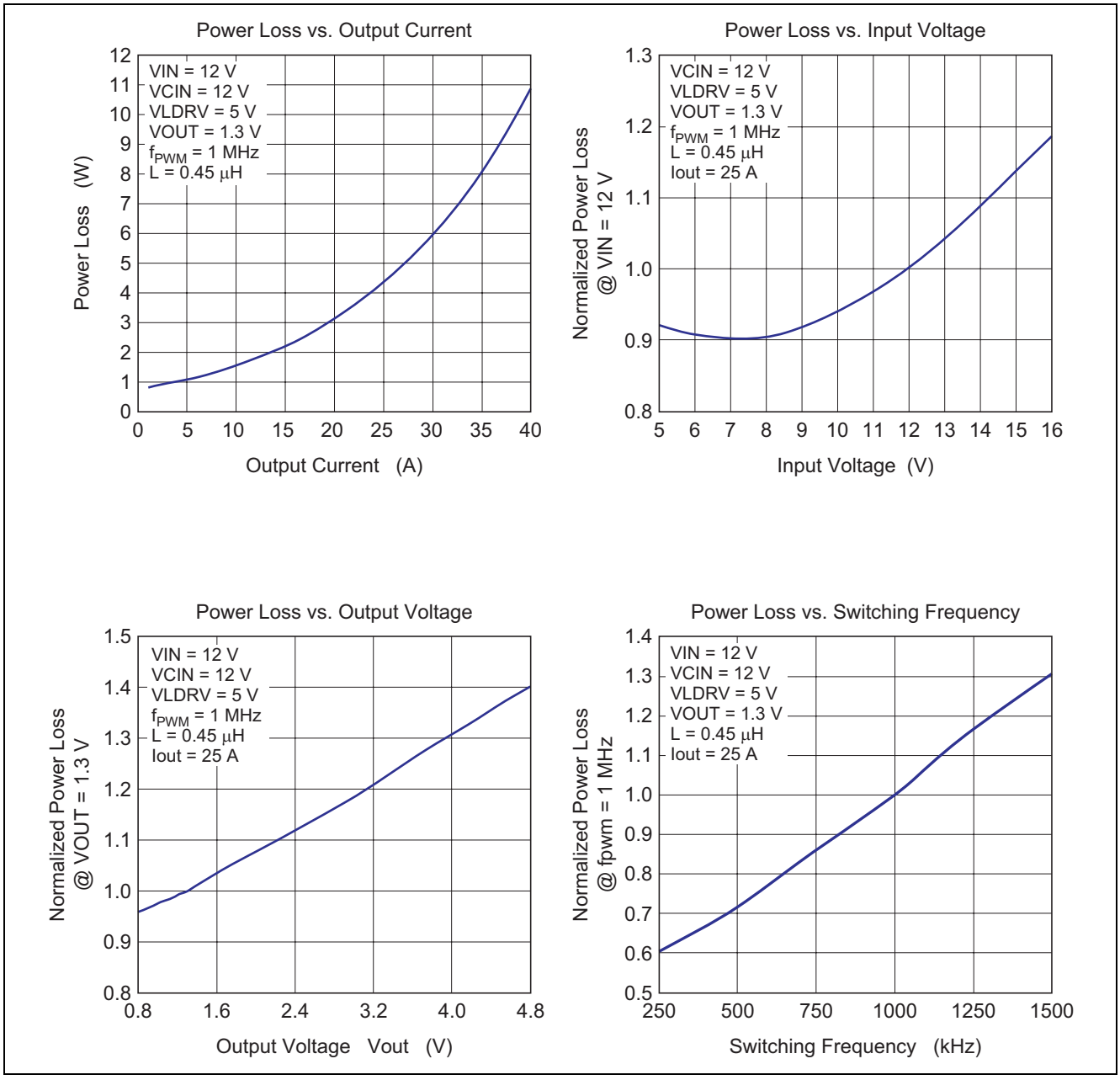


Test Circuit

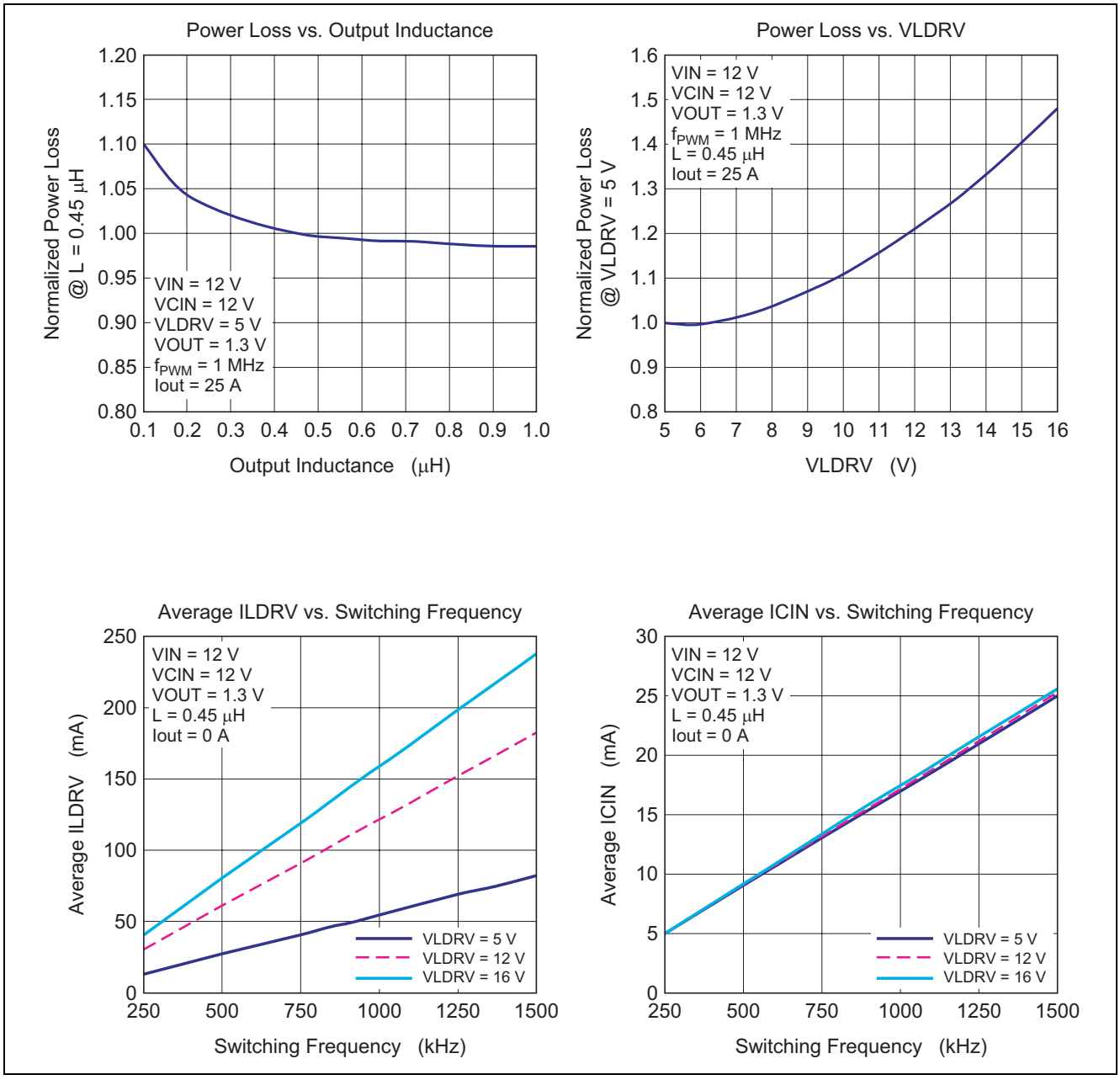


Note: $P_{IN} = I_{IN} \times V_{IN} + I_{LDRV} \times V_{LDRV} + I_{CIN} \times V_{CIN}$
$P_{OUT} = I_O \times V_O$
Efficiency = P_{OUT} / P_{IN}
P_{LOSS}(DrMOS) = $P_{IN} - P_{OUT}$
Ta = 27°C

Typical Data



Typical Data (cont.)



Description of Operation

The DrMOS multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. Since the parasitic inductance between each chip is extremely small, the module is highly suitable for use in buck converters to be operated at high frequencies. The control timing between the high-side MOS FET, low-side MOS FET, and driver is optimized so that high efficiency can be obtained at low output-voltage.

Driver

The driver has two types of power-supply voltage input pin, VCIN and VLDRV. VCIN supplies the operating voltage to the internal logic circuit. The low-side driving voltage is applied to VLDRV, so setting of the gate-driving voltage for the low-side MOS FET is independent of the voltage on VCIN. The VLDRV setting voltage is from 5 V to 16 V.

The VCIN pin is connected to the UVL (under-voltage lockout) module, so that the driver is disabled as long as VCIN is 7.4 V or less. On cancellation of UVL, the driver remains enabled until the UVL input is driven to 7.0 V or less. The signal on pin DISBL# also enables or disables the circuit. When UVL disables the circuit, the built-in 5 V regulator does not operate, but when the signal on DISBL# disables the circuit, only output-pulse generation is terminated, and the 5 V regulator is not disabled.

VCIN	VLDRV	DISBL#	Reg5V	Driver State
L	> 5 V	*	0	Disable (GL, GH = L)
H	> 5 V	L	5 V	Disable (GL, GH = L)
H	> 5 V	H	5 V	Active
H	> 5 V	Open	5 V	Disable (GL, GH = L)

Voltages from –0.3 V to VCIN can be applied to the DISBL# pin, so on/off control by a logic IC or the use of a resistor, etc., to pull the DISBL# line up to VCIN are both possible.

The built-in 5 V regulator is a series regulator with temperature compensation. The voltage output by this regulator determines the operating voltage of the internal logic and gate-voltage swing for the high-side MOS FET. A ceramic capacitor with a value of 0.1 μF or more must be connected between the CGND plane and the Reg5V pin.

The PWM pin is the signal input pin for the driver chip. The input-voltage range is –0.3 V to (Reg5V + 3 V). When the PWM input is high, the gate of the high-side MOS FET (GH) is high and the gate of the low-side MOS FET (GL) is low.

PWM	GH	GL
L	L	H
H	H	L

The PWM input is TTL level and has hysteresis. When the PWM input signal is abnormal, e.g., when the signal route from the control IC is abnormal, the tri-state function turns off the high- and low-side MOS FETs. This function operates when the PWM input signal stays in the input hysteresis window for 240 ns (typ.). After the tri-state mode has been entered and GH and GL have become low, a PWM input voltage of 2.1 V or more is required to make the circuit return to normal operation.

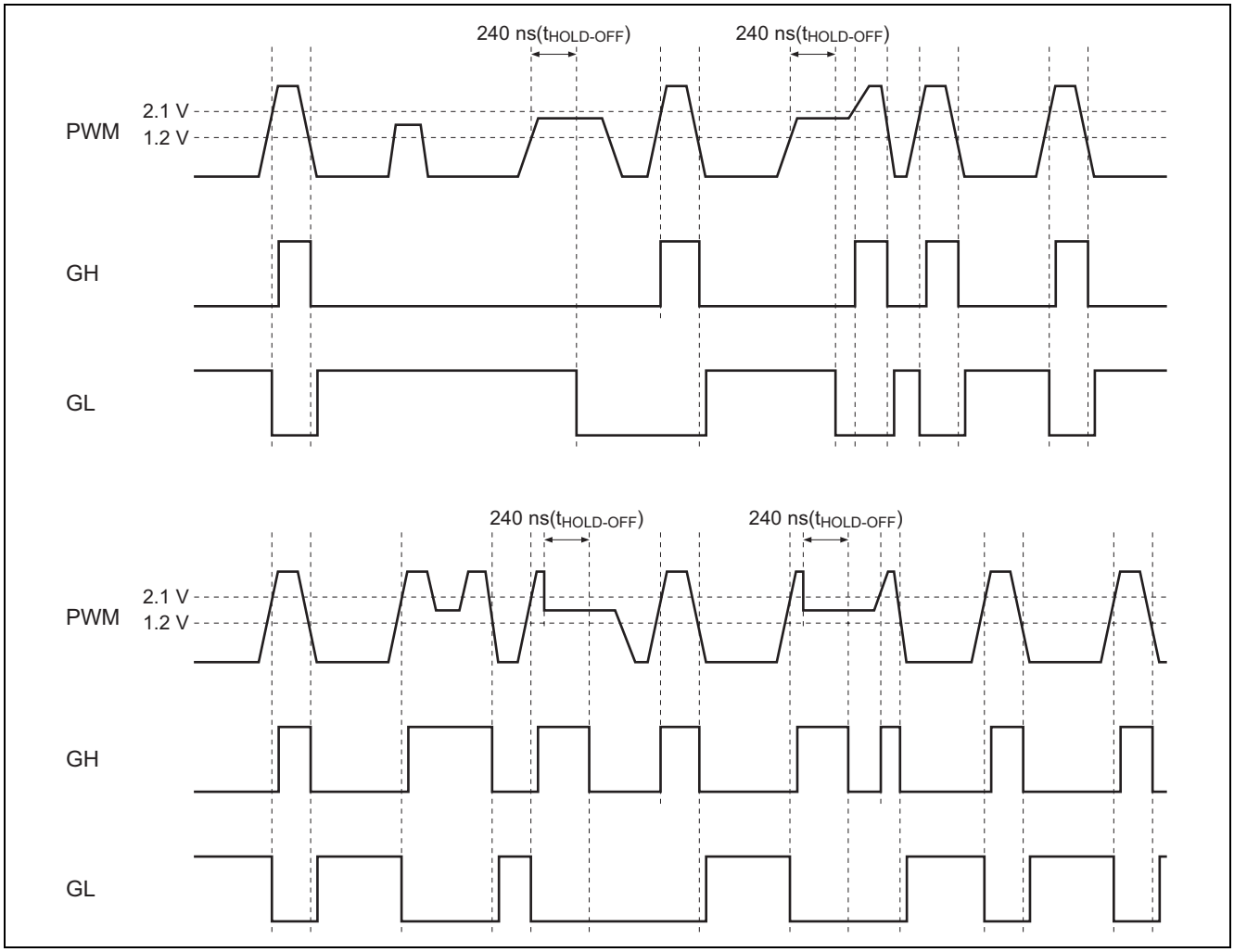


Figure 1

For the high-side driver, the BOOT pin is the power-supply voltage pin and voltage VSWH provides a standard for operation of the high-side driving circuit. Consequently, the difference between the voltage on the BOOT and VSWH pins becomes the gate swing for the high-side MOS FET. Connect a bootstrap capacitor between the BOOT pin and the VSWH pin. Since the Schottky barrier diode (SBD) is connected between the BOOT and Reg5V pins, this bootstrap capacitor is charged up to 5 V. When the high-side MOS FET is turned on, voltage VSWH becomes equal to VIN, so VBOOT is boosted to VSWH + 5 V.

The GH and GL pins are the gate-monitor pins for each MOS FET.

MOS FETs

The MOS FETs incorporated in R2J20604NP are highly suitable for synchronous-rectification buck conversion. For the high-side MOS FET, the drain is connected to the VIN pin and the source is connected to the VSWH pin. For the low-side MOS FET, the drain is connected to the VSWH pin and the source is connected to the PGND pin.

PCB Layout Example

Figure 2 shows an example of a PCB layout for the R2J20604NP in application. The several ceramic capacitors (e.g. 10 µF) close to VIN and PGND can be expected to decrease switching noise and improve efficiency. In that case, all sections of the GND pattern must be connected with other PCB layers via low impedances. Moreover, the wide VSWH pattern can be expected to have the effect of dissipating heat from the low-side MOS FET.

When R2J20604NP is mounted on small circuit boards, such as those for point-of-load (POL) applications, heating of the device can be alleviated by adding thermal via-holes under the VIN and VSWH pads.

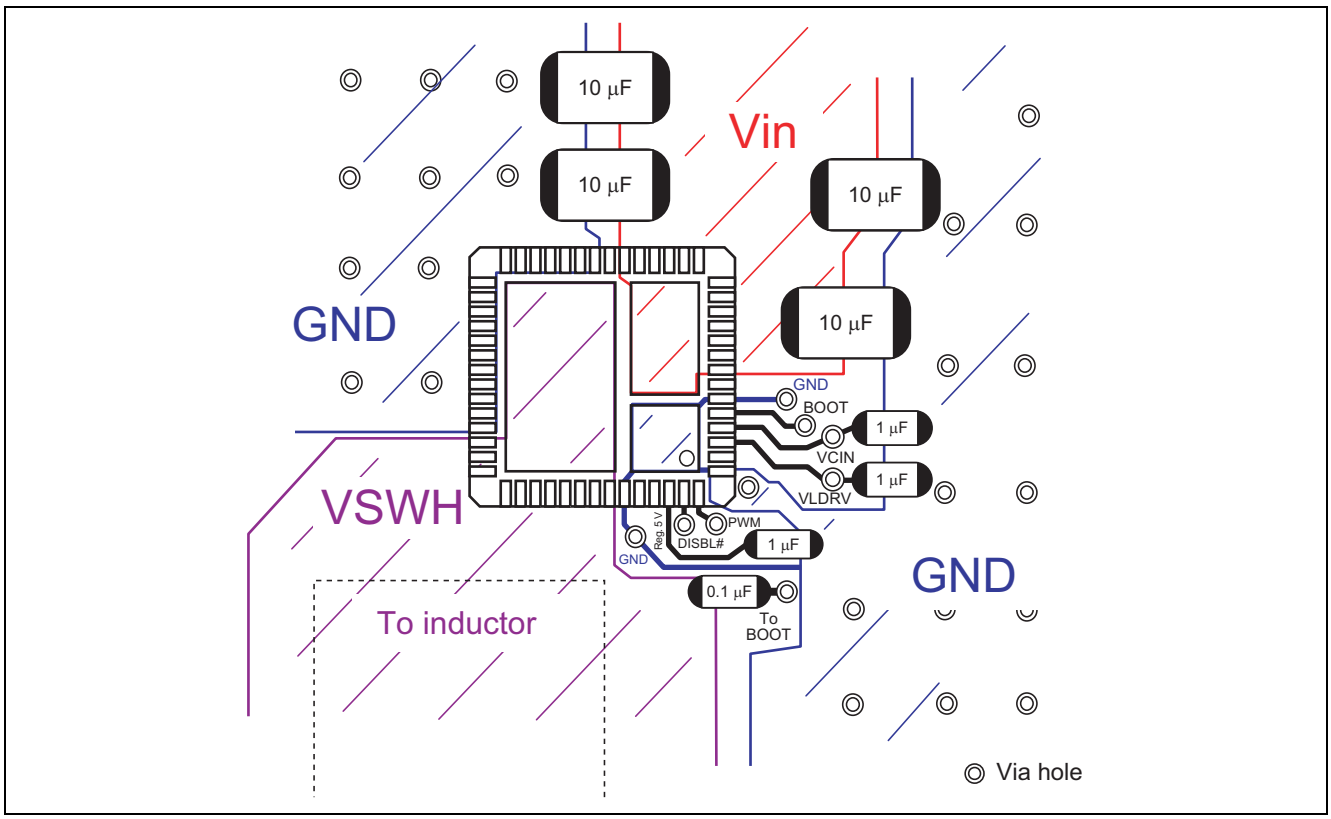


Figure 2 R2J20604NP PCB Layout Example (Top View)

Footprint Example

(Unit: mm)

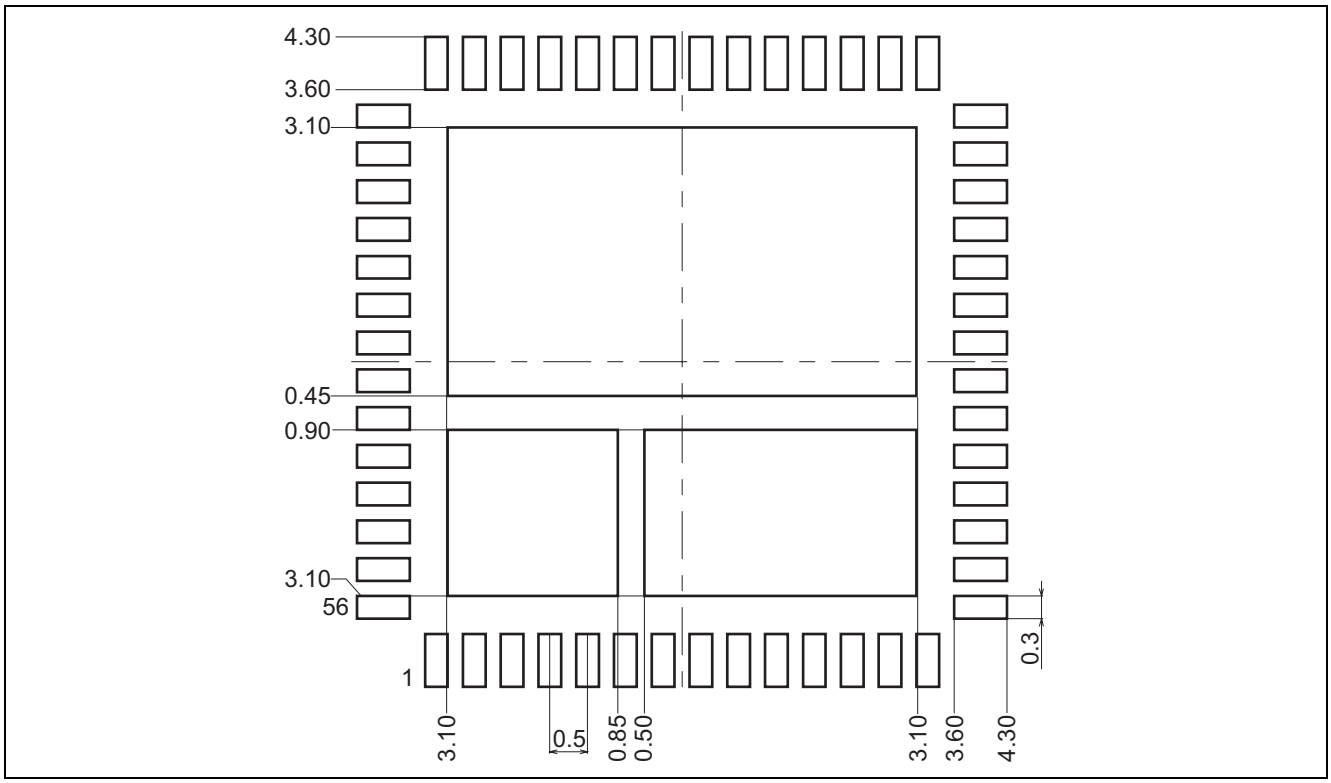
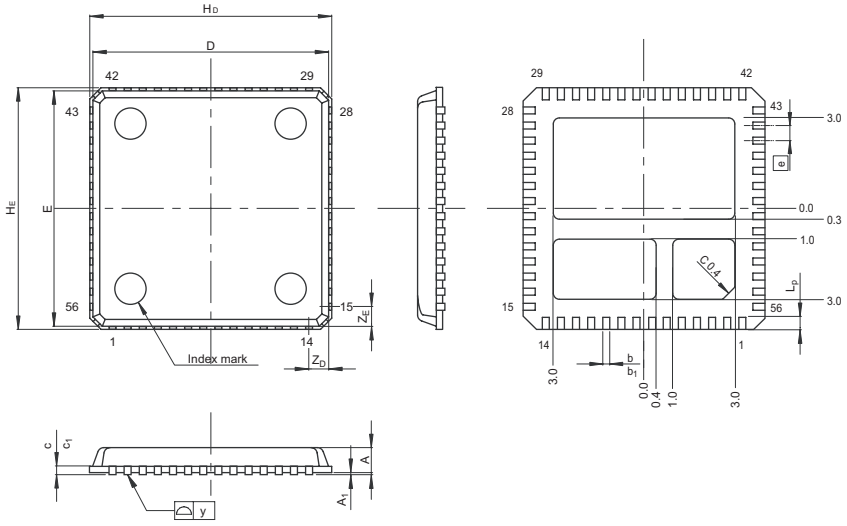


Figure 3 Footprint Example

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HVQFN56-8x8-0.50	PVQN0056KA-A	—	0.2g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	7.95	8.00	8.05
E	7.95	8.00	8.05
A_2	—	—	—
A	—	—	0.95
A_1	0.005	—	—
b	0.20	0.25	0.30
b_1	—	0.23	—
e	—	0.50	—
L_p	0.40	0.50	0.60
x	—	—	—
y	—	—	0.05
y_1	—	—	—
t	—	—	—
H_D	8.10	8.20	8.30
H_E	8.10	8.20	8.30
Z_D	—	0.75	—
Z_E	—	0.75	—
c	0.17	0.22	0.27
c_1	—	0.20	—

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