TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

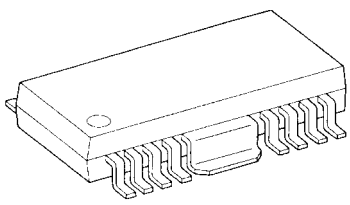
TB62802F

CCD Clock Driver

TB62802F is a clock distribution driver for CCD linear image sensors.

The IC can functionally drive the CCD input capacitance. It also supports inverted outputs, eliminating the need for crosspoint control.

The IC contains a 1 to 4 clock distribution driver and 4-bit buffer.



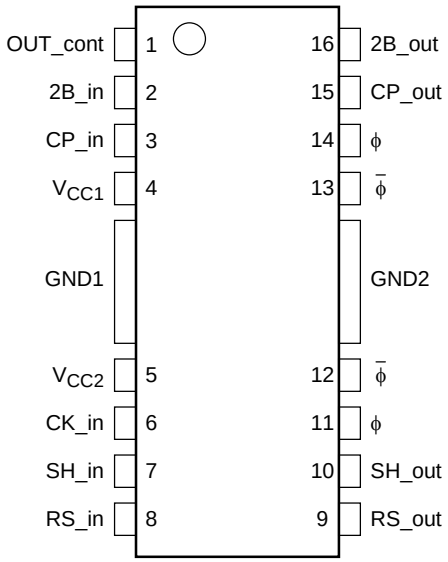
HSOP16-P-300-1.00

Weight: 0.5 g (typ.)

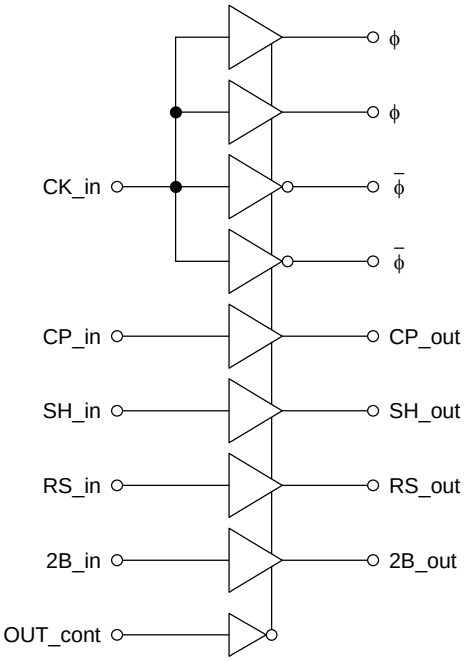
Features

- High drivability: Guaranteed driving 250 [pF] load capacitance @fclock = 25 [MHz]
  (4-bit distribution driver)
- Operating temperature range: Ta = 0°C to 60°C

Pin Connection (top view)



Logic Diagram



Pin Description

Pin No.	Pin Name	Functions	Remarks
1	OUT_cont	Output control pin	—
2	2B_in	Light load drive input	Driver input for CCD last-stage clock
3	CP_in	Light load drive input	CCD clamp gate driver input
4	V_{CC1}	Light load power supply	—
—	GND1	Light load ground	—
5	V_{CC2}	Heavy load power supply	—
6	CK_in	Heavy load drive input	Driver input for CCD transfer clock
7	SH_in	Light load drive input	CCD shift gate driver input
8	RS_in	Light load drive input	CCD reset gate driver input
9	RS_out	Light load drive output (not inverted)	CCD reset gate driver output
10	SH_out	Light load drive output (not inverted)	CCD shift gate driver output
11	ϕ	Heavy load drive output (not inverted)	Driver output for CCD transfer clock
12	$\bar{\phi}$	Heavy load drive output (inverted)	Driver output for CCD transfer clock
—	GND2	Heavy load ground	—
13	$\bar{\phi}$	Heavy load drive output (inverted)	Driver output for CCD transfer clock
14	ϕ	Heavy load drive output (not inverted)	Driver output for CCD transfer clock
15	CP_out	Light load drive output (not inverted)	CCD clamp gate driver output
16	2B_out	Light load drive output (not inverted)	Driver output for CCD last-stage clock

Note: The internal circuits for heavy load drive pins ϕ and $\bar{\phi}$ have the same configuration as those of light load drive pins RS_out, SH_out, CP_out and 2B_out. Thus, these internal circuits have the same characteristics.

Truth Table

Input				Output	
Pin Name	Logic	Pin Name	Logic	Pin Name	Logic
OUT_cont	L	CK_in	L	ϕ	L
				$\bar{\phi}$	H
			H	ϕ	H
				$\bar{\phi}$	L
		CP_in	L	CP_out	L
			H		H
		SH_in	L	SH_out	L
			H		H
		RS_in	L	RS_out	L
			H		H
		2B_in	L	2B_out	L
			H	2B_out	H
	H	—	—	All Output	L

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CC}	−0.5 to 7.0	V
Input voltage		V_{IN}	−1.2 to V_{CC} + 0.5	V
Output voltage		V_O	−0.5 to V_{CC}	V
Input clamp diode current ($V_{IN} < 0$)		I_{IK}	−50.0	mA
Output clamp diode current ($V_O < 0$)		I_{OK}	−50.0	mA
Output current excluding other than ϕ, $\bar{\phi}$ outputs	High level	I_{OH} (O)	−16.0	mA
	Low level	I_{OL} (O)	+16.0	mA
ϕ output current	High level	I_{OH} (ϕ)	−150	mA
	Low level	I_{OL} (ϕ)	150	mA
Storage temperature		T_{stg}	−40 to 150	°C
Junction temperature		T_j	150	°C
Thermal resistance	Chip to ambient air	θ_{ja}	83	°C/W

Note: Output current is specified as follows: V_{OH} = 4.0 V, V_{OL} = 0.5 V.

Recommended Operating Conditions (Ta = 25°C)

Characteristics		Symbol	Min	Typ.	Max	Unit
Power supply voltage		V_{CC}	4.7	5.0	5.5	V
Input voltage		V_{IN}	0	—	V_{CC}	V
Output voltage		V_O	0	—	V_{CC}	V
Output current excluding ϕ, $\overline{\phi}$ outputs	High level	V_{OH} (O)	—	—	−8.0	mA
	Low level	V_{OL} (O)	—	—	8.0	mA
ϕ output current	High level	V_{OH} (ϕ)	—	—	−10.0	mA
	Low level	V_{OL} (ϕ)	—	—	10.0	mA
Thermal resistance (chip to case)		θ_{jc}	—	12	—	°C/W
Operating temperature		T_{opr}	0	25	60	°C
Input rise/fall time	(Note)	tri/tfi	—	2.5	5.0	ns

Note: This IC does not have hysteresis in the input block. Thus, please take the following notes.
A CMOS integrated circuit charges and discharges the capacitance load (internal equivalent capacitance) of the internal circuit while operating. The charged or discharged current flows in the package of the IC and inductance of transmission line, which causes inductive spike voltage to be generated.
When the spike voltage is generated in the reference GND, it affects the amplitude of an input signal. The amplitude seems to be fluctuating compare to when no spike voltage is generated in the reference GND.
In this case, some induced spike's waveforms exceed the input threshold level. For low-frequency inputs, the rate of which a spike exceeds the level increases, resulted in unstable output.
Therefore, do not apply input signals lower than 1 μs. When designing a board, please take the inductance of transmission line into consideration.

Electrical Characteristics

DC Characteristics (unless otherwise specified, V_{CC} = 4.7 to 5.5 V, Ta = 0 to 60°C)

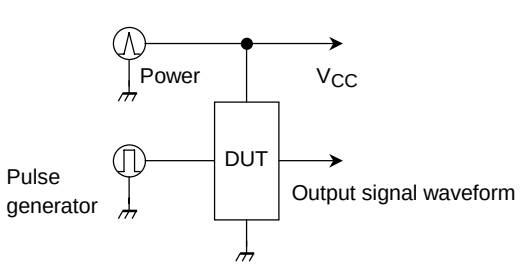
Characteristics		Symbol	Test Circuit	Test Condition	V_{CC}	Min	Typ.	Max	Unit
Input voltage	High	V_{IH}	1		4.7	2.0	—	V_{CC}	V
	Low	V_{IL}			4.7	0	—	0.8	
Input clamp voltage		V_{IK}	2	I_{IK} = –20 mA	4.7	—	—	1.0	V
Output voltage excluding ϕ, ϕ outputs		V_{OH} (O)	3	I_{OH} = –50 μA	4.7	4.5	—	V_{CC}	V
				I_{OH} = –8 mA	4.7	3.9	—	V_{CC}	
		V_{OL} (O)	5	I_{OL} = 50 μA	4.7	0	—	0.2	
				I_{OL} = 8 mA	4.7	0	—	0.7	
ϕ output voltage		V_{OH} (ϕ/$\bar{\phi}$)	3, 4	I_{OH} = –10 mA	4.7	4.5	—	V_{CC}	V
				I_{OH} = –30 mA	4.7	3.9	—	V_{CC}	
				I_{OH} = –120 mA	4.7	3.0	—	V_{CC}	
		V_{OL} (ϕ/$\bar{\phi}$)	5, 6	I_{OL} = 50 μA	4.7	0	—	0.3	
				I_{OL} = 30 mA	4.7	0	—	0.5	
				I_{OL} = 120 mA	4.7	0	—	2.0	
Input voltage		I_{IN}	7	V_{IN} = V_{CC} or GND	5.5	—	—	1.0	μA
Static current consumption	Total	I_{CC}	8	For light load output, all bits are High. For heavy load output, 2 bits are High. 2 bits are Low.	5.5	—	—	15.0	mA
	Forced low for all bits	I_{CCL}	—	Out_cont = "H"	5.5	—	—	30.0	
	Each bit	ΔI_{CC}	9	One input : V_{IN} = 0.5 V or V_{CC} – 2.1 V Other inputs : V_{IN} = V_{CC} or GND	—	—	—	1.5	
Output off mode supply voltage		V_{POR}	(Note)	Light load power supply (V_{CC1}) reference	—	—	3.0	—	V

Note: Refer to the description of the P.O.R below.

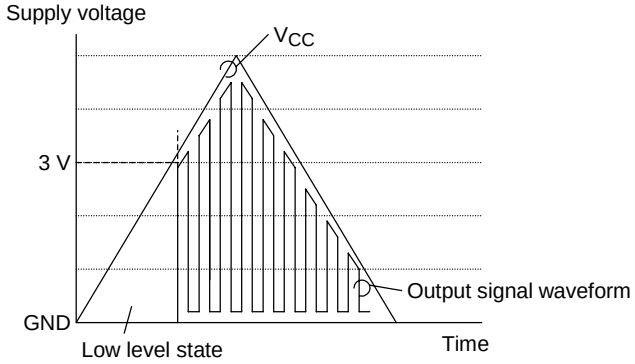
Mode in which Output is Held at Low at Power-On (P.O.R: Power On Reset circuit)

To eliminate the unstable period for the internal logic, this IC has function to monitor light load power supply (V_{CC1}) at power-on to maintain the outputs at Low.

- At power-on, all output are held at Low until light load power supply (V_{CC1}) reaches the voltage level of 3 V.
- When light load power supply (V_{CC1}) voltage is higher than 3 V (typ.), internal logic operates according to input signals.
- For normal operation, please use the power supply at 4.7 V or higher as guaranteed.



P.O.R test circuit



Please refer to Subsection 10. "Propagation Delay Time" in AC Parameters.

AC Characteristics (input transition rise or fall time: t_r/t_f = 3.0 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C, V_{CC} = 5.0 V			Ta = 0 to 60°C V_{CC} = 4.7 to 5.5 V		Unit	Reference Measurement Diagram
			Min	Typ.	Max	Min	Max		
Propagation delay time	tpLH (ϕ)	C_L = 250 pF	5.3	10.8	15.5	5.0	16.0	ns	Measurement diagram 1
	tpHL (ϕ)		5.3	9.8	15.5	5.0	16.0		
	tpLH (O)	C_L = 20 pF	2.5	5.4	9.5	2.0	10.0		Measurement diagram 2
	tpHL (O)		2.5	6.0	10.5	2.0	12.0		
Output OFF time	tpCLH (ϕ)	C_L = 250 pF	9.5	14.0	24.0	9.0	25.0	ns	Measurement diagram 1
	tpCHL (ϕ)		9.5	15.4	24.0	9.0	25.0		
	tpCLH (O)	C_L = 20 pF	7.2	10.7	19.0	6.0	23.0		Measurement diagram 2
	tpCHL (O)		7.3	18.5	30.0	6.0	35.0		
Light load drive output skew	to (skw)	C_L = 20 pF	0	—	2.0	0	2.0	ns	Measurement diagram 3
Heavy load drive output cross points	VT (crs)	C_L = 100 to 250 pF	1.5	—	—	1.5	—	V	Measurement diagram 4
Equivalent internal capacitance (Note 1)	CPD (ϕ)		—	57	—	—	—	pF	
	CPD (O)		—	18	—	—	—		

Note 1: CPD denotes “power dissipation capacitance”. Using the CPD value, dynamic power dissipation can be calculated.

$$Pd = \Sigma [CPD \times V_{CC}^2 \times Fin] + \Sigma (CL \times V_{CC}^2 \times Fout)$$

CL: Load capacitance per output
CPD: Power dissipation capacitance
Fin: Input clock frequency
Fout: output clock frequency

For example,
For heavy load drive output, drive 250-pF load capacitor at 25 MHz
For light load drive output, drive 20-pF load capacitor at 25 MHz

Note 2: In practical, the frequencies of some control signals for a shift gate are lower than the transfer clock. Thus, the power dissipation for practical use is smaller than the calculated value below.

$$Pd = [57\ pF \times 5.0\ V \times 5.0\ V \times 25\ MHz] \times 4\ bit + (250\ pF \times 5.0\ V \times 5.0\ V \times 25\ MHz) \times 4\ bit + [18\ pF \times 5.0\ V \times 5.0\ V \times 25\ MHz] \times 4\ bit + (20\ pF \times 5.0\ V \times 5.0\ V \times 25\ MHz) \times 4\ bit \simeq 862\ mW$$

The typical power dissipation is approximately 862 mW.

Notes when Designing a System

As shown above, TB62802F consumes high current while operating. Temporarily the current flows more than the calculated value. To prevent bouncing from power supply and GND, decoupling is required for the power supply.

An example of calculating the capacitance of decoupling capacitor is shown below. Please refer to it when designing a system.

The decoupling capacitor should be placed underneath the IC to reduce the high-frequency components.

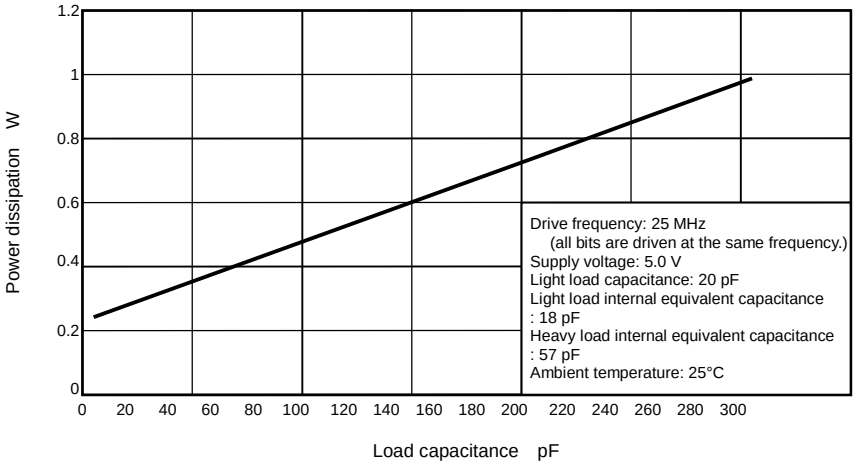
Supply current variable: 350 mA (estimated variable in 1 bit)
Supply voltage variable: 0.3 V
Noise pulse width: 10 ns (time when varying)

$$C = \Delta I_{CC}/(\Delta V/\Delta T)$$
$$= 350\ mA \times 4\ bit/(0.3\ V/10\ ns)$$
$$\simeq 47\ nF$$
$$\simeq 0.047\ \mu F \text{ (when using a normal capacitor)}$$

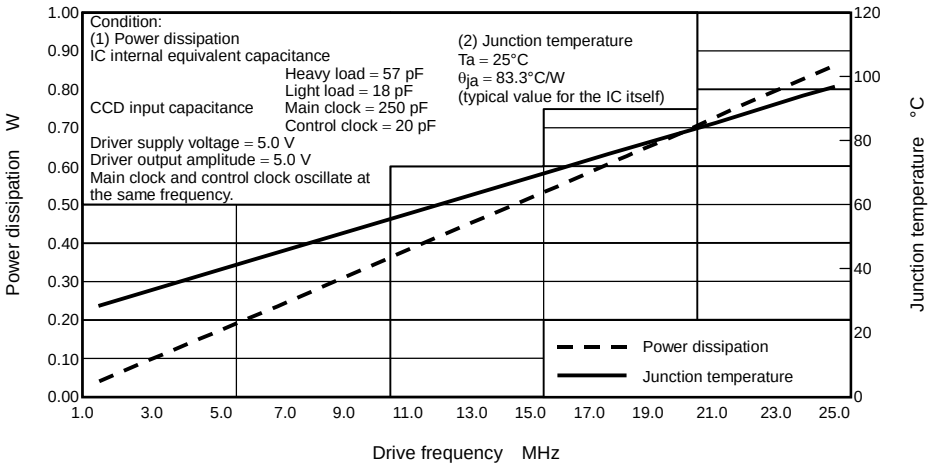
To control the fluctuation in the low-frequency components, it is recommended that the power supply on the board be decoupled using a 10-μF to 50-μF capacitor.

Reference Characteristics

Load Capacitance vs. Power Dissipation



Power Dissipation and Junction Temperature (reference value)



Thermal Design

Junction temperature is expressed as follows.

$T_j = Ta + (\theta jc + \theta ca) \times Pd$

$= Ta + \theta ja \times Pd$

T_j: Junction temperature

Ta: Ambient temperature

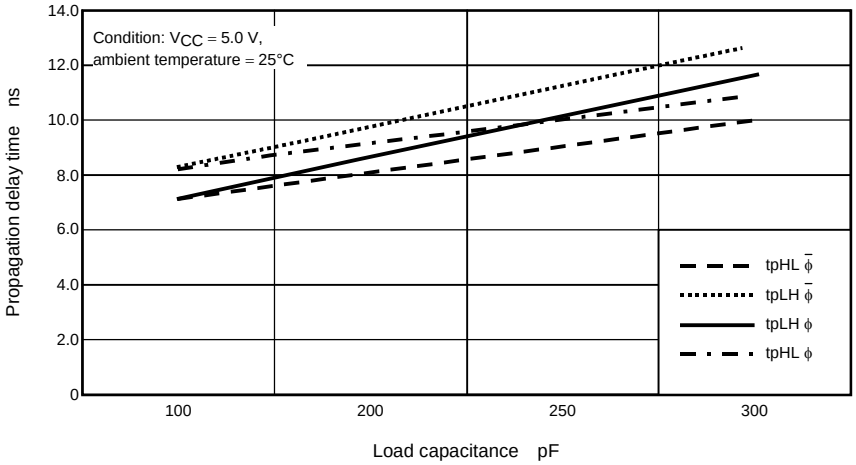
θjc: Thermal resistance from chip to case (it is the specific value and is not affected by environment.)

θja: Thermal resistance from chip to ambient temperature (it is affected by environment.)

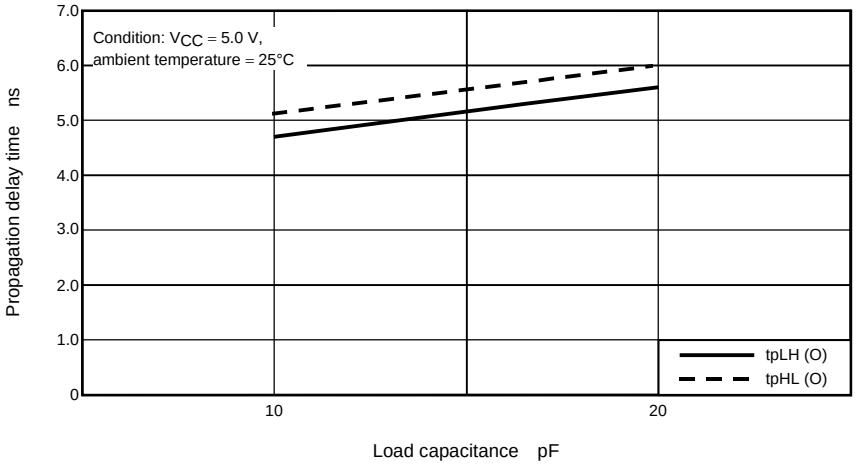
Pd: Power dissipation when driving external load

Design the thermal performance including heat dispersion on PCB and ambient temperature setting, so that the calculated value here can be within the specified range.

Propagation Delay Time Capacitance Dependency of
TB62802F Heavy Load Drive Pin



Propagation Delay Time Capacitance Dependency of
TB62802F Light Load Drive Pin



Waveform Measuring Point

Propagation Delay Time Setting

Input signal
- 2B_in
- CK_in
- SH_in
- RS_in
- CP_in
- out_cont

Measurement Diagram 1

- ϕ Output signal

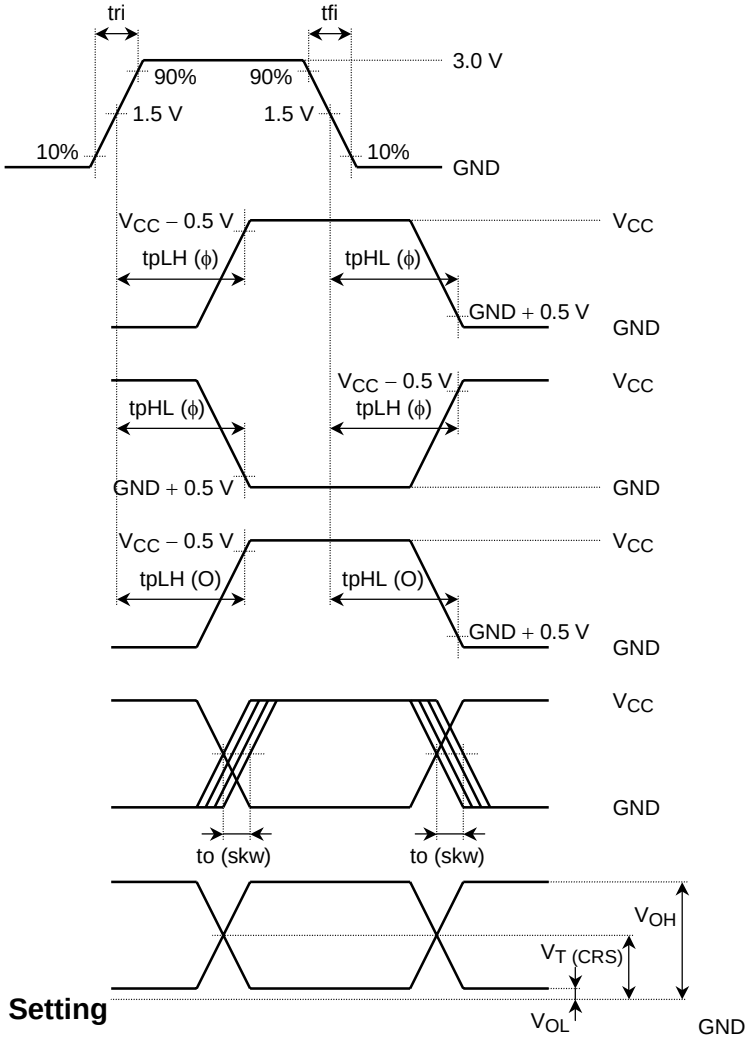
- $\bar{\phi}$ Output signal

Measurement Diagram 2

- 2B_out
- CK_out
- SH_out
- RS_out
- CP_out

Measurement Diagram 3

- 2B_out
- CK_out
- SH_out
- RS_out
- CP_out



Output Waveform Crosspoint/Level Setting

Measurement Diagram 4

- ϕ Output signal

- $\bar{\phi}$ Output signal

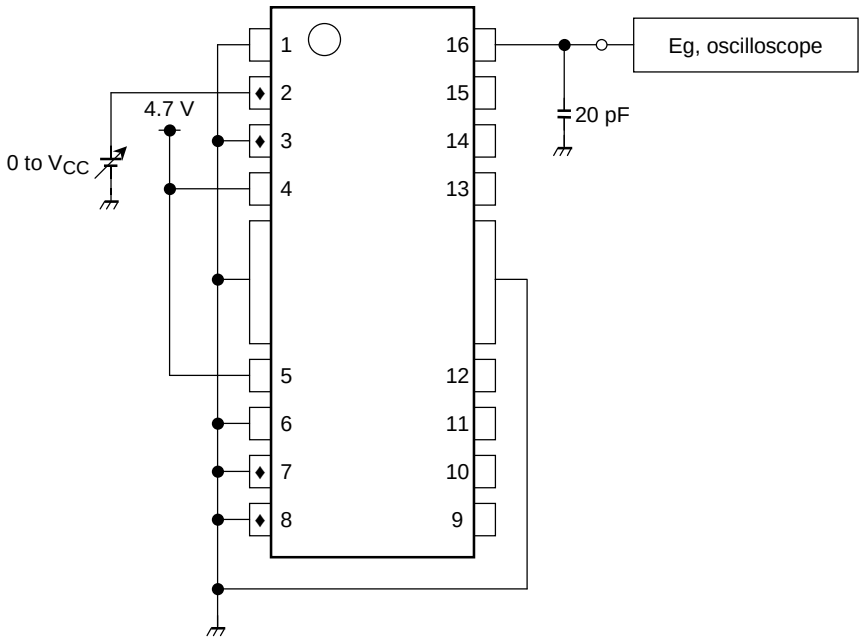
Test Circuit

DC Parameters

Pins marked with an asterisk (*) are test pins. Ground input pins which are not used as test pins so that logic is determined. Unless otherwise specified, bits of the same type are measured the same way.

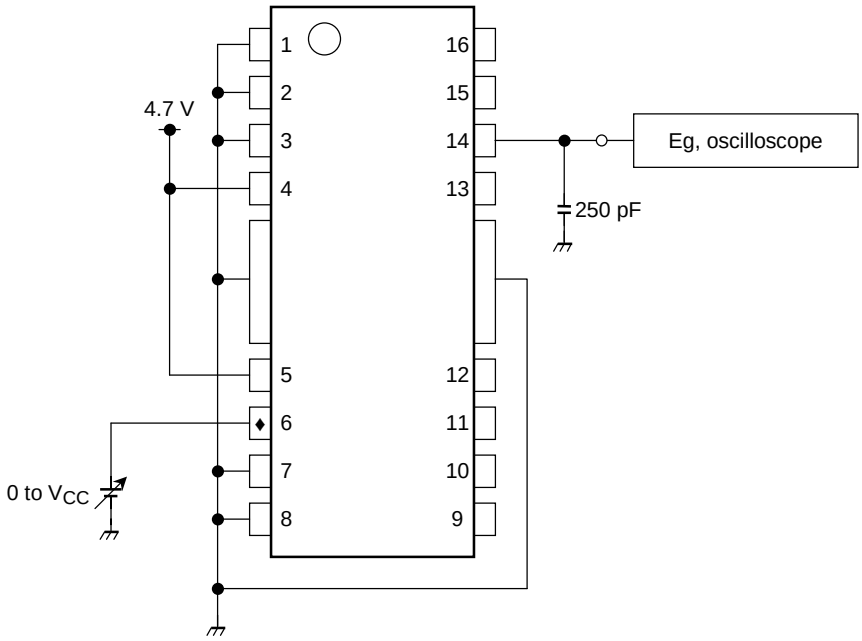
1. V_{IH}/V_{IL}

(1) Light load drive bits



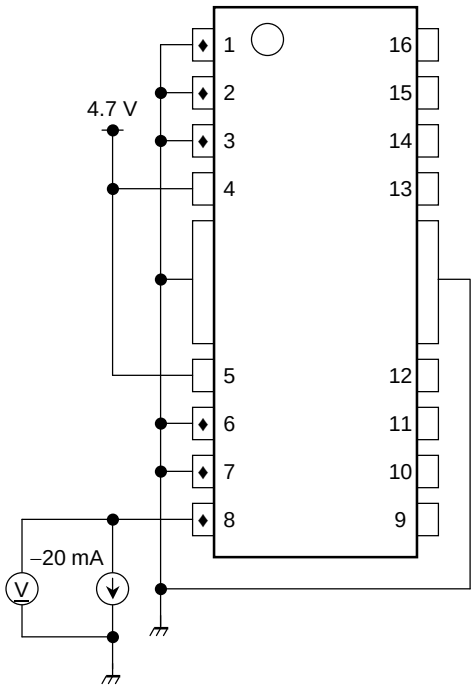
Note 1: When measuring input pins, connect the input pins which are not measured to GND.

(2) Heavy load drive bits



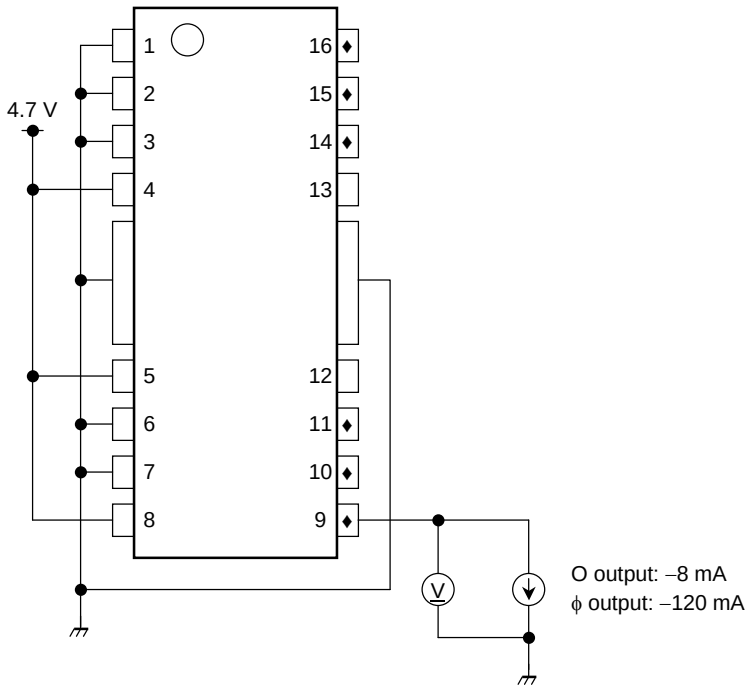
Note 2: Connect the input pins, which are not measured, to GND.

2. V_{IK}



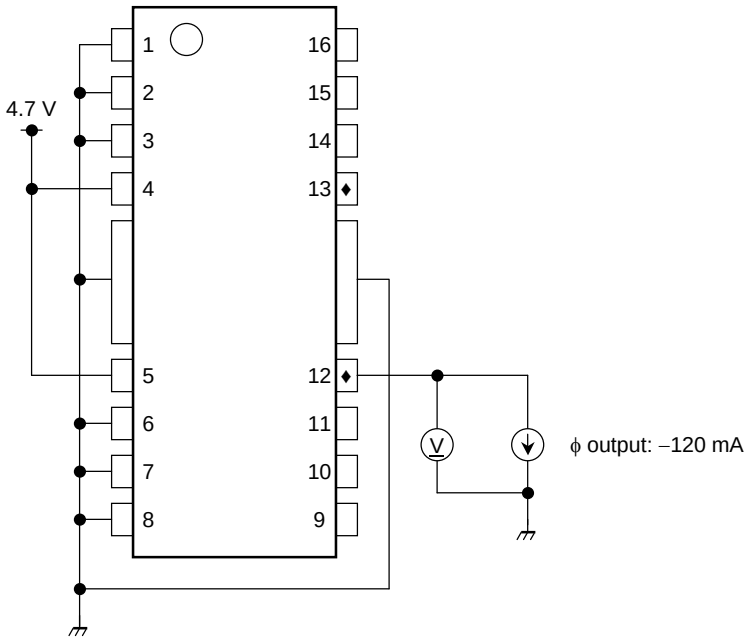
Note 1: When measuring input pins, connect the input pins which are not measured to GND.

3. V_{OH} (O/ϕ)



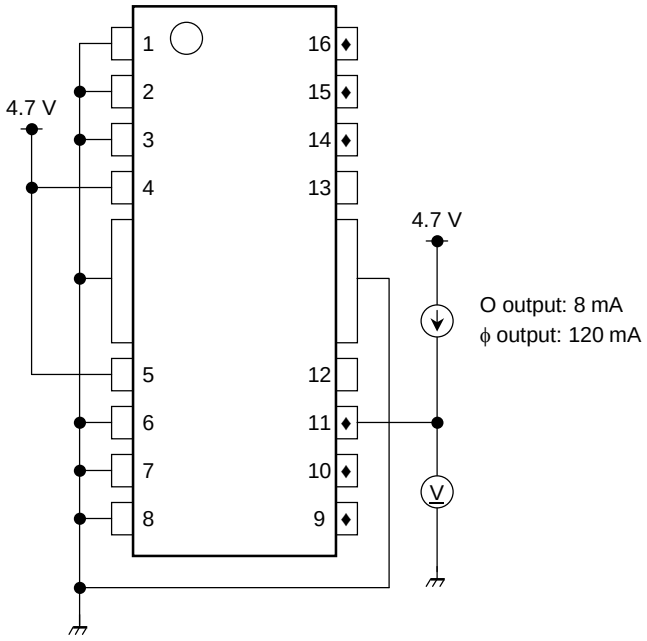
Note 2: Connect the input pins, which are not measured, to GND.

4. V_{OH} ($\bar{\phi}$)



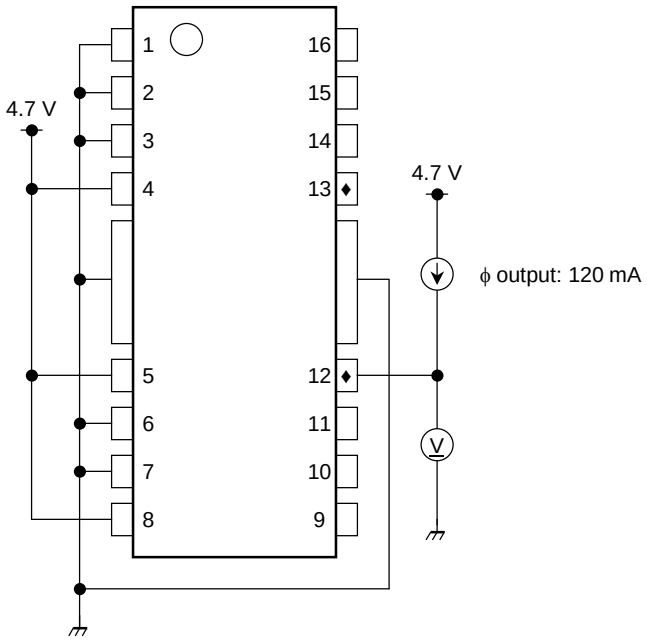
Note 1: Connect the input pins, which are not measured, to GND.

5. V_{OL} (O/ϕ)



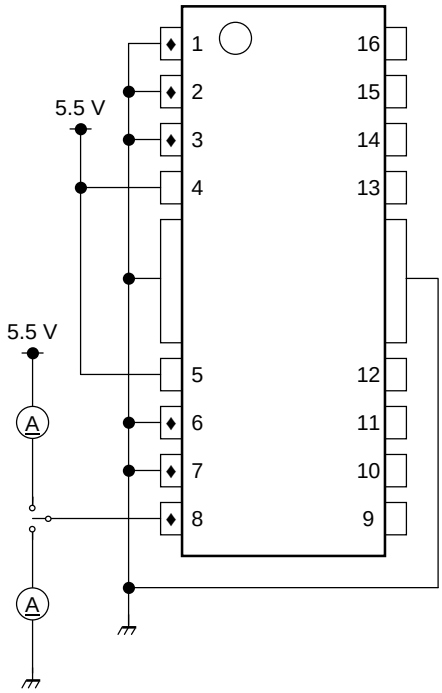
Note 2 Connect the input pins, which are not measured, to GND.

6. V_{OL} ($\overline{\phi}$)



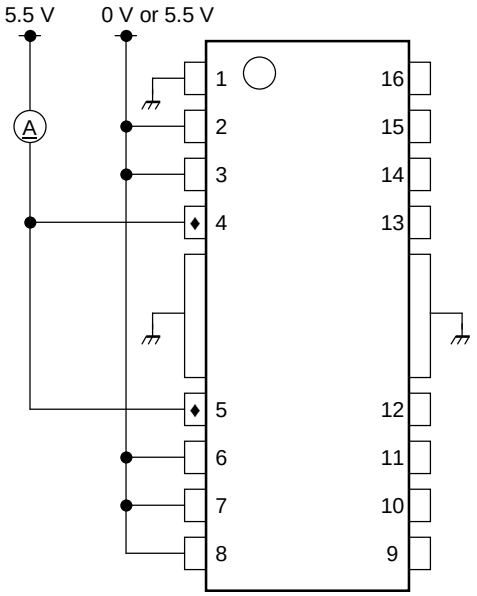
Note 1: Connect the input pins, which are not measured, to GND.

7. I_{IN}



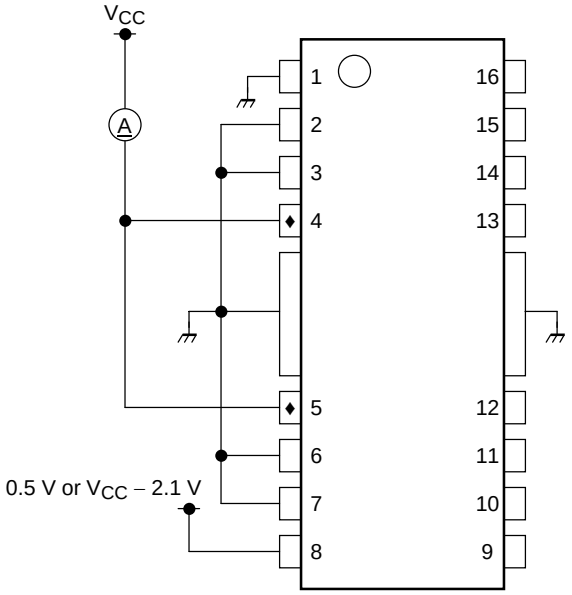
Note 2: When measuring input pins, connect the input pins which are not measured to GND.

8. I_{CC}



Note 1: Input logic of heavy load drive clock input pin (pin 6) is the same for high or low.

9. ΔI_{CC}



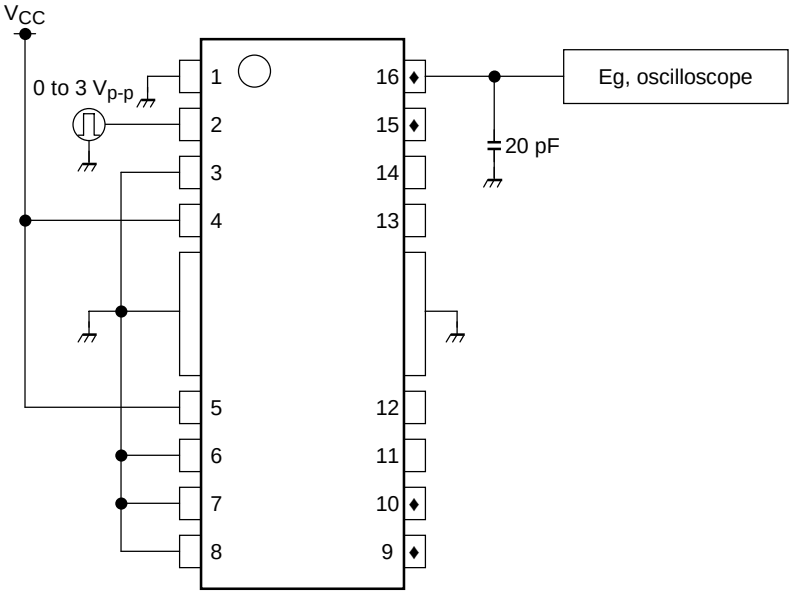
Note 2: When measuring input pins, connect the input pins which are not measured to GND or power.

AC Parameters

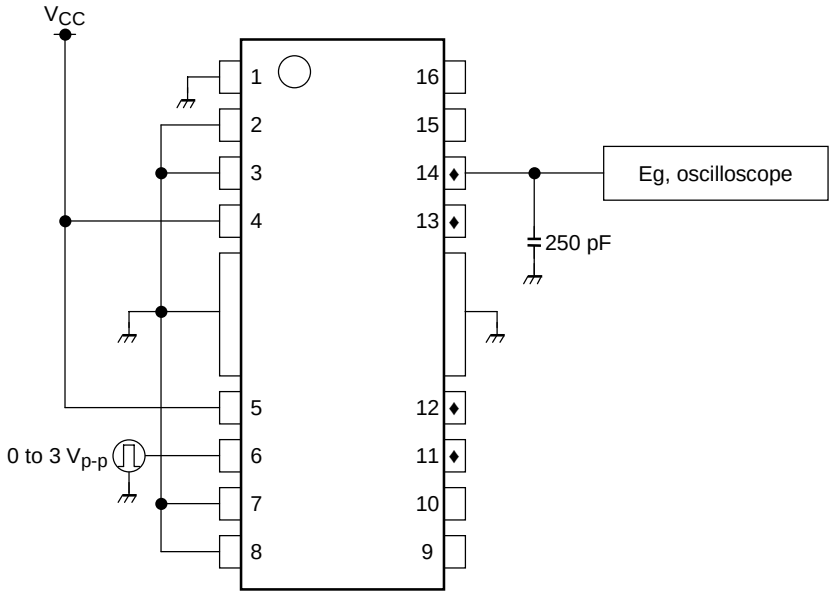
Pins marked with an asterisk (*) are test pins. Ground the input pins which are not used as test pins so that logic is determined. Unless otherwise specified, bits of the same type are measured the same way.

10. Propagation Delay Time

(1) Light load drive bits

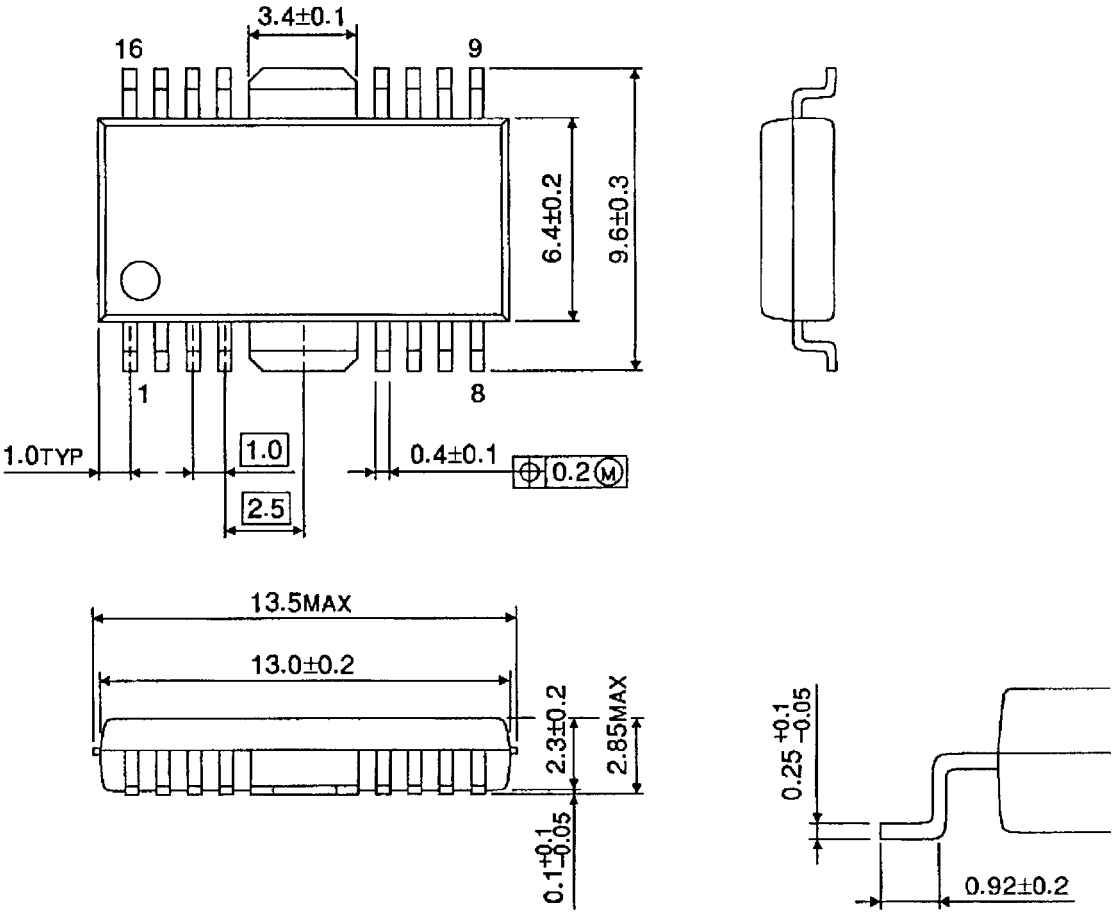


(2) Heavy load drive bits



Package Dimensions

HSOP16-P-300-1.00 Unit : mm



Weight: 0.5 g (typ.)

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