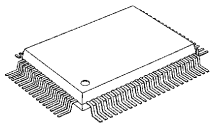
CMOS 4-Bit Microcontroller

TMP47P823VF

The TMP47P823V is the system evaluation LSI of the TMP47C623/823 with 64 Kbits one-time PROM. The TMP47P823V programs / verifies using an adapter socket to connect with PROM programmer, an it is in TMM27128AD.
In addition, the TMP47P823V and the TMP47C623/823 are pin compatible. The TMP47P823V operates as the same as the TMP47C623/823 by programming to the internal PROM.

Part No.	ROM	RAM	Package	Adapter Socket
TMP47P823VF	OTP 8192 × 8-bit	512 × 4-bit	P-QFP64-1420-1.00A	BM1146

P-QFP64-1420-1.00A

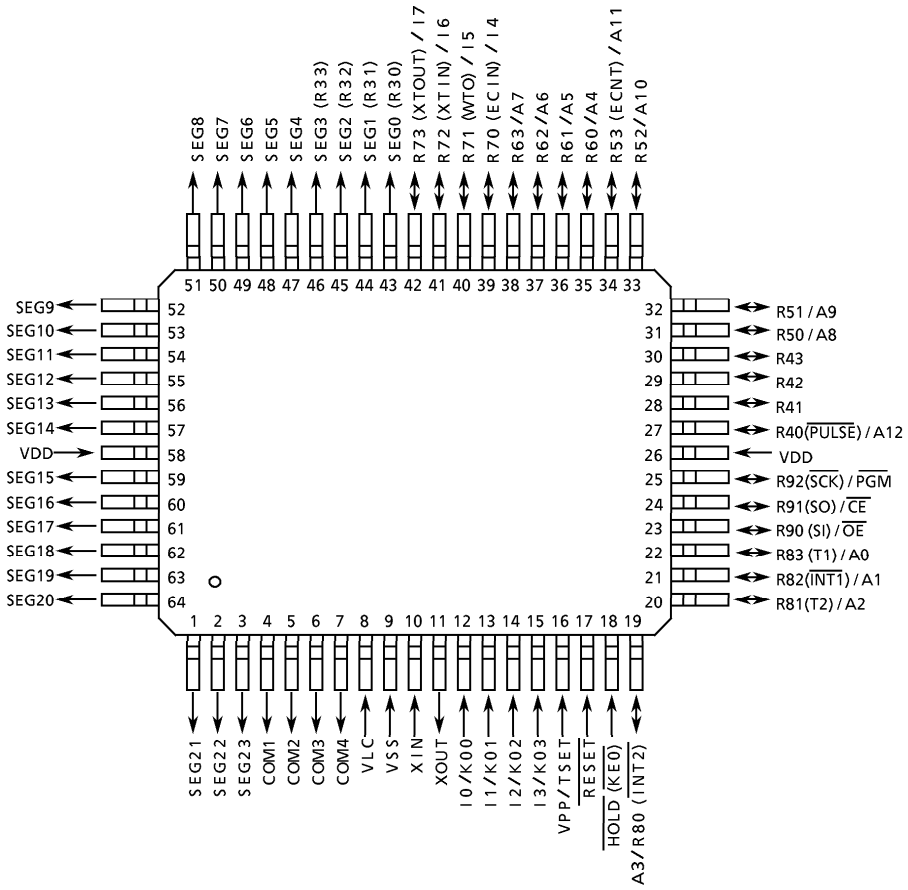


TMP47P823VF

000707EBA1

Pin Assignment (Top View)

P-QFP64-1420-1.00A



Pin Function

The TMP47P823V has MCU mode and PROM mode.

(1) MCU mode

The TMP47C823 and the TMP47P823V are pin compatible (TEST pin for out-going test, Be fixed to low level).

(2) PROM mode

Pin Name	Input / Output	Functions	Pin Name (MCU Mode)
A12	Input	Address inputs	R40
A11 to A8			R50 to R53
A7 to A4			R60 to R63
A3 to A0			R80 to R83
I7 to I4	I/O	Data inputs / outputs	R73 to R70
I3 to I0			K03 to K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Chip Enable input	R90
VPP	Power supply	+ 12.5 V / 6 V (Program supply voltage)	TEST
VCC		+ 5 V	VDD
VSS		0 V	VSS
SEG31 to SEG0	Output	Open	
COM4 to COM1			
VLC	Power supply		
N.C.			
R53 to R51	I/O	Be fixed to low level	
R63 to R60			
R43 to R40			
R33 to R30			
$\overline{RESET}$	Input	PROM mode setting pins. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pins	
XOUT	Output		

Operational Description

The following is an explanation of hardware configuration and operation in relation to the TMP47P823V. The TMP47P823V is the same as the TMP47C623/823 except that an EPROM or OTP is used instead of a Mask ROM.

1. Operation Mode

The TMP47P823V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU mode is the same as for the TMP47C623/823, except that the TEST / VPP pin does not have pull-down resistor and cannot be used open.

1.1.1 Program memory

The program storage area is the same as for the TMP47C823. Data conversion tables must be set in two locations when using the TMP47P823V to check TMP47C623 operation.

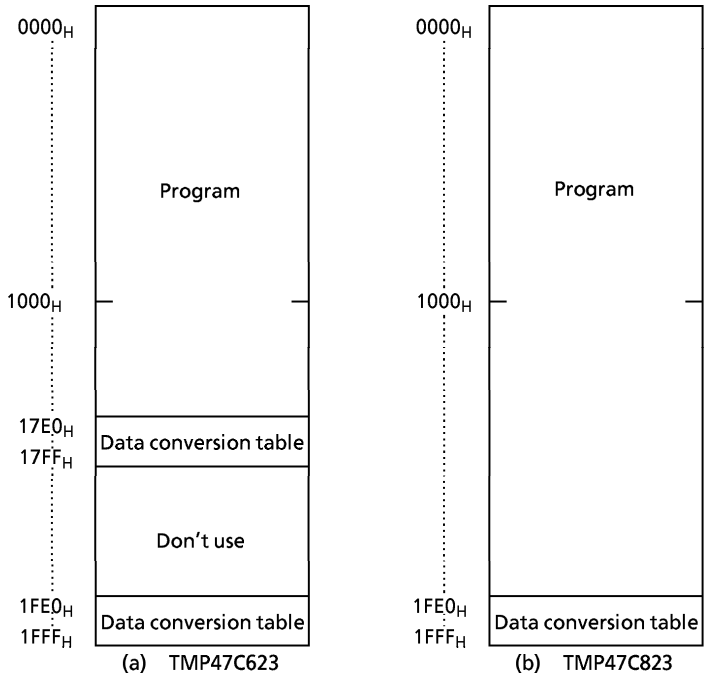


Figure 1-1. Program area

1.1.2 Data memory

The TMP47P823V has two 256 × 4-bit data memory banks (DMB0, DMB1).

When using the TMP47P823V as a TMP47C623 evaluator, do not write data to address 80_H and following, even though the DMB1 addresses are 00-FF_H. There is no necessary to take into consideration a special function Shared area because one is built in DMB0.

1.1.3 Input/output circuitry

(1) Control pins
This is the same as for the TMP47C623/823 except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the TMP47P823V is the same as I/O code GA of the TMP47C623/823. External resistance, for example, is required when using as evaluator of other I/O codes (GB to GF) (Refer to Figure 1-3).

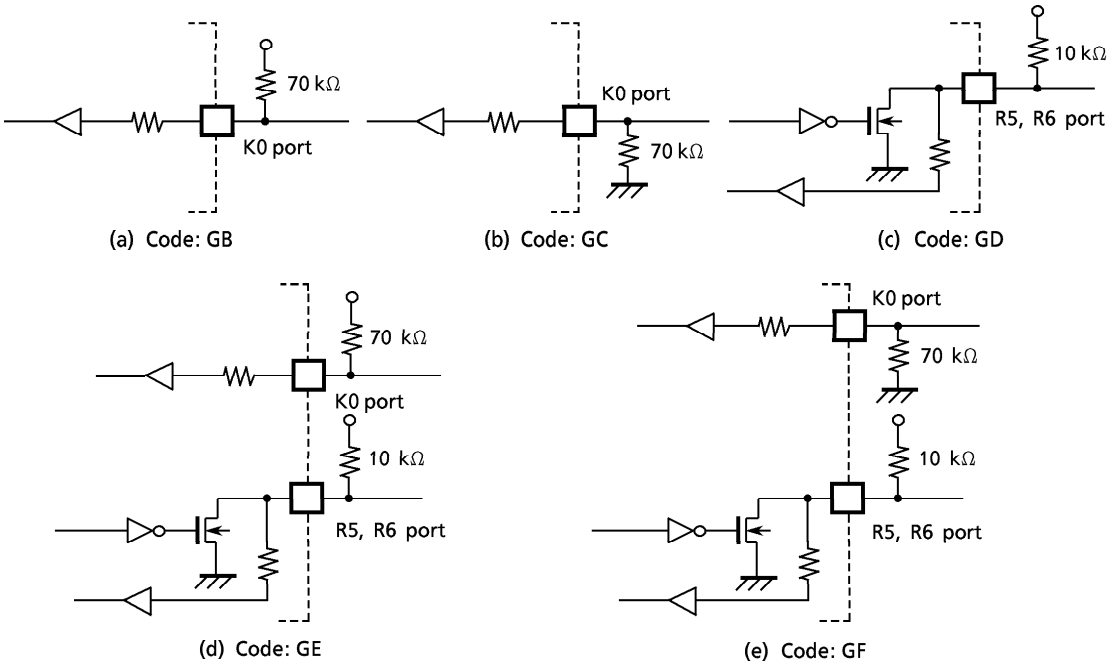


Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM2764AD).
An adapter socket (part No. BM1146) is available for connecting a PROM writer.

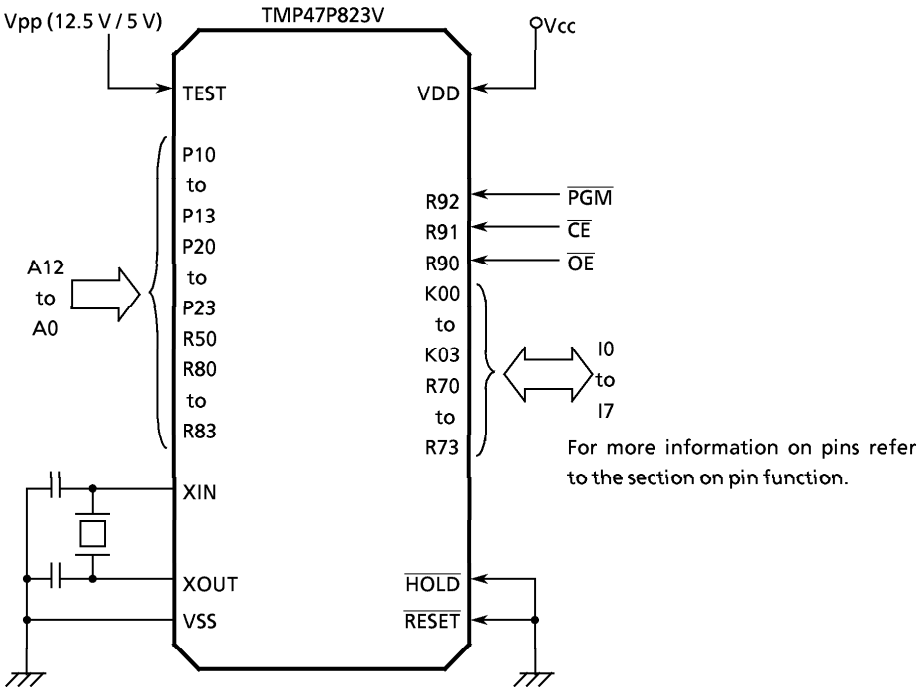


Figure 1-3. Setting for PROM mode

1.2.1 High-speed programming mode

The device is set up in the high speed programming mode when the programming voltage (12.5 V) is applied to the Vpp terminal with Vcc = 6 V and $\overline{\text{PGM}} = V_{IH4}$. The programming is achieved by applying a Single TTL low level 1 ms, pulse the $\overline{\text{PGM}}$ input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

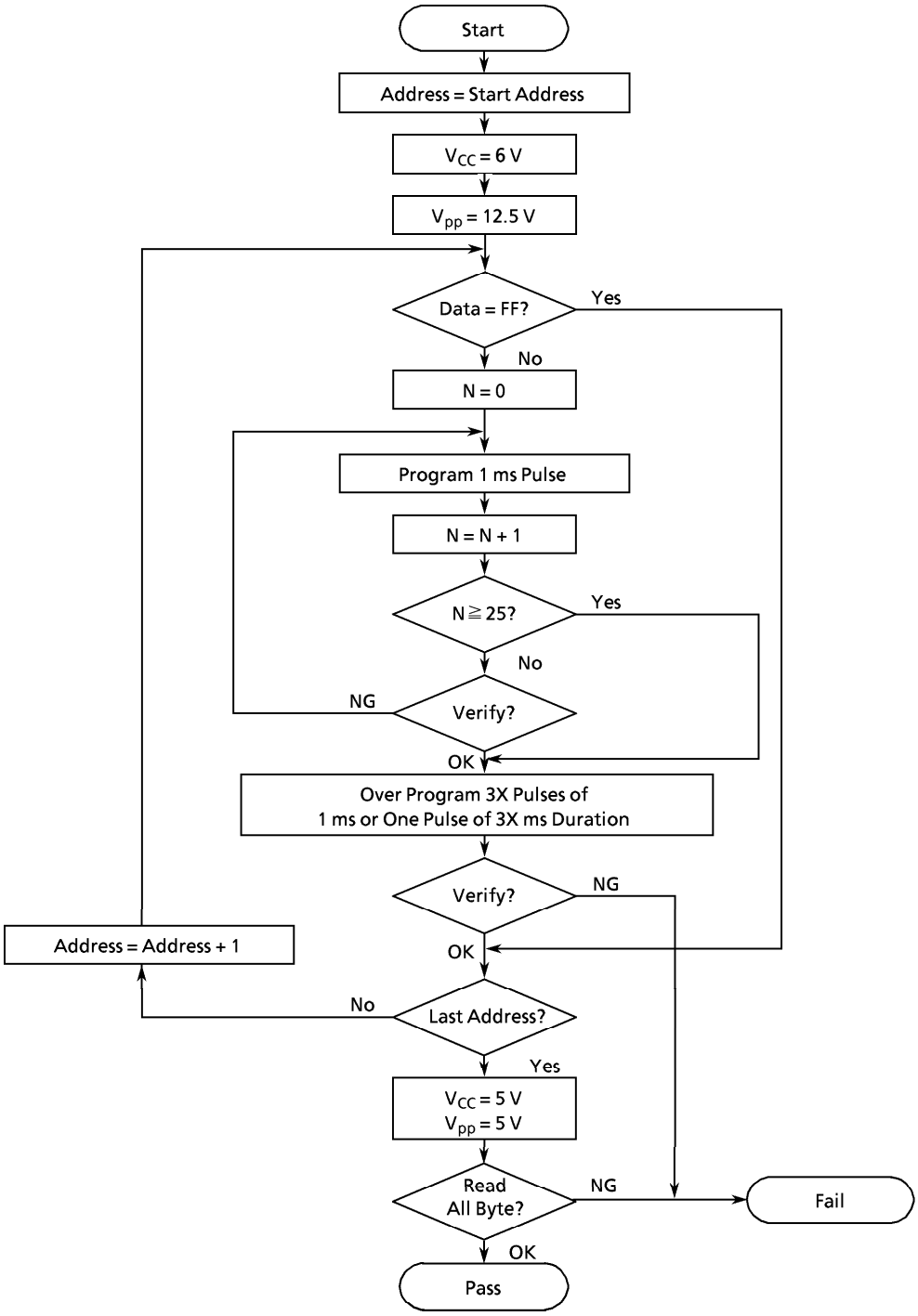


Figure 1-4. Flowchart

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 7	V
Supply Voltage (LCD drive)	V_{LC}		– 0.3 to V_{DD} + 0.3	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include ports R7, R3	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin, but include ports R7, R3	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Exept port R4	3.2	mA
	I_{OUT2}	Port R4	30	
Output Current (Total)	ΣI_{OUT}	Port R4	60	mA
Power Dissipation [Topr = 50°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Opeating Conditions (V_{SS} = 0 V, Topr = – 40 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		In the Normal mode (fc = 4.2 MHz)	2.7	6.0	V
			In the Normal mode (fc = 5.0 MHz) Note 2	2.9		
			In the Normal mode (fc = 6.0 MHz)	4.5		
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT	High freq. $V_{DD} \geqq 2.7$ V	0.4	4.2	MHz
			High freq. $V_{DD} \geqq 2.9$ V Note 3		5.0	
			High freq. $V_{DD} \geqq 4.5$ V		6.0	
	fs	XTIN, XTOUT	Low freq.	30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input Voltage VIH3, VIL3: in the SLOW and HOLD mode.

Note 3: Operating Temperature – 30 to 50°C

DC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V /0 V	—	—	± 2	μA
	I_{IN2}	Open drain R port					
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5 V, V_{IN} = 0.4 V	—	—	– 2	mA
Input Registance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain port R	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	—	—	V
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Output Low Current	I_{OL}	Port 4	V_{DD} = 4.5 V, V_{OL} = 1.0 V	15	20	—	mA
Segment Output Low Registance	R_{OS1}	SEG pin	V_{DD} = 5 V, V_{DD} – V_{LC} = 3 V	—	10/20	—	kΩ
Common Output Low Registance	R_{OC1}	COM pin					
Segment Output High Registance	R_{OS2}	SEG pin		—	70/200	—	
Common Output High Registance	R_{OC2}	COM pin					
Segment/Common Output Registance	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V, V_{LC} = V_{SS} fc = 4 MHz	—	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0 V, V_{LC} = V_{SS} fs = 32.768 kHz	—	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note 1: Typ. values show those at T_{opr} = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Output Resistance R_{os}, R_{oc} ; Shows on-resistance at the level switching.

Note 4: $V_{O2/3}$; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5: $V_{O1/2}$; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.

Note 6: $V_{O1/3}$; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 7: Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.
Supply Current I_{DDS} ; V_{IN} = 2.8 V / 0.2 V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).

Note 8: When using LCD, it is necessary to consider values of $R_{OS1/2}$ and $R_{OC1/2}$.

Note 9: Times for SEG / COM output switching on ; R_{OS1}, R_{OC1}: 2/fs (s)
R_{OS2}, R_{OC2}: 1/(n·f_F) (1/n: duty, f_F: frame frequency)

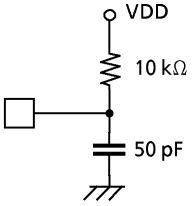
AC Characteristics

(V_{SS} = 0 V, T_{opr} = – 40 to 70°C)

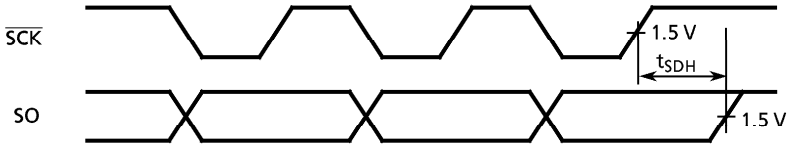
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Instruction Cycle Time	tcy	in the Normal mode	1.3	—	20	μs
		in the SLOW mode	235	—	267	μs
High Level Clock Pulse Width	t_{WCH}	For external clock operation	80	—	—	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		0.5 tcy – 0.3	—	—	μs
High Speed Timer / Counter input frequency	f_{HT}	ECIN input	—	—	fc	MHz

Note: Shift data Hold time:

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



Recommended Oscillating Conditions

(V_{SS} = 0 V, T_{opr} = – 40 to 70°C)

Recommended oscillating conditions of the TMP47P823V are equal to the TMP47C623/823's.

DC / AC Characteristics

(V_{SS} = 0 V)

(1) Read Operation

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Level High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	V_{CC} × 0.1	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	0	–	350	ns