

LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

Check for Samples: [LMV821-Q1](#), [LMV822-Q1](#), [LMV824-Q1](#)

FEATURES

- Qualified for Automotive Applications
- 2.5-V, 2.7-V, and 5-V Performance
- 40°C to 125°C Operation
- No Crossover Distortion
- Low Supply Current at $V_{CC+} = 5$ V
 - LMV821: 0.3 mA Typ
 - LMV822: 0.5 mA Typ
 - LMV824: 1 mA Typ
- Rail-to-Rail Output Swing
- Gain Bandwidth of 5.5 MHz Typ at 5 V
- Slew Rate of 1.9 V/μs Typ at 5 V

DESCRIPTION/ORDERING INFORMATION

The LMV821 single, LMV822 dual, and LMV824 quad devices are low-voltage (2.5 V to 5.5 V), low-power commodity operational amplifiers. Electrical characteristics are very similar to the LMV3xx operational amplifiers (low supply current, rail-to-rail outputs, input common-mode range that includes ground). However, the LMV82x devices offer a higher bandwidth (5.5 MHz typical) and faster slew rate (1.9 V/μs typical).

The LMV82x devices are cost-effective solutions for applications requiring low-voltage/low-power operation and space-saving considerations. The LMV821 saves space on printed circuit boards and enables the design of small portable electronic devices (cordless and cellular phones, laptops, PDAs, PCMIA). It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾			ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 125°C	Single	SOT-23 – DBV	Reel of 3000	LMV821QDBVRQ1	RB1_
	Dual	MSOP/VSSOP – DGK	Reel of 2500	LMV822QDGKRQ1	R8B
	Quad	SOIC – D	Reel of 2500	LMV824QDRQ1	LMV824Q
		TSSOP – PW	Reel of 2000	LMV824QPWRQ1	MV824Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

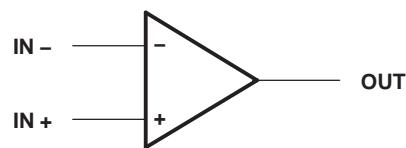
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) DBV: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

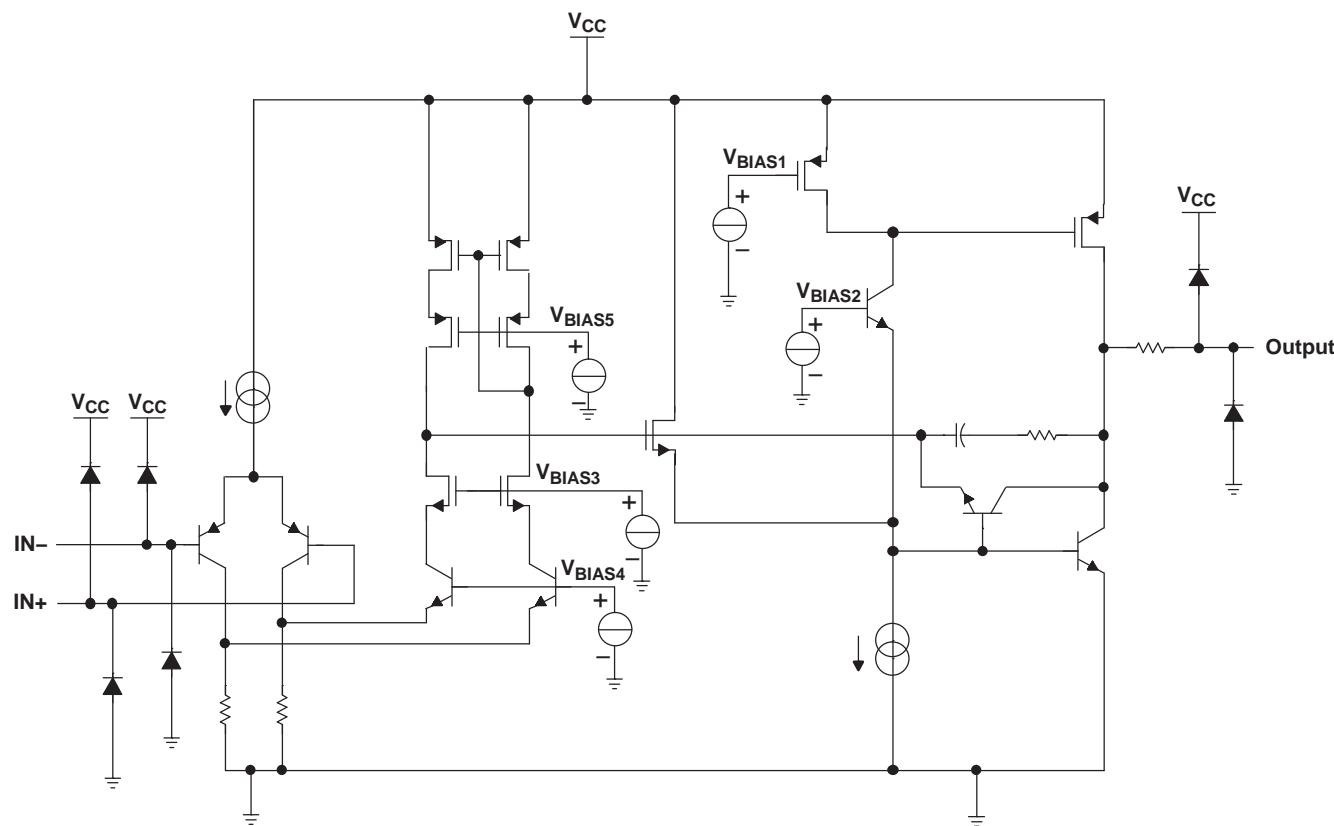


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SYMBOL (EACH AMPLIFIER)



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage ⁽²⁾	5.5 V
V_{ID}	Differential input voltage ⁽³⁾	$\pm V_{CC}$
V_I	Input voltage range (either input)	V_{CC-} to V_{CC+}
	Duration of output short circuit (one amplifier) to ground ⁽⁴⁾	At or below $T_A = 25^\circ\text{C}$, $V_{CC} \leq 5.5 \text{ V}$ Unlimited
θ_{JA}	Package thermal impedance ^{(5) (6)}	D package 97°C/W
		DBV package 206°C/W
		DGK package 172°C/W
		PW package 113°C/W
T_J	Operating virtual-junction temperature	150°C
T_{stg}	Storage temperature range	-65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
- (5) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)	2.5	5	V
T_A	Operating free-air temperature	-40	125	°C

2.5-V ELECTRICAL CHARACTERISTICS

$V_{CC+} = 2.5 \text{ V}$, $V_{CC-} = 0 \text{ V}$, $V_{IC} = 1 \text{ V}$, $V_O = 1.25 \text{ V}$, and $R_L > 1 \text{ M}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage		25°C		1	6	mV
		-40°C to 125°C			6	
V_O Output swing	$V_{CC+} = 2.5 \text{ V}$, $R_L = 600 \Omega$ to 1.25 V	High level	25°C	2.28	2.37	V
			-40°C to 125°C	2.18		
		Low level	25°C		0.13	
			-40°C to 125°C		0.32	
	$V_{CC+} = 2.5 \text{ V}$, $R_L = 2 \text{ k}\Omega$ to 1.25 V	High level	25°C	2.38	2.46	
			-40°C to 125°C	2.28		
		Low level	25°C		0.08	
			-40°C to 125°C		0.22	

2.7-V ELECTRICAL CHARACTERISTICS

$V_{CC+} = 2.7 \text{ V}$, $V_{CC-} = 0 \text{ V}$, $V_{IC} = 1 \text{ V}$, $V_O = 1.35 \text{ V}$, and $R_L > 1 \text{ M}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage		25°C		1	6	mV
		–40°C to 125°C			6	
α_{VIO} Average temperature coefficient of input offset voltage		25°C		1		$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current		25°C		30	90	nA
		–40°C to 125°C			140	
I_{IO} Input offset current		25°C		0.5	30	nA
		–40°C to 125°C			50	
CMRR Common-mode rejection ratio	$V_{IC} = 0 \text{ to } 1.7 \text{ V}$	25°C	70	85		dB
		–40°C to 125°C	68			
$+k_{SVR}$ Positive supply-voltage rejection ratio	$V_{CC+} = 1.7 \text{ V to } 4 \text{ V}$, $V_{CC-} = –1 \text{ V}$, $V_O = 0$, $V_{IC} = 0$	25°C	75	85		dB
		–40°C to 125°C	70			
$-k_{SVR}$ Negative supply-voltage rejection ratio	$V_{CC+} = 1.7 \text{ V}$, $V_{CC-} = –1 \text{ V to } –3.3 \text{ V}$, $V_O = 0$, $V_{IC} = 0$	25°C	73	85		dB
		–40°C to 125°C	70			
V_{ICR} Common-mode input voltage range	$CMRR \geq 50 \text{ dB}$	25°C	–0.2 to 1.9	–0.3 to 2		V
A_v Large-signal voltage amplification	$R_L = 600 \Omega \text{ to } 1.35 \text{ V}$, $V_O = 1.35 \text{ V to } 2.2 \text{ V}$	Sourcing	25°C	90	100	dB
			–40°C to 125°C	85		
	$R_L = 600 \Omega \text{ to } 1.35 \text{ V}$, $V_O = 1.35 \text{ V to } 0.5 \text{ V}$	Sinking	25°C	85	90	
			–40°C to 125°C	80		
	$R_L = 2 \text{ k}\Omega \text{ to } 1.35 \text{ V}$, $V_O = 1.35 \text{ V to } 2.2 \text{ V}$	Sourcing	25°C	95	100	
			–40°C to 125°C	90		
	$R_L = 2 \text{ k}\Omega \text{ to } 1.35 \text{ V}$, $V_O = 1.35 \text{ V to } 0.5 \text{ V}$	Sinking	25°C	90	95	
			–40°C to 125°C	85		
V_O Output swing	$V_{CC+} = 2.7 \text{ V}$, $R_L = 600 \Omega \text{ to } 1.35 \text{ V}$	High level	25°C	2.5	2.58	V
			–40°C to 125°C	2.4		
		Low level	25°C		0.13 0.2	
			–40°C to 125°C		0.3	
	$V_{CC+} = 2.7 \text{ V}$, $R_L = 2 \text{ k}\Omega \text{ to } 1.35 \text{ V}$	High level	25°C	2.6	2.66	
			–40°C to 125°C	2.5		
		Low level	25°C		0.08 0.12	
			–40°C to 125°C		0.2	
I_O Output current	$V_O = 0 \text{ V}$	Sourcing	25°C	12	16	mA
	$V_O = 2.7 \text{ V}$	Sinking	25°C	12	26	
I_{CC} Supply current	LMV821		25°C		0.22 0.3	mA
			–40°C to 125°C		0.5	
	LMV822 (both amplifiers)		25°C		0.45 0.6	
			–40°C to 125°C		0.8	
	LMV824 (all four amplifiers)		25°C		0.72 1	
			–40°C to 125°C		1.2	

2.7-V ELECTRICAL CHARACTERISTICS (continued)

$V_{CC+} = 2.7$ V, $V_{CC-} = 0$ V, $V_{IC} = 1$ V, $V_O = 1.35$ V, and $R_L > 1$ M Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR Slew rate ⁽¹⁾		25°C		1.7		V/ μ s
GBW Gain bandwidth product	(2)	25°C		5		MHz
Φ_m Phase margin	(2)	25°C		60		deg
Gain margin	(2)	25°C		8.6		dB
Amplifier-to-amplifier isolation	$V_{CC+} = 5$ V, $R_L = 100$ k Ω to 2.5 V ⁽³⁾	25°C		135		dB
V_n Equivalent input noise voltage	$f = 1$ kHz, $V_{IC} = 1$ V	25°C		45		nV/ $\sqrt{\text{Hz}}$
I_n Equivalent input noise current	$f = 1$ kHz	25°C		0.18		pA/ $\sqrt{\text{Hz}}$
THD Total harmonic distortion	$f = 1$ kHz, $A_V = -2$, $R_L = 10$ k Ω , $V_O = 4.1$ V _{p-p}	25°C		0.01		%

(1) Connected as voltage follower with 1-V step input. Value specified is the slower of the positive and negative slew rates.

(2) 40-dB closed-loop dc gain, $C_L = 22$ pF

(3) Each amplifier excited in turn with 1 kHz to produce $V_O = 3$ V_{p-p}

5-V ELECTRICAL CHARACTERISTICS

$V_{CC+} = 5 \text{ V}$, $V_{CC-} = 0 \text{ V}$, $V_{IC} = 2 \text{ V}$, $V_O = 2.5 \text{ V}$, and $R_L > 1 \text{ M}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP	MAX	UNIT	
V _{IO}	Input offset voltage			25°C		1	6	mV	
				–40°C to 125°C			6		
α_{VIO}	Average temperature coefficient of input offset voltage			25°C		1		$\mu\text{V}/^\circ\text{C}$	
I _{IB}	Input bias current			25°C		40	100	nA	
				–40°C to 125°C			150		
I _{IO}	Input offset current			25°C		0.5	30	nA	
				–40°C to 125°C			50		
CMRR	Common-mode rejection ratio	$V_{IC} = 0 \text{ to } 4 \text{ V}$		25°C	72	90		dB	
				–40°C to 125°C	70				
+k _{SVR}	Positive supply-voltage rejection ratio	$V_{CC+} = 1.7 \text{ V to } 4 \text{ V}$, $V_{CC-} = –1 \text{ V}$, $V_O = 0$, $V_{IC} = 0$		25°C	75	85		dB	
				–40°C to 125°C	70				
–k _{SVR}	Negative supply-voltage rejection ratio	$V_{CC+} = 1.7 \text{ V}$, $V_{CC-} = –1 \text{ V to } –3.3 \text{ V}$, $V_O = 0$, $V_{IC} = 0$		25°C	73	85		dB	
				–40°C to 125°C	70				
V _{ICR}	Common-mode input voltage range	CMRR $\geq 50 \text{ dB}$		25°C	–0.2 to 4.2	–0.3 to 4.3		V	
A _v	Large-signal voltage amplification	$R_L = 600 \Omega \text{ to } 2.5 \text{ V}$, $V_O = 2.5 \text{ V to } 4.5 \text{ V}$	Sourcing	25°C	95	105		dB	
				–40°C to 125°C	90				
		$R_L = 600 \Omega \text{ to } 2.5 \text{ V}$, $V_O = 2.5 \text{ V to } 0.5 \text{ V}$	Sinking	25°C	95	105			
				–40°C to 125°C	90				
		$R_L = 2 \text{ k}\Omega \text{ to } 2.5 \text{ V}$, $V_O = 2.5 \text{ V to } 4.5 \text{ V}$	Sourcing	25°C	95	105			
				–40°C to 125°C	90				
		$R_L = 2 \text{ k}\Omega \text{ to } 2.5 \text{ V}$, $V_O = 2.5 \text{ V to } 0.5 \text{ V}$	Sinking	25°C	95	105			
				–40°C to 125°C	90				
V _O	Output swing	$V_{CC+} = 5 \text{ V}$, $R_L = 600 \Omega \text{ to } 2.5 \text{ V}$	High level	25°C	4.75	4.84		V	
				–40°C to 125°C	4.6				
			Low level	25°C		0.17	0.25		
				–40°C to 125°C			0.3		
		$V_{CC+} = 5 \text{ V}$, $R_L = 2 \text{ k}\Omega \text{ to } 2.5 \text{ V}$	High level	25°C	4.85	4.9			
				–40°C to 125°C	4.8				
			Low level	25°C		0.1	0.15		
				–40°C to 125°C			0.2		
I _O	Output current	$V_O = 0 \text{ V}$	Sourcing	25°C	20	45		mA	
				–40°C to 125°C	15				
		$V_O = 5 \text{ V}$	Sinking	25°C	20	40			
				–40°C to 125°C	15				
I _{CC}	Supply current	LMV821		25°C		0.3	0.4	mA	
				–40°C to 125°C			0.6		
		LMV822 (both amplifiers)		25°C		0.5	0.7		
				–40°C to 125°C			0.9		
		LMV824 (all four amplifiers)		25°C		1	1.3		
				–40°C to 125°C			1.5		

5-V ELECTRICAL CHARACTERISTICS (continued)

$V_{CC+} = 5 \text{ V}$, $V_{CC-} = 0 \text{ V}$, $V_{IC} = 2 \text{ V}$, $V_O = 2.5 \text{ V}$, and $R_L > 1 \text{ M}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR Slew rate	$V_{CC+} = 5 \text{ V}^{(1)}$	25°C	1.4	1.9		$\text{V}/\mu\text{s}$
GBW Gain bandwidth product	(2)	25°C		5.5		MHz
Φ_m Phase margin	(2)	25°C		64.2		deg
Gain margin	(2)	25°C		8.7		dB
Amplifier-to-amplifier isolation	$V_{CC+} = 5 \text{ V}$, $R_L = 100 \text{ k}\Omega$ to $2.5 \text{ V}^{(3)}$	25°C		135		dB
V_n Equivalent input noise voltage	$f = 1 \text{ kHz}$, $V_{IC} = 1 \text{ V}$	25°C		42		$\text{nV}/\sqrt{\text{Hz}}$
I_n Equivalent input noise current	$f = 1 \text{ kHz}$	25°C		0.2		$\text{pA}/\sqrt{\text{Hz}}$
THD Total harmonic distortion	$f = 1 \text{ kHz}$, $A_V = -2$, $R_L = 10 \text{ k}\Omega$, $V_O = 4.1 \text{ V}_{\text{p-p}}$	25°C		0.01		%

(1) Connected as voltage follower with 3-V step input. Value specified is the slower of the positive and negative slew rates.

(2) 40-dB closed-loop dc gain, $C_L = 22 \text{ pF}$

(3) Each amplifier excited in turn with 1 kHz to produce $V_O = 3 \text{ V}_{\text{p-p}}$

TYPICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{-V}$ single supply (unless otherwise noted)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

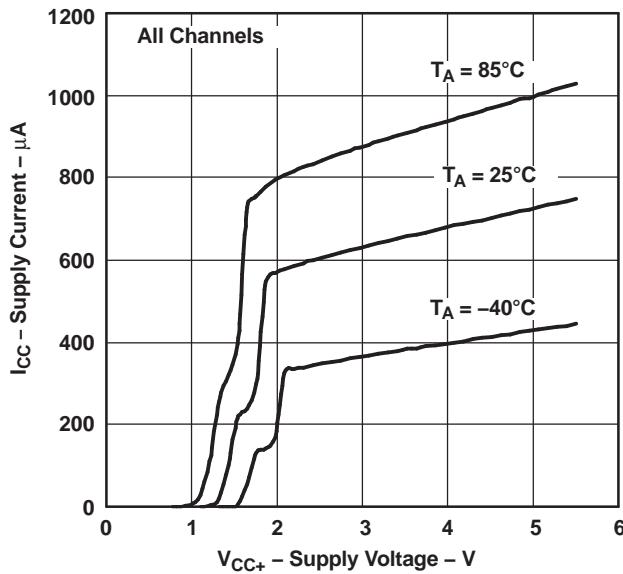


Figure 1.

INPUT CURRENT
vs
TEMPERATURE

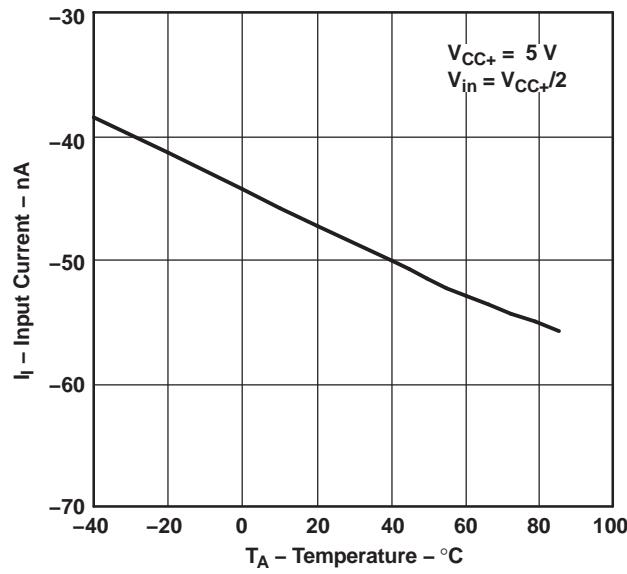


Figure 2.

SOURCING CURRENT
vs
OUTPUT VOLTAGE

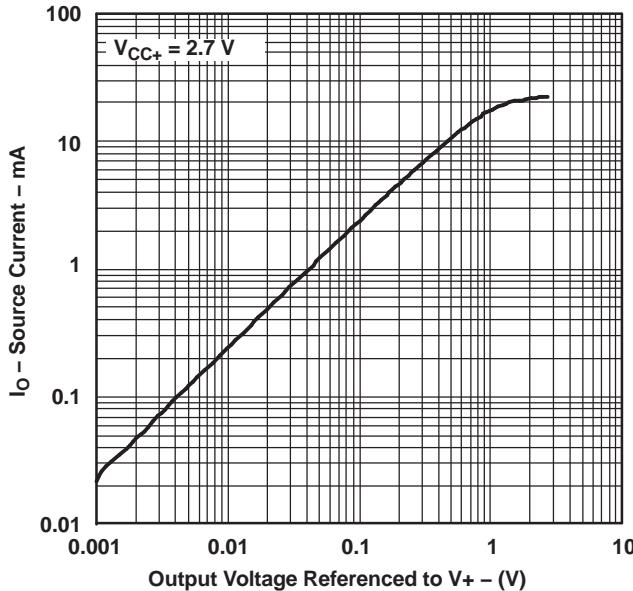


Figure 3.

SOURCING CURRENT
vs
OUTPUT VOLTAGE

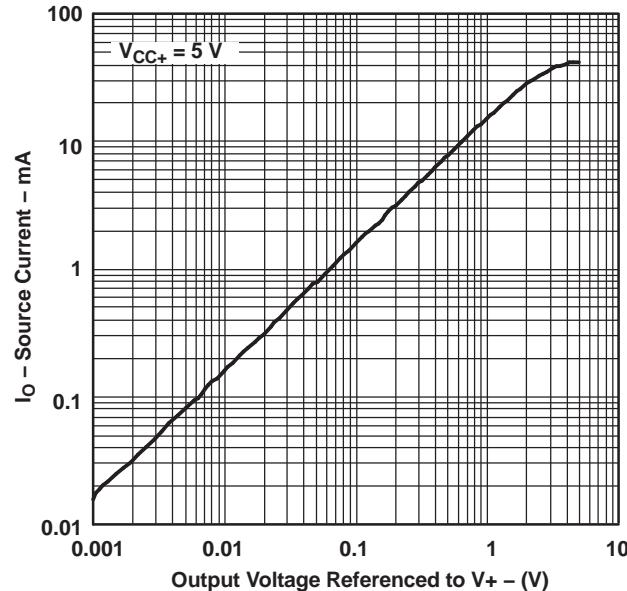


Figure 4.

TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{-V}$ single supply (unless otherwise noted)

**SINKING CURRENT
vs
OUTPUT VOLTAGE**

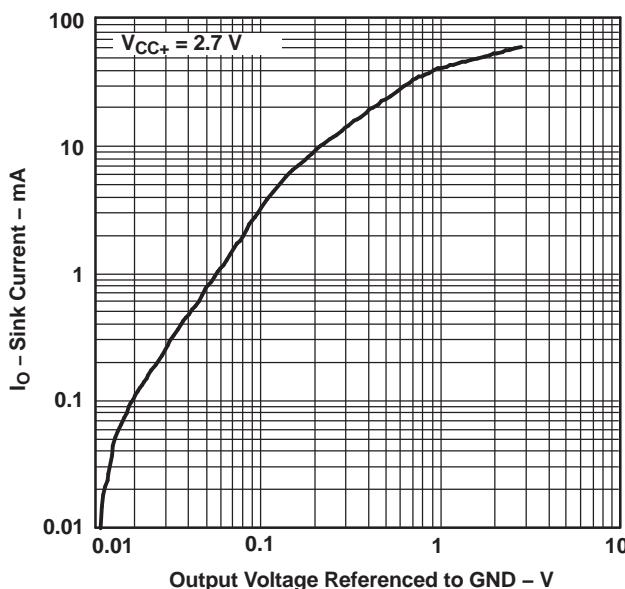


Figure 5.

**SINKING CURRENT
vs
OUTPUT VOLTAGE**

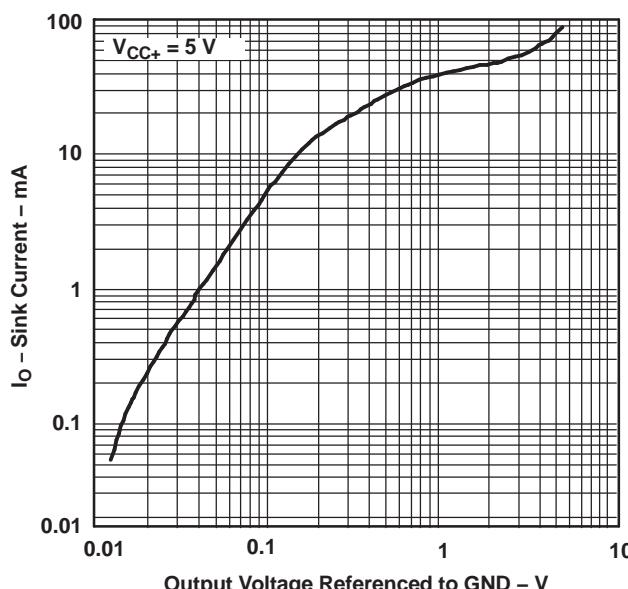


Figure 6.

**OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE**

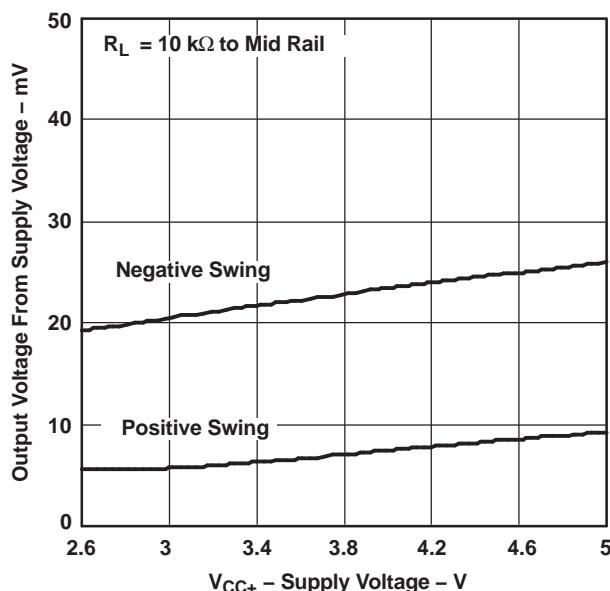


Figure 7.

**OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE**

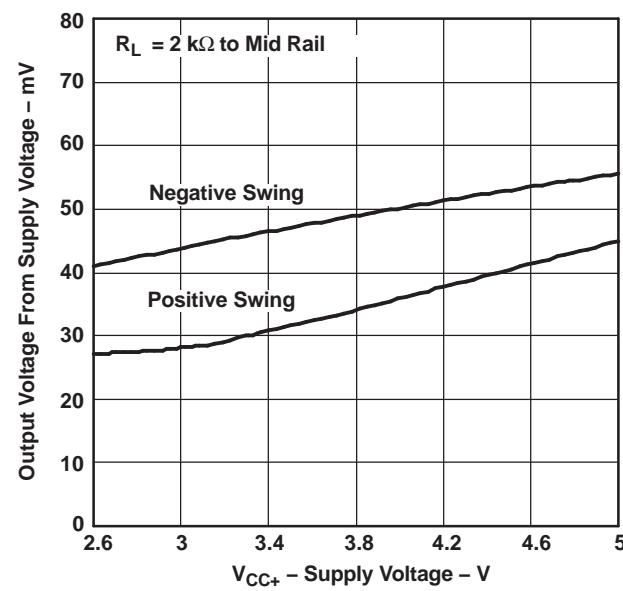


Figure 8.

TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{-V}$ single supply (unless otherwise noted)

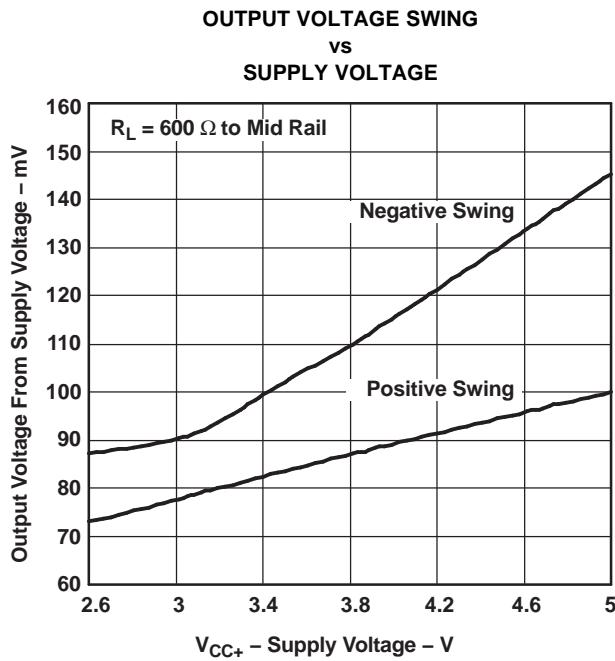


Figure 9.

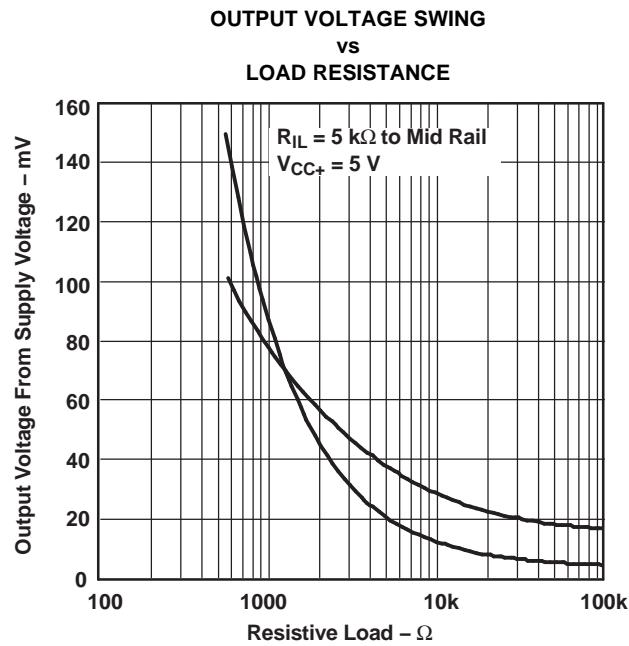


Figure 10.

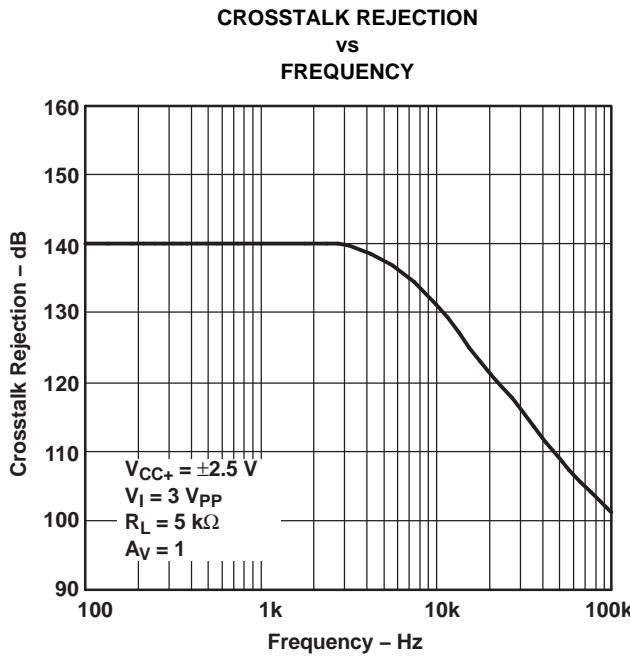


Figure 11.

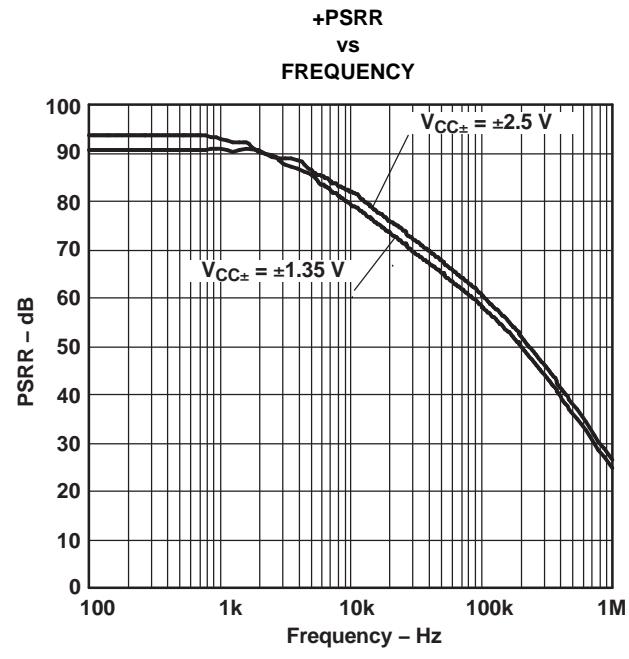


Figure 12.

TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{-V}$ single supply (unless otherwise noted)

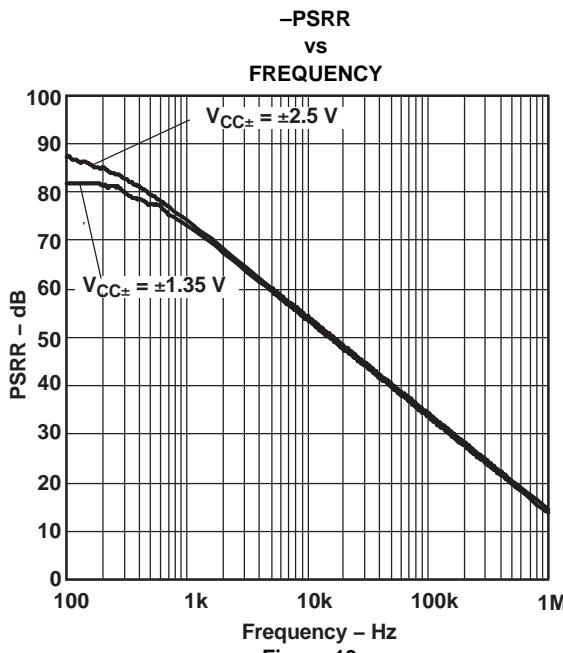


Figure 13.

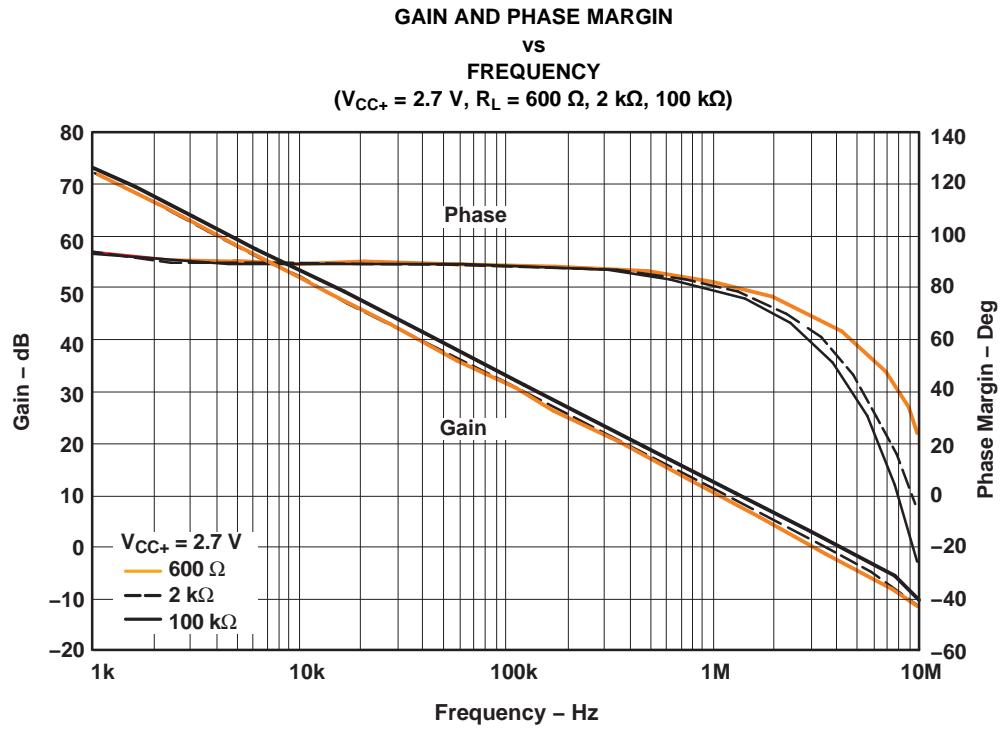


Figure 14.

TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{-V}$ single supply (unless otherwise noted)

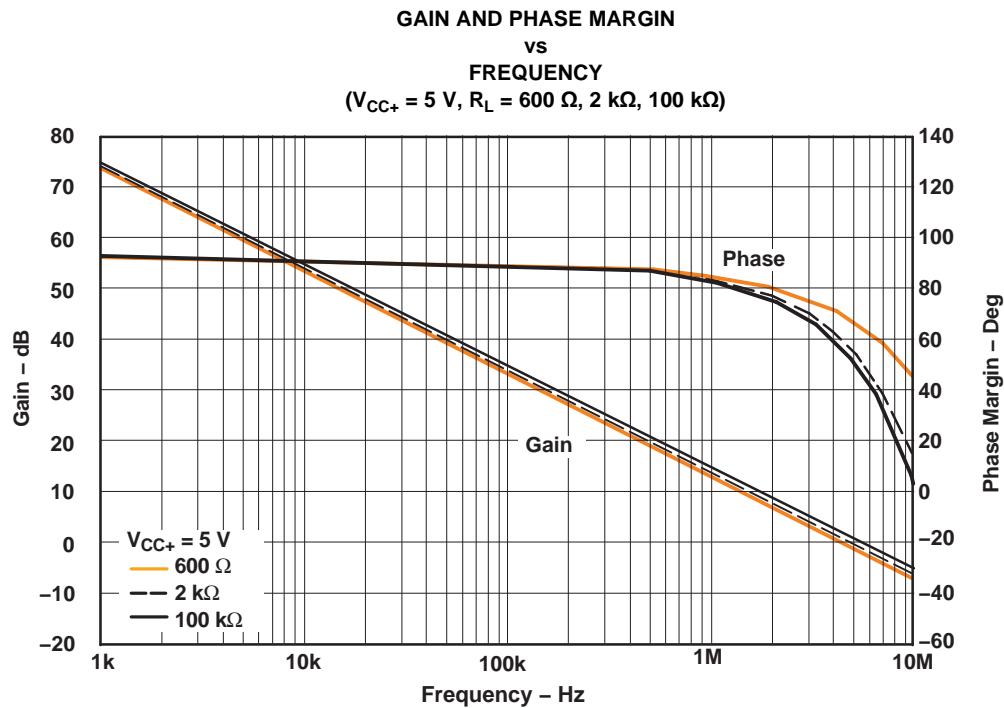


Figure 15.

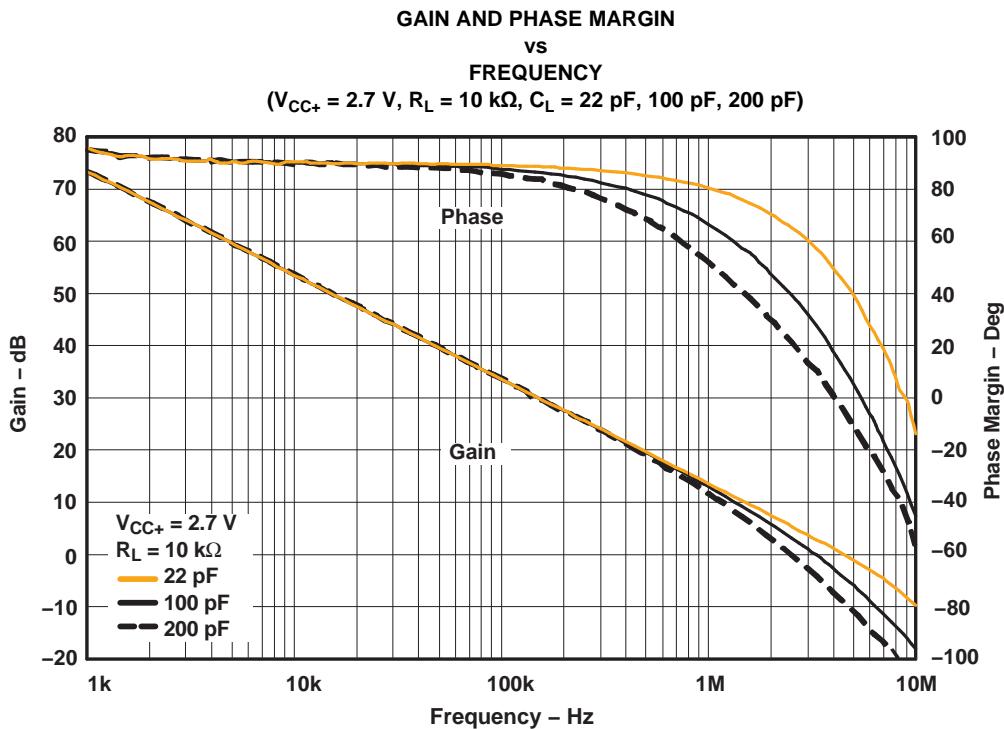


Figure 16.

TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{-V}$ single supply (unless otherwise noted)

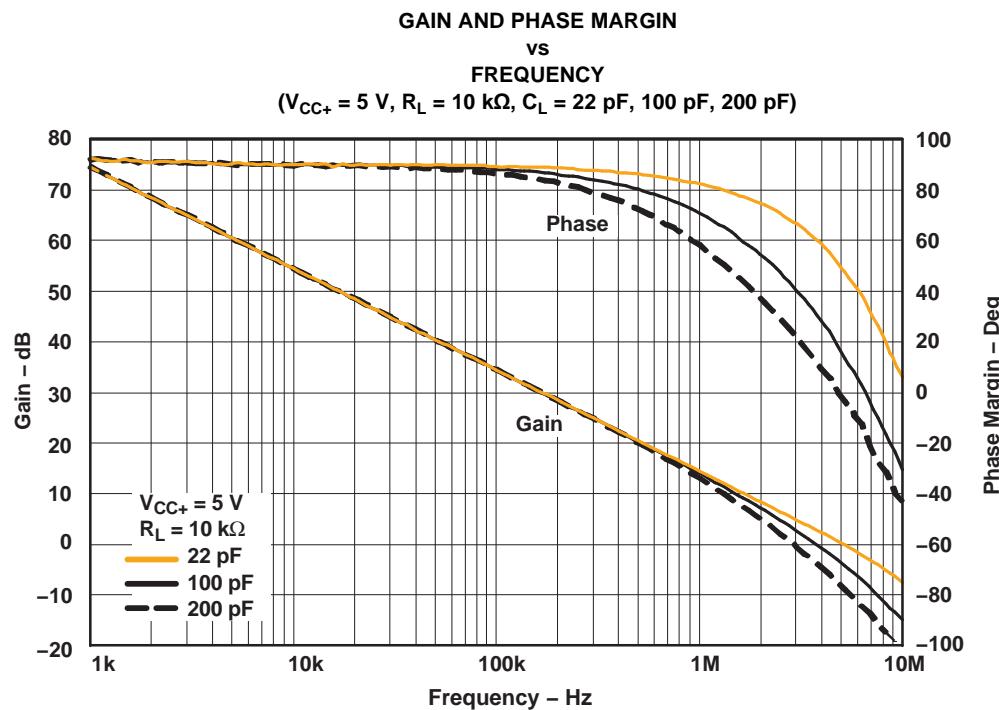


Figure 17.

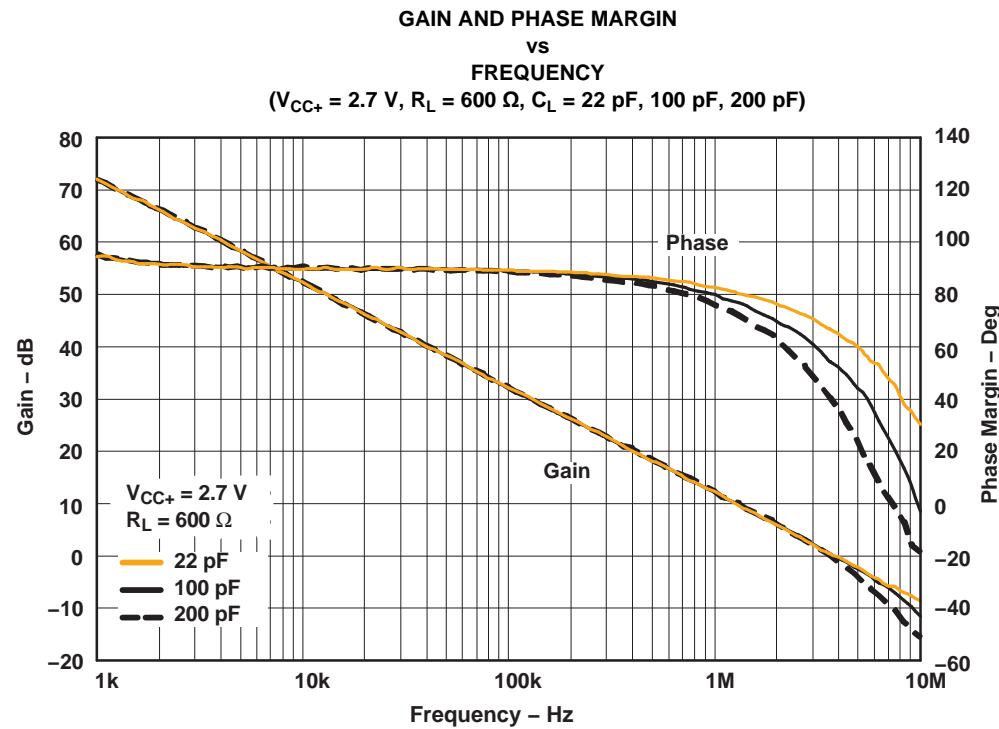


Figure 18.

TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{-V}$ single supply (unless otherwise noted)

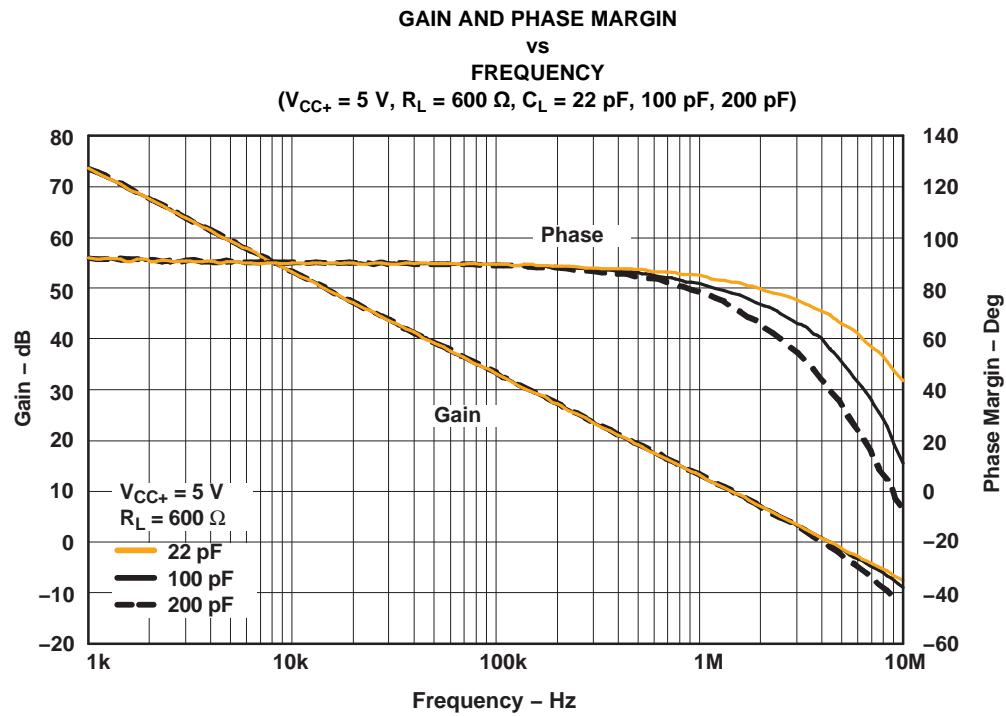


Figure 19.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LMV821QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
LMV822QDGKRQ1	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
LMV824QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
LMV824QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF LMV821-Q1, LMV822-Q1, LMV824-Q1 :



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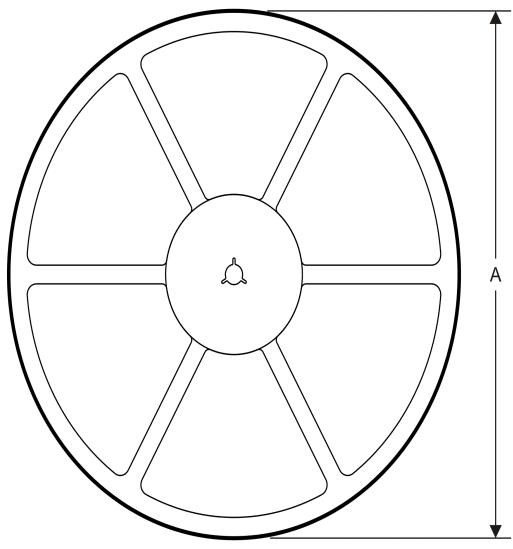
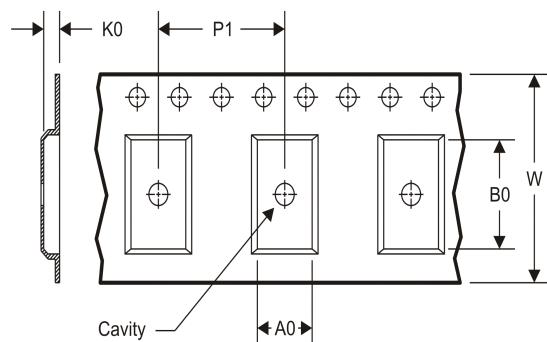
PACKAGE OPTION ADDENDUM

22-Sep-2010

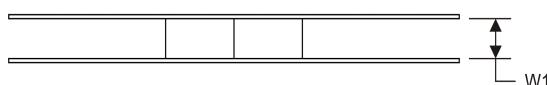
- Catalog: [LMV821](#), [LMV822](#), [LMV824](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

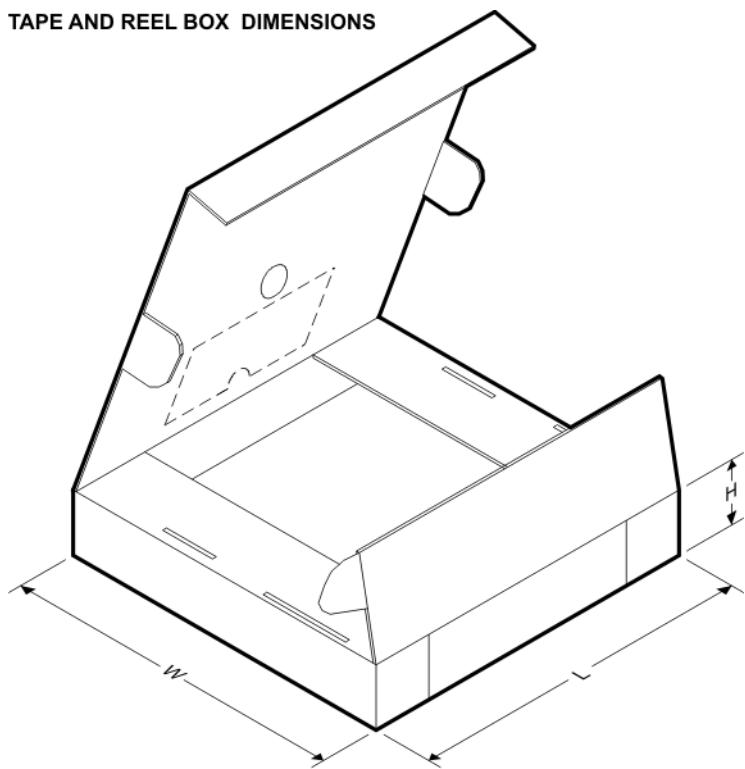
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV824QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

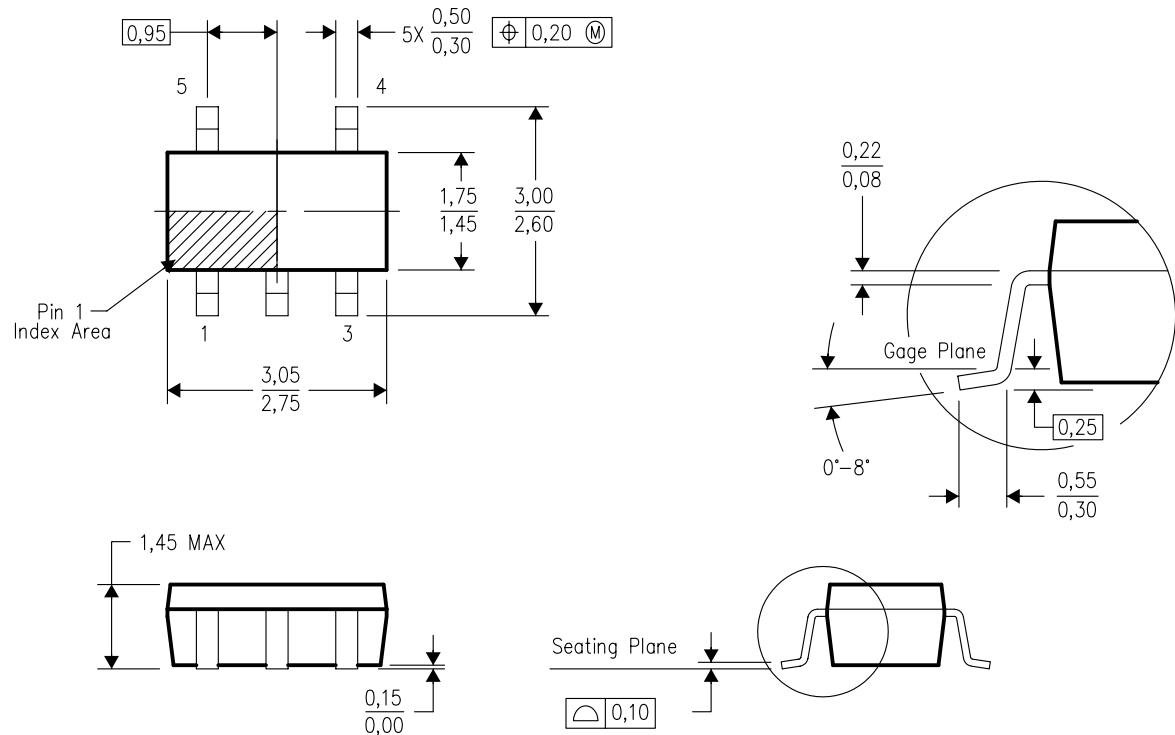
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV824QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

DBV (R-PDS0-G5)

PLASTIC SMALL-OUTLINE PACKAGE



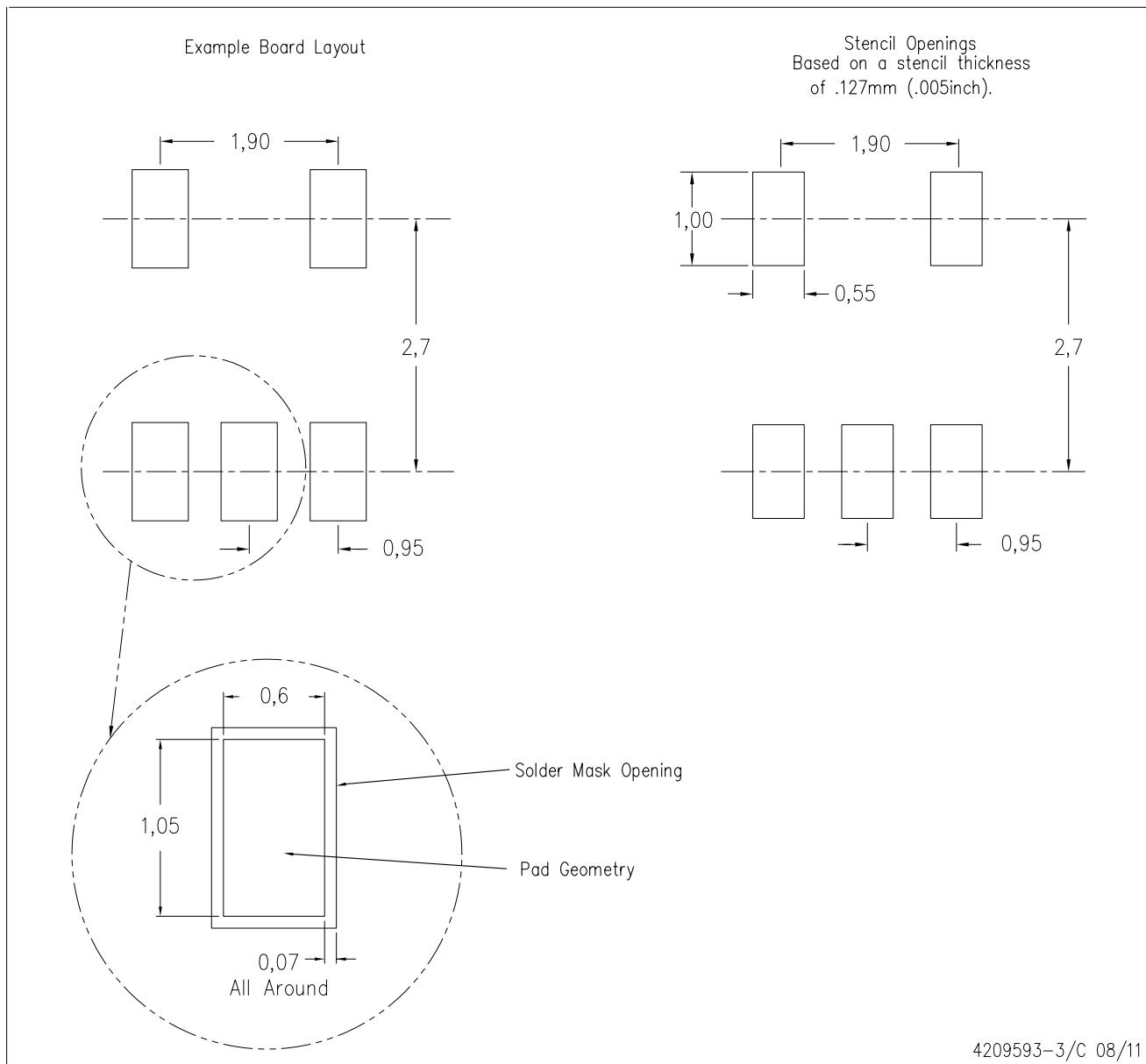
4073253-4/K 03/2006

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

LAND PATTERN DATA

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

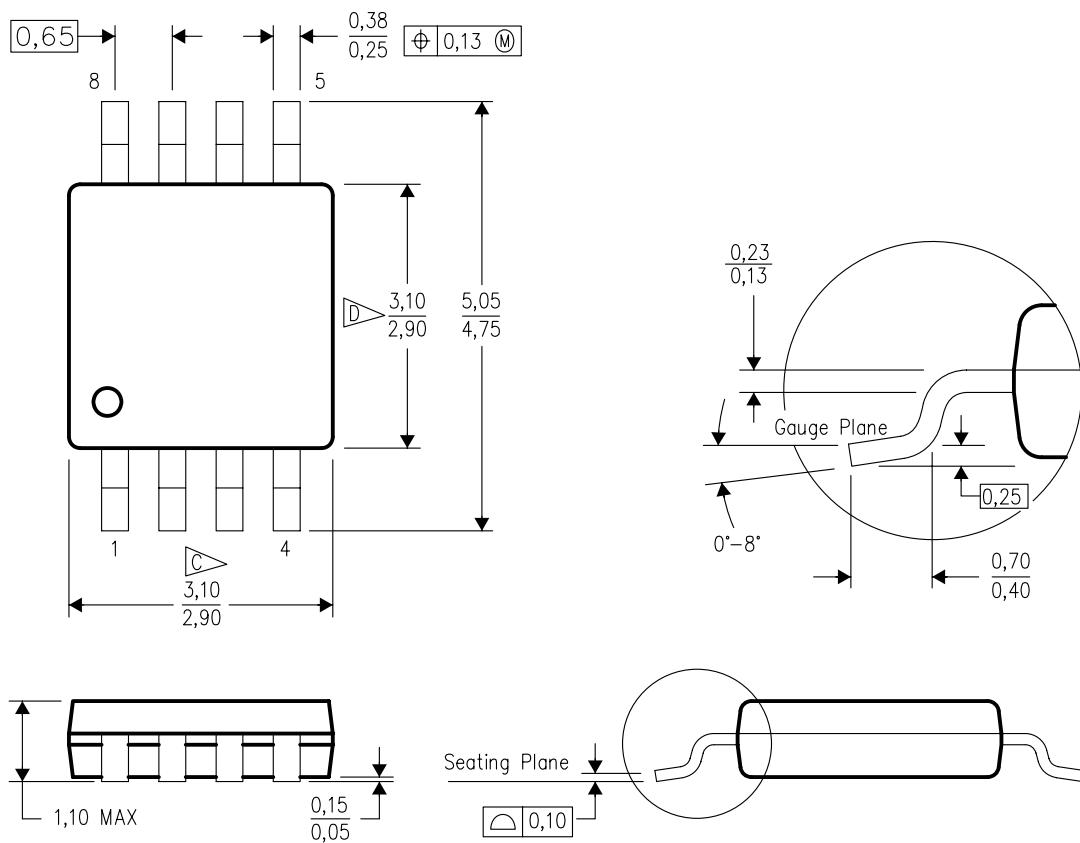


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

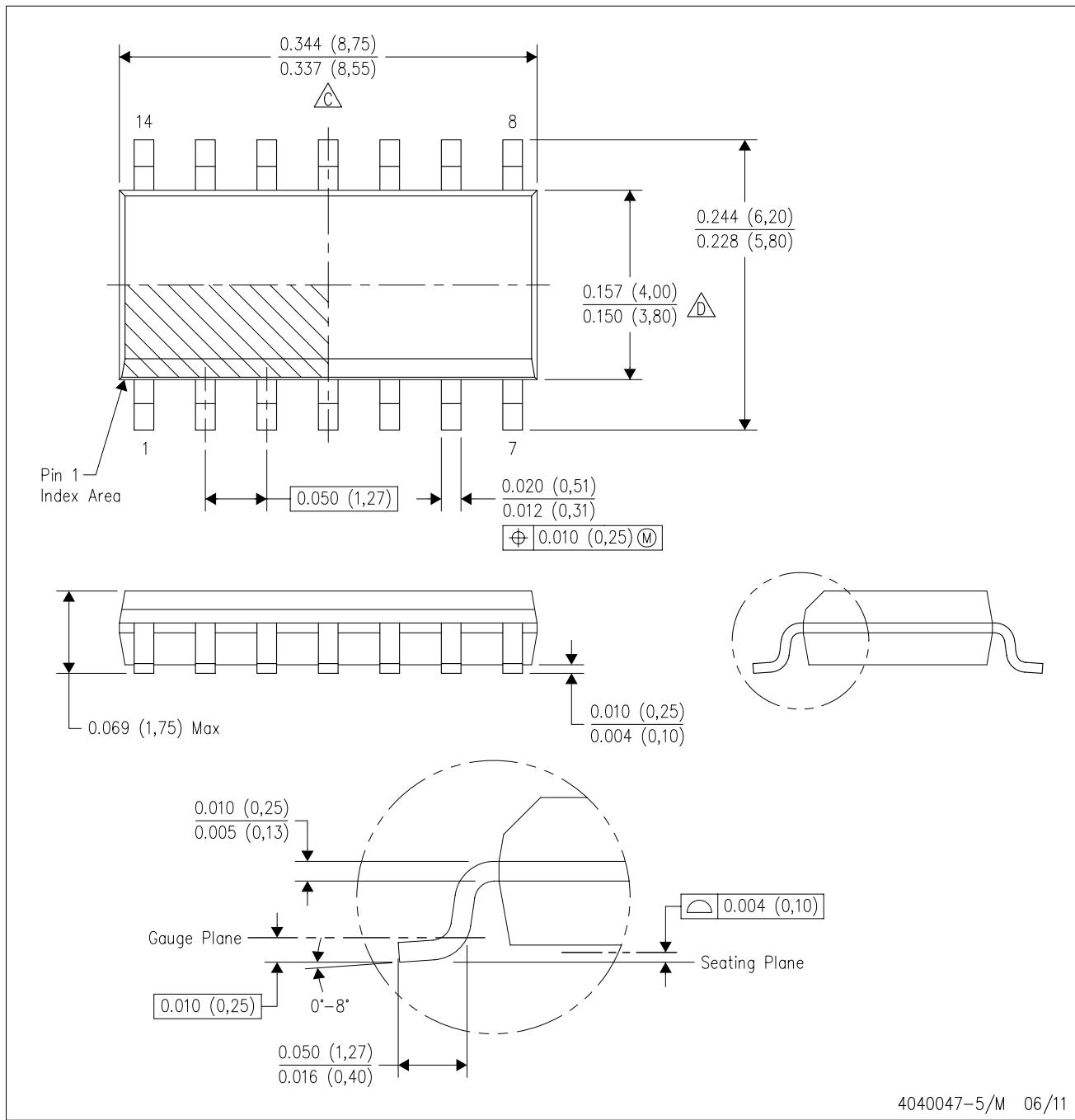
 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

 Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

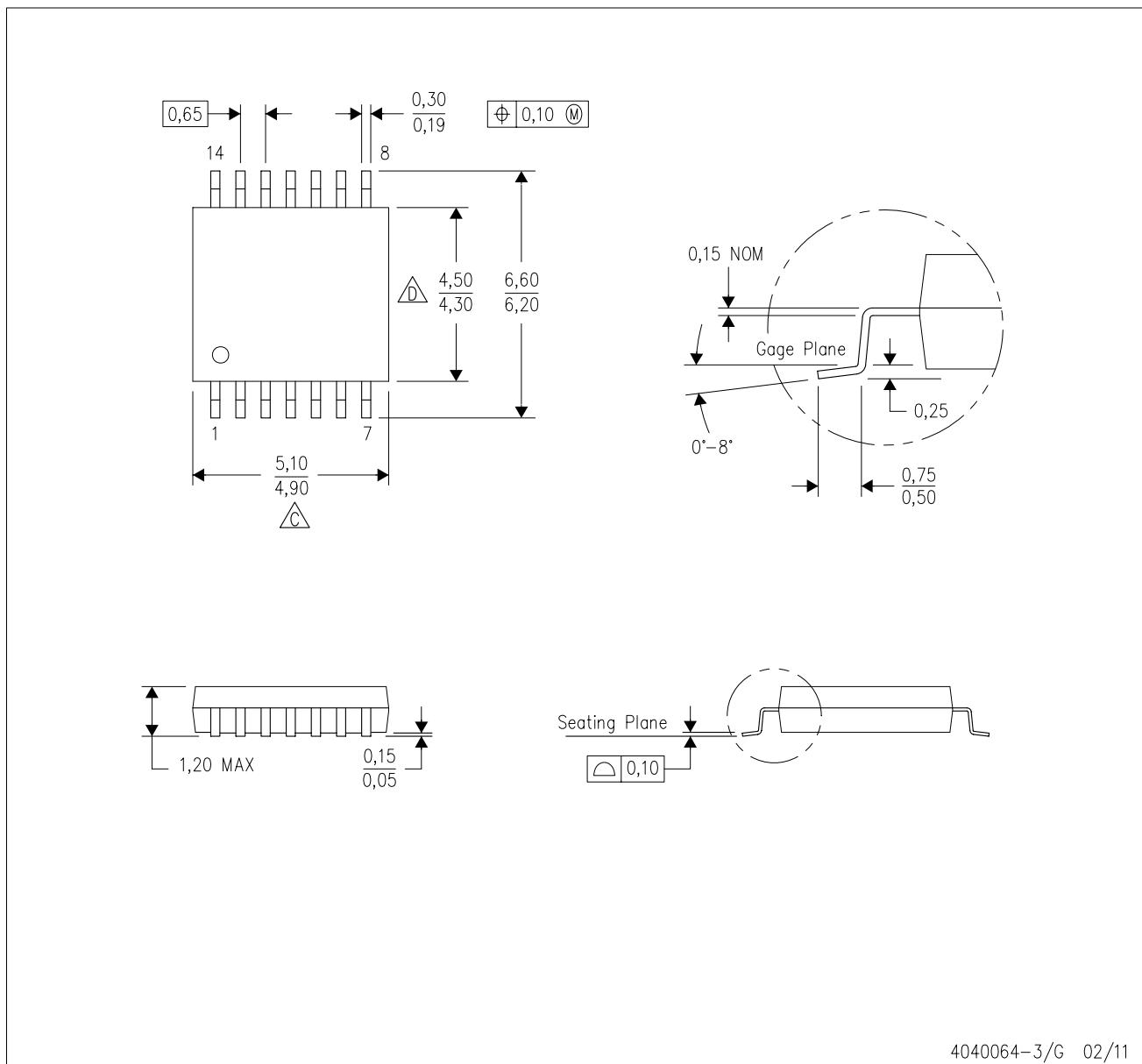
(C) Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

(D) Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

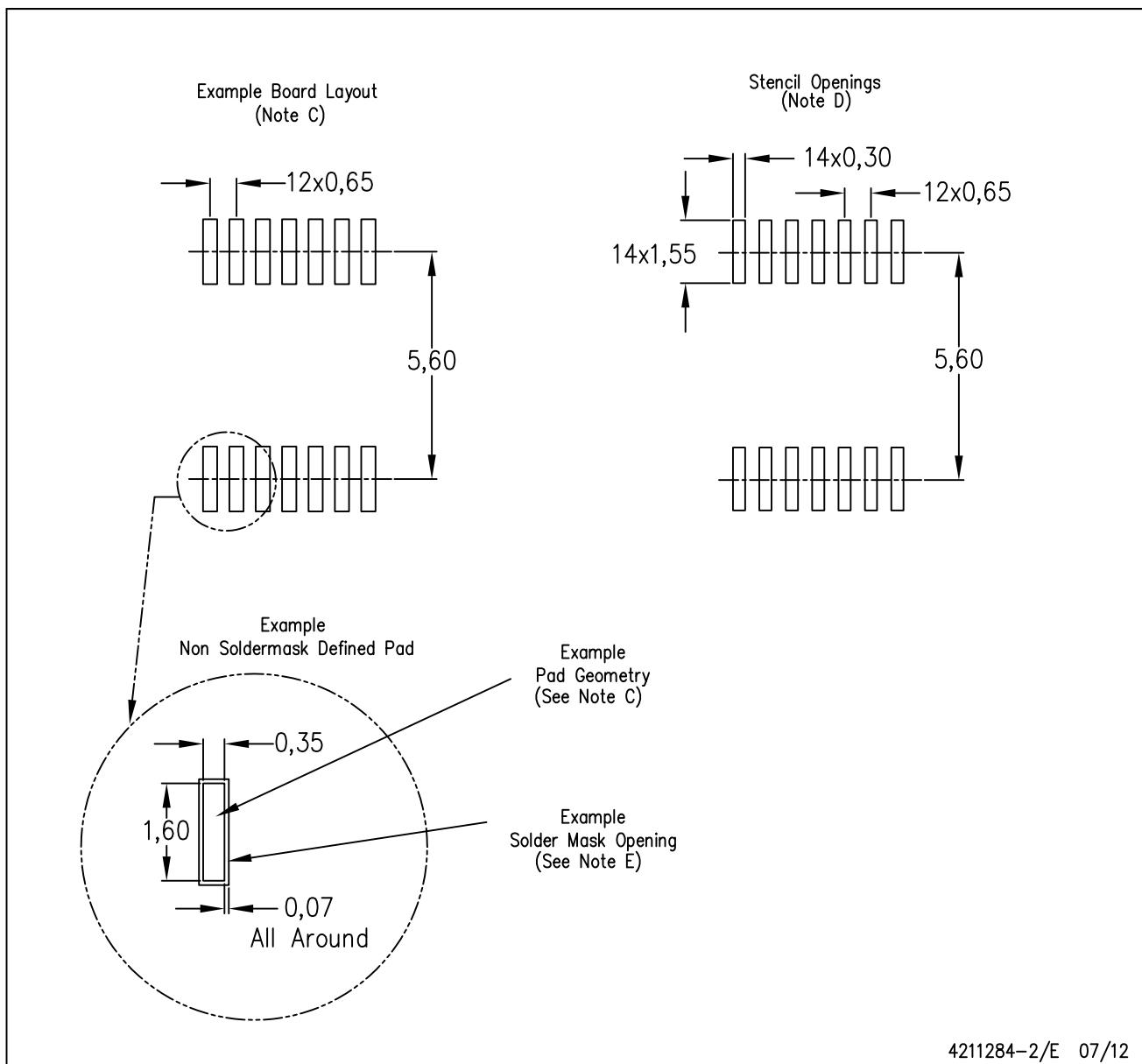
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/E 07/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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