TEXAS INSTRUMENTS

CY74FCT16240T
CY74FCT162240T

16-Bit Buffers/Line Drivers

Features

- **I_{off} supports partial-power-down mode operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of –40˚C to +85˚C**
- **V_{CC} = 5V $\pm$ 10%**

CY74FCT16240T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162240T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**
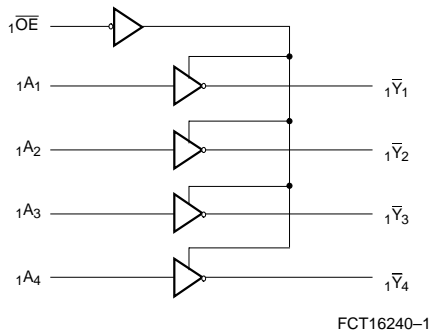
Functional Description

These 16-bit buffer/line drivers are used in memory driver, clock driver, or other bus interface applications, where high speed and low power are required. With flow-through pinout and small shrink packaging, board layout is simplified. The three-state controls are designed to allow 4-, 8-, or 16-bit operation.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.
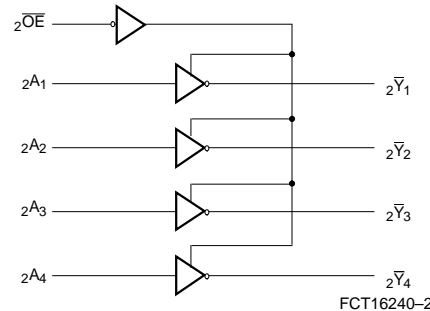
The CY74FCT16240T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162240T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162240T is ideal for driving transmission lines.
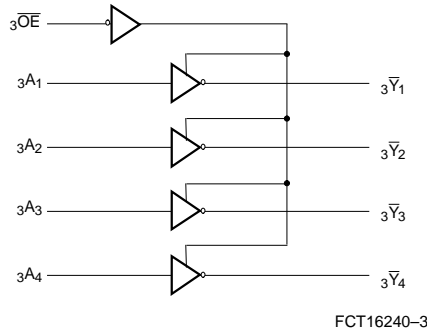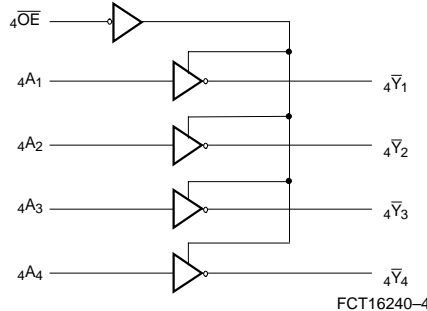
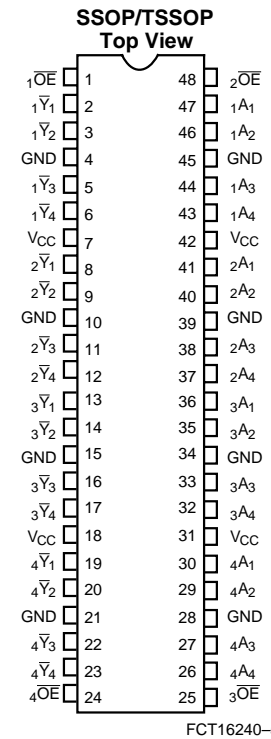## Logic Block Diagrams

FCT16240–1

FCT16240–3

FCT16240–2

FCT16240–4

Pin Configuration

**SSOP/TSSOP
Top View**

$1\overline{OE}$	1	48	$2\overline{OE}$
$1\overline{Y}_1$	2	47	$1A_1$
$1\overline{Y}_2$	3	46	$1A_2$
GND	4	45	GND
$1\overline{Y}_3$	5	44	$1A_3$
$1\overline{Y}_4$	6	43	$1A_4$
V_{CC}	7	42	V_{CC}
$2\overline{Y}_1$	8	41	$2A_1$
$2\overline{Y}_2$	9	40	$2A_2$
GND	10	39	GND
$2\overline{Y}_3$	11	38	$2A_3$
$2\overline{Y}_4$	12	37	$2A_4$
$3\overline{Y}_1$	13	36	$3A_1$
$3\overline{Y}_2$	14	35	$3A_2$
GND	15	34	GND
$3\overline{Y}_3$	16	33	$3A_3$
$3\overline{Y}_4$	17	32	$3A_4$
V_{CC}	18	31	V_{CC}
$4\overline{Y}_1$	19	30	$4A_1$
$4\overline{Y}_2$	20	29	$4A_2$
GND	21	28	GND
$4\overline{Y}_3$	22	27	$4A_3$
$4\overline{Y}_4$	23	26	$4A_4$
$4\overline{OE}$	24	25	$3\overline{OE}$

FCT16240–5

Pin Summary

Name	Description
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
A	Data Inputs
$\overline{Y}$	Three-State Outputs

Function Table[1]

Inputs		Outputs
$\overline{OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....Com'l . −55°C to +125°C

Ambient Temperature with
Power Applied..................................Com'l . −55°C to +125°C

DC Input Voltage .... −0.5V to +7.0V

DC Output Voltage.. −0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) ....−60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage
(per MIL-STD-883, Method 3015) ....>2001V

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_{H}	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN}= −18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = V_{CC}			±1	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = GND			±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC} = Max., V_{OUT} = 2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC} = Max., V_{OUT} = 0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND	−80	−140	−200	mA
I_{O}	Output Drive Current[6]	V_{CC} = Max., V_{OUT} = 2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC} = 0V, $V_{OUT} \le 4.5V$[7]			±1	µA

Output Drive Characteristics for CY74FCT16240T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH}= −3 mA	2.5	3.5		V
		V_{CC} = Min., I_{OH}= −15 mA	2.4	3.5		V
		V_{CC} = Min., I_{OH}= −32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL}= 64 mA		0.2	0.55	V

Notes:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=5.0V, T_A= +25˚C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Tested at +25˚C.

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Output Drive Characteristics for CY74FCT162240T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 24 mA		0.3	0.55	V

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN}\leq0.2V$, $V_{IN}\geq V_{CC}−0.2V$	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[8]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	60	100	μA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	2.4	4.5[11]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[11]	mA

Notes:
8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	CY74FCT16240AT		CY74FCT162240CT		Unit	Fig. No.[13]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	4.8	1.5	4.3	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.6	1.5	5.2	ns	1, 7, 8
$t_{SK(O)}$	Output Skew[14]		0.5		0.5	ns	—

Note:
12. Minimum limits are specified but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.
14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16240

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.8	CY74FCT16240ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162240

| Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	74FCT162240CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162240CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162240CTPVCT	O48	48-Lead (300-Mil) SSOP	

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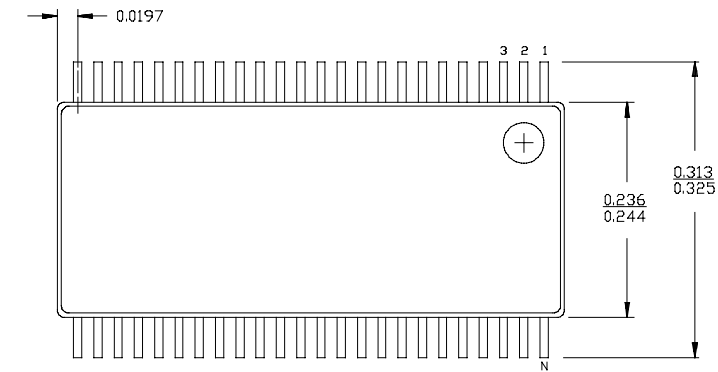## Package Diagrams

48-Lead Shrunk Small Outline Package O48
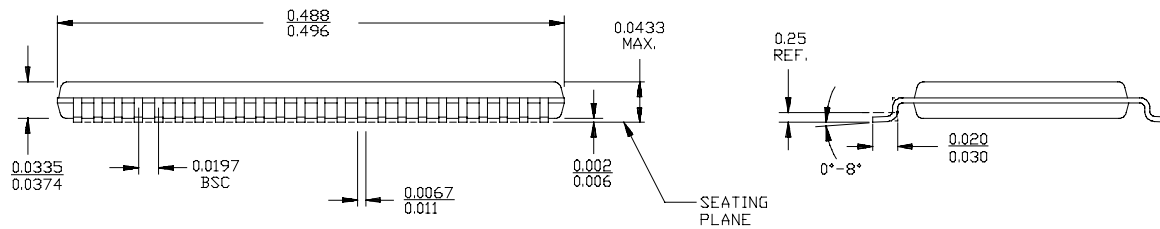

DIMENSIONS IN INCHES MIN.
                      MAX.

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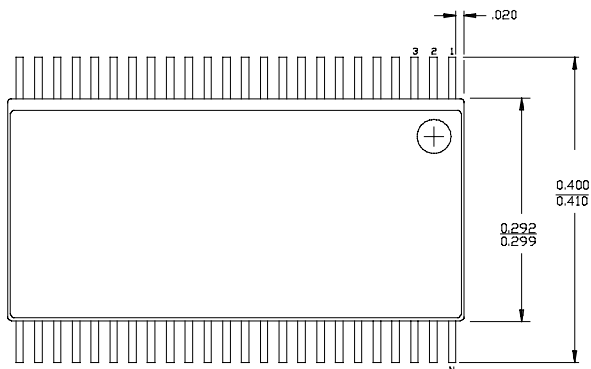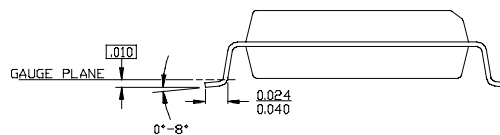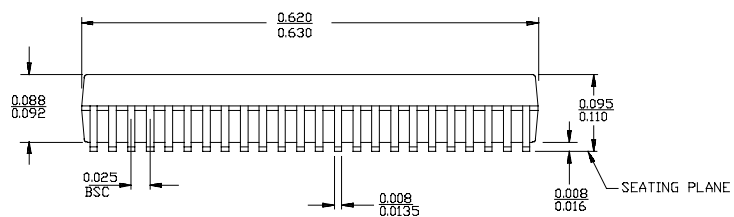
Package Diagrams

48-Lead Thin Shrunk Small Outline Package

0.0197

3 2 1

$\frac{0.313}{0.325}$

$\frac{0.236}{0.244}$

N

DIMENSIONS IN INCHES $\frac{\text{MIN.}}{\text{MAX.}}$

$\frac{0.488}{0.496}$

$\frac{0.0433}{\text{MAX.}}$

0.25
REF.

$\frac{0.0335}{0.0374}$

0.0197
BSC

$\frac{0.0067}{0.011}$

$\frac{0.002}{0.006}$

SEATING
PLANE

0°–8°

$\frac{0.020}{0.030}$

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74FCT162240ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162240CTPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162240CTPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162240ETPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
74FCT162240ETPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
74FCT16240ATPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162240CTPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162240ETPAC	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
CY74FCT162240ETPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
CY74FCT16240ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16240ATPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16240ATPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16240ETPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
CY74FCT16240ETPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
FCT162240ATPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162240CTPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D. Falls within JEDEC MO-118

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DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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