

TEST AND MEASUREMENT PRODUCTS
Description

The SK10E/100E111 is a low skew 1-to-9 differential driver designed with clock distribution in mind. It accepts one signal input which can be either differential or single-ended if the VBB output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all Q* outputs HIGH.

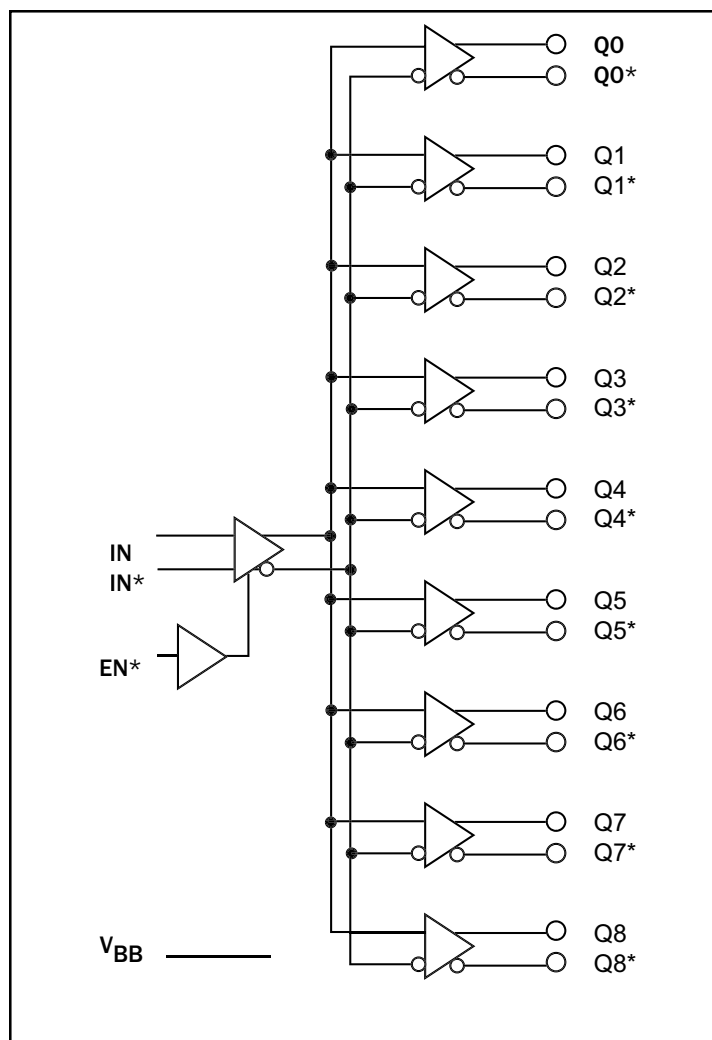
The device is specifically designed, modeled, and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within-device, and characterization is used to determine process control limits that ensure consistent tpd distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

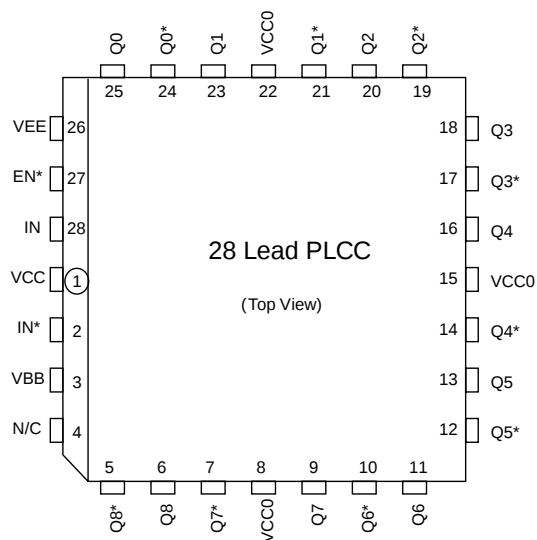
To ensure that the tight skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω , even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same VCCO) as the pair(s) being used on that side in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The SK10/100E111 provides VBB output for either single-ended use or as a DC bias for AC coupling to the device. The VBB output pin should be used only as a DC bias for the E111 as its current sink/source capability is limited. Whenever used, the VBB pin should be bypassed to VCC via a 0.01 μF capacitor.

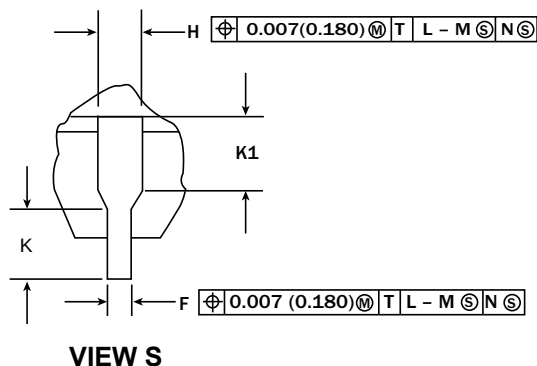
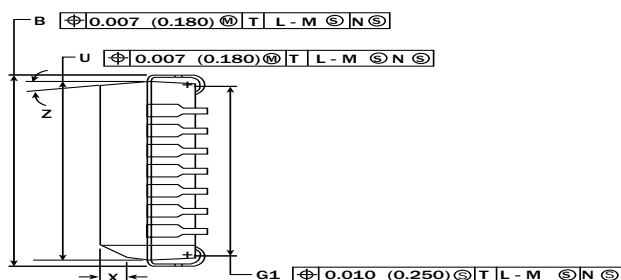
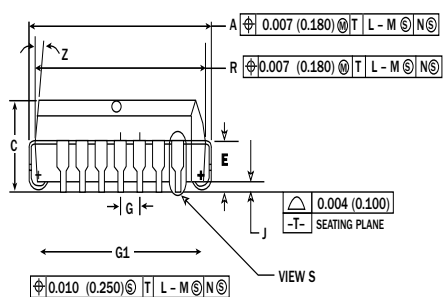
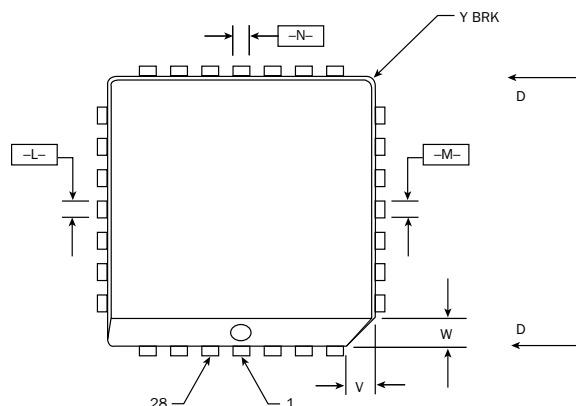
Features

- Low Skew
- Guaranteed Skew Spec
- Differential Design
- VBB Output
- Enable Input
- Extended 100E VEE Range of -4.2 to -5.5V
- Internal $75\text{K}\Omega$ Input Pulldown Resistors
- Compatible with MC10/100E111
- Specified Over Industrial Temperature Range: -40°C to $+85^\circ\text{C}$
- ESD Protection of $>4000\text{V}$
- Available in 28-Lead PLCC Package

Functional Block Diagram


TEST AND MEASUREMENT PRODUCTS
Pin Description
Pinout

Pin Names

Pin	Function
IN, IN*	Differential Input Pair
EN*	Enable
Q0, Q0* - Q8, Q8*	Differential Outputs
VBB	VBB Output
VCC, VCC0	Positive Supply
VEE	Negative Supply
NC	No Connect

TEST AND MEASUREMENT PRODUCTS
Package Information

NOTES:

1. Datums -L-, -M-, and -N- determined where top of lead shoulder exits plastic body at mold parting line.
2. DIM G1, true position to be measured at Datum -T-, Seating Plane.
3. DIM R and U do not include mold flash. Allowable mold flash is 0.010 (0.250) per side.
4. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
5. Controlling Dimension: Inch.
6. The package top may be smaller than the package bottom by up to 0.012 (0.300). Dimensions R and U are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
7. Dimension H does not include Dambar protrusion or intrusion. The Dambar protrusion(s) shall not cause the H dimension to be greater than 0.037 (0.940). The Dambar intrusion(s) shall not cause the H dimension smaller than 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
H	0.026	0.032	0.66	0.81
J	0.020	-	0.51	-
K	0.025	-	0.64	-
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	-	0.020	-	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	-	1.02	-

TEST AND MEASUREMENT PRODUCTS
DC Characteristics
SK10/100E111 DC Electrical Characteristics (Notes 1, 2, 14)

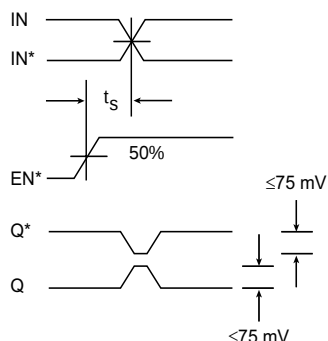
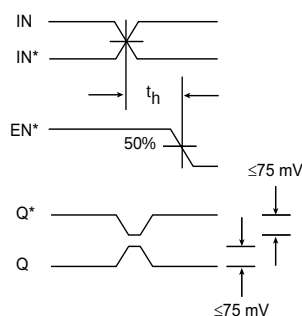
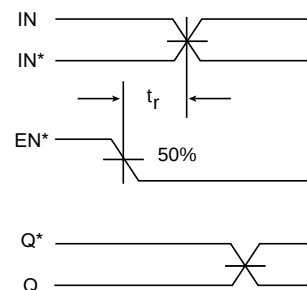
($V_{CC} - V_{EE} = 4.2V$ to $5.5V$; V_{OUT} Loaded 50Ω to $V_{CC} - 2.0V$)

Symbol	Characteristic	TA = - 40°C		TA = 0°C		TA = +25°C		TA = +85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{BB}	Output Reference Voltage ¹³	-1430	-1300	-1380	-1270	-1350	-1250	-1310	-1190	mV
	10EL 100EL	-1380	-1260	-1380	-1260	-1380	-1260	-1380	-1260	mV
I _{IN}	Input Current (Diff) (SE)	-150	150 150	-150	150 150	-150	150 150	-150	150 150	μA μA
I _{EE}	Power Supply Current		64		64		64		69	mA

AC Characteristics
SK10/100E111 AC Electrical Characteristics

($V_{CC} - V_{EE} = 4.2V$ to $5.5V$; V_{OUT} Loaded 50Ω to $V_{CC} - 2.0V$)

Symbol	Characteristic	TA = - 40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{PLH} t _{PHL}	Propagation Delay to Output IN (Diff) ⁵	420		630	440		655	450		660	470		655	ps
	IN (SE) ⁶	280		780	330		730	330		730	330		730	ps
	Enable ⁷	400		900	450		850	450		850	450		850	ps
	Disable	400		900	450		850	450		850	450		850	ps
t _s	Setup Time ⁹ EN to IN	250	0		200	0		200	0		200	0		ps
t _H	Hold Time ¹⁰ IN to EN	50	-200		0	-200		0	-200		0	-200		ps
t _R	Release Time ¹¹ EN* to IN	350	100		300	100		300	100			300	100	ps
t _{skew}	Within-Device Skew ⁸		25	75		25	50		25	50		25	50	ps
V _{PP(AC)}	Minimum Input Swing ¹²	250		1000	250		1000	250		1000	250		1000	mV
V _{CMR}	Common Mode Range ⁴	V _{EE} + 2.6		V _{CC} - 0.4	V _{EE} + 2.6		V _{CC} - 0.4	V _{EE} + 2.6		V _{CC} - 0.4	V _{EE} + 2.6		V _{CC} - 0.4	V
t _r , t _f	Rise/Fall Time (20% to 80%)	215	450	545	225	375	570	230	375	545	240	375	475	ps

TEST AND MEASUREMENT PRODUCTS
AC Characteristics (continued)

Figure 1. Setup Time

Figure 2. Hold Time

Figure 3. Release Time
Notes:

- 10E circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
- 100E circuits are designed to meet the DC specifications shown in the table where transverse airflow greater than 500 lfpm is maintained.
- Differential input voltage required to obtain a full ECL swing on the outputs.
- V_{CMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between $V_{PP(min)}$ and 1V. The lower end of V_{CMR} range varies 1:1 with V_{EE} and is equal to $V_{EE}+2.6V$.
- The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
- The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
- Enable is defined as the propagation delay from the 50% point of a **negative** transition on EN^* to the 50% point of a **positive** transition on Q (or a negative transition on Q^*). Disable is defined as the propagation delay from the 50% point of a **positive** transition on EN^* to the 50% point of a **negative** transition on Q (or a positive transition on Q^*).
- The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
- The setup time is the minimum time that EN^* must be asserted prior to the next transition of IN/IN^* to prevent an output response greater than ± 75 mV to that IN/IN^* transition (see Figure 1).
- The hold time is the minimum time that EN must remain asserted after a negative going IN or a positive going IN^* to prevent an output response greater than ± 75 mV to the IN/IN^* transition (see Figure 2).
- The release time is the minimum time that EN must be deasserted prior to the next IN/IN^* transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
- $V_{pp(min)}$ is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The $V_{pp(min)}$ is AC limited for the E111 as a differential input as low as 250 mV will still produce full ECL levels at the output.
- Voltages referenced to $V_{CC} = 0V$.
- For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
- For part ordering descriptions, see HPP Part Ordering Information Data Sheet.

TEST AND MEASUREMENT PRODUCTS**Ordering Information**

Ordering Code	Package ID
SK10E111PJ	28-PLCC
SK10E111PJT	28-PLCC
SK100E111PJ	28-PLCC
SK100E111PJT	28-PLCC

Application Notes

AN1002 - Interfacing Between ECL / LVECL / PECL / LVPECL - to - TTL / LVTTTL / CMOS / LVCMOS

AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices

AN1005 - Using ECL / LVECL Devices as PECL / LVPECL

AN1006 - Designing with 10K and 100K ECL / PECL Devices

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