

# SIDEC

Smart Integrated Digital Echo Canceller

PEF/PEB 20954 HT, Version 1.1

PEF/PEB 20954 E, Version 1.1

Wireline Communications



Never stop thinking.

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## SIDEC

**Revision History:**        **2004-07-28**

Rev. 2

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**Previous Version:**        **Data Sheet, DS1, 1999-04**

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| <b>Page</b> | <b>Subjects (major changes since last revision)</b> |
|-------------|-----------------------------------------------------|
|-------------|-----------------------------------------------------|

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**Changes from previous version DS3, 2003-06-01 to DS4, 2003-09-01**

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| <b>Page 141</b> | timing t_smon_delay |
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|  | Additional configuration hints in the <b>“Operational Description”</b> on <b>Page 51</b> and following pages |
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## 1 Introduction

The **S**mart **I**ntegrated **D**igital **E**cho **C**anceller (SIDECE) suppresses echoes in telecommunication networks which might disturb any kind of terrestrial or wireless communication. It incorporates leading edge CMOS technology as well as INFINEON's many years' experience in Telecommunication ICs.

In communication links reflections resulting in an electrical echo are due to hybrid splits or imperfect terminations in subscribe loops. Acoustical echoes may occur due to poor isolation of microphone and speaker of some telephone system. These electrical and acoustical echoes disturb the quality of the transmission. To ensure high quality, pure data transmission the ITU-T (International Telecommunications Union, Telecommunication Standardization Sector) suggests in the recommendation G.131 the use of echo cancellers. Echo cancellation is extremely desirable for data links with total round trip transmission times of more than 50 ms.

# SIDEC

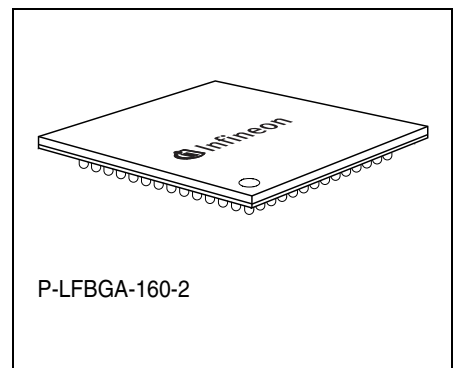
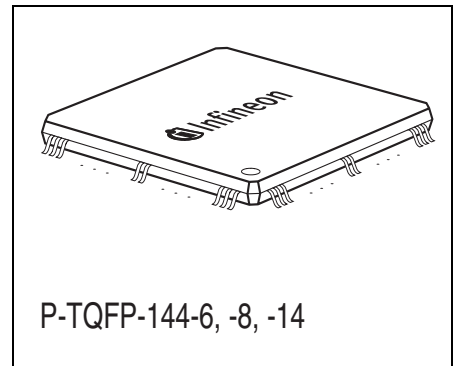
## Smart Integrated Digital Echo Canceller

PEF/PEB 20954 HT

### Version 1.1

#### 1.1 Key Features

- 2.048 MHz PCM input and output interfaces with selectable  $\mu$ - and A-Law coding according to ITU G.711
- Rapid convergence of patented algorithm at the beginning or during a connection even in the presence of background noise at the near end subscriber
- Echo return loss enhancement of > 30 dB (ERLE)
- Detection of double talk for adaptive convergence control
- Independently controlled voiceband echo cancelling according to ITU G.165 and G.168 for
  - 32 channels with end echo path delay of less than 63.75 ms
  - 16 channels with end echo path delay of less than 127.75 ms (usage of two SIDEC in parallel for simultaneous processing of 32 channels is easily possible)
- Smart Non Linear Processor controlled by echoloss, echo path delay and background noise
- Various options for comfort noise injection
- Maskable disabling functions
  - 2100 Hz tone with phase reversal detection
  - 2100 Hz tone without phase reversal detection
  - 2010 Hz continuity check (SS7)
  - via PCM timeslot 16 Bit a, b, c or d according to ITU G.704
  - individual channels maskable via Microprocessor Interface, UCC Interface and Serial Interface



| Type             | Package       |
|------------------|---------------|
| PEF/PEB 20954 HT | P-TQFP-144-8  |
| PEF/PEB 20954 E  | P-LFBGA-160-2 |

## Introduction

- Integrated Universal Control and Communication Interface (UCCI) for signaling highways with direct hardware control for:
  - disable cancelling
  - configurable disabling functions
  - communication between board controllers
- Support of Channel Associated Signaling (CAS) BR transparency (robbed bits) in send path
- Selectable  $\mu$ - to A-Law or A- to  $\mu$ -Law Conversion on a global or per channel basis
- Configurable idle channel supervision
- Clear channel capability (64 clear) on a per channel basis
- Special evaluation of bit 8 in T1 Modem calls possible (56 clear)
- Serial 256 kbit/s interface to control the functions disable cancelling, freeze coefficients, clear channel, disable NLP, PCM Law conversion control or combinations of above
- Monitor pins for several internal states
- Switchable global loop from receive output to send input and send output to receive input
- Switchable global attenuation (2.5 dB or 6 dB) at the receive and send output
- Flexible Microprocessor Interface (Intel or Motorola type, Mux and Demux mode) usable for:
  - configuration of parameters such as thresholds and functions on a global basis
  - Disable cancelling, freeze coefficients, clear channel, disable NLP, PCM Law conversion control (all functions individually for each channel)
  - support of background tests for disabled or idle timeslots (feeding and reading of test levels)
  - possibility to read levels, attenuations, internal states, signal values or all coefficients of a selected timeslot
  - control of the RAM Built In Self Test
- Advanced Integrated Watchdog Timer
- Supervision of the input clocks
- Various clock modes possible for 32.768 MHz and 8.192 MHz
- Boundary Scan according to IEEE 1149.1 Standard
- Power supply: 3.3 V, 5V tolerant inputs
- Typical power dissipation: 900 mW
- Plastic package P-TQFP 144-8, P-LFBGA 160-2
- Temperature range: -40°C - 85°C and 0°C - 70°C

**Ordering Information****Table 1      Ordering Information**

| <b>Product</b>      | <b>Package</b>                      | <b>Q-Number</b> |
|---------------------|-------------------------------------|-----------------|
| <b>PEB 20954 HT</b> | <b>P-TQFP 144-8 (0°C - 70°C)</b>    | Q67003 H9363    |
| <b>PEF 20954 HT</b> | <b>P-TQFP 144-8 (-40°C - 85°C)</b>  | Q67003 H9364    |
| <b>PEB 20954 E</b>  | <b>P-LFBGA-160-2 (0°C - 70°C)</b>   | Q67003 H9422    |
| <b>PEF 20954E</b>   | <b>P-LFBGA-160-2 (-40°C - 85°C)</b> | Q67003 H9423    |

## 1.2 Logic Symbol

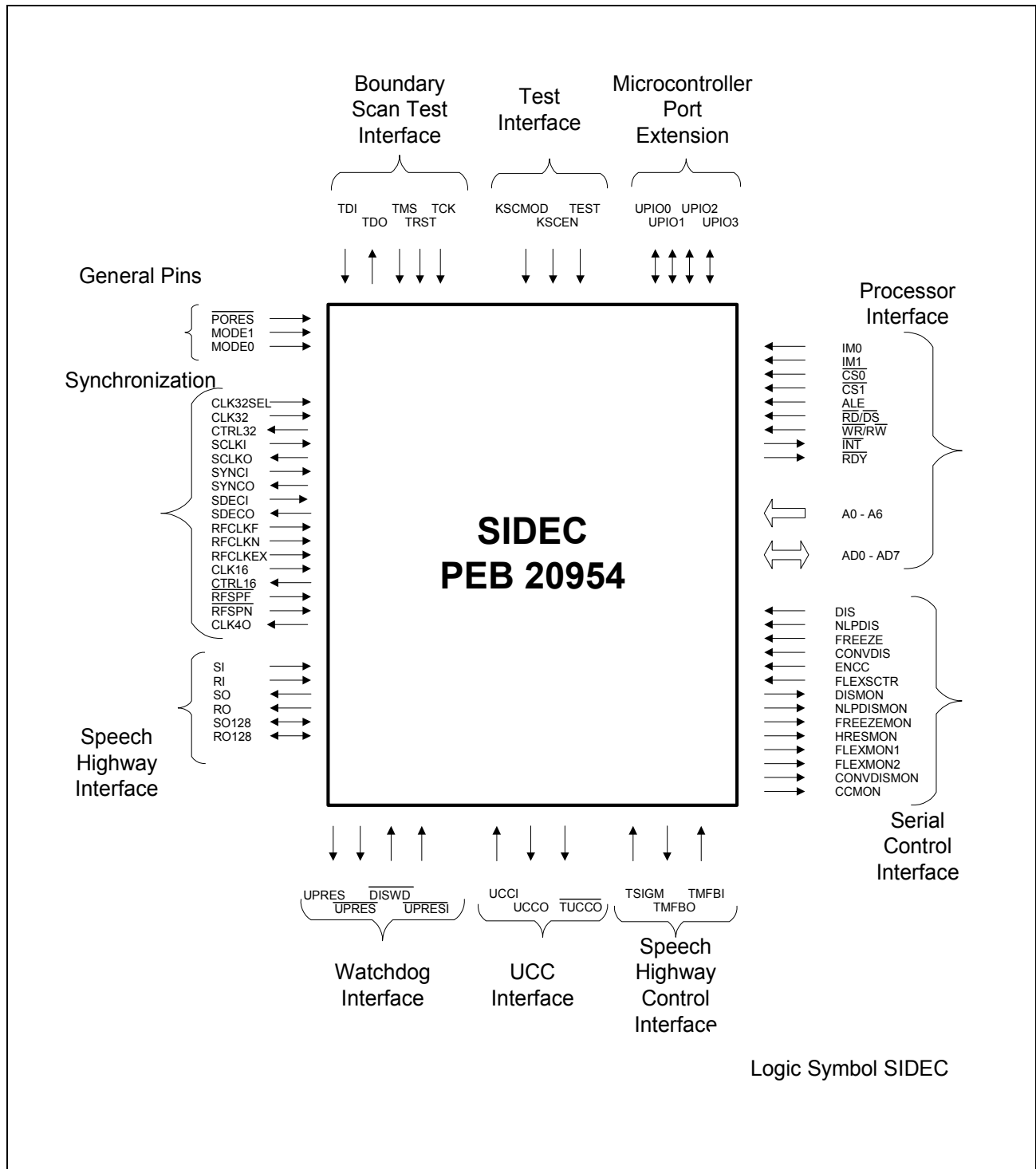
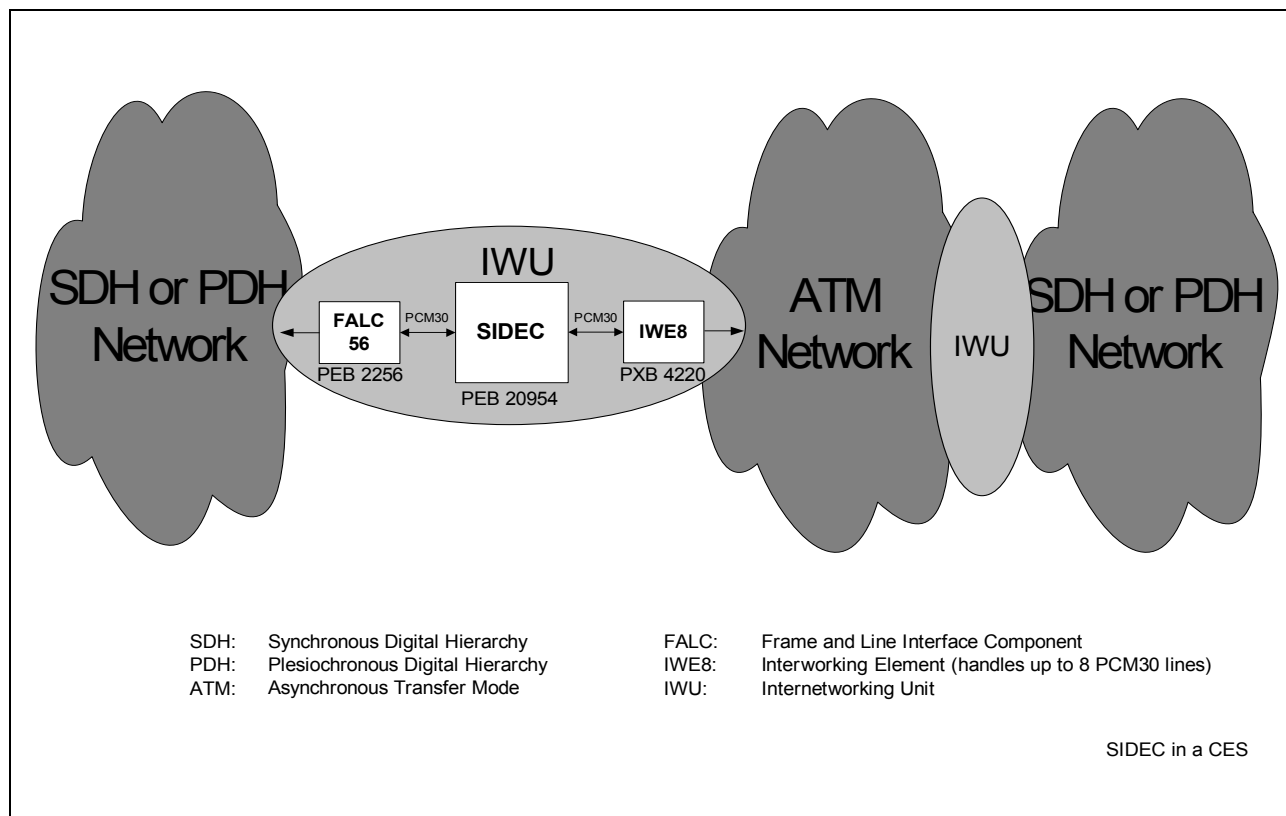


Figure 1 Logic Symbol of the SIDE C

### 1.3 Typical Applications

The SIDEDEC can be used for various applications.

**Figure 2** to **Figure 5** display typical examples.

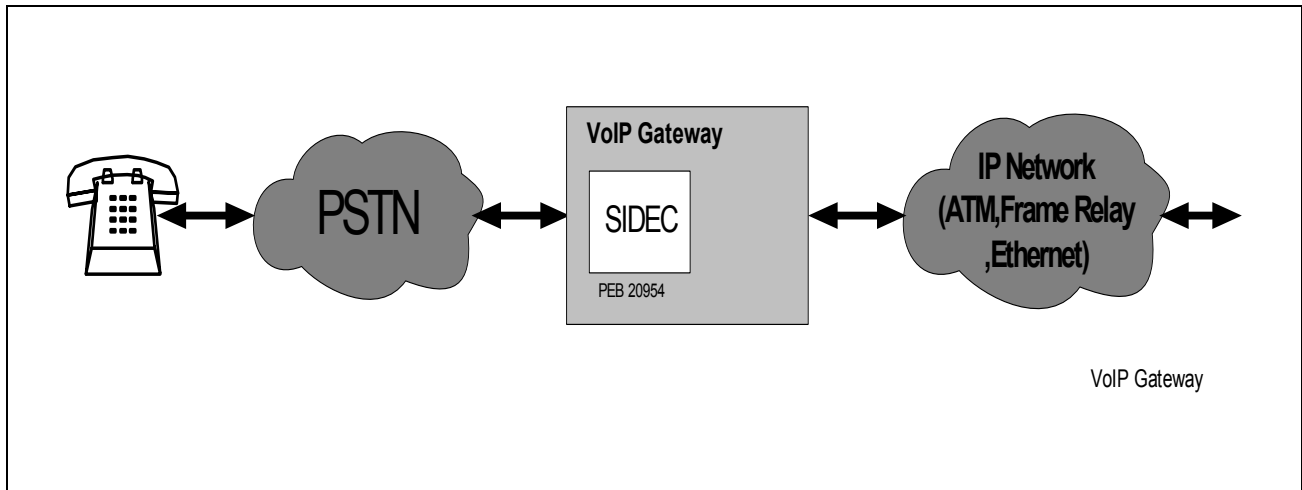


**Figure 2 SIDEDEC in a Circuit Emulation Service Carried over ATM**

In this interworking unit there are two INFINEON products connected to the SIDEDEC. The FALC 56 serves as a frame and line interface component whereas the IWE8 PXB 4220 operates as an interworking element.

The delays of networks and the inter working units are usually long. In the application above the SIDEDEC cancels the echo that is generated by reflection on the near end side and heard by the far end speaker. The SIDEDEC can cancel end echo paths (SDH or PDH Network on near end side) up to 128 ms. For details see **Figure 17**.

For the set up illustrated in **Figure 2** a application note "Using SIDEDEC in a Voice over ATM Application" is available.

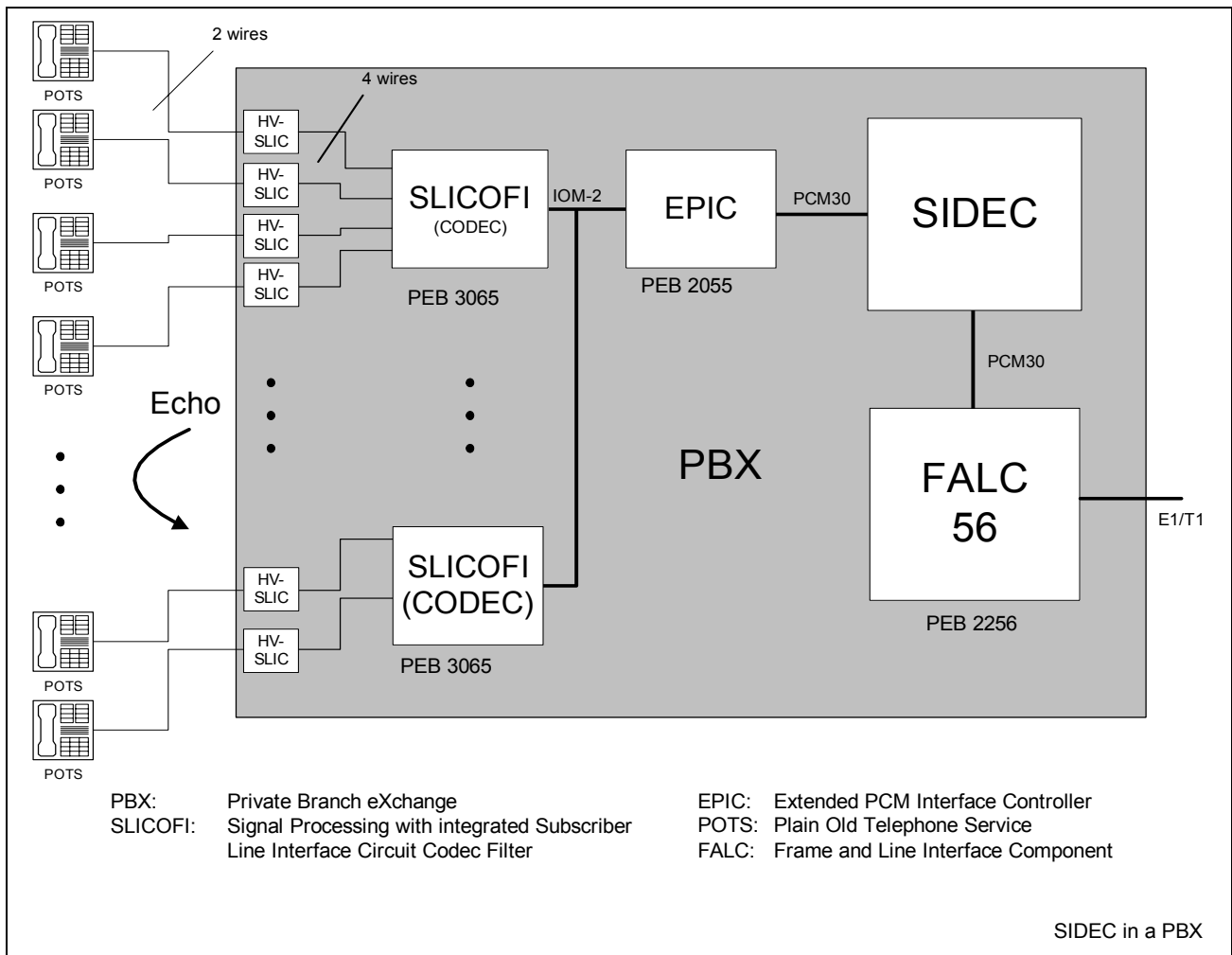


**Figure 3 SIDEc in a Voice over IP Gateway**

An emerging market in the telecom industry is “Voice Over IP”. Due to the long delay echo cancellation is required. The delay is introduced through packetizing and voice compression. The SIDEc handles different functions in a Voice over IP gateway, such as Voice Detection, Voice Activity Detection, Comfort Noise and A-law u-law conversion regarding G.711.

In a gateway the SIDEc points into the PSTN network as shown in [Figure 3](#). The echo itself is generated by the hybrid in the PSTN cloud. Before the voice signal from the POTS gets packetized into ATM, FR or Ethernet cells the echo is being cancelled by the SIDEc.

For a high voice quality in “Voice Over IP” environment echo cancellation is a major requirement.

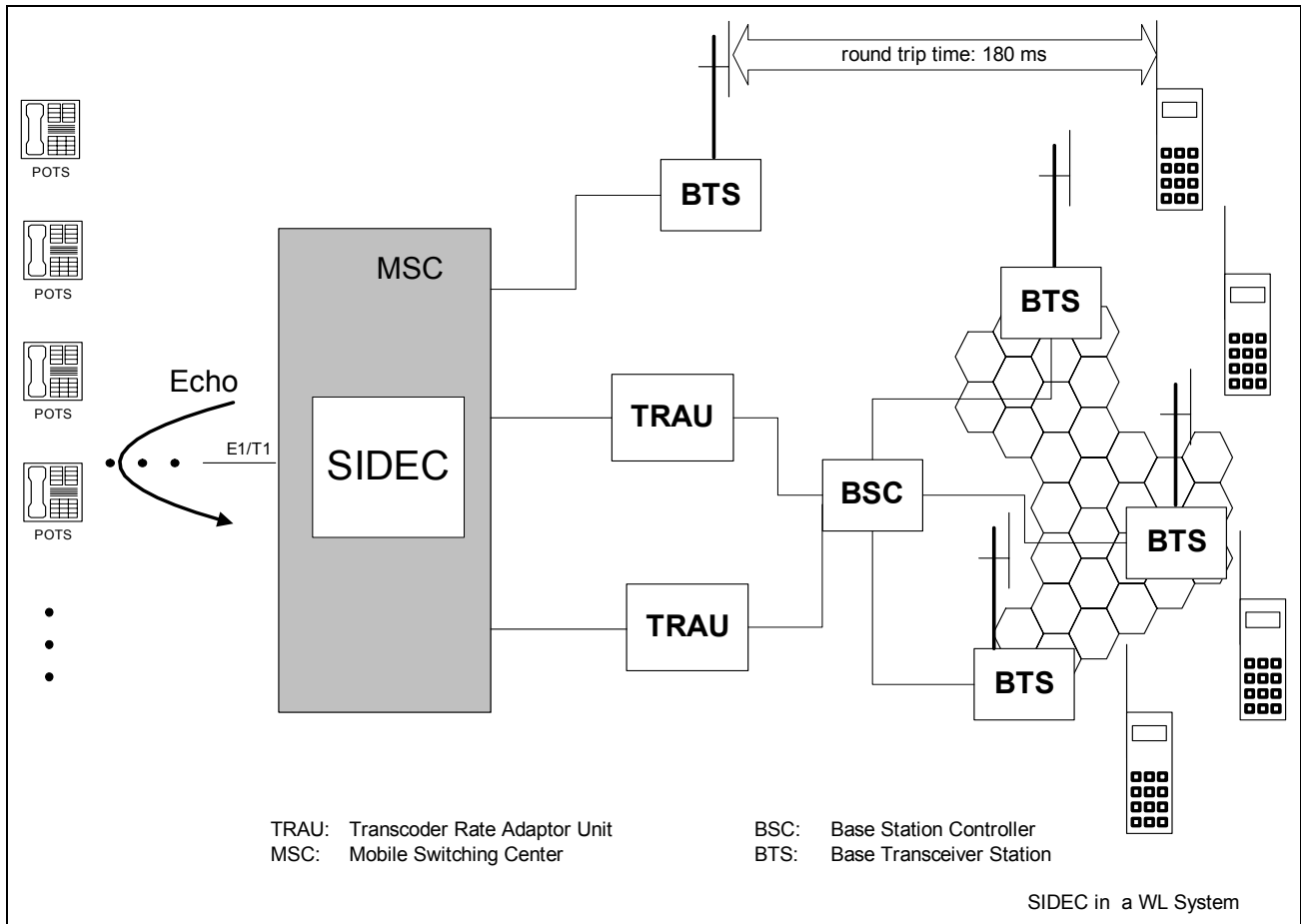


**Figure 4 SIDEDEC in a Private Branch Exchange (PBX)**

SIDEDEC can be used in a PBX or Central Office (CO) to cancel the echo next to the customer side (near end echo). The echo delay is kept short. The delay for this application is usually less than 64ms and the SIDEDEC can cancel up to 32 channels.

**Figure 4** shows a PBX with a T1/E1 interface FALC LH to the CO on the one side. On the other side analog phones are connected.

A possible INFINEON solution with the SICOFI (includes D/A and A/D conversion) and the SLIC (hybrid) to connect the analog phone is shown above.



**Figure 5 SIDEDEC in a Wireless System**

Due to voice compression and error correction the one way transmission time for wireless voice signals is typically 90 ms. With 180 ms roundtrip time the 50 ms roundtrip time for echo free transmission is exceeded by at least 130 ms. Hence, the speaker on the mobile phone will hear any kind of echo generated in the hybrid next to the POTS or the acoustical echo of the POTS. The SIDEDEC suppresses those two kinds of echoes if it is incorporated in the MSC. Depending on the individual call the end echo path can differ dramatically. In Europe the end echo path could even go to different countries causing strong dispersion of the echo. Only a high quality echo canceller with long end path delay options guarantees compensation of the strongly varying echoes.

## 2 Pin Description

### 2.1 Pin Diagram

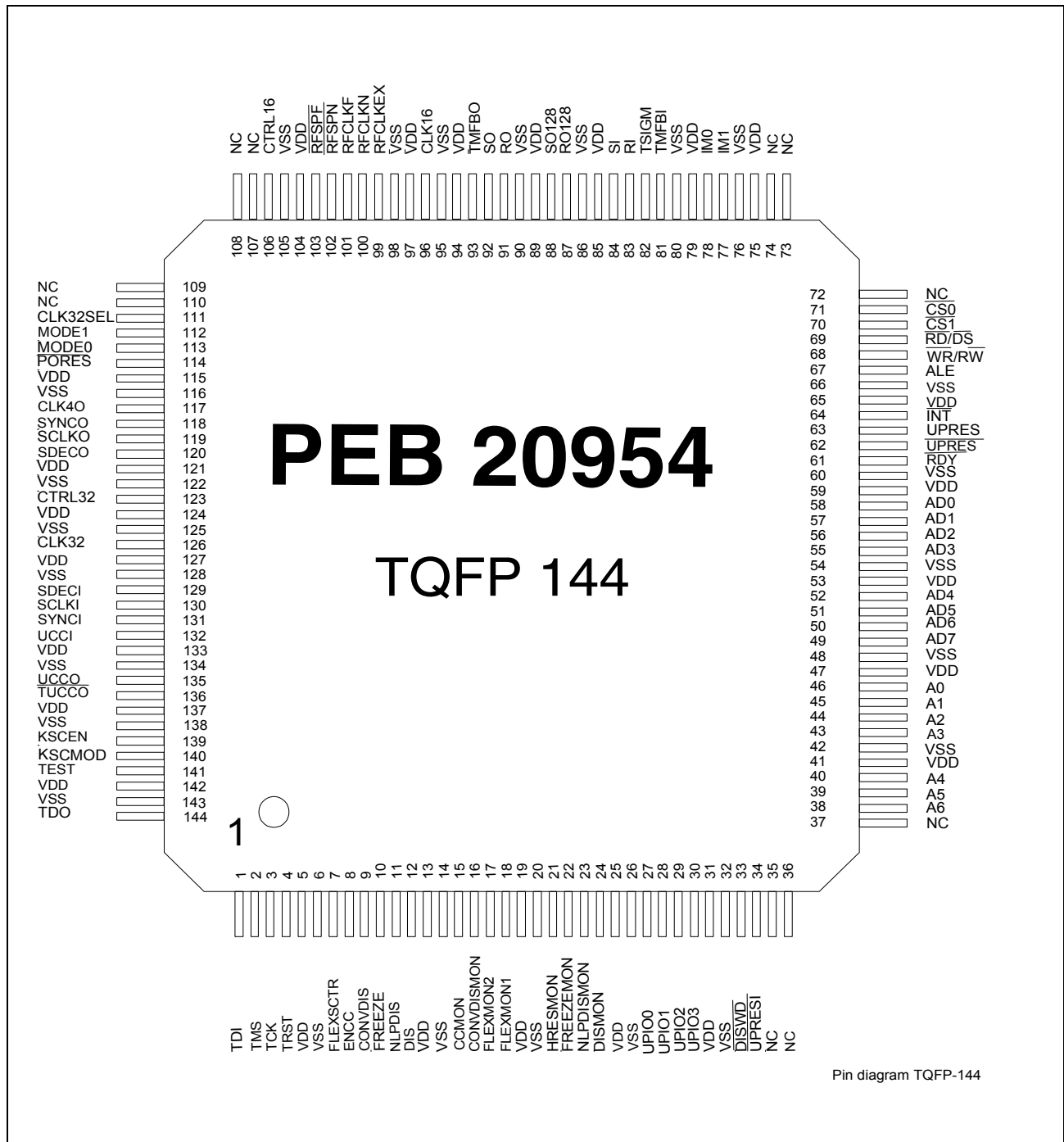


Figure 6 Pin Configuration P-TQFP-144-8

## Pin Description

|    | A       | B        | C       | D            | E           | F      | G              | H            | J             | K             | L     | M     | N             | P             |
|----|---------|----------|---------|--------------|-------------|--------|----------------|--------------|---------------|---------------|-------|-------|---------------|---------------|
| 14 | NC      | CTRL16   | RFSPF_N | RFCLKF       | RFCLKEX     | TMFBO  | RO             | SO128        | NC            | RI            | TMFBI | IM0   | IM1           | CS0_N         |
| 13 | MODE1   | CLK32SEL | NC      | RFSPN_N      | RFLKN       | CLK16  | SO             | RO128        | SI            | TSIGM         | NC    | NC    | NC            | CS1_N         |
| 12 | PORES_N | MODE0    | VSS     | VDD          | VSS         | VDD    | VDD            | VDD          | VDD           | VSS           | VDD   | VSS   | RD_N/<br>DS_N | WR_N/<br>RW_N |
| 11 | SYNCO   | CLK40    | VDD     | VSS          | VDD         | VSS    | VDD            | VDD          | VSS           | VDD           | VSS   | VDD   | ALE           | INT_N         |
| 10 | SDECO   | SCLKO    | VSS     | VDD          |             |        |                |              |               |               | VDD   | VSS   | UPRES         | UPRES_N       |
| 9  | CTRL32  | NC       | VDD     | VSS          |             |        |                |              |               |               | VSS   | VDD   | RDY_N         | AD0           |
| 8  | CLK32   | NC       | VDD     | VDD          |             |        |                |              |               |               | VDD   | VDD   | AD1           | AD2           |
| 7  | SDECI   | SCLKI    | VDD     | VDD          |             |        |                |              |               |               | VDD   | VDD   | AD4           | AD3           |
| 6  | SYNCI   | UCCI     | VDD     | VSS          |             |        |                |              |               |               | VSS   | VDD   | AD6           | AD5           |
| 5  | UCCO    | TUCCO_N  | VSS     | VDD          |             |        |                |              |               |               | VDD   | VSS   | A0            | AD7           |
| 4  | KSCEN   | NC       | VDD     | VSS          | VDD         | VSS    | VDD            | VDD          | VSS           | VDD           | VSS   | VDD   | A2            | A1            |
| 3  | KSCMOD  | NC       | VSS     | VDD          | VSS         | VDD    | VDD            | VDD          | VDD           | VSS           | VDD   | VSS   | A4            | A3            |
| 2  | TEST    | TDI      | TCK     | FLEX<br>SCTR | CONV<br>DIS | NLPDIS | CCMON          | FLEX<br>MON1 | FREEZE<br>MON | DISMON        | UPIO1 | UPIO3 | A6            | A5            |
| 1  | TDO     | TMS      | TRST    | ENCC         | FREEZE      | DIS    | CONV<br>DISMON | FLEX<br>MON2 | HRES<br>MON   | NLP<br>DISMON | UPIO0 | UPIO2 | DISWD_N       | UPRESI_N      |
|    | A       | B        | C       | D            | E           | F      | G              | H            | J             | K             | L     | M     | N             | P             |

Pin diagram LFBGA160

**Figure 7** Pin Configuration P-LFBGA-160-2(top view)

## 2.2 Pin Definitions and Functions for the P-TQFP-144-8 package

**Table 2 General Pins**

| Pin No. | Symbol | Input (I)<br>Output (O)<br>Pull Up /<br>Pull Down | Function                                                                                 |                                |   |                               |
|---------|--------|---------------------------------------------------|------------------------------------------------------------------------------------------|--------------------------------|---|-------------------------------|
| 114     | PORES  | I, PU                                             | Power On Reset. A low on this pin forces all registers and counters to predefined values |                                |   |                               |
| 112     | MODE1  | I, PU                                             | 1                                                                                        | End delay < 64ms               | 1 | For future use                |
| 113     | MODE0  | I, PU                                             | 1                                                                                        |                                | 0 |                               |
| 112     | MODE1  | I, PU                                             | 0                                                                                        | End delay < 128 ms Master Mode | 0 | End delay < 128 ms Slave Mode |
| 113     | MODE0  | I, PU                                             | 1                                                                                        |                                | 0 |                               |

**Table 3 Synchronization**

| Pin No. | Symbol   | I/O, PU/PD | Function                                                                                                                                                             |
|---------|----------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 111     | CLK32SEL | I, PU      | Selects from which source SCLKO will be derived:<br>'1': SCLKO will be derived from CLK32 by dividing by 4<br>'0': SCLKO will be derived from CLK16 by dividing by 2 |
| 126     | CLK32    | I, PU      | 32.768 MHz Operating Clock for the SDEC                                                                                                                              |
| 123     | CTRL32   | O          | Control voltage for the 32.768 MHz operating Clock VCO, maskable for reduced power consumption                                                                       |
| 130     | SCLKI    | I, PU      | System clock input (8.192 MHz) for PCM- and UCCI                                                                                                                     |
| 119     | SCLKO    | O          | 8.192 MHz system clock output, source CLK32 or CLK16 is selectable via pin CLK32SEL, maskable for reduced power consumption                                          |
| 117     | CLK4O    | O          | 4.096 MHz system clock output for subsequent circuits, derived from SCLKI, maskable for reduced power consumption                                                    |

## Pin Description

**Table 3 Synchronization (cont'd)**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                                                                                                                                                                                                                                       |
|---------|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 131     | SYNCI  | I, PU      | System Synchronization input pulse. Defines the frame alignment of PCM and UCCI signals in conjunction with the values in registers RIALIGN, SIALIGN, SOALIGN, UCCALIGN, PHALIGN and also the multiframe alignment of the UCCI. Must be integer multiple of 125 $\mu$ s if UCC Interface is not used. Must be multiple integer of 4 ms if UCC interface is used. Leave open if not used or connect to $V_{DD}$ |
| 118     | SYNCO  | O          | System Synchronization output pulse (see SYNCI), duration configurable one or two SCLKO periods, period 125 $\mu$ s. If the UCC interface is not used and no SYNCI is applied, SYNCO can take over the part and role of SYNCI.                                                                                                                                                                                 |
| 120     | SDECO  | O          | Synchronization output pulse for other SIDECS if this SIDECS uses its own 32.768 MHz VCO. Can also be used for synchronization of external devices to the serial control input and monitor output signals of the SIDECS. The pulse width is 488 ns with a period of 125 $\mu$ s.                                                                                                                               |
| 129     | SDECI  | I, PU      | Synchronization input pulse if the SIDECS uses the 32.768 MHz VCO of another SIDECS. The same SCLKI signal can be applied to SDECI and SCLKI pin if the SCLKI is supplied by a source with correct phase condition to the CLK32 (see <a href="#">Figure 15</a> ). If the pin is not used leave it open or connect it to $V_{DD}$ .                                                                             |
| 101     | RFCLKF | I, PU      | Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPV[6:5]="00"                                                                                                                                                                                                                                                                      |
| 100     | RFCLKN | I, PU      | Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPV[6:5]="01"                                                                                                                                                                                                                                                                      |

## Pin Description

**Table 3 Synchronization (cont'd)**

| Pin No. | Symbol                    | I/O, PU/PD | Function                                                                                                                                                                                                                                   |
|---------|---------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 99      | RFCLKEX                   | I, PU      | Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6]='1'                                                                                                    |
| 96      | CLK16                     | I, PU      | Clock from 16.384 MHz VCXO                                                                                                                                                                                                                 |
| 106     | CTRL16                    | O          | Control voltage for the 16.384 MHz VCXO                                                                                                                                                                                                    |
| 103     | $\overline{\text{RFSPF}}$ | I, PU      | Receive Frame Sync Pulse from the far end side (F1). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '0'.  |
| 102     | $\overline{\text{RFSPN}}$ | I, PU      | Receive Frame Sync Pulse from the near end side (F2). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '1'. |

**Table 4 Microprocessor Interface**

| Pin No.        | Symbol                  | I/O, PU/PD | Function                                                                                        |
|----------------|-------------------------|------------|-------------------------------------------------------------------------------------------------|
| 78             | IM0                     | I, PU      | Interface Mode Intel = low, Motorola = high                                                     |
| 77             | IM1                     | I, PU      | Interface Mode MUXED = low, DEMUXED = high                                                      |
| 71             | $\overline{\text{CS0}}$ | I, PU      | Chip Select. A low signal selects the SIDEC (internally "anded" with $\overline{\text{CS1}}$ ). |
| 70             | $\overline{\text{CS1}}$ | I, PU      | Chip Select. A low signal selects the SIDEC (internally "anded" with $\overline{\text{CS0}}$ ). |
| 46-43<br>40-38 | A0..A6                  | I, PU      | Address Bus. Only used in demuxed mode, can be left open in muxed mode.                         |
| 58-55<br>52-49 | AD0..AD7                | I/O, -     | Multiplexed Address/Data Bus in multiplexed mode, Data Bus in demultiplexed mode                |

## Pin Description

**Table 4 Microprocessor Interface (cont'd)**

| Pin No. | Symbol                                      | I/O, PU/PD | Function                                                                                                                                                                                                                                                                                                                     |
|---------|---------------------------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 67      | ALE                                         | I, PU      | Address Latch Enable in multiplexed mode. Address on AD bus is internally latched with the falling edge of ALE. This signal is also used for the internal clock supervision. In Demuxed mode there must be provided an external independent clock signal (i.e. processor clock) in order to enable proper clock supervision. |
| 69      | $\overline{\text{RD}}/\overline{\text{DS}}$ | I, PU      | Intel mode. A low indicates a read operation. Motorola mode. Data Strobe, active low to control read/write                                                                                                                                                                                                                   |
| 68      | $\overline{\text{WR}}/\overline{\text{RW}}$ | I, PU      | Intel mode. A low indicates a write operation. Motorola mode. High = read cycle, low = write cycle                                                                                                                                                                                                                           |
| 64      | $\overline{\text{INT}}$                     | O, (od)    | Interrupt request from the SIDEDEC, active low                                                                                                                                                                                                                                                                               |
| 61      | $\overline{\text{RDY}}$                     | O, (od)    | Ready signal for $\mu\text{C}$ devices that support this feature. For read cycles the signal is asserted after the data on the AD bus is valid. For writing cycles the signal is asserted when a write access is ready to be concluded.                                                                                      |

**Table 5 Microcontroller Port Extension**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                        |
|---------|--------|------------|---------------------------------------------------------------------------------|
| 27      | UPIO0  | I/O, PU    | Pin that can be read and controlled by the on board processor via register UPIO |
| 28      | UPIO1  | I/O, PU    | Pin that can be read and controlled by the on board processor via register UPIO |
| 29      | UPIO2  | I/O, PU    | Pin that can be read and controlled by the on board processor via register UPIO |
| 30      | UPIO3  | I/O, PU    | Pin that can be read and controlled by the on board processor via register UPIO |

## Pin Description

**Table 6 Processor Watchdog Circuit**

| Pin No. | Symbol                     | I/O, PU/PD | Function                                                                                                                                                                                                                                                             |
|---------|----------------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63      | UPRES                      | O          | $\mu$ P-Reset. High pulse (125 $\mu$ s) if the $\mu$ P fails to write predefined values to the registers WDG1 to WDG3 in this sequence within 2 s and $\overline{\text{DISWD}}='1'$ . Also active if $\overline{\text{PORES}}='0'$ or $\overline{\text{UPRESI}}='0'$ |
| 62      | $\overline{\text{UPRES}}$  | O          | Same as UPRES, but low active                                                                                                                                                                                                                                        |
| 33      | $\overline{\text{DISWD}}$  | I, PU      | Disable of $\mu$ P-Reset on active watchdog condition if set to low                                                                                                                                                                                                  |
| 34      | $\overline{\text{UPRESI}}$ | I, PU      | Produces a reset signal at UPRES, $\overline{\text{UPRES}}$ if set to low                                                                                                                                                                                            |

**Table 7 Speech Highways**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                      |
|---------|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 84      | SI     | I, PD      | 2.048 Mbit/s Send speech highway input. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers SIALIGN and PHALIGN[3:2]    |
| 83      | RI     | I, PD      | 2.048 Mbit/s Receive speech highway input. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers RIALIGN and PHALIGN[1:0] |
| 92      | SO     | O          | 2.048 Mbit/s Send speech highway output. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers SOALIGN and PHALIGN[5:4]   |
| 91      | RO     | O          | 2.048 Mbit/s Receive speech highway output. This signal will have a fixed delay of one PCM frame (125 $\mu$ s) with respect to RI                                             |

## Pin Description

**Table 7 Speech Highways**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                                                                                                                                                                                                                               |
|---------|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 88      | SO128  | I/O, PU    | Auxiliary 2.048 Mbit/s Send speech highway output in 128 ms mode. Input in master mode, output in slave mode. The pins of master and slave SIDEDEC in 128 ms mode should be connected to enable a 32 channel system. The signal from the slave is multiplexed in the master with the internally generated signal and output (clocked) with the system clock. Tristate and meaningless in 64 ms mode    |
| 87      | RO128  | I/O, PU    | Auxiliary 2.048 Mbit/s Receive speech highway output in 128 ms mode. Input in master mode, output in slave mode. The pins of master and slave SIDEDEC in 128 ms mode should be connected to enable a 32 channel system. The signal from the slave is multiplexed in the master with the internally generated signal and output (clocked) with the system clock. Tristate and meaningless in 64 ms mode |

**Table 8 UCC Interface**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                     |
|---------|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 132     | UCCI   | I, PD      | 2.048 Mbit/s UCC highway input. Start of timeslot 0, bit 7 and frame number can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers UCCMFR, UCCALIGN and PHALIGN[7:6] |

## Pin Description

**Table 8 UCC Interface**

| Pin No. | Symbol                    | I/O, PU/PD | Function                                                                                                                                                                                                                                                                               |
|---------|---------------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 135     | UCCO                      | O          | 2.048 Mbit/s UCC highway output. Start of timeslot 0, bit 7 and frame number can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers UCCMFR, UCCALIGN and PHALIGN[7:6]                                                                                          |
| 136     | $\overline{\text{TUCCO}}$ | O          | Tristate control signal for external tristate output buffer at the UCCO bus, active low. Remains inactive after a power on reset until the configuration by the $\mu\text{P}$ has been settled. Active only at UCC timeslot 0 for UCC frames that correspond to processed PCM channels |

**Table 9 Speech Highway Control Signals for CAS in T1 Systems**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                             |
|---------|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 82      | TSIGM  | I, PD      | Transmit Signaling Marker, indicating robbed bits at SI, corresponding to the delay of SI                                            |
| 81      | TMFBI  | I, PD      | Transmit Multiframe Begin Input corresponding to the delay of SI                                                                     |
| 93      | TMFBO  | O          | Transmit Multiframe Begin Output corresponding to the delay of SO. The delay of TMFBI to TMFBO is identical to the delay of SI to SO |

**Table 10 Channelwise Serial Interface**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                                                  |
|---------|--------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12      | DIS    | I, PD      | Serial 256 kbit/s disable signal to bypass the canceller, NLP and attenuator and to reset the H-Register and Speech Control unit on a per channel basis. High active, maskable, leave open or connect to ground if unused |
| 11      | NLPDIS | I, PD      | Serial 256 kbit/s signal to disable the NLP on a per channel basis. High active, maskable, leave open or connect to ground if unused                                                                                      |

## Pin Description

**Table 10 Channelwise Serial Interface (cont'd)**

| Pin No. | Symbol    | I/O, PU/PD | Function                                                                                                                                                                                                                                                                            |
|---------|-----------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10      | FREEZE    | I, PD      | Serial 256 kbit/s signal to freeze the H-Registers on a per channel basis. High active, maskable, leave open or connect to ground if unused                                                                                                                                         |
| 9       | CONVDIS   | I, PD      | Serial 256 kbit/s signal to disable A/ $\mu$ -Law conversion on a per channel basis. High active, maskable, leave open or connect to ground if unused                                                                                                                               |
| 8       | ENCC      | I, PD      | Serial 256 kbit/s signal to enable clear channel transparency on a per channel basis. High active, maskable, leave open or connect to ground if unused, same function as DIS='1' and CONVDIS='1'                                                                                    |
| 7       | FLEXSCTR  | I, PD      | Flexible serial 256 kbit/s control signal on a per channel basis. Configurable by register CONFLEXSCTR. High active, maskable, leave open or connect to ground if unused                                                                                                            |
| 24      | DISMON    | O          | Serial 256 kbit/s EC disable (signals bypass channels) monitor output signal ('0': EC on, '1': EC off)                                                                                                                                                                              |
| 23      | NLPDISMON | O          | Serial 256 kbit/s NLP disable monitor output signal ('0': NLP on, '1': NLP off)                                                                                                                                                                                                     |
| 22      | FREEZEMON | O          | Serial 256 kbit/s H-Register freeze monitor output signal ('1': freeze, '0': no freeze)                                                                                                                                                                                             |
| 21      | HRESMON   | O          | Serial 256 kbit/s H-Register reset monitor output signal ('1': reset, '0': no reset)                                                                                                                                                                                                |
| 18      | FLEXMON1  | O          | Serial 256 kbit/s monitor output signal (32 channels at 8 kbit/s), monitoring according to settings of the bits CONFLEXMON[7:4], e.g. Idle channel detection, 2010 Hz tone detected, 2100 Hz tone with or without phase reversal detected, double talk detected, no speech detected |

## Pin Description

**Table 10 Channelwise Serial Interface (cont'd)**

| Pin No. | Symbol     | I/O, PU/PD | Function                                                                                                                                                                                                                                                                            |
|---------|------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17      | FLEXMON2   | O          | Serial 256 kbit/s monitor output signal (32 channels at 8 kbit/s), monitoring according to settings of the bits CONFLEXMON[3:0], e.g. Idle channel detection, 2010 Hz tone detected, 2100 Hz tone with or without phase reversal detected, double talk detected, no speech detected |
| 16      | CONVDISMON | O          | Serial 256 kbit/s law conversion disable monitor output signal ('1': conversion disabled, '0': conversion enabled)                                                                                                                                                                  |
| 15      | CCMON      | O          | Serial 256 kbit/s clear channel transparency (64 clear) monitor output signal ('1': clear channel on, '0': clear channel off), same as DISMON='1' and CONVDISMON='1'                                                                                                                |

**Table 11 Test Interface for Boundary Scan according to IEEE 1149.1**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                     |
|---------|--------|------------|------------------------------------------------------------------------------|
| 1       | TDI    | I, PU      | Test Data Input                                                              |
| 144     | TDO    | O          | Test Data Output                                                             |
| 2       | TMS    | I, PU      | Test Mode Select                                                             |
| 3       | TCK    | I, PU      | Test Clock                                                                   |
| 4       | TRST   | I, PU      | Boundary Test Reset (active low, should be tied to '0' for normal operation) |

**Table 12 Test Interface**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                            |
|---------|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 140     | KSCMOD | I, PD      | SCAN MODE ENABLE pin for enabling of scan test. For normal operation this pin should be left unconnected or connected to $V_{SS}$ . |

## Pin Description

**Table 12 Test Interface (cont'd)**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                        |
|---------|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 139     | KSCEN  | I, PD      | SCAN SHIFT ENABLE pin for shift enabling in scan test. For normal operation this pin should be left unconnected or connected to $V_{SS}$ .                                                      |
| 141     | TEST   | I, -       | Reserved for special tests (i.e. IDDQ, MBIST, etc.). For normal operation this pin must be connected to $V_{SS}$ . Disables all pull resistances for IDDQ if set to '1'. Normal operation: '0'. |

*Note: The Test interface will be used by the manufacturer. For normal operation, this pins should be connected to the recommended fixed value in the table.*

**Table 13 Power Supply**

| Pin No.                                                                                                    | Symbol | I/O, PU/PD | Function           |
|------------------------------------------------------------------------------------------------------------|--------|------------|--------------------|
| 6,14,20,26,<br>32,42,48,54,6<br>0,66,76,80,86<br>,90,95,98,105<br>,116,<br>122,125,<br>128,134,<br>138,143 | VSS    |            | Common ground rail |
| 5,13,19,25,<br>31,41,47,<br>59,65,75,<br>79,85,89,94,<br>97,104,115,<br>121,124,<br>127,133,<br>137,142    | VDD    |            | Core power supply  |

**Table 14 Unused Pins**

| Pin No.                                            | Symbol | I/O, PU/PD | Function           |
|----------------------------------------------------|--------|------------|--------------------|
| 35,36,<br>37,72,7<br>3,74,10<br>7,108,1<br>09,110, | NC     |            | Common ground rail |

## 2.3 Pin Definitions and Functions for the P-LFBGA-160-2 Package

**Table 15 General Pins**

| Ball No.   | Symbol         | Input (I)<br>Output (O)<br>Pull Up /<br>Pull Down | Function                                                                                 |                                      |        |                                     |
|------------|----------------|---------------------------------------------------|------------------------------------------------------------------------------------------|--------------------------------------|--------|-------------------------------------|
| A12        | PORES          | I, PU                                             | Power On Reset. A low on this pin forces all registers and counters to predefined values |                                      |        |                                     |
| A13<br>B12 | MODE1<br>MODE0 | I, PU<br>I, PU                                    | 1<br>1                                                                                   | End delay <<br>64ms                  | 1<br>0 | For future use                      |
| A13<br>B12 | MODE1<br>MODE0 | I, PU<br>I, PU                                    | 0<br>1                                                                                   | End delay <<br>128 ms Master<br>Mode | 0<br>0 | End delay <<br>128 ms Slave<br>Mode |

**Table 16 Synchronization**

| Ball No. | Symbol   | I/O, PU/PD | Function                                                                                                                                                             |
|----------|----------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B13      | CLK32SEL | I, PU      | Selects from which source SCLKO will be derived:<br>'1': SCLKO will be derived from CLK32 by dividing by 4<br>'0': SCLKO will be derived from CLK16 by dividing by 2 |
| A8       | CLK32    | I, PU      | 32.768 MHz Operating Clock for the SDEC                                                                                                                              |
| A9       | CTRL32   | O          | Control voltage for the 32.768 MHz operating Clock VCO, maskable for reduced power consumption                                                                       |
| B7       | SCLKI    | I, PU      | System clock input (8.192 MHz) for PCM- and UCCI                                                                                                                     |
| B10      | SCLKO    | O          | 8.192 MHz system clock output, source CLK32 or CLK16 is selectable via pin CLK32SEL, maskable for reduced power consumption                                          |
| B11      | CLK4O    | O          | 4.096 MHz system clock output for subsequent circuits, derived from SCLKI, maskable for reduced power consumption                                                    |

## Pin Description

**Table 16 Synchronization (cont'd)**

| Ball No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A6       | SYNCI  | I, PU      | System Synchronization input pulse. Defines the frame alignment of PCM and UCCI signals in conjunction with the values in registers RIALIGN, SIALIGN, SOALIGN, UCCALIGN, PHALIGN and also the multiframe alignment of the UCCI. Must be integer multiple of 125 $\mu$ s if UCC Interface is not used. Must be multiple integer of 4 ms if UCC interface is used. Leave open if not used or connect to $V_{DD}$ |
| A11      | SYNCO  | O          | System Synchronization output pulse (see SYNCI), duration configurable one or two SCLKO periods, period 125 $\mu$ s. If the UCC interface is not used and no SYNCI is applied, SYNCO can take over the part and role of SYNCI.                                                                                                                                                                                 |
| A10      | SDECO  | O          | Synchronization output pulse for other SIDECS if this SIDECS uses its own 32.768 MHz VCO. Can also be used for synchronization of external devices to the serial control input and monitor output signals of the SIDECS. The pulse width is 488 ns with a period of 125 $\mu$ s.                                                                                                                               |
| A7       | SDECI  | I, PU      | Synchronization input pulse if the SIDECS uses the 32.768 MHz VCO of another SIDECS. The same SCLKI signal can be applied to SDECI and SCLKI pin if the SCLKI is supplied by a source with correct phase condition to the CLK32 (see <a href="#">Figure 15</a> ). If the pin is not used leave it open or connect it to $V_{DD}$ .                                                                             |
| D14      | RFCLKF | I, PU      | Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6:5]="00"                                                                                                                                                                                                                                                                     |
| E13      | RFCLKN | I, PU      | Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6:5]="01"                                                                                                                                                                                                                                                                     |

## Pin Description

**Table 16 Synchronization (cont'd)**

| Ball No. | Symbol                    | I/O, PU/PD | Function                                                                                                                                                                                                                                   |
|----------|---------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E14      | RFCLKEX                   | I, PU      | Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6]='1'                                                                                                    |
| F13      | CLK16                     | I, PU      | Clock from 16.384 MHz VCXO                                                                                                                                                                                                                 |
| B14      | CTRL16                    | O          | Control voltage for the 16.384 MHz VCXO                                                                                                                                                                                                    |
| C14      | $\overline{\text{RFSPF}}$ | I, PU      | Receive Frame Sync Pulse from the far end side (F1). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '0'.  |
| D13      | $\overline{\text{RFSPN}}$ | I, PU      | Receive Frame Sync Pulse from the near end side (F2). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '1'. |

**Table 17 Microprocessor Interface**

| Ball No.                            | Symbol                  | I/O, PU/PD | Function                                                                                         |
|-------------------------------------|-------------------------|------------|--------------------------------------------------------------------------------------------------|
| M14                                 | IM0                     | I, PU      | Interface Mode Intel = low, Motorola = high                                                      |
| N14                                 | IM1                     | I, PU      | Interface Mode MUXED = low, DEMUXED = high                                                       |
| P14                                 | $\overline{\text{CS0}}$ | I, PU      | Chip Select. A low signal selects the SIDECS (internally "anded" with $\overline{\text{CS1}}$ ). |
| P13                                 | $\overline{\text{CS1}}$ | I, PU      | Chip Select. A low signal selects the SIDECS (internally "anded" with $\overline{\text{CS0}}$ ). |
| N5,P4,<br>N4,P3,<br>N3,P2N<br>2     | A0..A6                  | I, PU      | Address Bus. Only used in demuxed mode, can be left open in muxed mode.                          |
| P9,N8,P<br>8,P7,N7<br>,P6,N6,<br>P5 | AD0..AD7                | I/O, -     | Multiplexed Address/Data Bus in multiplexed mode, Data Bus in demultiplexed mode                 |

## Pin Description

**Table 17 Microprocessor Interface**

| Ball No. | Symbol                                      | I/O, PU/PD | Function                                                                                                                                                                                                                                                                                                                     |
|----------|---------------------------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| N11      | ALE                                         | I, PU      | Address Latch Enable in multiplexed mode. Address on AD bus is internally latched with the falling edge of ALE. This signal is also used for the internal clock supervision. In Demuxed mode there must be provided an external independent clock signal (i.e. processor clock) in order to enable proper clock supervision. |
| N12      | $\overline{\text{RD}}/\overline{\text{DS}}$ | I, PU      | Intel mode. A low indicates a read operation. Motorola mode. Data Strobe, active low to control read/write                                                                                                                                                                                                                   |
| P12      | $\overline{\text{WR}}/\overline{\text{RW}}$ | I, PU      | Intel mode. A low indicates a write operation. Motorola mode. High = read cycle, low = write cycle                                                                                                                                                                                                                           |
| P11      | $\overline{\text{INT}}$                     | O, (od)    | Interrupt request from the SIDEDEC, active low                                                                                                                                                                                                                                                                               |
| N9       | $\overline{\text{RDY}}$                     | O, (od)    | Ready signal for $\mu\text{C}$ devices that support this feature. For read cycles the signal is asserted after the data on the AD bus is valid. For writing cycles the signal is asserted when a write access is ready to be concluded.                                                                                      |

**Table 18 Microcontroller Port Extension**

| Ball No. | Symbol | I/O, PU/PD | Function                                                                        |
|----------|--------|------------|---------------------------------------------------------------------------------|
| L1       | UPIO0  | I/O, PU    | Pin that can be read and controlled by the on board processor via register UPIO |
| L2       | UPIO1  | I/O, PU    | Pin that can be read and controlled by the on board processor via register UPIO |
| M1       | UPIO2  | I/O, PU    | Pin that can be read and controlled by the on board processor via register UPIO |
| M2       | UPIO3  | I/O, PU    | Pin that can be read and controlled by the on board processor via register UPIO |

## Pin Description

**Table 19 Processor Watchdog Circuit**

| Ball No. | Symbol                     | I/O, PU/PD | Function                                                                                                                                                                                                                                                             |
|----------|----------------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| N10      | UPRES                      | O          | $\mu$ P-Reset. High pulse (125 $\mu$ s) if the $\mu$ P fails to write predefined values to the registers WDG1 to WDG3 in this sequence within 2 s and $\overline{\text{DISWD}}='1'$ . Also active if $\overline{\text{PORES}}='0'$ or $\overline{\text{UPRESI}}='0'$ |
| P10      | $\overline{\text{UPRES}}$  | O          | Same as UPRES, but low active                                                                                                                                                                                                                                        |
| N1       | $\overline{\text{DISWD}}$  | I, PU      | Disable of $\mu$ P-Reset on active watchdog condition if set to low                                                                                                                                                                                                  |
| P1       | $\overline{\text{UPRESI}}$ | I, PU      | Produces a reset signal at UPRES, $\overline{\text{UPRES}}$ if set to low                                                                                                                                                                                            |

**Table 20 Speech Highways**

| Ball No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                      |
|----------|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| J13      | SI     | I, PD      | 2.048 Mbit/s Send speech highway input. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers SIALIGN and PHALIGN[3:2]    |
| K14      | RI     | I, PD      | 2.048 Mbit/s Receive speech highway input. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers RIALIGN and PHALIGN[1:0] |
| G13      | SO     | O          | 2.048 Mbit/s Send speech highway output. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers SOALIGN and PHALIGN[5:4]   |
| G14      | RO     | O          | 2.048 Mbit/s Receive speech highway output. This signal will have a fixed delay of one PCM frame (125 $\mu$ s) with respect to RI                                             |

## Pin Description

**Table 20 Speech Highways**

| Ball No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                                                                                                                                                                                                                               |
|----------|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H14      | SO128  | I/O, PU    | Auxiliary 2.048 Mbit/s Send speech highway output in 128 ms mode. Input in master mode, output in slave mode. The pins of master and slave SIDEDEC in 128 ms mode should be connected to enable a 32 channel system. The signal from the slave is multiplexed in the master with the internally generated signal and output (clocked) with the system clock. Tristate and meaningless in 64 ms mode    |
| H13      | RO128  | I/O, PU    | Auxiliary 2.048 Mbit/s Receive speech highway output in 128 ms mode. Input in master mode, output in slave mode. The pins of master and slave SIDEDEC in 128 ms mode should be connected to enable a 32 channel system. The signal from the slave is multiplexed in the master with the internally generated signal and output (clocked) with the system clock. Tristate and meaningless in 64 ms mode |

**Table 21 UCC Interface**

| Ball No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                     |
|----------|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B6       | UCCI   | I, PD      | 2.048 Mbit/s UCC highway input. Start of timeslot 0, bit 7 and frame number can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers UCCMFR, UCCALIGN and PHALIGN[7:6] |

## Pin Description

**Table 21 UCC Interface**

| Ball No. | Symbol                    | I/O, PU/PD | Function                                                                                                                                                                                                                                                                               |
|----------|---------------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A5       | UCCO                      | O          | 2.048 Mbit/s UCC highway output. Start of timeslot 0, bit 7 and frame number can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers UCCMFR, UCCALIGN and PHALIGN[7:6]                                                                                          |
| B5       | $\overline{\text{TUCCO}}$ | O          | Tristate control signal for external tristate output buffer at the UCCO bus, active low. Remains inactive after a power on reset until the configuration by the $\mu\text{P}$ has been settled. Active only at UCC timeslot 0 for UCC frames that correspond to processed PCM channels |

**Table 22 Speech Highway Control Signals for CAS in T1 Systems**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                             |
|---------|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------|
| K13     | TSIGM  | I, PD      | Transmit Signaling Marker, indicating robbed bits at SI, corresponding to the delay of SI                                            |
| L14     | TMFBI  | I, PD      | Transmit Multiframe Begin Input corresponding to the delay of SI                                                                     |
| F14     | TMFBO  | O          | Transmit Multiframe Begin Output corresponding to the delay of SO. The delay of TMFBI to TMFBO is identical to the delay of SI to SO |

**Table 23 Channelwise Serial Interface**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                                                  |
|---------|--------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F1      | DIS    | I, PD      | Serial 256 kbit/s disable signal to bypass the canceller, NLP and attenuator and to reset the H-Register and Speech Control unit on a per channel basis. High active, maskable, leave open or connect to ground if unused |
| F2      | NLPDIS | I, PD      | Serial 256 kbit/s signal to disable the NLP on a per channel basis. High active, maskable, leave open or connect to ground if unused                                                                                      |

## Pin Description

**Table 23 Channelwise Serial Interface (cont'd)**

| Pin No. | Symbol    | I/O, PU/PD | Function                                                                                                                                                                                                                                                                            |
|---------|-----------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E1      | FREEZE    | I, PD      | Serial 256 kbit/s signal to freeze the H-Registers on a per channel basis. High active, maskable, leave open or connect to ground if unused                                                                                                                                         |
| E2      | CONVDIS   | I, PD      | Serial 256 kbit/s signal to disable A/ $\mu$ -Law conversion on a per channel basis. High active, maskable, leave open or connect to ground if unused                                                                                                                               |
| D1      | ENCC      | I, PD      | Serial 256 kbit/s signal to enable clear channel transparency on a per channel basis. High active, maskable, leave open or connect to ground if unused, same function as DIS='1' and CONVDIS='1'                                                                                    |
| D2      | FLEXSCTR  | I, PD      | Flexible serial 256 kbit/s control signal on a per channel basis. Configurable by register CONFLEXSCTR. High active, maskable, leave open or connect to ground if unused                                                                                                            |
| K2      | DISMON    | O          | Serial 256 kbit/s EC disable (signals bypass channels) monitor output signal ('0': EC on, '1': EC off)                                                                                                                                                                              |
| K1      | NLPDISMON | O          | Serial 256 kbit/s NLP disable monitor output signal ('0': NLP on, '1': NLP off)                                                                                                                                                                                                     |
| J2      | FREEZEMON | O          | Serial 256 kbit/s H-Register freeze monitor output signal ('1': freeze, '0': no freeze)                                                                                                                                                                                             |
| J1      | HRESMON   | O          | Serial 256 kbit/s H-Register reset monitor output signal ('1': reset, '0': no reset)                                                                                                                                                                                                |
| H2      | FLEXMON1  | O          | Serial 256 kbit/s monitor output signal (32 channels at 8 kbit/s), monitoring according to settings of the bits CONFLEXMON[7:4], e.g. Idle channel detection, 2010 Hz tone detected, 2100 Hz tone with or without phase reversal detected, double talk detected, no speech detected |

## Pin Description

**Table 23 Channelwise Serial Interface (cont'd)**

| Pin No. | Symbol     | I/O, PU/PD | Function                                                                                                                                                                                                                                                                            |
|---------|------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H1      | FLEXMON2   | O          | Serial 256 kbit/s monitor output signal (32 channels at 8 kbit/s), monitoring according to settings of the bits CONFLEXMON[3:0], e.g. Idle channel detection, 2010 Hz tone detected, 2100 Hz tone with or without phase reversal detected, double talk detected, no speech detected |
| G1      | CONVDISMON | O          | Serial 256 kbit/s law conversion disable monitor output signal ('1': conversion disabled, '0': conversion enabled)                                                                                                                                                                  |
| G2      | CCMON      | O          | Serial 256 kbit/s clear channel transparency (64 clear) monitor output signal ('1': clear channel on, '0': clear channel off), same as DISMON='1' and CONVDISMON='1'                                                                                                                |

**Table 24 Test Interface for Boundary Scan according to IEEE 1149.1**

| Ball No. | Symbol | I/O, PU/PD | Function                                                                     |
|----------|--------|------------|------------------------------------------------------------------------------|
| B2       | TDI    | I, PU      | Test Data Input                                                              |
| A1       | TDO    | O          | Test Data Output                                                             |
| B1       | TMS    | I, PU      | Test Mode Select                                                             |
| C2       | TCK    | I, PU      | Test Clock                                                                   |
| C1       | TRST   | I, PU      | Boundary Test Reset (active low, should be tied to '0' for normal operation) |

**Table 25 Test Interface**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                            |
|---------|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------|
| A3      | KSCMOD | I, PD      | SCAN MODE ENABLE pin for enabling of scan test. For normal operation this pin should be left unconnected or connected to $V_{SS}$ . |

## Pin Description

**Table 25 Test Interface (cont'd)**

| Pin No. | Symbol | I/O, PU/PD | Function                                                                                                                                                                                        |
|---------|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A4      | KSCEN  | I, PD      | SCAN SHIFT ENABLE pin for shift enabling in scan test. For normal operation this pin should be left unconnected or connected to $V_{SS}$ .                                                      |
| A2      | TEST   | I, -       | Reserved for special tests (i.e. IDDQ, MBIST, etc.). For normal operation this pin must be connected to $V_{SS}$ . Disables all pull resistances for IDDQ if set to '1'. Normal operation: '0'. |

*Note: The Test interface will be used by the manufacturer. For normal operation, this pins should be connected to the recommended fixed value in the table.*

**Table 26 Power Supply**

| Pin No.                                                                                                                               | Symbol | I/O, PU/PD | Function           |
|---------------------------------------------------------------------------------------------------------------------------------------|--------|------------|--------------------|
| E3,F4,J4,K3,L4,L6,L9,L11,M3,M5,M10,M12,C3,C5,C10,C12,D4,D6,D9,D11,E12,F11,J11,K12                                                     | VSS    |            | Common ground rail |
| D3,E4,F3,G3,G4,L5,L7,L8,L10,M4,D12,E11,F12,G11,G12,H11,H12,C4,C6,C7,C8,C9,C11,D5,H3,J3,L3,H4,K4,M6,D7,M7,D8,M8,M9,D10,K11,M11,J12,L12 | VDD    |            | Core power supply  |

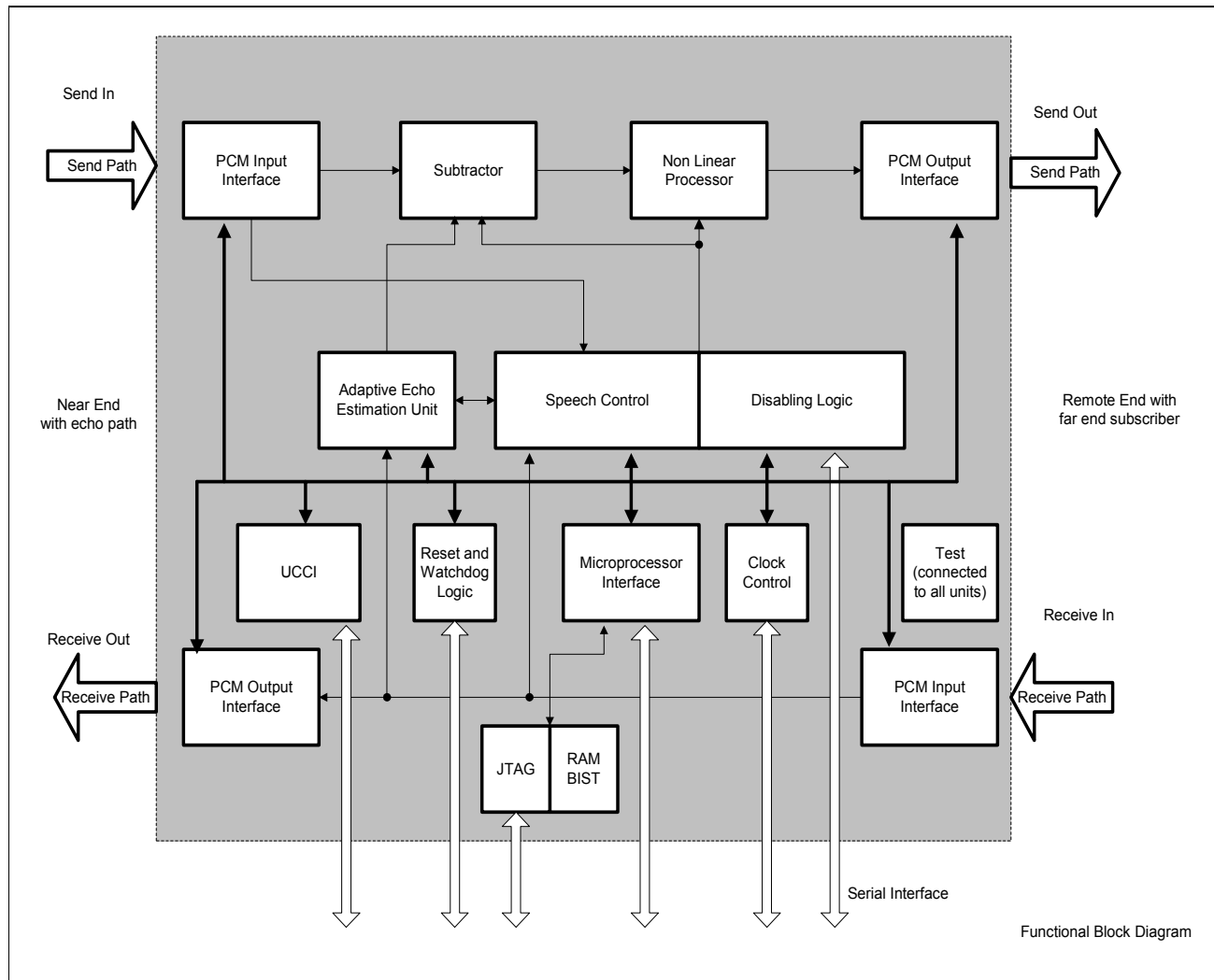
Pin Description

**Table 27      Unused Pins**

| Pin No.                             | Symbol | I/O, PU/PD | Function           |
|-------------------------------------|--------|------------|--------------------|
| A14,B3,B4,B8,B9,C13,L13,M13,N13,J14 | NC     |            | Common ground rail |

## 3 Functional Description

### 3.1 Functional Block Diagram and Description



**Figure 8 Block Diagram**

The following paragraphs describe the functions of the SIDEDEC block diagram shown in [Figure 8](#).

#### 3.1.1 Speech Control

The Speech Control analyzes the data from the PCM Input Interfaces and external inputs and supervises the functions of the other system components. As soon as the far end subscriber talks, the Adaptive Echo Estimation Unit is activated by the Speech Control. If the double talk condition is detected or a non speech signal with an adequate echo loss enhancement is identified by the Speech Control, the content of the Adaptive Echo Estimation Unit is frozen. Under specific circumstances a reset of the H-Register

---

**Functional Description**

(described in Section **Figure 3.1.3**) of the Adaptive Echo Estimation Unit might be necessary. The H-Register reset signal is also provided by the Speech Control.

### **3.1.2 Disabling Logic**

Upon request of the Speech Control and depending on external inputs the Disabling Logic disables the Non Linear Processor and/or the Subtractor or even the complete Echo Canceller.

If the Speech Control Unit detects, that one of the following conditions is applied to the Echo Canceller, it will disable the device via the Disabling Logic:

- Disabling via 2100 Hz tone without phase reversal
- Disabling via 2100 Hz tone with phase reversal
- Disabling via 2010 Hz continuity check
- Disabling via PCM timeslot 16 Bit a, b, c or d according to ITU G. 704
- Disabling via Idle channel detection.
- Disabling of individual channels via external interfaces ( $\mu$ P, serial and/or UCC interface)

### **3.1.3 Adaptive Echo Estimation Unit**

The Adaptive Echo Estimation Unit contains for each 8 bit signal sampled at 8 kHz memory for 512 / 1024 byte. This is equivalent to 64 / 128 ms end echo path delay. Depending on the end echo path delay of 64 or 128 ms the Adaptive Echo Estimation Unit processes 32 or 16 channels simultaneously, respectively. The corresponding 32 / 16 H-Register for each channel representing the pulse response of the complete echo path are also stored in the Adaptive Echo Estimation Unit. This information simplifies the detection of double speech. A highly sophisticated and patented algorithm guarantees fast and stable convergence even in the presence of near end speech.

The Adaptive Echo Estimation Unit is connected to the Microprocessor Interface in order to configure parameters of the algorithm and to read the content of the H-Register.

### **3.1.4 PCM Input/Output Interface**

Each PCM Input/Output Interface contains a delay element, that is adjustable for max 125  $\mu$ s delay in 122 ns steps in order to align the corresponding PCM signal to the synchronizing pulse. Unless not bypassed, the delay from Receive In to Receive Out is fixed to one PCM Frame equivalent to 125  $\mu$ s. The signal Multiframe Begin is delayed accordingly to the send path delay.

Encoder to convert A- or  $\mu$ -Law PCM signals to linear, and decoder to convert linear PCM signals to A- or  $\mu$ -Law allow for channelwise Law Conversion (transcoding).

## Functional Description

Offset adjustment is implemented at the output of the canceller. The attenuation of 0 dB, 2.5 dB or 6 dB is programmable by a register. The use of this feature requires that the cancelling function for the corresponding timeslot is enabled.

The complete bypassing of individual timeslots and connections from and to the processor interface with the internal canceller is provided for testing of cancelling timeslots.

The least significant bit in the send path can be transmitted transparently to the output if the corresponding external pin TSIGM is activated (CAS bit robbing).

The block PCM Input/Output Interface provides time multiplexing/demultiplexing for 16 or 32 timeslots. (depending on configuration, see section above). In 128 ms echo end path mode the selection of timeslots at the input is assigned as follows:

- Master: Timeslot0,1,2,3, 8,9,10,11,16,17,18,19, 24,25,26,27
- Slave: Timeslot4,5,6,7, 12,13,14,15,20,21,22,23, 28,29,30,31

The PCM Input/Output Interfaces are connected to the Speech Control Unit, Disabling Logic and the Microprocessor Interface.

### 3.1.5 Subtractor

The subtractor calculates the difference between the signal from the PCM Send In Interface and the artificial echo provided by the Adaptive Echo Estimation Unit. The subtractor is controlled by the Speech Control.

### 3.1.6 Non Linear Processor

The Non Linear Processor (NLP) limits the residual echo if only far end talk is present. Three programmable functions are available:

- Block echo and background noise.
- Replace echo and background noise by comfort noise with the level of the determined background noise.
- Clip the level of the echo and the background noise to the level of the background noise. (Experiments show that most people prefer this configuration)

The NLP is controlled by the Disabling Logic and Speech Control.

### 3.1.7 Microprocessor Interface

The Microprocessor Interface can operate in Intel and Motorola Mode. It provides access to the internal configuration, control states and monitor registers.

### 3.1.8 Universal Control and Communication Interface

The UCC Interface is a serial hardware interface for SIDEDEC control and supervision by other boards via a Microprocessor. A special feature of the SIDEDEC-UCC Interface is, that

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**Functional Description**

certain controlling functions like the channelwise disabling or A/ $\mu$ -Law conversion can be operated directly by the hardware without intervention of the microprocessor. This feature reduces the work load of the processor dramatically.

### **3.1.9 Watchdog Timer**

A Watchdog timer is implemented to reset the on board processor if the software gets stuck in an undefined state as a result of a faulty operation. A reset condition is met if the microprocessor fails to write predefined values to the three watchdog registers in the correct sequence within 2 s. As long as the watchdog is active the SDEC generates interrupts and/or reset pulses of 125  $\mu$ s width with a period of 2 s.

### **3.1.10 Clock Control**

The Clock Control supervises and generates all clock signals for proper operation of the ASIC hardware.

### **3.1.11 JTAG and RAM BIST**

The JTAG (Joint Test Application Group) has been implemented according to IEEE 1149.1. A RAM BIST (Random Access Memory Built In Self Test) is also provided.

### **3.1.12 Test**

The Test Unit controls the background test on disabled channels. A built in self test is used for testing internal RAMs. This test can be activated after switching on the supply voltage. The test unit also supervises the Clock Control Unit.

A notebook register allows the check of the  $\mu$ P Interface.

Within the Test Unit the registers for background testing of idling channels are implemented. In this test a pattern is input in the idling channel at Receive in and Send in and evaluated at the Send out port.

During normal operation the Test Unit supervises functions such as read out of levels, internal states and coefficients.

## 3.2 Description of Functional Features

### 3.2.1 Channelwise and Global A- and $\mu$ -Law Conversion

The SIDEC allows channel individual conversion. **Figure 9** depicts the implementation of the different options for the A- to  $\mu$ - or  $\mu$ - to A-Law conversion. Depending on the requirements of the application two settings can be configured: Either global or channel individual law conversion.

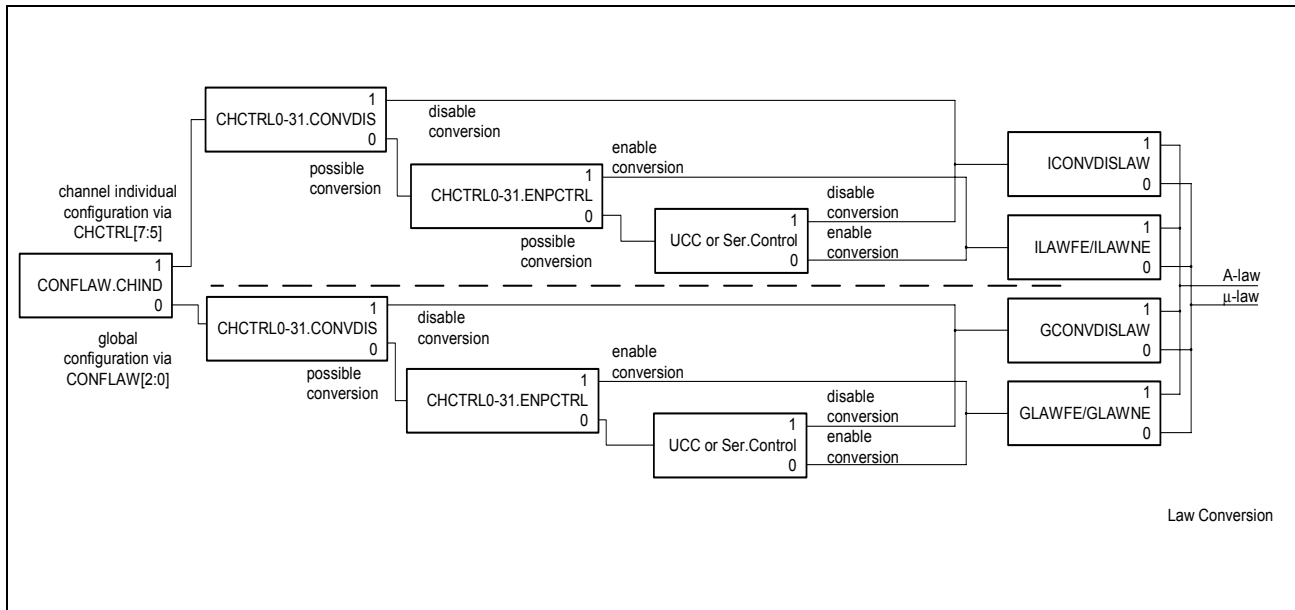
Global A- to  $\mu$ - and  $\mu$ - to A-Law conversion:

If this modus is chosen by setting CONFLAW.CHIND='0' all 32 PCM channels are converted according to the settings of GALAWFE for the far end and GALAWNE for the near end. A '1' in GALAWFE and GALAWNE indicates that A-Law is used for the corresponding end. A '0' indicates usage of  $\mu$ -Law. The conversion can be disabled channel individually by setting the CHCTRL0-31.CONVDIS = '1' via software. Law decoding/encoding is then carried out according to GCONVDISLAW. To activate the serial control signal and the UCC interface as disabling source for the PCM law conversion the bits CHCTRL0-31.ENPCTRL must be set to '0'.

Channel individual A- to  $\mu$ - and  $\mu$ - to A-Law conversion:

For channel individual conversion the user can configure independently for each channel whether A- to  $\mu$ -,  $\mu$ - to A- or no Law conversion is selected via setting IALAWNE for the near end and IALAWFE for the far end with the corresponding value for A- or  $\mu$ -Law. The conversion can be disabled channel individually by setting the CHCTRL0-31.CONVDIS = '1' via software. Law decoding/encoding is then carried out according to CHCTRL0-31.CONVDISLAW. To activate the serial control signal and the UCC interface as disabling source for the PCM law conversion the bits CHCTRL0-31.ENPCTRL must be set to '0'.

## Functional Description



**Figure 9 Explanation of Options for A- and  $\mu$ -Law Conversion**

### 3.2.2 Bypass and Disabling Functions

**Figure 10** depicts the bypass and disabling functions of the SDEC. They can be configured via UCC, Serial and  $\mu$ P Interface.

Setting  $NLPDIS = '1'$  (pin or register setting) leads to bypassing of the Non Linear Processor.

Setting  $BYPASS = '1'$  (Serial control signal, UCC or 2100 Hz tone via register settings) results in bypassing the Attenuator in the Receive Path as well as in bypassing the Subtractor, the Non Linear Processor and the Attenuator in the Send Path.

Disabling a channel or the complete canceller will result in a  $BYPASS$  function, a H-Register reset and a reset of the Speech Control Unit. A bypassed or disabled channel of the SDEC can still be converted from A/ $\mu$ - Law or vice versa.

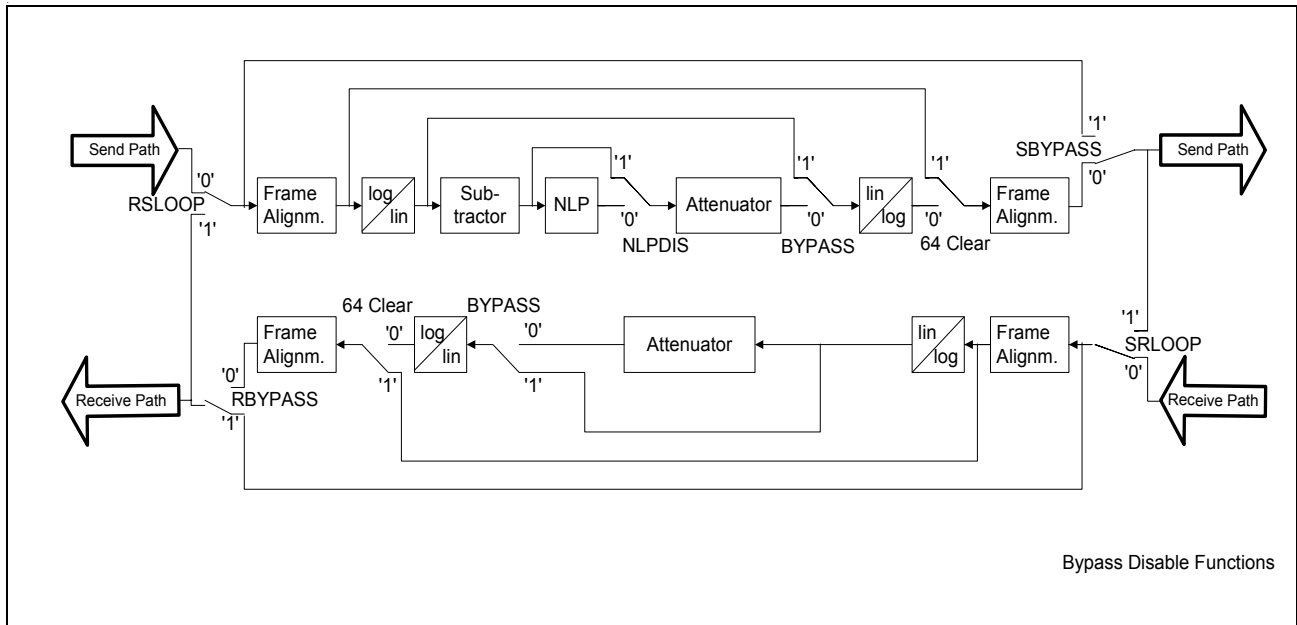
If a Modem call is detected the user can define what action is related to the detection of a Modem call (2100 Hz with phase reversal or without reversal): bypassing, NLP bypassing, H-Register Reset or combination of the functions.

The 64 Clear mode is activated by bypassing and defining the same Law Conversion at near end and far end. In 64 Clear mode the signal is still passed through the frame alignment.

For testing purposes the canceller can be completely bypassed by setting  $SBYPASS$  and  $RBYPASS$ .

The Receive out signal can be input directly to the Send In port by setting the  $RSLOOP = '1'$ . The Send out signal can be input directly to the Receive in port by setting the  $SRLOOP = '1'$ . If both loops are configured only  $RSLOOP$  will be enabled in the SDEC.

## Functional Description



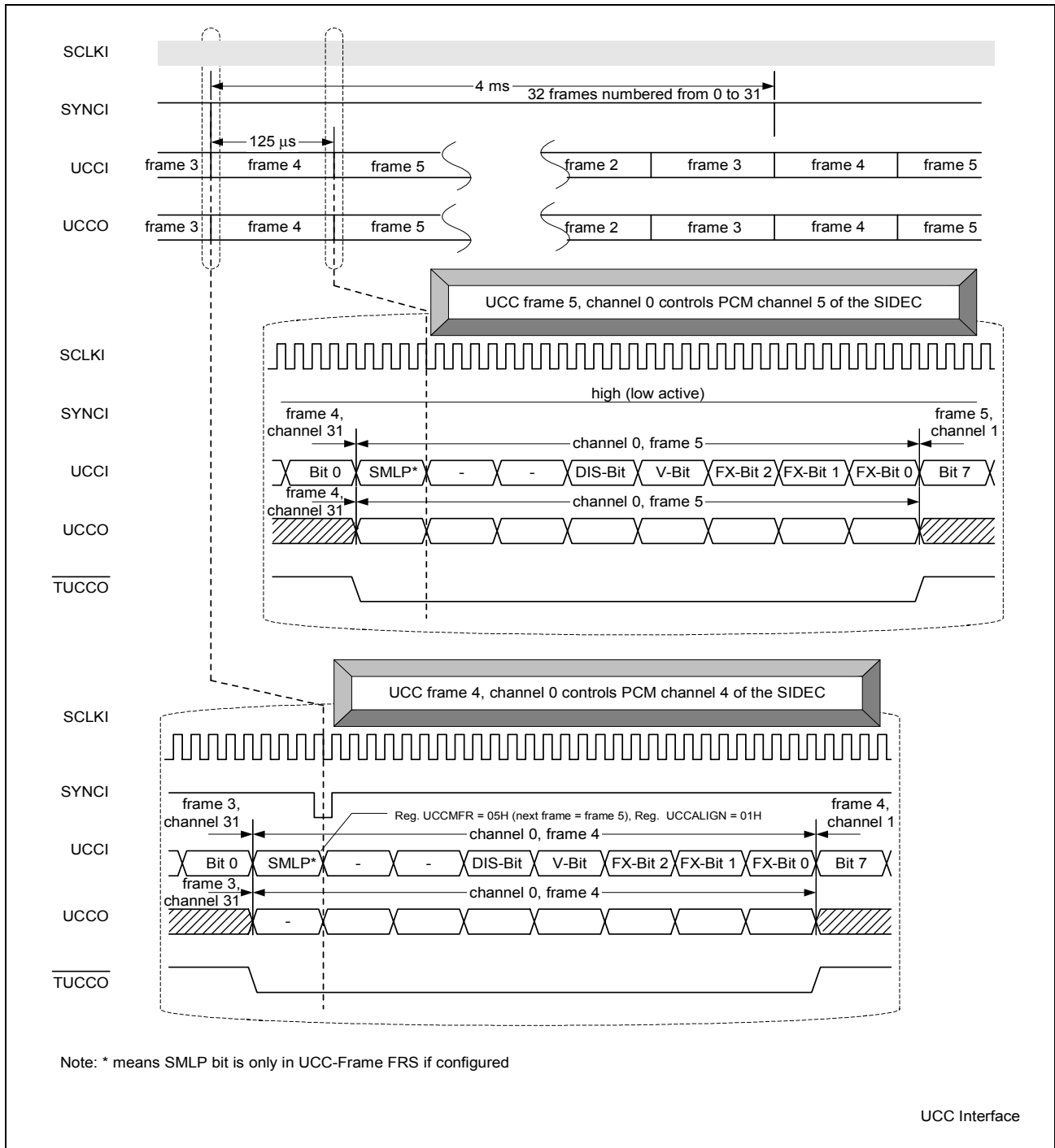
**Figure 10 Bypass and Disabling Functions of the SIDEC**

### 3.2.3 UCC Interface

The UCC Interface uses a clock frequency of 2048 kHz. The UCC Signal is structured into frames (period 125  $\mu$ s) consisting of 32 channels (period 3.9  $\mu$ s) and a multiframe consisting of 32 frames (period 4 ms). The multiframe is synchronized with the SYNCI Input pulse. The SIDEC reads and writes (tristate controlled) only the channels 0 of the frames. The 32 channels 0 of each multiframe are used to control and supervise the associated PCM channels. UCC Frame 0 corresponds to PCM channel 0, UCC Frame 1 corresponds to PCM channel 1, .... This relation is depicted in [Figure 11](#). It is also possible to use one special UCC-Frame for a general purpose. With the registers UCCMFR, UCCALIGN and PHALIGN[7:6] the UCC channel 0 of frame 0 can be shifted to any channel and frame. Hence, up to 32 different devices can be connected in parallel to the UCC Interface.

The output signal UCCO is always in phase with the UCCI input signal.

## Functional Description



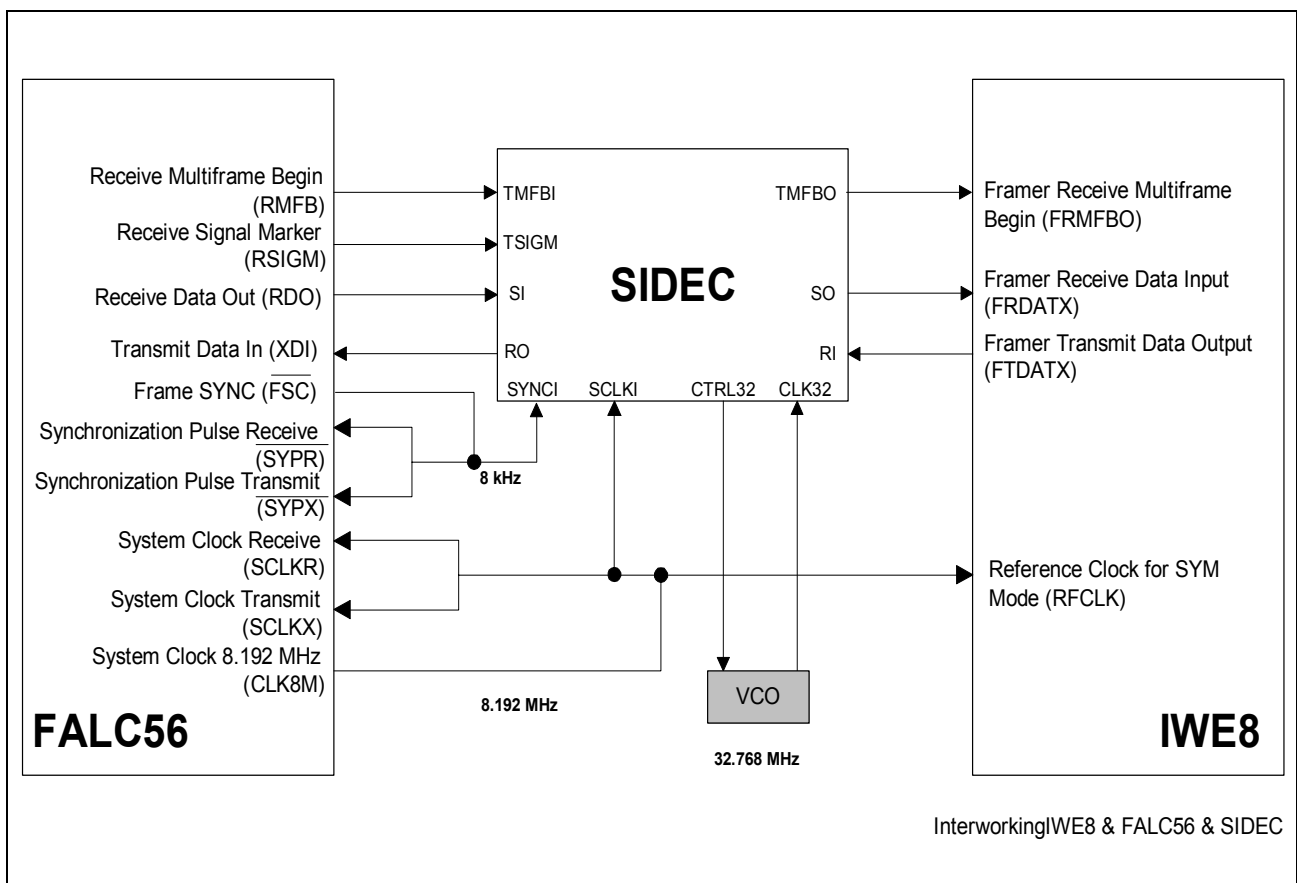
**Figure 11 UCC Signal for control of PCM Signal**

## 4 Operational Description

### 4.1 Pin Connection Diagram for SIDEC

**Figure 12** illustrates an example for the pin connection of the SIDEC to an E1/T1 IC and to an interworking element IC.

The SIDEC is used to cancel the echo on the side of the FALC 56 which is the near end in this case. There are two INFINEON products in this Inter working unit connected to the SIDEC. The FALC serves as a frame and line interface component whereas the IWE8 PEB 4220 operates as an interworking element. For multiframe alignment in the IWE8, FRMFBX must have a correct timing relation to FRDATX. For this purpose the SIDEC adjusts the delay from the TMFBI input to the TMFBO output to the delay of the SI input to the SO output. For the support of the CAS-BR transparency the SIDEC passes the robbed bits that are indicated by the FALC via the TSIGM input directly through to the SO output by overwriting the computed value of the robbed bit with the value of the SI input.



**Figure 12 Internet Working Unit: SIDEC between a FALC and IWE8**

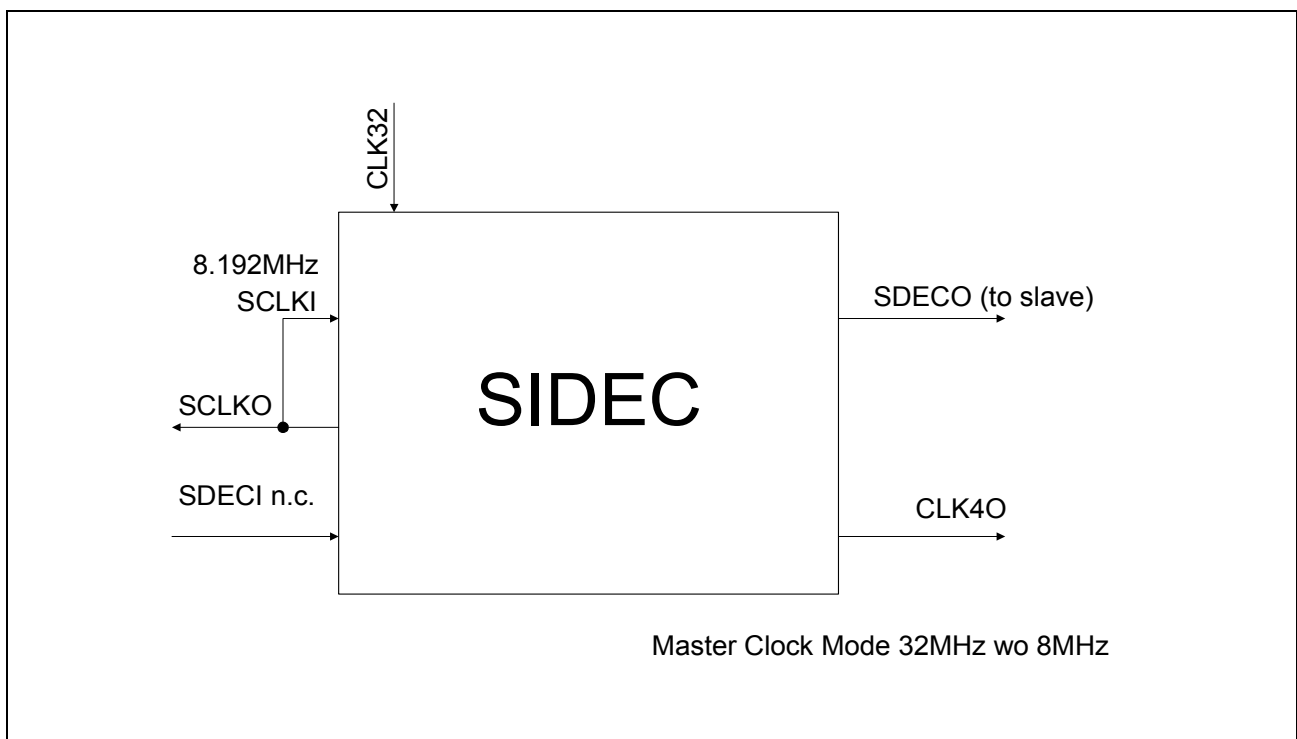
## 4.2 Synchronization and Clock Modes

The SIDEc can be connected in different synchronization and clock modes. These modes can be used for several applications.

Basically there are two clock modes, slave and master clock mode (not to be mixed up with 128 ms master and slave mode). The internal clock system in master clock mode is automatically synchronized to the system clock by using an external 32.768 MHz VCO or by generating and deriving the system clock at output pin SCLKO directly from the CLK32 input. SIDEc in master clock mode provides a synchronization pulse at pin SDECO. This pulse can be used by a SIDEc in slave clock mode to synchronize its internal clock system to the system clock without the needs for additional external VCO.

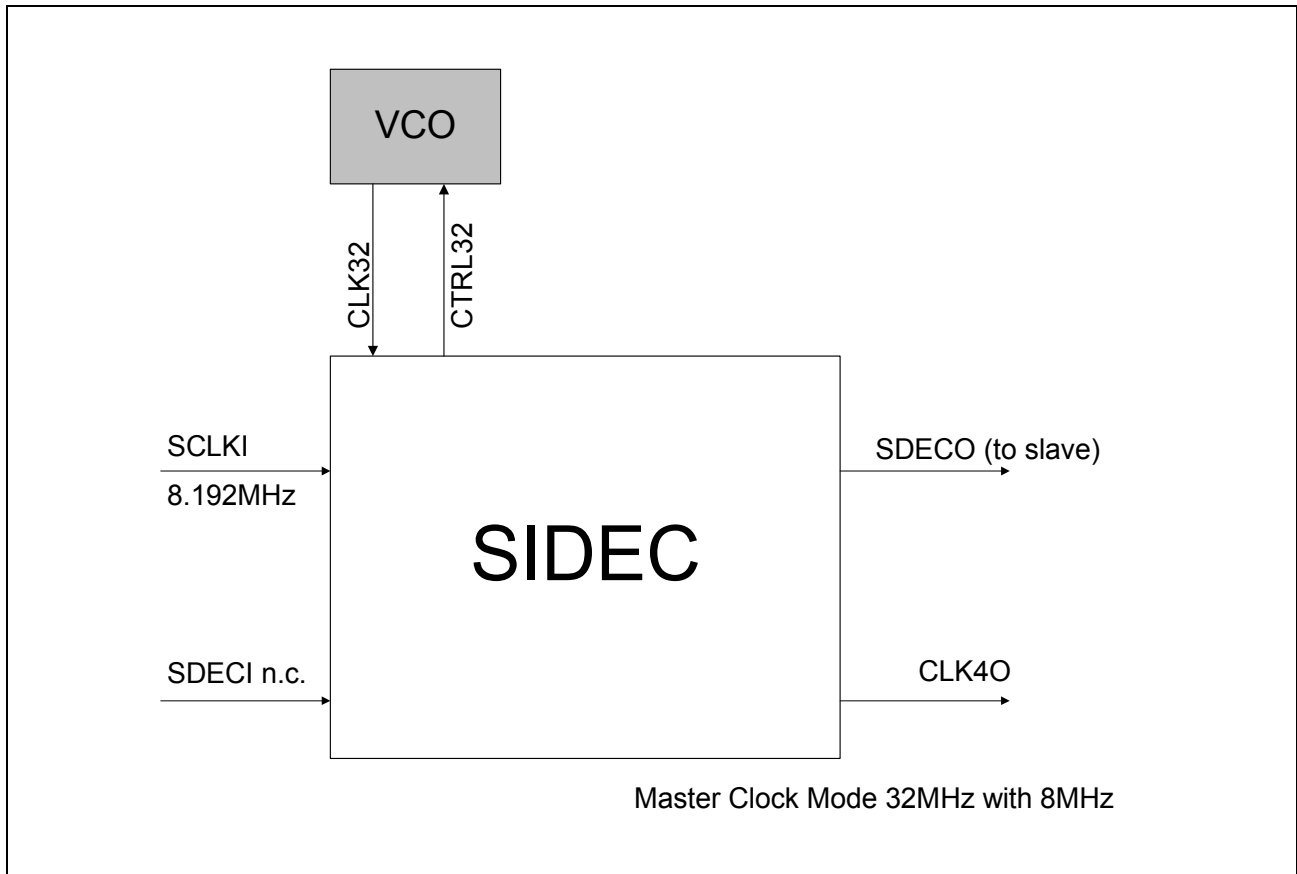
Examples for this mode are the 128 ms delay application and the multiple SIDEc application, see also [Figure 17](#) and [Figure 18](#).

CLK4O is 4.096 MHz system clock output for subsequent circuits, derived from SCLKI.



**Figure 13 Master Clock Mode, ext. 32.768 MHz, no SDECI Clock**

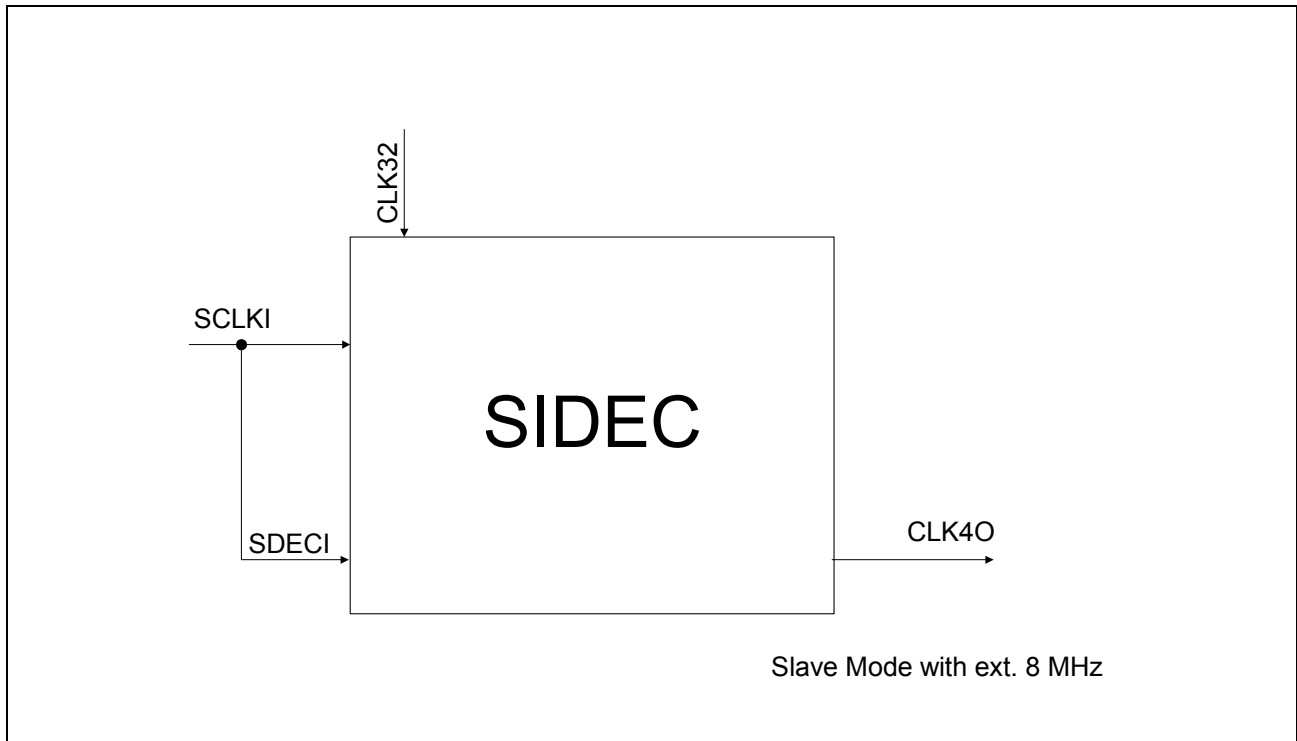
In [Figure 13](#) the system clock is reconnected from SCLKO to SCLKI in order to properly process the PCM signals. The system clock at pin SCLKO can also be provided for other devices. The SDECI pin is not connected in the master clock mode. A 32.768 MHz clock has to be provided by an external clock oscillator or other clock source on the system.



**Figure 14 Master Clock Mode with External 8.192 MHz Clock**

In the master clock mode with 8.192 MHz clock ([Figure 14](#)), the 32.768 MHz operating clock is supplied by the VCO. The SIDEc provides a controlling voltage for the VCO in order to synchronize the CLK32 to the system clock SCLKI.

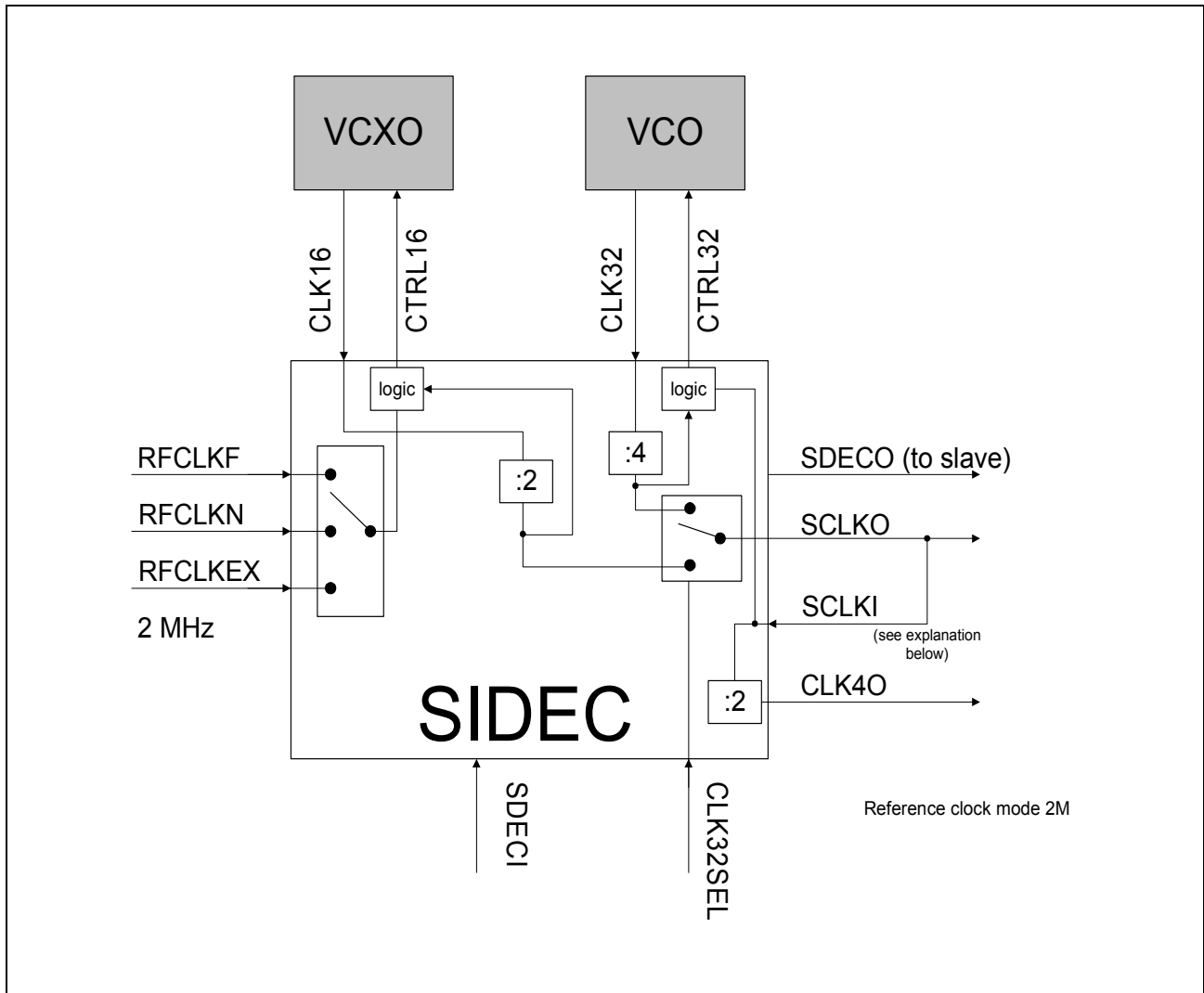
SDECi is not connected and the SDECO can be connected to other SIDEcs.



**Figure 15 Slave Clock Mode with External 8.192 MHz and 32.768 MHz**

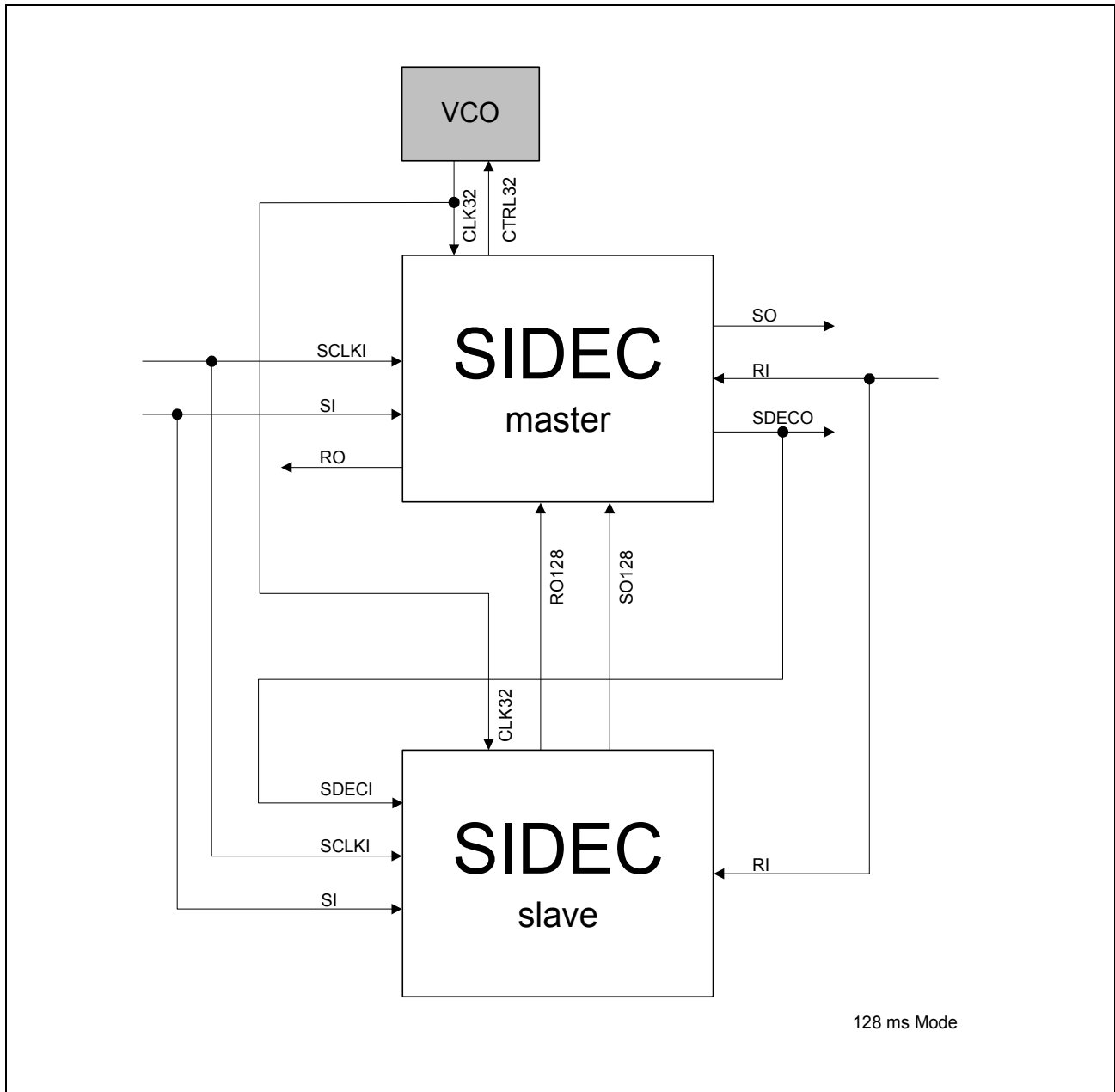
In the slave clock mode the 8.192 MHz and the 32.768 MHz clock have to be synchronous and phase aligned (e.g. SCLKI has been derived from CLK32 by some external device). There is no internal synchronization between SCLKI and CLK32. SDECI is needed for correct phase alignment of SCLKI to the internal system clock.

CLK4O is a 4.096 MHz system clock output for subsequent circuits, derived from SCLKI



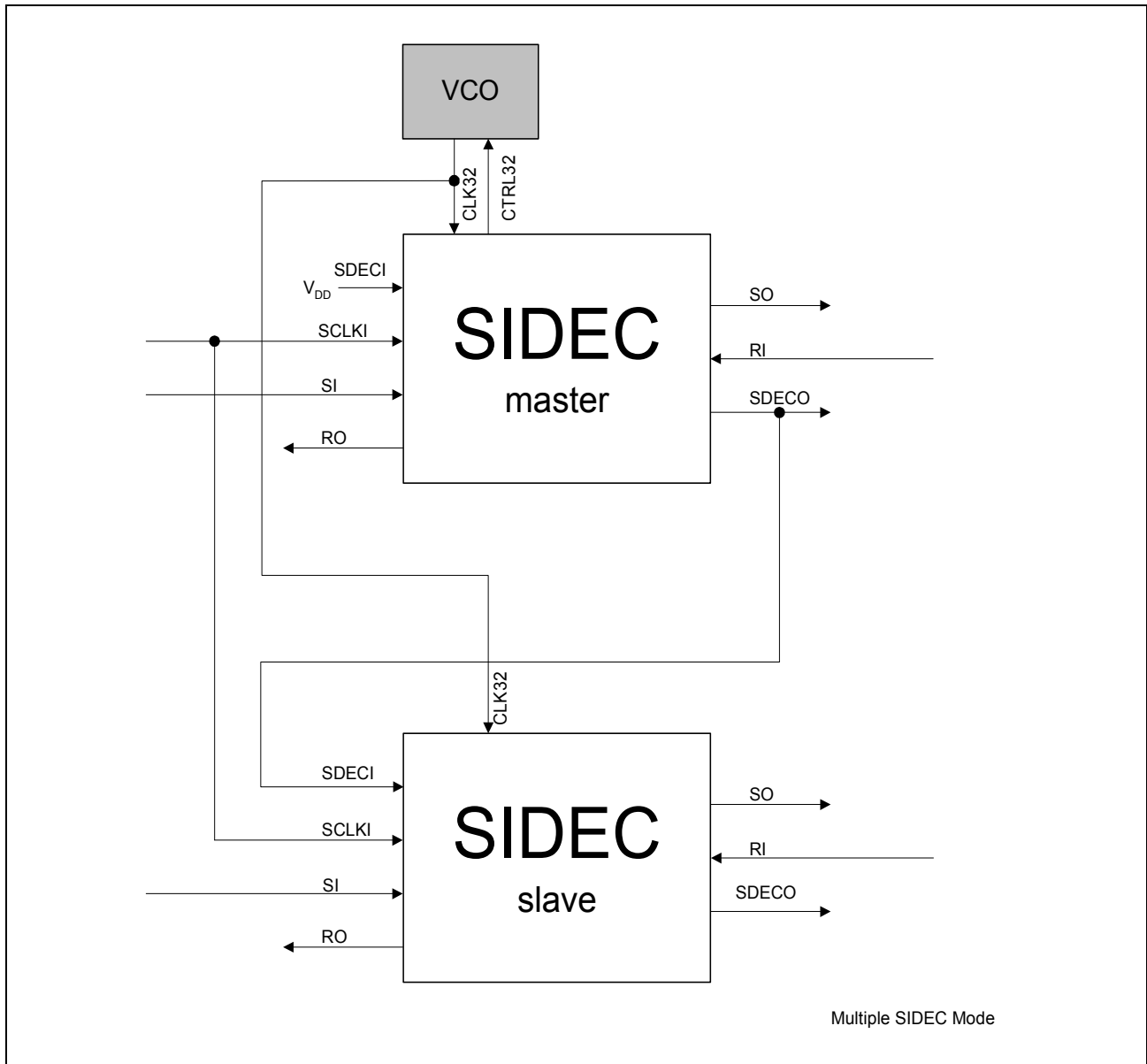
### Figure 16 Reference Clock Mode with 2.048 MHz

In this mode a 2.048 MHz system clock is provided at either the RFCLKF, RFCLKN or the RFCLKEX pin. The VCXO and VCO supply the operating clocks for the SDEC. SDECO can be connected to slave. The feedback from SCLKO to SCLKI in order to generate a control voltage for the 32 MHz VCO makes only sense if SCLKO is derived from CLK16. The SDECI initializes the counter.



### Figure 17 128 ms Delay Mode

The pin connection of a 128 ms master and slave SIEC is shown in **Figure 17**. The SI and RI is supplied to both SIECs. The RO and SO is provided by the master. The RO128 and SO128 signals are used to multiplex the 128 ms slave data into the PCM data stream outputs of the master.



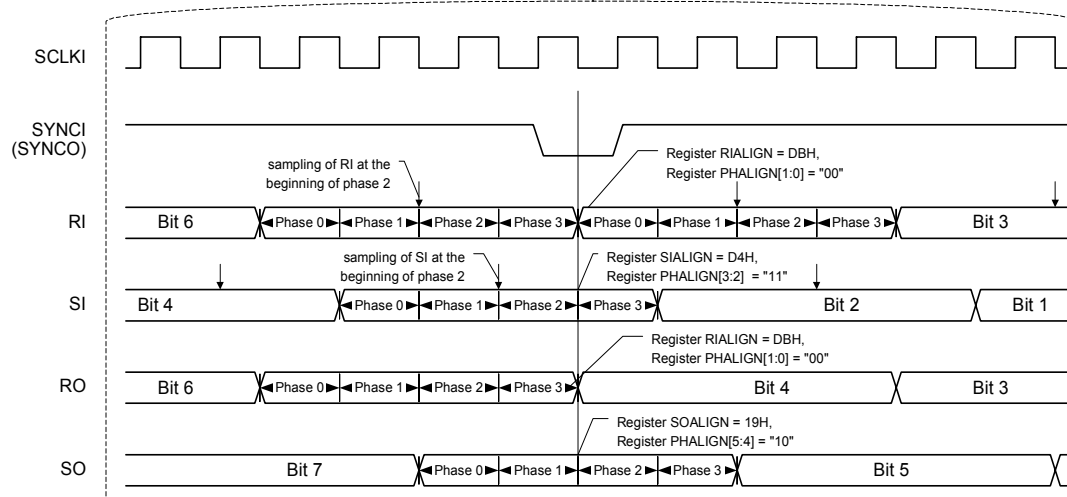
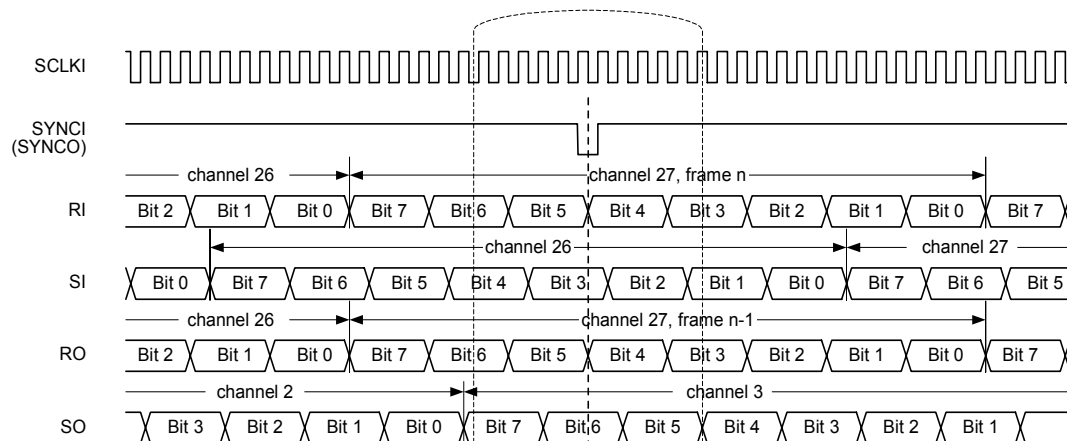
### Figure 18 Multiple SIDEc

In multiple SIDEc mode the output SDECO of the clock master SIDEc is used to synchronize clock slave SIDEcs to the system clock. In this application multiple E1/T1 lines can be echo cancelled, one E1/T1 line per SIDEc. Leave the SDECI of the master SIDEc open or connect it to ground  $V_{DD}$ .

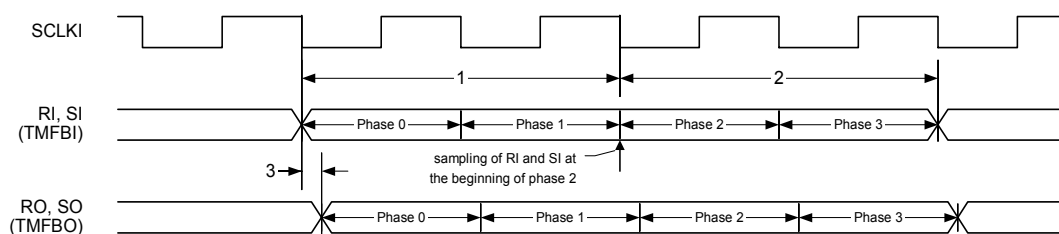
### 4.2.1 PCM Signal Timing and Frame Alignment

The SIDEc requires the MSB (bit7) first and the LSB (bit0) last as input.

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### Timing Characteristics



### PCM Signal Timing and Frame Alignment

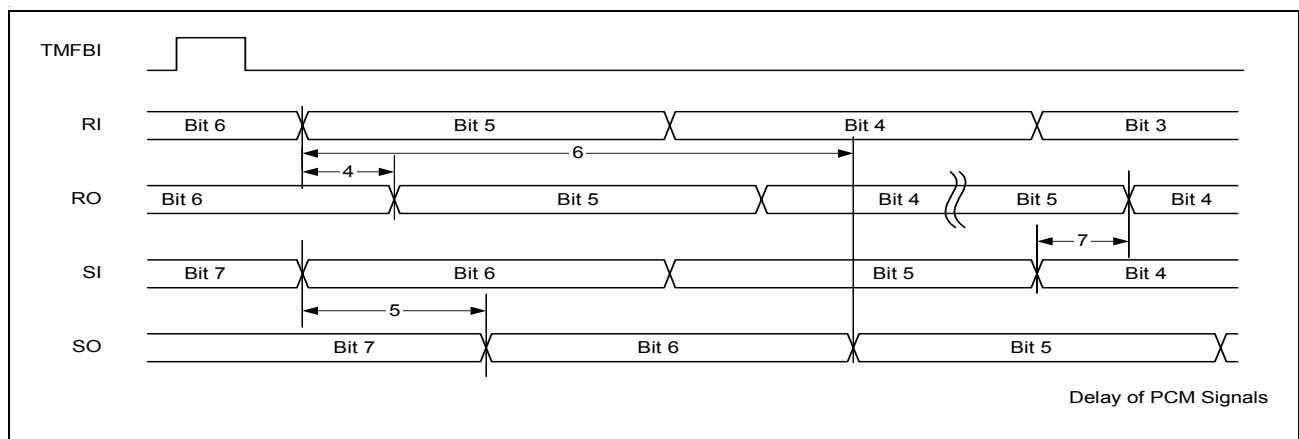
**Figure 19 PCM Signal Timing and Frame Alignment**

**Note:** Above values are examples only. PCM frame alignment with respect to the first detection of an active SYNCI (or SYNCO: If no SYNCI is applied, SYNCO takes over the part and role of SYNCI) with the falling edge of SCLKI can be configured by writing to the

## Operational Description

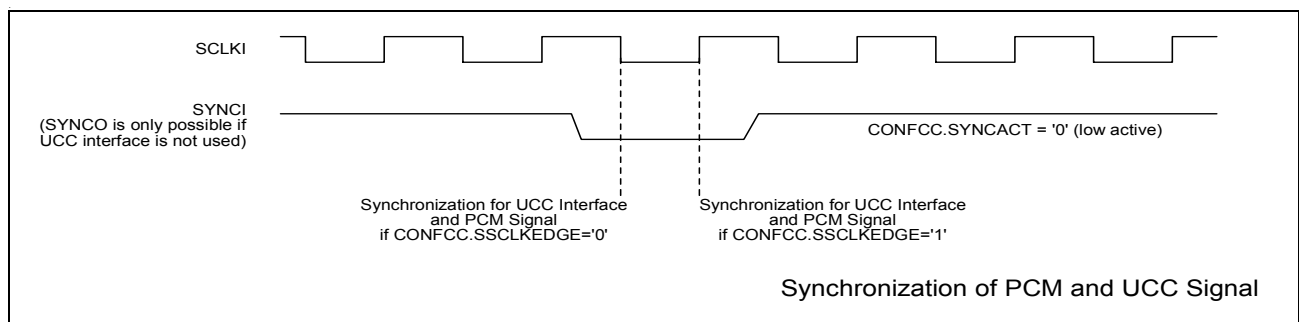
registers RIALIGN, SIALIGN and SOALIGN. For finer adjustments, the valid bit phase of the PCM signals at the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the register PHALIGN. The configured frame and bit phase alignment always denotes the beginning of the ideal bit phase (no signal delay) at the falling edge of SCLKI.

PCM inputs are always sampled with the falling edge of SCLKI at the beginning of bit phase 2, outputs are clocked with the falling edge of SCLKI at the beginning of bit phase 0. Unless not bypassed the PCM output RO has a fixed delay of one PCM frame (125  $\mu$ s) with respect to RI.



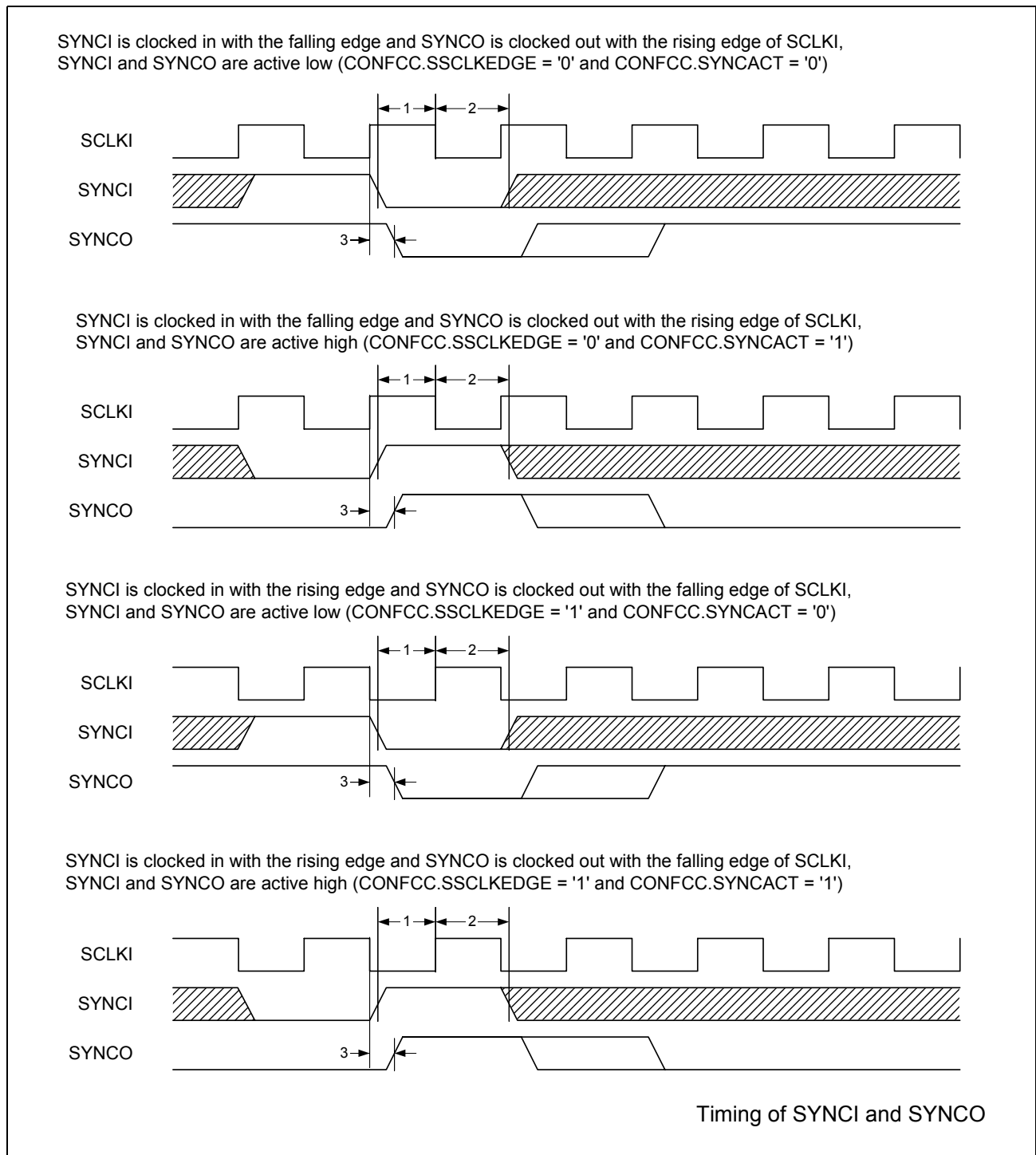
**Figure 20 Delay of PCM Signals**

**Figure 21** illustrates the synchronization of the 2048 kBit/s PCM and UCC signal for a low active SYNCI signal with respect to the internal 8192 kHz SCLKI signal. If SYNCI is sampled with the falling edge of SCLKI (CONFCC.SSCLKEDGE='0') this edge is the synchronization point for PCM and UCC signals. If SYNCI is sampled with the rising edge of SCLKI (CONFCC.SSCLKEDGE='1') the next falling SCLKI edge is the synchronization point for PCM and UCC signals. The SYNCO signal may only be used instead of the SYNCI signal if the UCC Interface is not used



**Figure 21 PCM and UCC Signal synchronization to SCLKI and SYNCI**

## 4.2.2 Timing of SYNCI and SYNCO

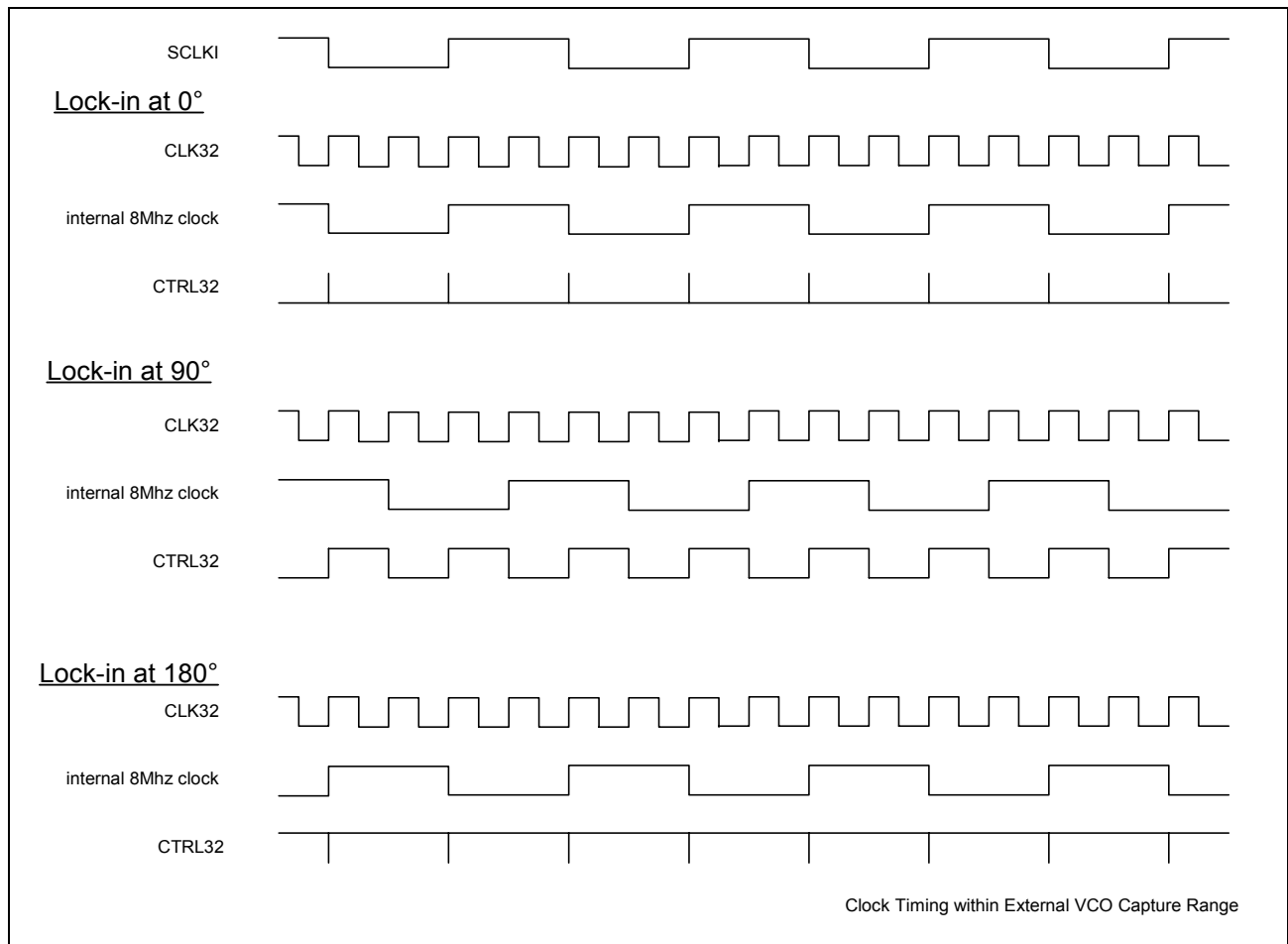


**Figure 22** Timing of SYNCI and SYNCO

**Figure 22** shows the timing of the synchronization pulses for different configurations.

**Note:** The duration of SYNCO pulse can be configured by register CONFCC.SYNCODUR to either one or two SCLKI (8.192 MHz) periods.

### 4.2.3 Clock Timing within External VCO Capture Range

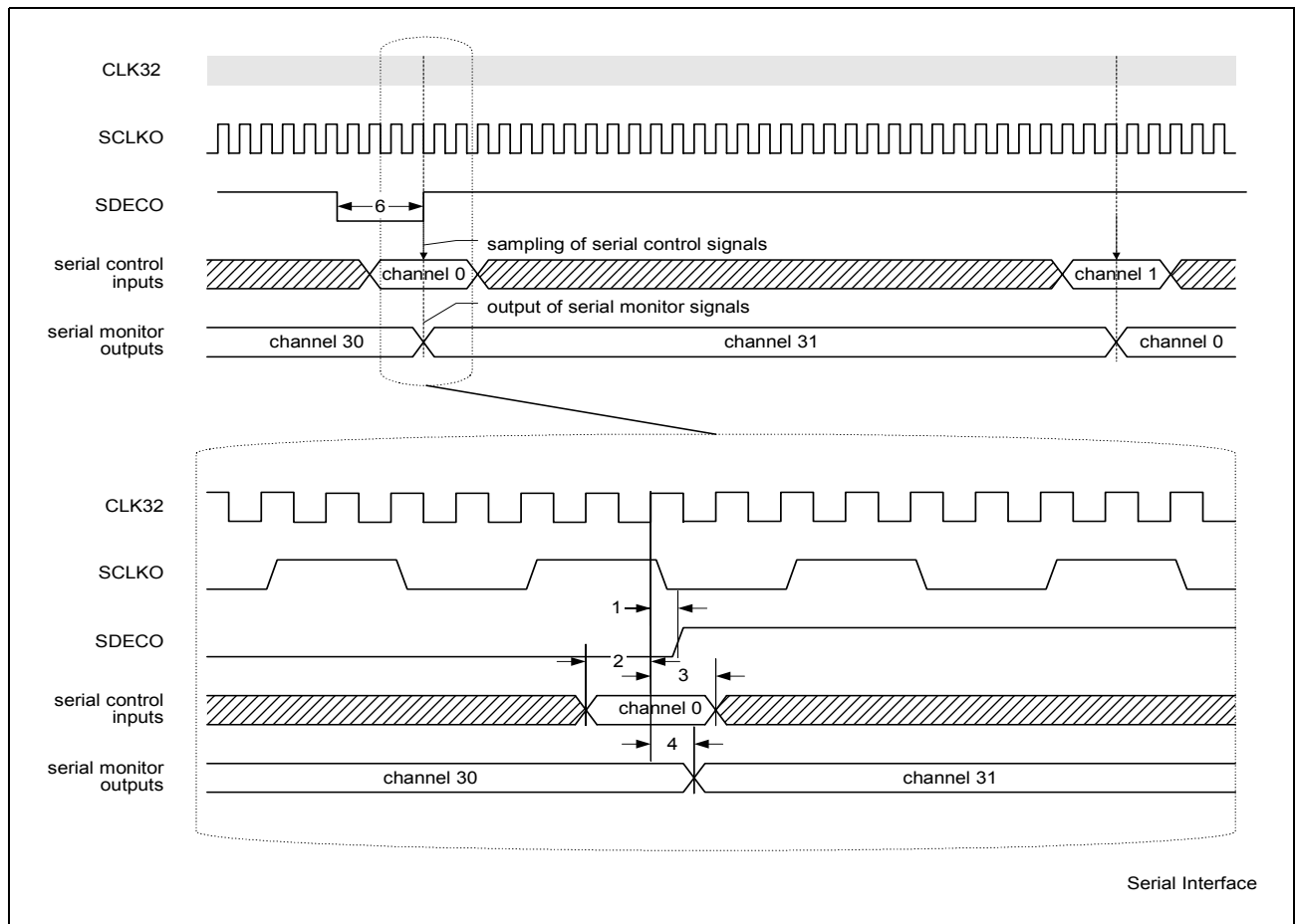


**Figure 23 Clock Timing within External VCO Capture Range**

In case a 32.768 MHz clock has to be generated and synchronized to the system clock at SCLKI, the signal at pin CTRL32 can be used to control an external VCO. The output at CTRL32 is the signal at SCLKI that is internally 'xored' with an internal 8.192 MHz clock that is derived from the signal pin CLK32 by division by 4. For proper operation of the SIDECC the system clock SCLKI and the internal 8.192 MHz clock must lock in within the capture range from 0° to 180°. CTRL32 can be inverted by bit CONFCC.INVCTRL32 for use of VCOs that increase the frequency with falling voltage.

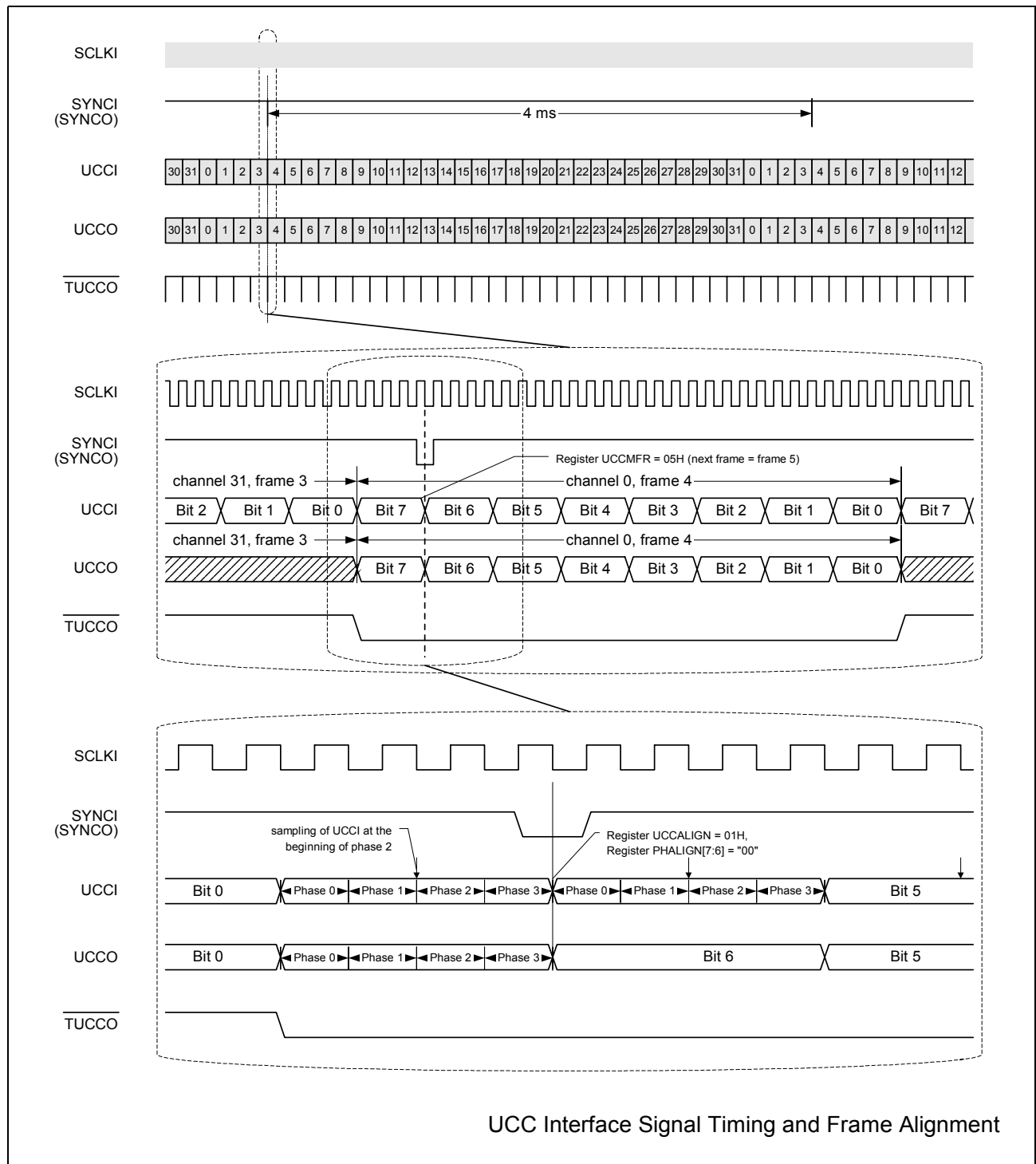
The internal 8.192 MHz clock can be monitored at pin SCLKO with a delay of three CLK32 periods plus internal signal delay if pin CLK32SEL is set to logic '1'.

#### 4.2.4 Serial Interface (Controlling and Monitoring) Timing



**Figure 24** Serial Interface (Controlling and Monitoring) Timing

## 4.2.5 UCC Interface Signal Timing and Frame Alignment



**Figure 25 UCC Interface Signal Timing and Frame Alignment**

**Note:** Above values are examples only. For the use of the UCC Interface a SYNCI signal with a period of 4 ms (equivalent to one multiframe) must be applied to the SIDECD. UCC frame and multiframe alignment with respect to the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the registers UCCALIGN

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## Operational Description

and UCCMFR. For finer adjustments, the valid bit phase of the UCC signals at the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the two MSBs of register PHALIGN.

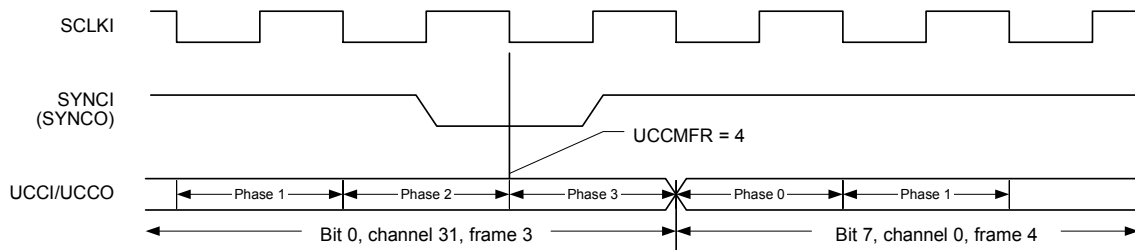
The configured frame and bit phase alignment always denotes the beginning of the ideal bit phase (no signal delay) at the falling edge of SCLKI. If SYNCI is sampled with the falling edge of SCLKI (CONFCC.SSCLKEDGE='0') this edge is the synchronization point for PCM and UCC signals. If SYNCI is sampled with the rising edge of SCLKI (CONFCC.SSCLKEDGE='1') the next falling SCLKI edge is the synchronization point for PCM and UCC signals. This behavior is identical to the PCM signal behavior and illustrated in [Figure 21](#) in [Chapter 4.2.1](#)

UCC inputs are always sampled with the falling edge of SCLKI at the beginning of bit phase 2, UCCO and  $\overline{\text{TUCCO}}$  are clocked out with the falling edge of SCLKI at the beginning of bit phase 0. The value of register UCCMFR denotes the frame number of the next complete frame that starts with phase 0, bit 7, channel 0 **after** the first detection of an active SYNCI with the falling edge of SCLKI (see figure below).

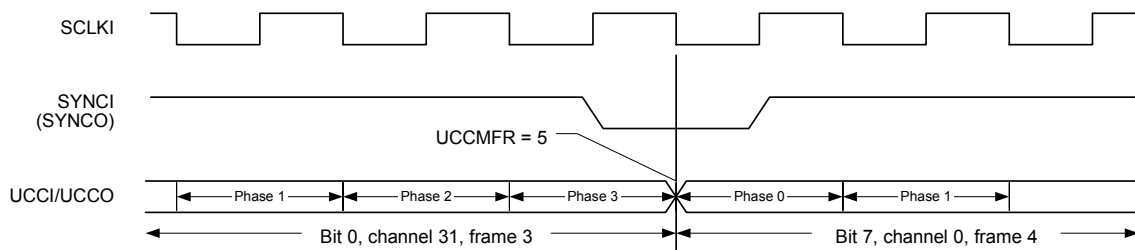
## Operational Description

### Special Cases for Multiframe Alignment

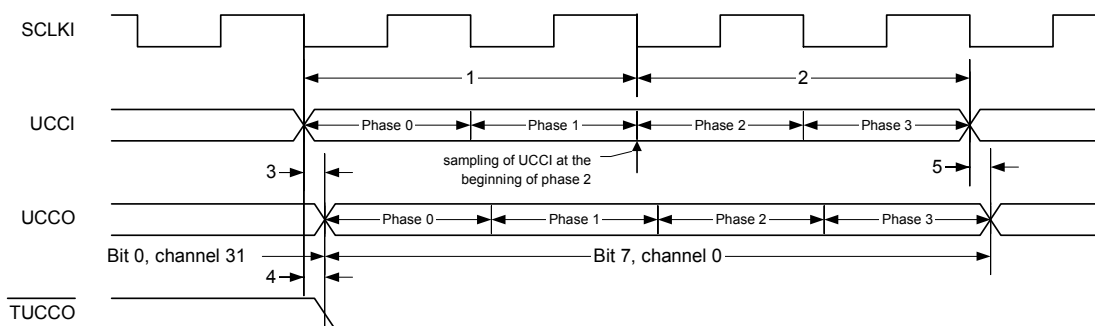
#### Case 1: SYNCI at channel 31, bit 0, phase 3



#### Case 2: SYNCI at channel 0, bit 7, phase 0



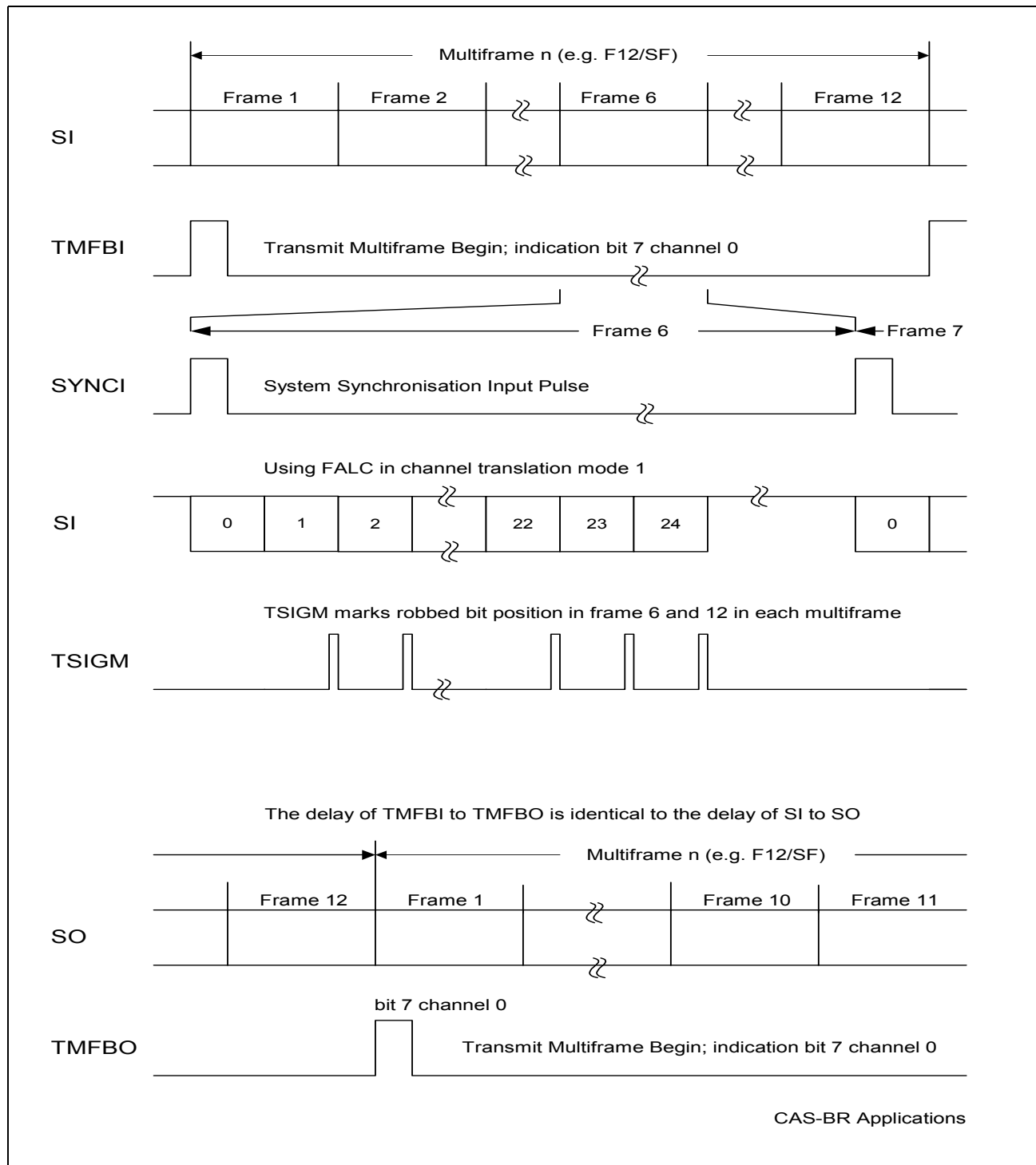
### Timing Characteristics



Special Case for Multiframe Alignment

**Figure 26 Special Cases for Multiframe Alignment and Timing Characteristics**

## 4.2.6 Speech Highway Control Signals for CAS in T1 Systems



**Figure 27 Timing of Supporting signals for CAS-BR Applications**

### 4.2.7 Microprocessor Interface

The SIDEC Microprocessor Interface supports both, Intel and Motorola mode. In each mode the address can be provided either through the multiplexed address/data or a parallel address bus. In multiplexed mode the address is always sampled with the falling edge of the address latch enable signal on the lower 7 bits of the multiplexed address/data bus. hence, addresses from 00H to 7FH are possible.

Read and write access in Intel mode is controlled by the assigned read and write signals. In Motorola mode it is provided by the data strobe and read/write signal.

The chip select signal is internally simply 'ored' with the read and write signal in Intel mode and with the data strobe signal in Motorola mode, thus enabling register access through chip select controlled Microprocessor cycles.

For fast processors there is also a ready/acknowledgment signal provided in order to eliminate the need for processor configured wait state insertion.

To write a value in a write protected register the value 95H needs to be written in the register Write Protection.

## 4.3 Operational functions overview

### 4.3.1 Adaptive filter function

The adaptive filtering algorithm implemented in the SIDEC is some derivative form of the normalized LMS (least mean square) adaptive algorithm that utilizes an adaptive step range.

### 4.3.2 Filter

The SIDEC filter consist of a full-tapped 511 step transversal filter that can be limited to shorter impulse responses/echo delays for increased quality.

The filter coefficients can be fully monitored through the P-Interface.

### 4.3.3 Filter coefficient adaptation

Other than with ordinary LMS algorithms the SIDEC the filter coefficients (H-register) do not get updated directly with a fixed update step size, but instead the patented adaptive algorithm of the SIDEC utilizes so called auxiliary coefficients that adaptively control the update step size of (main) coefficients. This yields a much more stable operation and allows for the implementation of an additional fast convergence (turbo) mode that results in rapid convergence even in the presence of double talk.

Please note that turbo mode is a status that is individual for each single coefficient. The turbo mode indicator (monitor) only shows that at least one coefficient update works in turbo mode.

#### **4.3.4 Stability / divergence protection**

##### **4.3.4.1 Coefficient damping**

A configurable damping feature of main and auxiliary coefficients increases the algorithmical stability even further, thus preventing possible divergence even in difficult situation.

##### **4.3.4.2 Auxiliary coefficient supervision**

In order to prevent misadaptation or sudden divergence the auxiliary coefficients can be monitored for conspicuous patterns and the main filter adaptation limited to smaller step sizes.

##### **4.3.4.3 Sinusoidal (non-voice) signal protection**

In order to prevent possible divergence or misadaptation due to the presence of a (dominant) periodical signal (an unfortunate vulnerability inherent to all LMS algorithms) a flexible non-voice detector is built in to SIDEDEC.

##### **4.3.4.4 Overcompensation protection**

SIDEDEC can detect if it produces more echo than it receives and control the adaptive algorithm accordingly.

##### **4.3.4.5 Low frequency RI superimposing**

Low frequency (sawtooth) or DC components can be superimposed to the receive in signal in order to increase the stability or even the adaptability to certain waveforms. This is a legacy feature and no longer needed for the adaptive step range algorithm.

#### **4.3.5 Non linear processing**

SIDEDEC has a unique highly configurable and flexible non linear processing capability that is highly integrated with adaptive filter functionality in order to suppress any noticeable residual echo in the case of no near end voice activity.

##### **4.3.5.1 Background noise measurement**

A quite elaborate and configurable function constantly monitors the near end background noise level.

##### **4.3.5.2 Background noise insertion**

SIDEDEC implements the ITU required NLP noise insertion settings plus one additional subjectively superior noise function with configurable adaptive signal levels.

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## Operational Description

In ITU comfort noise mode SIDEC inserts a white noise with a constant amplitude and sign generated by a PN-generator.

In the SIDEC unique subjective mode, SIDEC simply limits the outgoing SO signal to an amplitude defined by the adaptive background noise level.

### 4.3.5.3 NLP control

The NLP activation (background noise insertion instead of echo compensated near end signal) of the SIDEC is controlled through sophisticated functions by several conditions that are tightly coupled with the adaptive filtering function and double talk conditions. The user can control these functions through a multitude of configuration settings.

### 4.3.6 Double talk detection

SIDEC features a configurable multi-step double talk detection that is needed by several other functions of the device.

### 4.3.7 Voice activity detection

SIDEC can detect far and near end signal activity for controlling of the echo cancelling functionality.

### 4.3.8 Offset compensation

For optimization of the adaptive filter algorithm SIDEC removes DC components from the SO signal. This offset-compensation function is also applied to the SI-signal to ensure AC only level measurement.

### 4.3.9 Disable tone detection functions

SIDEC can be configured to several operational states on the detection of the following "disable" tone signals:

- 2100 Hz (G.164)
- 2100 Hz with phase reversal (G.165)
- 2000 Hz (SS7 continuity check tone)

All of the detectors for the above signal forms can be configured to the special needs of the implemented telecommunications system.

### 4.3.10 Other disable event detection functions

- Idle pattern detection (ITU confirming and flexibly configurable)
- TS16 evaluation (in E1 system)
- External serial signal (FLEXCTRL)
- Direct register control through the P-Interface.

## 4.4 Operational functions configuration

This sections shows you the correlation of the different SIDEC configuration registers settings with the SIDEC operational functions and the effect of the settings on these functions.

For further explanation or the exact values please refer to the detailed register description.

### 4.4.1 Adaptive filter function

The following tables give some more insight on the configuration options of the adaptive filters.

#### 4.4.1.1 Filter

**Table 28 Filter Parameter**

| Register | Addr. | Value | Mod. | Effect                                                                                                           |
|----------|-------|-------|------|------------------------------------------------------------------------------------------------------------------|
| AEPD     | 72H   | DELAY | Up   | increase the (end echo path) filter length                                                                       |
|          |       |       | Down | decrease the (end echo path) filter length                                                                       |
| ACONF    | 79H   | EMAF  | 0    | SIDEC works up to 0 dB echo attenuation                                                                          |
|          |       |       | 1    | SIDEC works up to 6 dB echo attenuation, granularity of the filter is doubled, quality of artificial echo better |

The transversal filter can be modified in length (amount of taps) and maximum coefficient value / granularity.

ACONF.EMAF set to 1 results in an additional attenuation of the artificial by 6 dB, thus the values of the coefficients are in bigger and the echo filter model more accurate.

#### 4.4.1.2 Filter coefficient Adaptation Speed

**Table 29 Filter coefficient adaptation speed adjustment**

| Register | Addr. | Value | Mod. | Effect                                                                          |
|----------|-------|-------|------|---------------------------------------------------------------------------------|
| AFSTC    | 71H   | ACSPT | Up   | decrease damping effect on aux. coef., convergence speed "Up", stability "Down" |
|          |       |       | Down | increase damping effect on aux. coef., convergence speed "Down", stability "Up" |
|          |       | CSPT  | Up   | decrease damping effect on main coef., convergence speed "Up", stability "Down" |

## Operational Description

**Table 29 Filter coefficient adaptation speed adjustment (cont'd)**

| Register | Addr. | Value | Mod. | Effect                                                                          |
|----------|-------|-------|------|---------------------------------------------------------------------------------|
|          |       |       | Down | increase damping effect on main coef., convergence speed "Down", stability "Up" |
| ATMAT    | 77H   | TURBO | Up   | convergence speed "Down", stability "Up"                                        |
|          |       |       | Down | convergence speed "Up", stability "Down"                                        |

Modification of the AFSTC has some dramatic effect on stability and convergence speed, be careful with those settings.

Modification of the turbo threshold is not as severe and a good means for algorithm fine-tuning.

The lower the turbo threshold the faster the turbo mode for the affected coefficient will be activated resulting in faster convergence.

### 4.4.1.3 Stability / divergence protection

For stability please see also the previous paragraph

**Table 30 Coefficient damping**

| Register | Addr. | Value     | Mod. | Effect                                   |
|----------|-------|-----------|------|------------------------------------------|
| AFSTC    | 71H   | ACSP<br>T | Up   | stability "Down", convergence speed "Up" |
|          |       |           | Down | stability "Up", convergence speed "Down" |
|          |       | CSPT      | Up   | stability "Down", convergence speed "Up" |
|          |       |           | Down | stability "Up", convergence speed "Down" |

**Table 31 Auxiliary coefficient supervision**

| Register | Addr. | Value  | Mod. | Effect                                                  |
|----------|-------|--------|------|---------------------------------------------------------|
| AACSC    | 78H   | ACSCTH | Up   | stability "Down", convergence speed "Up", if ACSCTH > 0 |
|          |       |        | Down | stability "Up", convergence speed "Down", if ACSCTH > 0 |
|          |       | ACSTH  | Up   | stability "Down", convergence speed "Up", if ACSCTH > 0 |
|          |       |        | Down | stability "Up", convergence speed "Down", if ACSCTH > 0 |

## Operational Description

**Table 31 Auxiliary coefficient supervision (cont'd)**

| Register | Addr. | Value         | Mod. | Effect                                                     |
|----------|-------|---------------|------|------------------------------------------------------------|
|          |       | ACSEFF<br>ECT | 0    | stability "Down", convergence speed "Up", if<br>ACSCTH > 0 |
|          |       |               | 1    | stability "Up", convergence speed "Down", if<br>ACSCTH > 0 |
| ATMAT    | 77H   | TURBO         | Up   | stability "Down", if AACSC.ACSCTH > 0                      |
|          |       |               | Down | stability "Up", if AACSC.ACSCTH > 0                        |

AACSC modifications mainly prevent misadaptation and divergence on periodical signals. The effect is not very strong but noticeable. Be careful not to unnecessarily activate the feature, since its effect on other functions has not been elaborately evaluated. The strongest setting for the AACSC register would be 84H and should be avoided. For fine-tuning play with the turbo-threshold. Lowering the turbo-threshold might increase convergence speed and stability if the auxiliary coefficient supervision feature is activated.

**Table 32 Sinusoidal (non-voice) signal protection**

| Register | Addr. | Value             | Mod. | Effect                                                    |
|----------|-------|-------------------|------|-----------------------------------------------------------|
| VDFCTRL  | 76H   | VDFRELEN          | 0    | stability "Down", ERLE "Up"                               |
|          |       |                   | 1    | stability "Up", ERLE "Down",                              |
|          |       | VDFREL            | Up   | stability "Down", ERLE "Up", if<br>VDFRELEN = 1           |
|          |       |                   | Down | stability "Up", ERLE "Down", if<br>VDFRELEN = 1           |
|          |       | VDFSOL            | Up   | stability "Down", ERLE "Up"                               |
|          |       |                   | Down | stability "Up", ERLE "Down"                               |
| AVDDI    | 77H   | VDMAXINTER<br>VAL | Up   | stability "Down", convergence speed<br>"Up", if activated |
|          |       |                   | Down | stability "Up", convergence speed<br>"Down", if activated |
|          |       | VDINTERVAL        | Up   | stability "Down", convergence speed<br>"Up", if activated |
|          |       |                   | Down | stability "Up", convergence speed<br>"Down", if activated |
| AVDHG    | 74H   | VDSODELAY         | Up   | stability "Up", convergence speed<br>"Down", if activated |

## Operational Description

**Table 32 Sinusoidal (non-voice) signal protection (cont'd)**

| Register     | Addr. | Value     | Mod. | Effect                                                 |
|--------------|-------|-----------|------|--------------------------------------------------------|
|              |       |           | Down | stability "Down", convergence speed "Up", if activated |
|              |       | VDDIFF    | Up   | stability "Up", convergence speed "Down", if activated |
|              |       |           | Down | stability "Down", convergence speed "Up", if activated |
| AVDCI        | 75H   | VDCI      | Up   | stability "Up", convergence speed "Down", if activated |
|              |       |           | Down | stability "Down", convergence speed "Up", if activated |
| CONFSCU<br>1 | 12H   | ADAPTFAST | Up   | ERLE "Down", NLP, DT detection slow                    |
|              |       |           | Down | ERLE "Up", NLP, DT detection slow                      |
|              |       | ADAPTSLOW | Up   | ERLE "Down", NLP, DT detection slow                    |
|              |       |           | Down | ERLE "Up", NLP, DT detection slow                      |

VDFCTRL defines the effects on the detection of a non-voice event. For stability reasons the adaptive algorithm should be frozen (VDFCTRL.VDFRELEN), when the echo attenuation reaches the specified level in VDFCTRL.VDFREL. Unfortunately this might lead to a locking of the adaptive algorithm, if the SIDEC has adapted to a periodical signal and the periodical signal changes its frequency, or if the SIDEC has momentarily misadapted to a periodical signal and the H-registers are frozen due to the reaching of the specified attenuation level and the presence of the periodical signal. In order to prevent this situation it is recommended to let the attenuation meters adapt slowly by modifying the ADAPTFAST and ADAPTSLOW values of the CONFSCU1 register and to set VDFCTRL.VDFREL to a high value in order to give the canceller the chance to converge better sufficiently well before getting frozen.

The AVDDI, AVDHG and AVDCI registers define the sensitivity and speed with which periodical signals are detected. Detection intervals longer than 64ms are not recommended in 128 ms mode in order to keep the H-register stable on sinusoidal signals. Be careful with sensitivity settings that are too aggressive since this might jeopardize your convergence speed and ERLE.

## Operational Description

**Table 33 Overcompensation protection**

| Register | Addr. | Value   | Mod. | Effect                          |
|----------|-------|---------|------|---------------------------------|
| CONFSCU4 | 15H   | OCINC   | Up   | OC detection sensitivity "Up"   |
|          |       |         | Down | OC detection sensitivity "Down" |
|          |       | OCDEC   | Up   | OC detection sensitivity "Down" |
|          |       |         | Down | OC detection sensitivity "Up"   |
|          |       | SIADD   | Up   | OC detection sensitivity "Down" |
|          |       |         | Down | OC detection sensitivity "Up"   |
|          |       | OCAMRES | 0    | OC detection effect "Down"      |
|          |       |         | 1    | OC detection effect "Up"        |
|          |       | OCHRES  | 0    | OC detection effect "Down"      |
|          |       |         | 1    | OC detection effect "Up"        |

SIDEC detects an overcompensation if the level of the supposedly echocancelled output signal SO is higher than the SI input signal level by an through CONFSCU4.SIADD configured amount for a sufficiently long period that can be configured through CONFSCU4.OCIND and CONFSCU4.OCDEC.

In case an overcompensation the effect can be configured with CONFSCU4. OCAMRES or CONFSCU4.OCHRES.

### Low frequency RI superimposing

Former implementations of the LMS algorithm without adaptive step ranging required superimposing of some low frequency components in the RI signals in order to limit the canceller degree of freedom in adapting to the end echo path, which resembles a bandpass filter.

With the introduction of the new adaptive step range algorithm this feature is no longer needed but still offered for legacy reasons. Please refer to the register description of the ASTOC register for details. It is recommended to keep this registers at it's default value 00H (feature disabled).

### 4.4.2 Non linear processing

The following tables will give some hint on the configuration of the non linear processor.

## Operational Description

**Table 34 Background noise measurement**

| Register | Addr. | Value    | Mod. | Effect                                                             |
|----------|-------|----------|------|--------------------------------------------------------------------|
| CONFSCU7 | 18H   | NOISEINC | Up   | comfort noise level "Up"                                           |
|          |       |          | Down | comfort noise level "Down"                                         |
|          |       | BNINC    | Up   | comfort noise level "Up", comfort noise level stability "Down"     |
|          |       |          | Down | comfort noise level "Down", comfort noise level stability "Up"     |
|          |       | BNDEC    | Up   | comfort noise level "Down", comfort noise level stability "Down"   |
|          |       |          | Down | comfort noise level "Up", comfort noise level stability "Up"       |
| CONFSCU8 | 19H   | BNMAXSL  | Up   | comfort noise level stability "Down", risk of level too low "Down" |
|          |       |          | Down | comfort noise level stability "Up", risk of level too low "Up"     |
|          |       | BNMAXRL  | Up   | comfort noise level stability "Down", risk of level too low "Down" |
|          |       |          | Down | comfort noise level stability "Up", risk of level too low "Up"     |

The final resulting inserted comfort noise level can be configured mainly by modifying the value CONFSCU7.NOISEINC.

Please keep in mind that ITU comfort noise will generate a constant amplitude signal, thus the inserted noise level will be generally 3dB higher than the measured level, it is recommended to set CONFSCU7.NOISEINC to 2H (-3dB) to compensate for this behavior.

In subjective mode the SO amplitude will simply be limited to the measured background noise level, in this case the measured level should be increased by 6dB (CONFSCU7.NOISEINC = 8H), which produced the subjectively best background noise signal. Please note that in this case the measured background noise level at the SO output heavily depends on the noise signal form that is inserted at SI.

CONFSCU7.BNINC and CONFSCU7.BNDEC can be modified for fine-tuning of the BN measurement. Any change has only little effect.

CONFSCU8. BNMAXSL and CONFSCU8. BNMAXRL only limit the range of the SI(SO) and RI signal levels for which background noise level measurement is enabled. If for example the level louder signal of SI or SO is higher than CONFSCU8. BNMAXSL the

## Operational Description

current signal is not considered to being a background noise and the background noise level measurement will be switched off.

CONFSCU8. BNMAXRL behaves the same way for the RI signal and may be lowered in order to reduce the effect of residual echo on the quality of the BN measurement.

**Table 35 Background noise insertion**

| Register | Addr. | Value             | Mod. | Effect                                              |
|----------|-------|-------------------|------|-----------------------------------------------------|
| CONFPCM  | 30H   | NLPITU            | 1    | ITU comfort noise (white noise, constant amplitude) |
|          |       |                   | 0    | subjective comfort noise (amplitude limited)        |
|          |       | NLPMOD            | 1    | ITU bandlimited noise with constant amplitude       |
|          |       | (if NLPITU = '1') | 0    | output level is 0 (dead line)                       |

Please see also the previous paragraph for details.

The above table shows what kind of signal can be configured to be inserted at SO in the case of NLP activation.

## 5 Register Description

### 5.1 Detailed Register Description

In the following section the meaning and addresses of the registers of the SDEC are described, The addresses and reset values are given in Hex-Code indicated by a subsequent capital H. A number '0' or '1' written in bold type denotes the reset value of the corresponding bit.

To write a value in a write protected register the value 95H needs to be written in the register Write Protection.

#### 5.1.1 Register Map

The following table lists all registers. The table displays the register name, the abbreviation, the reset value, the read/write mode and the page number with the detailed description. The registers are sorted by addresses.

| Addr | Short Name | Full name                                  | R/W | Res. value | page |
|------|------------|--------------------------------------------|-----|------------|------|
| 00H  | NOTEBOOK   | <b>Notebook</b>                            | R/W | 00H        | 83   |
| 01H  | WP         | <b>Write Protection</b>                    | W   | NOT 95H    | 85   |
| 02H  | WDG1       | <b>Watchdog 1</b>                          | W   |            | 85   |
| 03H  | WDG2       | <b>Watchdog 2</b>                          | W   |            | 86   |
| 04H  | WDG3       | <b>Watchdog 3</b>                          | W   |            | 86   |
| 05H  | UPIO       | μP-I/O-Pin extension                       | R/W | 0FH        | 83   |
| 06H  | PCMCTRL    | <b>PCM Bypass and loop Control</b>         | W   | 00H        | 86   |
| 07H  | IRMASK     | <b>Interrupt Mask</b>                      | W   | 7FH        | 85   |
| 08H  | IRREQ      | <b>Interrupt-Request</b>                   | R   |            | 118  |
| 09H  | CLKSTAT    | <b>Clock-Status</b>                        | R   |            | 118  |
| 0AH  | RAMBIST    | <b>RAMBIST</b>                             | R/W | 00H        | 83   |
| 0BH  | CONFCC     | <b>Configuration of Clock Control unit</b> | W   | 00H        | 109  |
| 0CH  | FSLPIV     | <b>Frame slip safety interval</b>          | W   | 28H        | 109  |
| 0DH  | RIALIGN    | <b>Receive input frame alignment</b>       | W   | 00H        | 110  |
| 0EH  | SIALIGN    | <b>Send input frame alignment</b>          | W   | 00H        | 110  |
| 0FH  | SOALIGN    | <b>Send output frame alignment</b>         | W   | 00H        | 110  |

## Register Description

| Addr | Short Name | Full name                                                      | R/W | Res. value | page |
|------|------------|----------------------------------------------------------------|-----|------------|------|
| 10H  | UCCALIGN   | <b>UCC</b> frame <b>alignment</b> ,write protected             | W   | 00H        | 111  |
| 11H  | PHALIGN    | Bit <b>Phase alignment</b> for RI, SI, SO and UCC              | W   | 00H        | 111  |
| 12H  | CONFSCU1   | <b>Configuration of speech control unit 1</b>                  | W   | 69H        | 101  |
| 13H  | CONFSCU2   | <b>Configuration of speech control unit 2</b>                  | W   | 97H        | 101  |
| 14H  | CONFSCU3   | <b>Configuration of speech control unit 3</b>                  | W   | A4H        | 102  |
| 15H  | CONFSCU4   | <b>Configuration of speech control unit 4</b>                  | W   | A7H        | 103  |
| 16H  | CONFSCU5   | <b>Configuration of speech control unit 5</b>                  | W   | 84H        | 103  |
| 17H  | CONFSCU6   | <b>Configuration of speech control unit 6</b>                  | W   | 2AH        | 104  |
| 18H  | CONFSCU7   | <b>Configuration of speech control unit 7</b>                  | W   | 8AH        | 104  |
| 19H  | CONFSCU8   | <b>Configuration of speech control unit 8</b>                  | W   | EEH        | 105  |
| 1AH  | CONFSCU9   | <b>Configuration of speech control unit 9</b>                  | W   | 44H        | 105  |
| 1BH  | CONFSCU10  | <b>Configuration of speech control unit 10</b>                 | W   | C0H        | 106  |
| 1CH  | CONFPSD    | <b>Configuration of 2100 Hz tone phase shift detector</b>      | W   | 43H        | 107  |
| 1DH  | CONFSS7    | <b>Configuration of SS7</b> continuity check tone detection    | W   | 00H        | 108  |
| 1EH  | MONSIL     | <b>Monitor send input level</b>                                | R   |            | 123  |
| 1FH  | MONSOL     | <b>Monitor send output leve</b>                                | R   |            | 123  |
| 20H  | MONRIL     | <b>Monitor of receive input level</b>                          | R   |            | 124  |
| 21H  | MONOFSI    | <b>Monitor offset in send path input</b>                       | R   |            | 124  |
| 22H  | MONOFSO    | <b>Monitor offset in send path output</b>                      | R   |            | 124  |
| 23H  | MONAEL     | <b>Monitor artificial echo level</b>                           | R   |            | 124  |
| 24H  | MONBNL     | <b>Monitor background noise level</b>                          | R   |            | 124  |
| 25H  | MONERL     | <b>Monitor Echo return loss</b>                                | R   |            | 125  |
| 26H  | MONCL      | <b>Monitor combined loss without NLP</b>                       | R   |            | 125  |
| 27H  | MONNLPTH   | <b>Monitor NLP threshold level</b>                             | R   |            | 125  |
| 28H  | MONOCDT    | <b>Monitor overcompensation and double talk hang-over time</b> | R   |            | 125  |

## Register Description

| Addr | Short Name  | Full name                                                         | R/W | Res. value | page |
|------|-------------|-------------------------------------------------------------------|-----|------------|------|
| 29H  | MONSI       | <b>Monitor send input signal</b> (A-/μ-Law encoded)               | R   |            | 122  |
| 2AH  | MONSO       | <b>Monitor send output signal</b> (A-/μ-Law encoded)              | R   |            | 122  |
| 2BH  | MONRI       | <b>Monitor of receive input signal</b> (A-/μ-Law encoded)         | R   |            | 122  |
| 2CH  | MONSTAT1    | <b>Monitor of internal/external control states 1</b>              | R   |            | 125  |
| 2DH  | MONSTAT2    | <b>Monitor of internal/external control states 2</b>              | R   |            | 126  |
| 2EH  | MONSTAT3    | <b>Monitor of internal/external control states 3</b>              | R   |            | 126  |
| 2FH  | CTRLTSMON   | <b>Control of TS to be monitored</b>                              | W   | 00H        | 84   |
| 30H  | CONFPCM     | Global <b>Configuration of PCM</b> outputs                        | W   | 03H        | 86   |
| 31H  | CONFTS16    | <b>Configuration of TS16 CAS</b><br>Evaluation for E1 frames      | W   | 12H        | 94   |
| 32H  | CONFIDLE    | <b>Configuration of IDLE</b> Detection                            | W   | 1DH        | 93   |
| 33H  | IDLEMASK    | <b>IDLE</b> detection bit compare <b>MASK</b>                     | W   | 00H        | 93   |
| 34H  | IDLEPATTERN | <b>Idlepattern</b>                                                | W   | 55H        | 94   |
| 35H  | ATE         | <b>Address of Test-channel</b>                                    | W   | 00H        | 98   |
| 36H  | SFATSES     | <b>Super frame alarm and requested timeslot en/disable status</b> | R   |            | 119  |
| 37H  | TESTTIMER   | μP <b>Test and Timer</b>                                          | W   | 00H        | 98   |
| 38H  | CTRLTEST    | <b>Control of test</b> channel                                    | W   | 00H        | 99   |
| 39H  | TSGSPP      | <b>Test signal generator for send path pattern</b>                | W   | 55H        | 99   |
| 3AH  | TSGRPP      | <b>Test signal generator for receive path pattern</b>             | W   | 55H        | 100  |
| 3BH  | HTIM        | <b>High-Byte for Timer</b>                                        | W   | 00H        | 100  |
| 3CH  | LTIM        | <b>Low-Byte for Timer</b>                                         | W   | 00H        | 101  |
| 3DH  | SOTP        | <b>Send path output test pattern</b>                              | R   |            | 119  |
| 3EH  | TESTSTAT    | Background <b>test status</b> signals                             | R   |            | 119  |

## Register Description

| Addr | Short Name | Full name                                              | R/W | Res. value | page |
|------|------------|--------------------------------------------------------|-----|------------|------|
| 3FH  | CONFLAW    | Global <b>configuration</b> of PCM encoding <b>law</b> | W   | 00H        | 87   |
| 40H  | CHCTRL0    | Individual <b>channel control 0</b>                    | W   | 00H        | 88   |
| 41H  | CHCTRL1    | Individual <b>channel control 1</b>                    | W   | 00H        | 88   |
| 42H  | CHCTRL2    | Individual <b>channel control 2</b>                    | W   | 00H        | 88   |
| 43H  | CHCTRL3    | Individual <b>channel control 3</b>                    | W   | 00H        | 88   |
| 44H  | CHCTRL4    | Individual <b>channel control 4</b>                    | W   | 00H        | 88   |
| 45H  | CHCTRL5    | Individual <b>channel control 5</b>                    | W   | 00H        | 88   |
| 46H  | CHCTRL6    | Individual <b>channel control 6</b>                    | W   | 00H        | 88   |
| 47H  | CHCTRL7    | Individual <b>channel control 7</b>                    | W   | 00H        | 88   |
| 48H  | CHCTRL8    | Individual <b>channel control 8</b>                    | W   | 00H        | 88   |
| 49H  | CHCTRL9    | Individual <b>channel control 9</b>                    | W   | 00H        | 88   |
| 4AH  | CHCTRL10   | Individual <b>channel control 10</b>                   | W   | 00H        | 88   |
| 4BH  | CHCTRL11   | Individual <b>channel control 11</b>                   | W   | 00H        | 88   |
| 4CH  | CHCTRL12   | Individual <b>channel control 12</b>                   | W   | 00H        | 88   |
| 4DH  | CHCTRL13   | Individual <b>channel control 13</b>                   | W   | 00H        | 88   |
| 4EH  | CHCTRL14   | Individual <b>channel control 14</b>                   | W   | 00H        | 88   |
| 4FH  | CHCTRL15   | Individual <b>channel control 15</b>                   | W   | 00H        | 88   |
| 50H  | CHCTRL16   | Individual <b>channel control 16</b>                   | W   | 00H        | 88   |
| 51H  | CHCTRL17   | Individual <b>channel control 17</b>                   | W   | 00H        | 88   |
| 52H  | CHCTRL18   | Individual <b>channel control 18</b>                   | W   | 00H        | 88   |
| 53H  | CHCTRL19   | Individual <b>channel control 19</b>                   | W   | 00H        | 88   |
| 54H  | CHCTRL20   | Individual <b>channel control 20</b>                   | W   | 00H        | 88   |
| 55H  | CHCTRL21   | Individual <b>channel control 21</b>                   | W   | 00H        | 88   |
| 56H  | CHCTRL22   | Individual <b>channel control 22</b>                   | W   | 00H        | 88   |
| 57H  | CHCTRL23   | Individual <b>channel control 23</b>                   | W   | 00H        | 88   |
| 58H  | CHCTRL24   | Individual <b>channel control 24</b>                   | W   | 00H        | 88   |
| 59H  | CHCTRL25   | Individual <b>channel control 25</b>                   | W   | 00H        | 88   |
| 5AH  | CHCTRL26   | Individual <b>channel control 26</b>                   | W   | 00H        | 88   |
| 5BH  | CHCTRL27   | Individual <b>channel control 27</b>                   | W   | 00H        | 88   |

## Register Description

| Addr | Short Name    | Full name                                                              | R/W | Res. value | page |
|------|---------------|------------------------------------------------------------------------|-----|------------|------|
| 5CH  | CHCTRL28      | Individual <b>channel control 28</b>                                   | W   | 00H        | 88   |
| 5DH  | CHCTRL29      | Individual <b>channel control 29</b>                                   | W   | 00H        | 88   |
| 5EH  | CHCTRL30      | Individual <b>channel control 30</b>                                   | W   | 00H        | 88   |
| 5FH  | CHCTRL31      | Individual <b>channel control 31</b>                                   | W   | 00H        | 88   |
| 60H  | CONFUCC       | <b>Configuration of UCC Interface</b>                                  | W   | 00H        | 94   |
| 61H  | UCCMFR        | <b>UCC Multiframe Alignment</b>                                        | W   | 00H        | 96   |
| 62H  | UCCFRS        | Selection of the special <b>UCC Frame FRS</b>                          | W   | 00H        | 96   |
| 63H  | WRUCC         | <b>Write/Read UCCI</b>                                                 | W   | 00H        | 97   |
| 64H  | DORAM         | <b>Data Output RAM</b>                                                 | W   | 00H        | 97   |
| 65H  | IMASKFRS      | <b>Interrupt Mask</b> for the special UCC frame <b>FRS</b>             | W   | 00H        | 97   |
| 66H  | IMASKFRN      | <b>Interrupt Mask</b> for channel individual UCC frames ( <b>FRN</b> ) | W   | 00H        | 98   |
| 67H  | DIRAM         | requested <b>Data Input RAM</b> value                                  | R   |            | 120  |
| 68H  | UCCOLD        | Changed <b>UCC</b> input data <b>old</b> value                         | R   |            | 120  |
| 69H  | UCCNEW        | Changed <b>UCC</b> input data <b>new</b> value                         | R   |            | 120  |
| 6AH  | UCCSTAT       | <b>UCC status</b>                                                      | R   |            | 120  |
| 6BH  | SCMASK        | <b>Serial Control Interface Mask</b>                                   | W   | 3FH        | 90   |
| 6CH  | CONFFLEX SCTR | <b>Configuration of the flexible serial control signal</b>             | W   | 00H        | 90   |
| 6DH  | CONFFLEXUCC   | <b>Configuration of the flexible UCC control bit (FX-Bit)</b>          | W   | 00H        | 91   |
| 6EH  | STATUS        | <b>Status</b>                                                          | R   |            | 118  |
| 6FH  | CONFFLEXMON   | <b>Configuration of Flexible Monitor Signals</b>                       | W   | FEH        | 91   |
| 70H  | ASTOC         | <b>AFI Saw-Tooth and Offset Characteristic</b>                         | W   | 00H        | 111  |
| 71H  | AFSTC         | <b>AFI Filter Spring Timer Configuration</b>                           | W   | 44H        | 112  |
| 72H  | AEEPDP        | <b>AFI End Echo Path Delay</b>                                         | W   | 0FH        | 112  |
| 73H  | AVDDI         | <b>AFI Voice Detection, Detection Intervals</b>                        | W   | 77H        | 113  |

## Register Description

| Addr | Short Name | Full name                                                  | R/W | Res. value | page |
|------|------------|------------------------------------------------------------|-----|------------|------|
| 74H  | AVDHG      | <b>AFI Voice Detection, Hysteresis and Gap</b>             | W   | 74H        | 114  |
| 75H  | AVDCI      | <b>AFI Voice Detection Count Init</b>                      | W   | 85H        | 115  |
| 76H  | VDFCTRL    | <b>Voice Detection Freeze Control</b>                      | W   | B4H        | 107  |
| 77H  | ATMAT      | <b>AFI Turbo Mode Activation Threshold</b>                 | W   | 08H        | 115  |
| 78H  | AACSC      | <b>AFI Auxiliary Coefficient Supervision Configuration</b> | W   | 00H        | 115  |
| 79H  | ACONF      | <b>AFI Configuration</b>                                   | W   | 10H        | 116  |
| 7AH  | AFCMC      | <b>AFI Filter Coefficients Monitoring Control</b>          | W   | 00H        | 117  |
| 7BH  | AFCD1      | <b>AFI Filter Coefficient Data 1</b>                       | R   |            | 121  |
| 7CH  | AFCD2      | <b>AFI Filter Coefficient Data 2</b>                       | R   |            | 121  |
| 7DH  | AFCD3      | <b>AFI Filter Coefficient Data 3</b>                       | R   |            | 122  |

## Register Description

### 5.1.2 Read-Write-Register

**NOTEBOOK[7:0]** (Addr.: 00H): **Notebook**, write protected, Reset value = 00H

| NOTE<br>BOOK[7] | NOTE<br>BOOK[6] | NOTE<br>BOOK[5] | NOTE<br>BOOK[4] | NOTE<br>BOOK[3] | NOTE<br>BOOK[2] | NOTE<br>BOOK[1] | NOTE<br>BOOK[0] |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

NOTEBOOK[7:0] Read/Write register for testing of the  $\mu$ P interface, content without effect, write protected

**UPIO[7:0]** (Addr.: 05H):  **$\mu$ P-I/O-Pin extension**, Reset value = 0FH

| UPIO3 | UPIO2 | UPIO1 | UPIO0 | TUPIO3 | TUPIO2 | TUPIO1 | TUPIO0 |
|-------|-------|-------|-------|--------|--------|--------|--------|
|-------|-------|-------|-------|--------|--------|--------|--------|

|        |                                                                                         |  |  |  |  |  |  |
|--------|-----------------------------------------------------------------------------------------|--|--|--|--|--|--|
| UPIO3  | If TUPIO3='1': Value from Pin UPIO3<br>If TUPIO3='0': Value that is output at Pin UPIO3 |  |  |  |  |  |  |
| UPIO2  | If TUPIO2='1': Value from Pin UPIO2<br>If TUPIO2='0': Value that is output at Pin UPIO2 |  |  |  |  |  |  |
| UPIO1  | If TUPIO1='1': Value from Pin UPIO1<br>If TUPIO1='0': Value that is output at Pin UPIO1 |  |  |  |  |  |  |
| UPIO0  | If TUPIO0='1': Value from Pin UPIO0<br>If TUPIO0='0': Value that is output at Pin UPIO0 |  |  |  |  |  |  |
| TUPIO3 | Tristate control for Pin UPIO3<br>'1': Pin UPIO3 is input<br>'0': Pin UPIO3 is output   |  |  |  |  |  |  |
| TUPIO2 | Tristate control for Pin UPIO2<br>'1': Pin UPIO2 is input<br>'0': Pin UPIO2 is output   |  |  |  |  |  |  |
| TUPIO1 | Tristate control for Pin UPIO1<br>'1': Pin UPIO1 is input<br>'0': Pin UPIO1 is output   |  |  |  |  |  |  |
| TUPIO0 | Tristate control for Pin UPIO0<br>'1': Pin UPIO0 is input<br>'0': Pin UPIO0 is output   |  |  |  |  |  |  |

**RAMBIST[5:0]** (Addr.: 0AH): **RAM BIST**, write protected, Reset value = 00H

| - | - | RUN<br>BIST | CUFAIL | AFI3<br>FAIL | AFI2<br>FAIL | AFI1<br>FAIL | AFI0<br>FAIL |
|---|---|-------------|--------|--------------|--------------|--------------|--------------|
|---|---|-------------|--------|--------------|--------------|--------------|--------------|

RUNBIST '1': set by  $\mu$ P: activates RAMBIST and signals running RAMBIST  
'0': set by hardware: signals that RAMBIST is finished (not running),

## Register Description

|          |                                                                                                                                                   |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------|
|          | the value RESULT is valid, if the RAMBIST was activated before                                                                                    |
| CUFAIL   | '1': RAMBIST of central unit failed, i.e. a RAM error was detected<br>'0': RAMBIST of central unit succesful: no error in RAM                     |
| AFI3FAIL | '1': RAMBIST of adaptive filter unit 3 failed, i.e. a RAM error was detected<br>'0': RAMBIST of adaptive filter unit 3 succesful: no error in RAM |
| AFI2FAIL | '1': RAMBIST of adaptive filter unit 2 failed, i.e. a RAM error was detected<br>'0': RAMBIST of adaptive filter unit 2 succesful: no error in RAM |
| AFI1FAIL | '1': RAMBIST of adaptive filter unit 1 failed, i.e. a RAM error was detected<br>'0': RAMBIST of adaptive filter unit 1 succesful: no error in RAM |
| AFI0FAIL | '1': RAMBIST of adaptive filter unit 0 failed, i.e. a RAM error was detected<br>'0': RAMBIST of adaptive filter unit 0 succesful: no error in RAM |

The bits CUFAIL, AFI3FAIL, AFI2FAIL, AFI1FAIL and AFI0FAIL are read only.

### 5.1.3 Write Register

All Write Registers are Write Only Registers and cannot be read out.

**CTRLTSMON[6:0]** (Addr.: 2FH): **Control of TS** to be **monitored**, Reset value = 00H

|   |              |      |        |        |        |        |        |
|---|--------------|------|--------|--------|--------|--------|--------|
| - | SNAP<br>SHOT | MVAL | MCH[4] | MCH[3] | MCH[2] | MCH[1] | MCH[0] |
|---|--------------|------|--------|--------|--------|--------|--------|

|          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SNAPSHOT | '1': Values of the monitor registers are only updated after writing to this register with MVAL set to '1'. The data remains stored in the monitor registers. An interrupt is generated as soon as the monitor values are valid. STATUS.TSMPOLL is cleared only when a new request is started by access to MVAL.<br>'0': Values of the monitor registers are continuously updated (each time the timeslot MCH[4:0] is detected) if MVAL = '1'.<br>An interrupt is generated only once and as soon as data becomes available in the monitor registers. |
| MVAL     | '0': resets the interrupt condition for TSMPOLL in the STATUS register. Stops updating of values if SNAPSHOT = '0'<br>'1': starts request for monitoring of the timeslot defined by MCH[4:0].                                                                                                                                                                                                                                                                                                                                                        |
| MCH[4:0] | selects the timeslot (channel) to be monitored                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

If MVAL = '1' the Monitor Read Registers are filled with the values of timeslot MCH[4:0] as soon as this timeslot is processed. The availability of the monitored values in the Monitor Read Registers is indicated by setting the bit IRREQ.TSM and STATUS.TSM.

## Register Description

**WP[7:0]** (Addr.: 01H) **Write Protection**, Reset Value 'protected'= NOT 95H

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WP[7] | WP[6] | WP[5] | WP[4] | WP[3] | WP[2] | WP[1] | WP[0] |
|-------|-------|-------|-------|-------|-------|-------|-------|

WP[7:0] Write access to the write protected configuration registers is released by writing the value 95H to this register. The write protection is activated by writing any other value.

**IRMASK[6:0]** (Addr.: 07H) **Interrupt Mask**, Reset Value = 7FH

|   |           |            |         |         |         |          |          |
|---|-----------|------------|---------|---------|---------|----------|----------|
| - | WDOG MASK | SYNCl MASK | CA MASK | TT MASK | TE MASK | UCC MASK | TSM MASK |
|---|-----------|------------|---------|---------|---------|----------|----------|

If an interrupt source is masked the information is shown in the STATUS register but not in the IRREQ register. Masking and unmasking does not affect the interrupt source. A new interrupt will be generated after masking and unmasking, if interrupt source is active (as indicated in STATUS register).

WDOGMASK '1': Watchdog condition does not cause an interrupt  
'0': normal operation

SYNClMASK '1': Incorrect SYNCl pulse does not cause an interrupt  
'0': normal operation

CAMASK '1': coefficient available is ignored  
'0': normal operation

TTMASK '1': test termination is ignored  
'0': normal operation

TEMASK '1': timer expired is ignored  
'0': normal operation

UCCMASK '1': UCC interrupt is ignored  
'0': normal operation

TSMMASK '1': timeslot monitor values available is ignored  
'0': normal operation

**WDG1[7:0]** (Addr.: 02H) **Watchdog 1**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| WDG1[7] | WDG1[6] | WDG1[5] | WDG1[4] | WDG1[3] | WDG1[2] | WDG1[1] | WDG1[0] |
|---------|---------|---------|---------|---------|---------|---------|---------|

WDG1[7:0] For watchdog test: Must be written with the defined value AAH as the first of the three watchdog registers within 2 seconds

## Register Description

### WDG2[7:0] (Addr.: 03H) Watchdog 2

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| WDG2[7] | WDG2[6] | WDG2[5] | WDG2[4] | WDG2[3] | WDG2[2] | WDG2[1] | WDG2[0] |
|---------|---------|---------|---------|---------|---------|---------|---------|

WDG2[7:0] For watchdog test: Must be written with the defined value 99H as the second of the three watchdog registers within 2 seconds

### WDG3[7:0] (Addr.: 04H) Watchdog 3

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| WDG3[7] | WDG3[6] | WDG3[5] | WDG3[4] | WDG3[3] | WDG3[2] | WDG3[1] | WDG3[0] |
|---------|---------|---------|---------|---------|---------|---------|---------|

WDG3[7:0] For watchdog test: Must be written with the defined value 1DH as the last of the three watchdog registers within 2 seconds

**PCMCTRL[3:0]** (Addr.: 06H) **PCM** Bypass and loop **Control**, write protected, Reset value = 00H

|   |   |   |   |            |            |             |             |
|---|---|---|---|------------|------------|-------------|-------------|
| - | - | - | - | SR<br>LOOP | RS<br>LOOP | R<br>BYPASS | S<br>BYPASS |
|---|---|---|---|------------|------------|-------------|-------------|

SRLOOP '1': Enables the internal loop from SO signal to RI signal

'0': Normal operation

RSLOOP '1': Enables the internal loop from RO signal to SI signal

'0': Normal operation

RBYPASS '1': Bypasses the RI input directly to the RO output

'0': Normal operation

SBYPASS '1': Bypasses the SI input directly to the SO output

'0': Normal operation

Note: If SRLOOP='1' and RSLOOP='1' only RSLOOP becomes active.

**CONFPCM[7:0]** (Addr.: 30H): Global **Configuration** of **PCM** outputs, write protected, Reset value = 03H

|            |            |             |              |             |              |            |                |
|------------|------------|-------------|--------------|-------------|--------------|------------|----------------|
| NLP<br>ITU | NLP<br>MOD | SOATT<br>EN | SOATT<br>MOD | ROATT<br>EN | ROATT<br>MOD | DYN<br>SUB | INVERR<br>SIGN |
|------------|------------|-------------|--------------|-------------|--------------|------------|----------------|

NLPITU '1': NLP comfort noise according to ITU

'0': NLP comfort noise subjective

NLPMOD only if NLPITU = '1': '1': output signal is band limited noise

'0': output signal is zero, i.e. line is dead

SOATTEN '1': Attenuation of send path output enabled and controlled by echo

## Register Description

|            |                                                                                                                                                                                                                                             |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|            | canceller en/disable                                                                                                                                                                                                                        |
| SOATTMOD   | '0': Attenuation of send path output is disabled for all channels<br>'1': Attenuation of send path output is 2.5 dB if enabled                                                                                                              |
| ROATTEN    | '0': Attenuation of send path output is 6 dB if enabled<br>'1': Attenuation of receive path output enabled and controlled by echo canceller en/disable                                                                                      |
| ROATTMOD   | '0': Attenuation of receive path output is disabled for all channels<br>'1': Attenuation of receive path output is 2.5 dB if enabled                                                                                                        |
| DYNSUB     | '0': Attenuation of receive path output is 6 dB if enabled<br>'1': The subtractor dynamically attenuates the send output signal if difference is derived from large signal levels                                                           |
| INVERRSIGN | '0': The subtractor operates in linear mode<br>'1': Sign of error signal (Echo + Near end speech) is inverted (normal operation)<br>'0': Sign of error signal (Echo + Near end speech) is not inverted (incorrect operation, for test only) |

**CONFLAW[3:0]** (Addr.: 3FH): Global **configuration** of PCM encoding **law**, write protected, Reset value = 00H

|   |   |   |   |       |                 |             |             |
|---|---|---|---|-------|-----------------|-------------|-------------|
| - | - | - | - | CHIND | GCONV<br>DISLAW | GALAW<br>NE | GALAW<br>FE |
|---|---|---|---|-------|-----------------|-------------|-------------|

For explanation of A/ $\mu$ -Law Conversion functions see also [Figure 10](#).

|             |                                                                                                                                                                                                                                                                                                                                        |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CHIND       | '1': Enables individual PCM encoding law settings for each channel by bits 7 to 5 of the individual control registers CHCTRL 0 to 31<br>'0': Enables global PCM encoding law configuration for all channels by bits 2 to 0 of this register                                                                                            |
| GCONVDISLAW | Determines the valid PCM law if the PCM-Law conversion of an individual channel is disabled by any source ( $\mu$ P, UCC or serial control signal) if CHIND = '0'<br>'1': All PCM channels for which conversion is disabled are A-Law en/decoded*<br>'0': All PCM channels for which conversion is disabled are $\mu$ -Law en/decoded* |
| GALAWNE     | Allows global configuration of near end PCM-Law:<br>'1': A-Law PCM encoding at near end side (RO and SI) if CHIND = '0' and CONVDIS = '0'<br>'0': $\mu$ -Law PCM encoding at near end side (RO and SI) if CHIND = '0' and CONVDIS = '0'                                                                                                |
| GALAWFE     | Allows global configuration of far end PCM-Law:<br>'1': A-Law PCM encoding at far end side (RI and SO)                                                                                                                                                                                                                                 |

## Register Description

if CHIND = '0' and CONVDIS = '0'  
 '0':  $\mu$ -Law PCM encoding at far end side (RI and SO)  
 if CHIND = '0' and CONVDIS = '0'

\*Note: In the case of no A-/ $\mu$ -Law conversion (same law at near and far end side) the PCM encoding law can temporarily be changed by any conversion disabling source ( $\mu$ P, UCC FX-Bit or serial control signal) if GCONVDISLAW is different from GALAWNE/GALAWFE.

**CHCTRL0-31[7:0]** (Addr.: 40H-5FH): Individual **channel control**, write protected, Reset value = 00H

| ICONV<br>DISLAW | IALAW<br>NE | IALAW<br>FE | CONV<br>DIS | FREEZE | NLPDIS | DIS<br>ABLE | ENP<br>CTRL |
|-----------------|-------------|-------------|-------------|--------|--------|-------------|-------------|
|-----------------|-------------|-------------|-------------|--------|--------|-------------|-------------|

The upper three bits ICONVDISLAW, IALAWNE and IALAWFE are only enabled if CONFLAW.CHIND = '1'. For explanation of law conversion see also [Figure 10](#).

|             |                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ICONVDISLAW | Determines the valid PCM-law of the corresponding channel if the PCM-Law conversion for this channel is disabled (CONVDIS = '1') and channel individual settings are enabled (Bit CONFLAW.CHIND = '1')<br>'1': The corresponding PCM channel is A-Law en/decoded if conversion is disabled*<br>'0': The corresponding PCM channel is $\mu$ -Law en/decoded if conversion is disabled* |
| IALAWNE     | '1': The corresponding PCM channel is A-Law PCM en/decoded at the near end side (RO and SI) if CONFLAW.CHIND = '1' and CONVDIS = '0'<br>'0': The corresponding PCM channel is $\mu$ -Law PCM en/decoded at the near end side (RO and SI) if CONFLAW.CHIND = '1' and CONVDIS = '0'                                                                                                     |
| IALAWFE     | '1': The corresponding PCM channel is A-Law PCM en/decoded at the far end side (RI and SO) if CONFLAW.CHIND = '1' and CONVDIS = '0'<br>'0': The corresponding PCM channel is $\mu$ -Law PCM en/decoded at the far end side (RI and SO) if CONFLAW.CHIND = '1' and CONVDIS = '0'                                                                                                       |
| CONVDIS     | '1': Disables the PCM Law conversion (GALAWNE, GALAWFE, IALAWNE, IALAWFE) for the corresponding channel. The valid encoding Law for this channel is determined by the values of the Bits ICONVDISLAW of this register if channel individual settings are configured (CHIND = '1') or the settings of the global register CONFLAW.GCONVDISLAW, if global configuration is configured   |

## Register Description

|         |                                                                                                                                                                                                                                                                                                         |
|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|         | (CHIND = '0').                                                                                                                                                                                                                                                                                          |
| FREEZE  | '0': Possible PCM Law conversion is enabled if Bit ENPCTRL = '1', Law conversion on/off depends on other hardware sources (serial control signals, UCC) if ENPCTRL = '0'.                                                                                                                               |
|         | '1': The H-register of the corresponding channel are frozen                                                                                                                                                                                                                                             |
| NLPDIS  | '0': The freezing of the H-Register for the corresponding channel depends on the internal control of the speech control unit only if ENPCTRL = '1', Freezing of H-Registers for the corresponding channel also depends on other hardware sources (serial control signals) if ENPCTRL = '0'.             |
|         | '1': The NLP of the corresponding channel is bypassed                                                                                                                                                                                                                                                   |
| DISABLE | '0': The bypass of the NLP for the corresponding channel depends on the internal control of the speech control unit only if ENPCTRL = '1', The bypassing of the NLP for the corresponding channel also depends on other hardware sources (serial control signals) if ENPCTRL = '0'.                     |
|         | '1': The entire echo canceling path (subtractor, NLP, attenuator in send and receive path) of the corresponding channel is bypassed and the H-Register and Speech Control Unit are reset.                                                                                                               |
| ENPCTRL | '0': The disabling (bypass) of the entire canceler for the corresponding channel depends on the internal control of the speech control unit only if ENPCTRL = '1', The disabling (bypass) of the entire canceler for the corresponding channel also depends on other hardware sources if ENPCTRL = '0'. |
|         | '1': Only the settings of the bits CONVDIS, FREEZE, NLPDIS, DISABLE are valid for the corresponding channel. All other hardware control sources (serial control signals, UCC, TS16, IDLE detection) for the corresponding channel are disabled.                                                         |
|         | '0': The settings of the bits CONVDIS, FREEZE, NLPDIS, DISABLE for the corresponding channel are 'ored' with other hardware control sources (serial control signals, UCC, TS16, IDLE detection).                                                                                                        |

\*Note: In the case of no A-/μ-Law conversion (same Law at near and far end side) the PCM encoding law can temporarily be changed by any conversion disabling source (μP, UCC FX-Bit or serial control signal) if ICONVDISLAW is different from IALAWNE/IALAWFE

## Register Description

**SCMASK[5:0]** (Addr.: 6BH): **S**erial **C**ontrol Interface **M**ask, write protected,  
Reset value = 3FH

|   |   |             |                |                |                     |              |                      |
|---|---|-------------|----------------|----------------|---------------------|--------------|----------------------|
| - | - | DIS<br>MASK | NLPDIS<br>MASK | FREEZE<br>MASK | CONV<br>DIS<br>MASK | ENCC<br>MASK | FLEX<br>SCTR<br>MASK |
|---|---|-------------|----------------|----------------|---------------------|--------------|----------------------|

This register is for masking of external pins of the Serial Interface. The effect of this register depends also on the value of CHCTRL0..31.ENPCTRL.

|              |                                                                                                           |
|--------------|-----------------------------------------------------------------------------------------------------------|
| DISMASK      | '1': serial control signal at pin DIS disabled<br>'0': serial control signal at pin DIS enabled           |
| NLPDISMASK   | '1': serial control signal at pin NLPDIS disabled<br>'0': serial control signal at pin NLPDIS enabled     |
| FREEZEMASK   | '1': serial control signal at pin FREEZE disabled<br>'0': serial control signal at pin FREEZE enabled     |
| CONVDISMASK  | '1': serial control signal at pin CONVDIS disabled<br>'0': serial control signal at pin CONVDIS enabled   |
| ENCCMASK     | '1': serial control signal at pin ENCC disabled<br>'0': serial control signal at pin ENCC enabled         |
| FLEXSCTRMASK | '1': serial control signal at pin FLEXSCTR disabled<br>'0': serial control signal at pin FLEXSCTR enabled |

**CONFFLEXSCTR[5:0]** (Addr.: 6CH): **C**onfiguration of the **f**lexible **s**erial **c**ontrol signal, write protected, Reset value = 00H

|   |   |              |              |              |                    |              |                   |
|---|---|--------------|--------------|--------------|--------------------|--------------|-------------------|
| - | - | FS<br>BYPASS | FS<br>NLPDIS | FS<br>FREEZE | FS<br>SCU<br>RESET | FS<br>HRESET | FS<br>CONV<br>DIS |
|---|---|--------------|--------------|--------------|--------------------|--------------|-------------------|

This register determines the function of pin FLEXSCTR if bit SCMASK.FLEXSCTRMASK = '0'

|            |                                                                                                                                                                                                                                                        |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FSBYPASS   | '1': serial control signal at pin FLEXSCTR leads to bypassing of the PCM signal of the entire cancelling path (canceller ,NLP, attenuator and bypassing of the attenuator in the receive path)<br>'0': No bypass of the entire compensator by FLEXSCTR |
| FSNLPDIS   | '1': serial control signal at pin FLEXSCTR disables the NLP and attenuator<br>'0': No disabling of the NLP and attenuator by FLEXSCTR                                                                                                                  |
| FSFREEZE   | '1': serial control signal at pin FLEXSCTR freezes the H-Register<br>'0': No freeze of the H-Register by FLEXSCTR                                                                                                                                      |
| FSSCURESET | '1': serial control signal at pin FLEXSCTR resets the attenuation meters in the speech control unit                                                                                                                                                    |

## Register Description

|           |                                                                                                                                                                                                               |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FSHRESET  | '0': No reset of the attenuation meters unit by FLEXSCTR<br>'1': serial control signal at pin FLEXSCTR resets the H-Register                                                                                  |
| FSCONVDIS | '0': No reset of the H-Register by FLEXSCTR<br>'1': serial control signal at pin FLEXSCTR disables the PCM-Law conversion (in receive and send path)<br>'0': No disable of the PCM-Law conversion by FLEXSCTR |

**CONFLEXUCC[5:0]** (Addr.: 6DH): **Configuration of the flexible UCC control bit (FX-Bit)**, write protected, Reset value = 00H

|   |   |              |              |              |                    |              |                   |
|---|---|--------------|--------------|--------------|--------------------|--------------|-------------------|
| - | - | FU<br>BYPASS | FU<br>NLPDIS | FU<br>FREEZE | FU<br>SCU<br>RESET | FU<br>HRESET | FU<br>CONV<br>DIS |
|---|---|--------------|--------------|--------------|--------------------|--------------|-------------------|

This register determines the function of the FX-Bit of the UCC signal. The FX bit is defined in register CONUCC.SELFX.

|            |                                                                                                                                                                                                    |
|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FUBYPASS   | '1': The FX-Bit leads to bypassing of the PCM signal of the entire cancelling path (canceller, NLP, attenuator in receive and send path)<br>'0': No bypass of the entire compensator by the FX-Bit |
| FUNLPDIS   | '1': THE FX-Bit disables the NLP and attenuator<br>'0': No disabling of the NLP and attenuator by the FX-Bit                                                                                       |
| FUFREEZE   | '1': THE FX-Bit freezes the H-Register<br>'0': No freeze of the H-Register by the FX-Bit                                                                                                           |
| FUSCURESET | '1': THE FX-Bit resets the attenuation meters in the speech controlling unit<br>'0': No reset of the attenuation meters by the FX-Bit                                                              |
| FUHRESET   | '1': THE FX-Bit resets the H-Register<br>'0': No reset of the H-Register by the FX-Bit                                                                                                             |
| FUCONVDIS  | '1': THE FX-Bit disables the PCM-Law conversion (in receive and send path)<br>'0': No disable of the PCM-Law conversion by the FX-Bit                                                              |

Note: Clear channel (64 clear) control by the FX-Bit can be enabled by setting this register to "xx1xxx1"

**CONFLEXMON[7:0]** (Addr.: 6FH): **Configuration of Flexible Monitor Signals**, Reset value = FEH

|                         |                         |                         |                         |                         |                         |                         |                         |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| CONF<br>FLEX<br>MON1[3] | CONF<br>FLEX<br>MON1[2] | CONF<br>FLEX<br>MON1[1] | CONF<br>FLEX<br>MON1[0] | CONF<br>FLEX<br>MON2[3] | CONF<br>FLEX<br>MON2[2] | CONF<br>FLEX<br>MON2[1] | CONF<br>FLEX<br>MON2[0] |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|

## Register Description

The bits CONFFLEXMON1[3:0] and CONFFLEXMON2[3:0] configure the serial control signals FLEXMON1 and FLEXMON2, respectively.

CONFFLEXMON1[3:0] / CONFFLEXMON2[3:0]

Configuration of the flexible monitor output signal at pin FLEXMON1/  
FLEXMON2

|         |                                                                                                                                                                 |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| "0000": | Idle channel detected is monitored at pin FLEXMON1 / FLEXMON2                                                                                                   |
| "0001": | 2010 Hz speech protection: first level reached (bypass of entire canceller) is monitored at pin FLEXMON1 / FLEXMON2                                             |
| "0010": | 2010 Hz speech protection: second level reached (H-Register reset) is monitored at pin FLEXMON1                                                                 |
| "0011": | 2010 Hz (SS Nr.7) detected but without speech protection is monitored at pin FLEXMON1 / FLEXMON2                                                                |
| "0100": | Convergence stability protection for non-speech signals active is monitored at pin FLEXMON1 / FLEXMON2                                                          |
| "0101": | Fast convergence mode active is monitored at pin FLEXMON1 / FLEXMON2                                                                                            |
| "0110": | Near end subscriber is louder than the far end subscriber (true double talk) is monitored at pin FLEXMON1 / FLEXMON2                                            |
| "0111": | Subtractor bypassed because ERL > value of BYPTH[4:0] is monitored at pin FLEXMON1 / FLEXMON2                                                                   |
| "1000": | 2100 Hz with phase shift and speech protection detected is monitored at pin FLEXMON1 / FLEXMON2                                                                 |
| "1001": | 2100 Hz detected with speech protection is monitored at pin FLEXMON1 / FLEXMON2                                                                                 |
| "1010": | 2100 Hz detected but without speech protection is monitored at pin FLEXMON1 / FLEXMON2                                                                          |
| "1011": | "No-voice" detected is monitored at pin FLEXMON1 / FLEXMON2                                                                                                     |
| "1100": | RITESTDATA in channel selected by register ATE ( 2 MHz stream valid only in selected test channel otherwise all zeros ) is monitored at pin FLEXMON1 / FLEXMON2 |
| "1101": | SITESTDATA in channel selected by register ATE ( 2 MHz stream valid only in selected test channel otherwise all zeros ) is monitored at pin FLEXMON1 / FLEXMON2 |
| "1110": | Far end speech exceeds level configured in CONFSCU3.MINLEV and background noise is monitored at pin FLEXMON1 / FLEXMON2                                         |

## Register Description

"1111": Near end speech exceeds level configured in CONFSCU3.MINLEV and background noise and estimated echo level is monitored at pin FLEXMON1 /FLEXMON2

**CONFIDLE[5:0]** (Addr.: 32H): **Configuration of IDLE** Detection, write protected, Reset value = 1DH

|   |   |        |         |         |         |              |               |
|---|---|--------|---------|---------|---------|--------------|---------------|
| - | - | ENIDLE | IDPT[2] | IDPT[1] | IDPT[0] | IDLE<br>MODE | SELSI<br>IDLE |
|---|---|--------|---------|---------|---------|--------------|---------------|

For idle detection the Receive In or Send In input pattern is compared either with itself or with a maskable configurable pattern of Register IDLEPATTERN. An idle channel can be indicated in MONSTAT2.MIDDLE. An idle channel can also be displayed at pins FLEXMON1 or FLEXMON2.

ENIDLE '1': Enables IDLE Detection for disabling of channels  
A channel that is detected to be idling will be disabled (H-Register reset, bypass, Speech Control reset)  
'0': Disables IDLE detection

IDPT[2:0] Determines the length of the IDLE detection/protection interval  
"000": protection time = 64 ms  
"001": protection time = 128 ms  
"010": protection time = 512 ms  
"011": protection time = 1 s  
"100": protection time = 4.1 s  
"101": protection time = 8.2 s  
"110": protection time = 32.8s  
"111": protection time = 65.5s (according ITU)

IDLEMODE '1': IDLE detection pattern comparison operates on the last received pattern of the actual surveyed channel  
'0': IDLE detection pattern comparison operates on the pattern in register IDLEPATTERN

SELSIIDLE '1': Idle detection operates on send path input  
'0': Idle detection operates on receive path input

**IDLEMASK[7:0]** (Addr.: 33H): **IDLE** detection bit compare **MASK**, write protected, Reset value = 00H

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| IDLE<br>MASK[7] | IDLE<br>MASK[6] | IDLE<br>MASK[5] | IDLE<br>MASK[4] | IDLE<br>MASK[3] | IDLE<br>MASK[2] | IDLE<br>MASK[1] | IDLE<br>MASK[0] |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

## Register Description

IDLEMASK [7:0] '1': The corresponding bit is ignored for pattern comparison  
'0': normal operation (bit comparison enabled)

**IDLEPATTERN[7:0]** (Addr.: 34H): **Idlepattern**, write protected, Reset value = 55H

|                        |                        |                        |                        |                        |                        |                        |                        |
|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| IDLE<br>PAT<br>TERN[7] | IDLE<br>PAT<br>TERN[6] | IDLE<br>PAT<br>TERN[5] | IDLE<br>PAT<br>TERN[4] | IDLE<br>PAT<br>TERN[3] | IDLE<br>PAT<br>TERN[2] | IDLE<br>PAT<br>TERN[1] | IDLE<br>PAT<br>TERN[0] |
|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|

The reset value corresponds to a level minus infinity for A-Law encoding  
IDLEPATTERN [7:0] IDLE Pattern for comparison with the receive values  
if CONFIDLE.IDLEMODE = '0'

**CONFTS16[5:0]** (Addr.: 31H) **Configuration of TS16 CAS Evaluation for E1 frames**, write protected, Reset value = 12H

|   |   |        |               |       |              |              |              |
|---|---|--------|---------------|-------|--------------|--------------|--------------|
| - | - | ENTS16 | SELSI<br>TS16 | FLINV | FL<br>SEL[1] | FL<br>SEL[0] | FL<br>FREEZE |
|---|---|--------|---------------|-------|--------------|--------------|--------------|

ENTS16 '1': TS16 CAS Evaluation enabled  
'0': TS16 CAS Evaluation disabled

SELSITS16 '1': TS16 CAS Evaluation operates on send path input  
'0': TS16 CAS Evaluation operates on receive path input

FLINV Inversion of selected flag bit, "Active" means an enabled time slot.  
A change of this bit means a change of the incoming TS 16 flag bit.  
'1': flag bit is active '0'  
'0': flag bit is active '1'

FLSEL [1:0] Selection of flag bit (MSB of TS 16 is bit 7):  
"00": En/Disable via D-Bit (bit 4 and bit 0 of TS 16 are evaluated)  
"01": En/Disable via C-Bit (bit 5 and bit 1 of TS 16 are evaluated)  
"10": En/Disable via B-Bit (bit 6 and bit 2 of TS 16 are evaluated)  
"11": En/Disable via A-Bit (bit 7 and bit 3 of TS 16 are evaluated)

FLFREEZE '1': Freeze (no update) of flag bits  
'0': normal operation

**CONFUCC[6:0]** (Addr.: 60H): **Configuration of UCC Interface**, write protected, Reset value = 00H

|   |             |             |             |              |              |                  |             |
|---|-------------|-------------|-------------|--------------|--------------|------------------|-------------|
| - | R<br>LISTEN | EN<br>TUCCO | EN<br>DISHW | SEL<br>FX[1] | SEL<br>FX[0] | EN<br>SMLP<br>HW | RSW<br>CTRL |
|---|-------------|-------------|-------------|--------------|--------------|------------------|-------------|

## Register Description

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RLISTEN     | <p>This bit is only active in Reflect Mode which can be configured via bit CONFUCC.RSWCTRL or SMLP bit of UCC Interface.</p> <p>'1': UCCI input data will be transferred to IRAM and interrupt will be generated</p> <p>'0': Normal operation: No data is transferred to IRAM, no interrupts are generated except by SMLP bit in UCC special frame if unmasked.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| ENTUCCO     | <p>'1': Control signal for external tristate buffer <math>\overline{\text{TUCCO}}</math> is enabled for processed channels only (all 32 channels in 64 ms mode or 16 channels in 128 ms mode if bit UCCFRS.128FRSEN is set to '1'). The mode depends on setting of Pins MODE1 and MODE0.</p> <p>'0': Tri-State-Buffer control signal <math>\overline{\text{TUCCO}}</math> is disabled, i.e. = '1'</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| ENDISHW     | <p>'1': The UCC DIS-Bit (Bit 4) of associated channel (see <a href="#">Figure 11</a>) is used for disabling of the associated channel.</p> <p>'0': disable special handling of the DIS-Bit (Bit 4) for channel individual UCC frames by hardware</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| SELFX [1:0] | <p>Selects the UCC bit for the flexible control bit (FX-Bit)</p> <p>"11" : UCC-Bit 2 is selected</p> <p>"10" : UCC-Bit 1 is selected</p> <p>"01" : UCC-Bit 0 is selected</p> <p>"00" : No UCC-Bit is selected, i.e. UCC FX-Bit is disabled</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| ENSMLPHW    | <p>Enables special handling of the SMLP bit in the special frame FRS by hardware if the special frame mode is enabled (Bit NOFRS = '0')</p> <p>'1': The reflection of UCCI to UCCO is activated by the hardware at the beginning of the next channel individual frame after the bit SMLP in FRS (UCC Special Frame) changes from '0' to '1'. The value of the current FRS is the last that is transferred to IRAM, all the following FRS's will no longer be transferred to the IRAM. Only a change of the SMLPbit in FRS is indicated by an interrupt if not masked by IMASKFRS[7]. Additionally the current status of the channel individual control bits DIS-Bit and FX-Bit is frozen. This reflection is deactivated with the beginning of the next channel individual frame after the FRS, in which the hardware detects a '1' to '0' change of the SMLP bit. The value of this FRS is transferred to the IRAM.</p> <p>'0': normal operation, reflection control by bit RSWCTRL</p> |
| RSWCTRL     | <p>Only effective if ENSMLPHW = '0', Reflection control by software.</p> <p>'1': The reflection of UCCI to UCCO is activated by the software, not by the hardware via SMLP bit evaluation. Only a change of the SMLP in FRS is indicated, and the current status of the channel individual control bits DIS-Bit and FX-Bit is frozen.</p> <p>The timing for de/activation of the reflection depends solely on</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

## Register Description

the performance of the software and is unpredictable!  
'0': normal operation

Note: In 128 ms mode the DIS-Bit and the FX-Bit are only evaluated in the 16 processed channels.

**UCCMFR[4:0]** (Addr.: 61H): **UCC Multiframe Alignment**, write protected,  
Reset value = 00H

|   |   |   |               |               |               |               |               |
|---|---|---|---------------|---------------|---------------|---------------|---------------|
| - | - | - | UCC<br>MFR[4] | UCC<br>MFR[3] | UCC<br>MFR[2] | UCC<br>MFR[1] | UCC<br>MFR[0] |
|---|---|---|---------------|---------------|---------------|---------------|---------------|

**UCCMFR[4:0]** Denotes the UCC frame number for the next complete UCC frame (beginning with bit 7, phase 0, channel 0) after the first detection of an active SYNCI impulse with the falling edge of SCLKI (UCC frame alignment is configured by register UCCALIGN). For explanation see also [Figure 25](#) and [Figure 26](#).

**UCCFRS[6:0]** (Addr.: 62H): Selection of the special **UCC** Frame **FRS**,  
write protected, Reset value = 00H

|   |       |              |               |               |               |               |               |
|---|-------|--------------|---------------|---------------|---------------|---------------|---------------|
| - | NOFRS | 128FRS<br>EN | UCC<br>FRS[4] | UCC<br>FRS[3] | UCC<br>FRS[2] | UCC<br>FRS[1] | UCC<br>FRS[0] |
|---|-------|--------------|---------------|---------------|---------------|---------------|---------------|

**NOFRS** '1': The UCC frame corresponding to the value in UCCFRS[4:0] is not handled as the special UCC frame containing global SIDEC information but as a frame that contains channel individual information (like the other UCC frames)  
'0': The UCC frame corresponding to the value in UCCFRS[4:0] is handled as the special UCC frame that contains global SIDEC related (not channel individual) information.  
Note: If this setting is configured, the PCM channel that corresponds to the value in UCCFRS[4:0] can not individually be controlled directly via UCC and is considered as a PCM channel containing no payload data. The DIS-Bit and the FX-Bit are not evaluated for this channel and set inactive. It is the responsibility of the software to disable the Echo Cancellor and Law conversion function via the channel individual control registers CHCTR\* in order to enable the transparent (64-clear) mode for this channel.

**128FRSEN** '1': enables the output of all frames at UCCO and the activation of TUCCO for all frames in 128 ms mode even if the number does not correspond to one of the 16 processed channels.\*

## Register Description

'0': disables the output of all frames at UCCO and the activation of  $\overline{\text{TUCCO}}$  for all frames in 128 ms mode if the number does not correspond to one of the 16 processed channels.\*

UCCFRS[4:0] Denotes the frame number of the special UCC frame FRS.

\*Caution: The activation of the bit 128FRSEN is solely intended for a configuration where only one SIDECS in 128 ms mode is used for one PCM30 interface processing only 16 channels. If two SIDECS in 128 ms master and slave mode are used in parallel for one PCM interface the activation of this bit could result in severe damage of the external driver at the UCCO bus.

**WRUCC[5:0]** (Addr.: 63H): **Write/Read UCCI**, Reset value = 00H

|   |   |            |         |         |         |         |         |
|---|---|------------|---------|---------|---------|---------|---------|
| - | - | WRO<br>RAM | ARAM[4] | ARAM[3] | ARAM[2] | ARAM[1] | ARAM[0] |
|---|---|------------|---------|---------|---------|---------|---------|

WRORAM '1': Write access: the byte stored in register DORAM is written to the UCC output RAM (ORAM) at UCC frame number ARAM [4:0].  
'0': read access: the byte stored in the UCC input RAM (IRAM) at UCC frame number ARAM [4:0] is copied to register DIRAM.  
Data can be read after 8 CLK32 cycles.

ARAM [4:0] Value corresponds to the ORAM or IRAM address where data is written to or read from

**DORAM[7:0]** (Addr.: 64H): **Data Output RAM**, Reset value = 00H

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| DO<br>RAM[7] | DO<br>RAM[6] | DO<br>RAM[5] | DO<br>RAM[5] | DO<br>RAM[3] | DO<br>RAM[2] | DO<br>RAM[1] | DO<br>RAM[0] |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

DORAM [7:0] Data to be written to the ORAM at address WRUCC. ARAM [4:0]

**IMASKFRS[7:0]** (Addr.: 65H): **Interrupt Mask** for the special UCC frame **FRS**,  
Reset value = 00H

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| IMASK<br>FRS[7] | IMASK<br>FRS[6] | IMASK<br>FRS[5] | IMASK<br>FRS[4] | IMASK<br>FRS[3] | IMASK<br>FRS[2] | IMASK<br>FRS[1] | IMASK<br>FRS[0] |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

IMASKFRS[7:0] Each activated (set to '1') mask bit prevents the generation of an UCC interrupt at a change of the corresponding bit in FRS.

Note: In 128 ms mode the change of an unmasked bit generates an interrupt condition only if the frame number of the special UCC frame corresponds to one of the 16 processed channels or bit UCCFRS.128FRSEN is set to '1'.

## Register Description

**IMASKFRN[7:0]** (Addr.: 66H): Interrupt **Mask** for channel individual UCC frames (**FRN**), Reset value = 00H

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| IMASK<br>FRN[7] | IMASK<br>FRN[6] | IMASK<br>FRN[5] | IMASK<br>FRN[4] | IMASK<br>FRN[3] | IMASK<br>FRN[2] | IMASK<br>FRN[1] | IMASK<br>FRN[0] |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

IMASKFRN[7:0] Each activated (set to '1') mask bit prevents the generation of an UCC interrupt at a change of the corresponding bit in any channel individual UCC frame FRN.

Note: In 128 ms mode the change of an unmasked bit in one of the channel individual UCC frames generates an interrupt condition only if the frame number of the changed frame corresponds to one of the 16 processed channels or bit UCCFRS.128FRSEN is set to '1'.

**TESTTIMER[1:0]** (Addr.: 37H):  $\mu$ P **Test** and **Timer**, write protected, Reset value = 00H

|   |   |   |   |   |   |         |              |
|---|---|---|---|---|---|---------|--------------|
| - | - | - | - | - | - | UPTTEST | RUN<br>TIMER |
|---|---|---|---|---|---|---------|--------------|

UPTTEST enable for the self test:  
'1': self test is executed in the test channel selected by ATE and values of register CTRLTEST are evaluated. This channel is bypassed according to [Figure 10](#) with "BYPASS".  
'0': self test disabled

RUNTIMER '1': start timer\*  
'0': disable/stop timer\*

\* Note: For using the timer in conjunction with the self-test, the timer should be started at the same time the test is activated.

**ATE[4:0]** (Addr.: 35H): **Address of Test-channel**, write protected, Reset value = 00H

|   |   |   |        |        |        |        |        |
|---|---|---|--------|--------|--------|--------|--------|
| - | - | - | ATE[4] | ATE[3] | ATE[2] | ATE[1] | ATE[0] |
|---|---|---|--------|--------|--------|--------|--------|

ATE [4:0] On the one hand this value corresponds to the channel for which the determination is made if it is en/disabled (result in bit TSEN in register SFATSES). On the other hand, the value corresponds to the channel in which the test is executed.

Note: A test can only be executed in a disabled channel. Therefore, it must be determined whether the channel is en/disabled. Once a test is started it can only be

## Register Description

terminated by the software by resetting the bit TESTTIMER.UPTTEST. If the channel that is background tested by the software suddenly becomes enabled by external sources before the test is terminated an interrupt is generated that informs the software to abort the test immediately.

**CTRLTEST[7:0]** (Addr.: 38H): **Control of test** channel, Reset value = 00H

| T<br>FREEZE | T<br>NLDPIS | T<br>ATTDIS | T<br>SINDIS | T<br>EN | T<br>ALAW | T<br>EDEL[1] | T<br>EDEL[0] |
|-------------|-------------|-------------|-------------|---------|-----------|--------------|--------------|
|-------------|-------------|-------------|-------------|---------|-----------|--------------|--------------|

|             |                                                                                                                                                       |  |  |  |  |  |  |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|
| TFREEZE     | Freeze of speech control unit and H-Register in selected test channel:<br>'1': speech control unit and H-Register are frozen<br>'0': normal operation |  |  |  |  |  |  |
| TNLDPIS     | NLP disable (bypass) in selected test channel:<br>'1': NLP disabled<br>'0': normal operation                                                          |  |  |  |  |  |  |
| TATTDIS     | Disable of output attenuator in selected test channel:<br>'1': Attenuator disabled<br>'0': normal operation, according to setting of register CONFPCM |  |  |  |  |  |  |
| TSINDIS     | Disable of "no speech" detection in selected test channel:<br>'1': "no speech" detection disabled<br>'0': normal operation                            |  |  |  |  |  |  |
| TEN         | En/Disable of selected test channel:<br>'1': test channel enabled<br>'0': test channel disabled (H-Register and Attenuation meters reset)             |  |  |  |  |  |  |
| TALAW       | PCM encoding Law selection of selected test channel:<br>'1': test channel A-Law encoded<br>'0': test channel $\mu$ -Law encoded                       |  |  |  |  |  |  |
| TEDEL [1:0] | end echo delay for test pattern:<br>"11": 7*125 $\mu$ s<br>"10": 6*125 $\mu$ s<br>"01": 5*125 $\mu$ s<br>"00": 4*125 $\mu$ s                          |  |  |  |  |  |  |

Note: For the internal functionality of the channel that is tested in the background all external control sources have no effect.

**TSGSPP[7:0]** (Addr.: 39H): **Test signal generator for send path pattern**, Reset value = 55H

| SG<br>MOD1 | SPTP[6] | SPTP[5] | SPTP[4] | SPTP[3] | SPTP[2] | SPTP[1] | SPTP[0] |
|------------|---------|---------|---------|---------|---------|---------|---------|
|------------|---------|---------|---------|---------|---------|---------|---------|

## Register Description

**SGMOD1** operation mode1 for signal generator (see [Table 36](#))  
**SPTP [6:0]** Send path test pattern amplitude, log, A-/μ-Law encoded

**TSGRPP[7:0]** (Addr.: 3AH): Test signal generator for receive path pattern,  
 Reset value = 55H

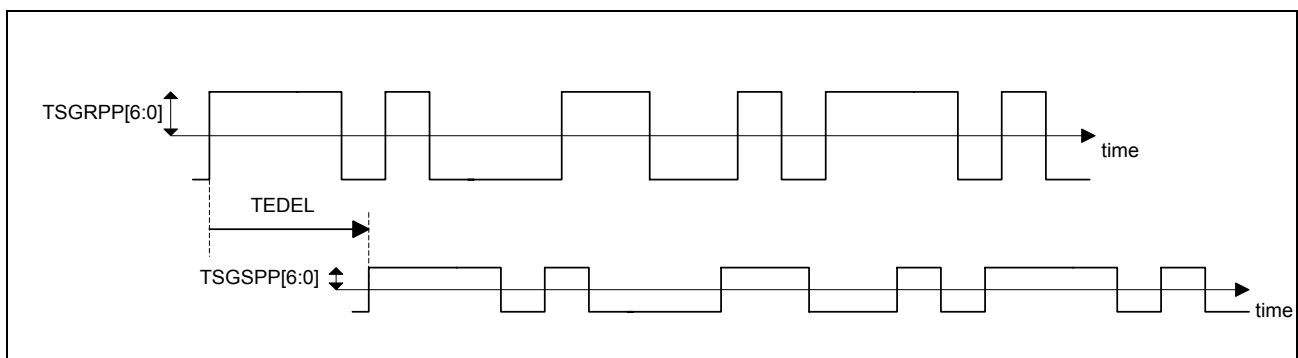
| SG<br>MOD0 | RP<br>TP[6] | RP<br>TP[5] | RP<br>TP[4] | RP<br>TP[3] | RP<br>TP[2] | RP<br>TP[1] | RP<br>TP[0] |
|------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
|------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**SGMOD0** operation mode 0 for signal generator (see [Table 36](#))  
**RPTP[6:0]** receive path test pattern amplitude, log, A-/μ-Law encoded

The sign of the test sequence is determined by the following table. The amplitude is given by TSGSPP[6:0] and TSGRPP[6:0]. Hence, rectified test signals are generated (see [Figure 28](#)).

**Table 36 SGMOD1/0 Configuration**

| SGMOD1 | SGMOD0 | Test Signal Sign changes according to: |
|--------|--------|----------------------------------------|
| 0      | 0      | 2105 Hz                                |
| 0      | 1      | 2105 Hz inverted                       |
| 1      | 0      | 2010 Hz                                |
| 1      | 1      | random sequence                        |



**Figure 28 Explanation of Test Pattern Generation (random sign signal)**

**HTIM[7:0]** (Addr.: 3BH): High-Byte for **T**imer, Reset value = 00H

| TIM[15] | TIM[14] | TIM[13] | TIM[12] | TIM[11] | TIM[10] | TIM[9] | TIM[8] |
|---------|---------|---------|---------|---------|---------|--------|--------|
|---------|---------|---------|---------|---------|---------|--------|--------|

## Register Description

The timer can be used by the processor, if the processor wants to do different operations inbetween. The timer is counting downward. The timing decrement is 1 ms. The accuracy of the timer is +0 ... 1 ms. The maximum value is 65535 ms.

TIM[15:8] load value for the Timer (high byte)

**LTIM[7:0]** (Addr. 3CH): **Low-Byte for Timer**, Reset value = 00H

|        |        |        |        |        |        |        |        |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TIM[7] | TIM[6] | TIM[5] | TIM[4] | TIM[3] | TIM[2] | TIM[1] | TIM[0] |
|--------|--------|--------|--------|--------|--------|--------|--------|

TIM[7:0] load value for the Timer (low byte)

**CONFSCU1[7:0]** (Addr.: 12H): **Configuration of speech control unit 1**, write protected, Reset value = 69H

|              |              |              |              |                  |                  |                  |                  |
|--------------|--------------|--------------|--------------|------------------|------------------|------------------|------------------|
| BN<br>ADD[3] | BN<br>ADD[2] | BN<br>ADD[1] | BN<br>ADD[0] | ADAPT<br>FAST[1] | ADAPT<br>FAST[0] | ADAPT<br>SLOW[1] | ADAPT<br>SLOW[0] |
|--------------|--------------|--------------|--------------|------------------|------------------|------------------|------------------|

BNADD [3:0] Safety distance for SO > background noise + BNADD comparison

|                 |                 |
|-----------------|-----------------|
| "0000": +0 dB   | "0001": 1.5 dB  |
| "0010": 3 dB    | "0011": 4.5 dB  |
| "0100": 6 dB    | "0101": 7.5 dB  |
| "0110": 9 dB    | "0111": 10.5 dB |
| "1000": 12 dB   | "1001": 13.5 dB |
| "1010": 15 dB   | "1011": 16.5 dB |
| "1100": 18 dB   | "1101": 21 dB   |
| "1110": 22.5 dB | "1111": 24 dB   |

Attenuation Measurement

ADAPTFAST[1:0] Fast count period for attenuation meters for total echo attenuation and transhybrid loss

"00": 2 ms "01": 1 ms "10": 500 µs "11": 250 µs

ADAPTSLOW[1:0] Slow count period for attenuation meters for total echo attenuation and transhybrid loss

"00": 64 ms "01": 32 ms "10": 16 ms "11": 8 ms

**CONFSCU2[7:0]** (Addr.: 13H): **Configuration of speech control unit 2**, write protected, Reset value = 97H

|               |               |               |               |               |              |              |        |
|---------------|---------------|---------------|---------------|---------------|--------------|--------------|--------|
| BYP<br>THL[4] | BYP<br>THL[3] | BYP<br>THL[2] | BYP<br>THL[1] | BYP<br>THL[0] | RE<br>ADD[1] | RE<br>ADD[0] | DHHLEC |
|---------------|---------------|---------------|---------------|---------------|--------------|--------------|--------|

## Register Description

|             |                                                                                     |
|-------------|-------------------------------------------------------------------------------------|
| BYPTHL[4:0] | Transhybrid loss as of which the canceling unit is bypassed                         |
| "00000":    | 0 dB                                                                                |
| "00001":    | 3 dB                                                                                |
| "00010":    | 6 dB                                                                                |
| "00011":    | 9 dB                                                                                |
| "00100":    | 12 dB                                                                               |
|             | ...                                                                                 |
| "10010":    | 54 dB                                                                               |
|             | ...                                                                                 |
| "11111":    | 93 dB (theoretical value only, attenuation will never be reached)                   |
| READD[1:0]  | Safety distance for SO > residual echo + READD comparison                           |
| "00": +0 dB | "01": +3 dB "10": +6 dB "11": +9 dB                                                 |
| DHHLEC      | '1': Enables detection of a change in end echo path in the case of high hybrid loss |
|             | '0': disabled                                                                       |

**CONFSCU3[7:0]** (Addr.: 14H): **Configuration of speech control unit 3**, write protected, Reset value = A4H

| MIN<br>LEV[4] | MIN<br>LEV[3] | MIN<br>LEV[2] | MIN<br>LEV[1] | MIN<br>LEV[0] | DT<br>TIME[1] | DT<br>TIME[0] | ITUDT |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|-------|
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|-------|

### H-Register Control:

|                             |                                                                                  |
|-----------------------------|----------------------------------------------------------------------------------|
| MINLEV[4:0]                 | Minimum level of SI and RI for controlling of the coefficients (H-Register)      |
| "00000":                    | minus infinite, no residual echo limitation                                      |
| "00001":                    | -67.5 dBm0                                                                       |
| "00010":                    | -66.0 dBm0                                                                       |
| "00011":                    | -64.5 dBm0                                                                       |
| "00100":                    | -63 dBm0                                                                         |
|                             | ...                                                                              |
| "10100":                    | -39.0 dBm0                                                                       |
|                             | ...                                                                              |
| "11111":                    | -22.5 dBm0                                                                       |
| Double Talk:<br>DTTIME[1:0] | Double talk hangover time                                                        |
| "00": 32 ms                 | "01": 64 ms "10": 128 ms "11": 256 ms                                            |
| ITUDT                       | '0': double talk detection operates up to 0 dB transhybrid loss                  |
|                             | '1': double talk detection according ITU: transhybrid loss greater or equal 6 dB |

## Register Description

**CONFSCU4[7:0]** (Addr.: 15H): **Configuration of speech control unit 4**, write protected, Reset value = A7H

|              |              |              |              |              |              |             |            |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|------------|
| OC<br>INC[1] | OC<br>INC[0] | OC<br>DEC[1] | OC<br>DEC[1] | SI<br>ADD[1] | SI<br>ADD[0] | OC<br>AMRES | OC<br>HRES |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|------------|

Overcompensation:

|            |                                                                                                                                      |
|------------|--------------------------------------------------------------------------------------------------------------------------------------|
| OCINC[1:0] | Increment period for overcompensation evaluation<br>"00": 32 ms   "01": 16 ms   " <b>10</b> ": 8 ms   "11": 4 ms                     |
| OCDEC[1:0] | Decrement period for overcompensation evaluation<br>"00": 16 ms   "01": 8 ms   " <b>10</b> ": 4 ms   "11": 2 ms                      |
| SIADD[1:0] | Safety distance for SO > SI + SIADD comparison<br>"00": +0 dB   " <b>01</b> ": +3 dB   "10": +6 dB   "11": +9 dB                     |
| OCAMRES    | '0': no reset of attenuation meters in case of overcompensation<br>'1': reset of attenuation meters only in case of overcompensation |
| OCHRES     | '0': no reset via overcompensation detection<br>'1': reset via overcompensation detection (H-Register reset only)                    |

**CONFSCU5[7:0]** (Addr.: 16H): **Configuration of speech control unit 5**, write protected, Reset value = 84H

|                     |                     |                     |                     |                     |                 |                 |                 |
|---------------------|---------------------|---------------------|---------------------|---------------------|-----------------|-----------------|-----------------|
| NLP<br>RANGE<br>[4] | NLP<br>RANGE<br>[3] | NLP<br>RANGE<br>[2] | NLP<br>RANGE<br>[1] | NLP<br>RANGE<br>[0] | SWMIN<br>ATT[2] | SWMIN<br>ATT[1] | SWMIN<br>ATT[0] |
|---------------------|---------------------|---------------------|---------------------|---------------------|-----------------|-----------------|-----------------|

Non Linear Processor (NLP) activation

|               |                                                                                                                                                                                                                                         |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NLPRANGE[4:0] | Operating range for the NLP<br>"00000": minus infinite: no residual echo limitation<br>"00001": -66 dBm0<br>"00010": -63 dBm0<br>"00011": -60 dBm0<br>"00100": -57 dBm0<br>...<br>" <b>10000</b> ": -21 dBm0<br>...<br>"11000": +3 dBm0 |
| SWMINATT[2:0] | Minimum attenuation for switchover to final residual echo level<br>"000": 0 dB   "001": 3 dB   "010": 6 dB   "011": 9 dB<br>" <b>100</b> ": 12 dB   "101": 15dB   "110": 18dB   "111": 21dB                                             |

## Register Description

**CONFSCU6[7:0]** (Addr.: 17H): **Configuration of speech control unit 6**, write protected, Reset value = 2AH

| REL<br>ADD[2] | REL<br>ADD[1] | REL<br>ADD[0] | RI<br>MIN[2] | RI<br>MIN[1] | RI<br>MIN[0] | OF<br>CNT[1] | OF<br>CNT[0] |
|---------------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|
|---------------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|

RELADD[2:0] Safety increment for the residual echo limiter threshold  
 "000": 0 dB "001": 3 dB "010": 6 dB "011": 9 dB  
 "100": 12 dB "101": 15 dB "110": 18 dB "111": 21 dB

RIMIN[2:0] Reduction of receive path level for determination of the temporary NLP threshold  
 "000": 0 dB "001": 3 dB "010": 6 dB "011": 9 dB  
 "100": 12 dB "101": 15 dB "110": 18 dB "111": 21 dB

Offset:  
 OFCNT[1:0] Count period for offset measurements  
 "00": disabled "01": 64 ms  
 "10": 16 ms "11": 1 ms

**CONFSCU7[7:0]** (Addr.: 18H): **Configuration of speech control unit 7**, write protected, Reset value = 8AH

| NOISE<br>INC[3] | NOISE<br>INC[2] | NOISE<br>INC[1] | NOISE<br>INC[0] | BN<br>INC[1] | BN<br>INC[0] | BN<br>DEC[1] | BN<br>DEC[0] |
|-----------------|-----------------|-----------------|-----------------|--------------|--------------|--------------|--------------|
|-----------------|-----------------|-----------------|-----------------|--------------|--------------|--------------|--------------|

NLP comfort noise:  
 NOISEINC[3:0] Increase of the noise level for maximum level evaluation  
 "0000": -6 dB "0001": -4.5 dB  
 "0010": -3 dB "0011": -1.5 dB  
 "0100": +0 dB "0101": +1.5 dB  
 "0110": +3 dB "0111": +4.5 dB  
 "1000": +6 dB "1001": +7.5 dB  
 "1010": +9 dB "1011": +10.5 dB  
 "1100": +12 dB "1101": +13.5 dB  
 "1110": +15 dB "1111": +16.5 dB

BNINC[1:0] Incrementing period for background noise evaluation counter  
 "00": 64 ms "01": 32 ms "10": 16 ms "11": 8 ms

BNDEC[1:0] Decrementing period for background noise evaluation counter  
 "00": 16 ms "01": 8 ms "10": 4 ms "11": 2 ms

## Register Description

**CONFSCU8[7:0]** (Addr.: 19H), **Configuration of speech control unit 8**, write protected, Reset value = EEH

| BNMAX<br>SL[3] | BNMAX<br>SL[2] | BNMAX<br>SL[1] | BNMAX<br>SL[0] | BNMAX<br>RL[3] | BNMAX<br>RL[2] | BNMAX<br>RL[1] | BNMAX<br>RL[0] |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

BNMAXSL[3:0] Maximum send path level for background noise measurement

"0000": minus infinite

"0001": -66 dBm0

"0010": -63 dBm0

"0011": -60 dBm0

"0100": -57 dBm0

...

"1110": -27 dBm0

"1111": -24 dBm0 (not possible)

BNMAXRL[3:0] Maximum receive path level for background noise measurement

"0000": minus infinite

"0001": -66 dBm0

"0010": -63 dBm0

"0011": -60 dBm0

"0100": -57 dBm0

...

"1110": -27 dBm0

"1111": -24 dBm0 (not possible)

**CONFSCU9[7:0]** (Addr.: 1AH), **Configuration of speech control unit 9**, write protected, Reset value = 44H

| DISBY | PSBY | DISNLP<br>DIS | PSNLP<br>DIS | DIS<br>HRES | PS<br>HRES | PSLM<br>RES | DIS<br>RES |
|-------|------|---------------|--------------|-------------|------------|-------------|------------|
|-------|------|---------------|--------------|-------------|------------|-------------|------------|

Bypass of Non Linear Processor (NLP), Subtractor and Attenuator (Receive and Send path):

DISBY '0': no bypass via 2100 Hz Disabler without phase shift

'1': bypass via 2100 Hz Disabler even without phase shift

PSBY '0': no bypass via 2100 Hz Disabler even with phase shift

'1': bypass via 2100 Hz Disabler with phase shift

Disable/Bypass of NLP:

DISNLPDIS '0': no disable via 2100 Hz Disabler without phase shift

'1': disable via 2100 Hz Disabler even without phase shift

PSNLPDIS '0': no disable via 2100 Hz Disabler even with phase shift

'1': disable via 2100 Hz Disabler with phase shift

## Register Description

Coefficient (H-Register) reset:

DISHRES '0': no reset via 2100 Hz Disabler without phase shift  
'1': reset via 2100 Hz Disabler even without phase shift  
PSHRES '0': no reset via 2100 Hz Disabler even with phase shift  
'1': reset via 2100 Hz Disabler with phase shift

Reset of attenuation meters in SCU:

PSLMRES '0': no reset of via 2100 Hz Disabler even with phase shift  
'1': reset via 2100 Hz Disabler with phase shift  
DISRES '0': no reset via 2100 Hz disable tone without phase shift  
'1': reset via 2100 Hz disable tone even without phase shift

**CONFSCU10[7:0]** (Addr.: 1BH): **Configuration of speech control unit 10**,  
write protected, Reset value = C0H

|                |                |                |                |                |             |            |            |
|----------------|----------------|----------------|----------------|----------------|-------------|------------|------------|
| DIS<br>LOCK[4] | DIS<br>LOCK[3] | DIS<br>LOCK[2] | DIS<br>LOCK[1] | DIS<br>LOCK[0] | DIS<br>56EN | ITU<br>DIS | SP<br>PROT |
|----------------|----------------|----------------|----------------|----------------|-------------|------------|------------|

Additional Controls:

DISLOCK[4:0] Self-locking level after response of the 2100 Hz tone disabler.  
The tone disabler is inactive if the level is below the following value.  
"00000": minus infinite  
"00001": -67.5dBm0  
"00010": -66.0dBm0  
"00011": -64.5dBm0  
"00100": -63 dBm0  
...  
"11000": -33.0 dBm0  
...  
"11111": -22.5 dBm0  
DIS56EN '0': no special evaluation of bit 8 (LSB) in T1 frames for modem calls  
'1': special evaluation of bit 8 (LSB) in T1 frames for modem calls:  
If all bit 8 (LSB) are '1' the first seven bit will bypass the echo  
canceller.  
ITUDIS '0': drop out time for tone disabler up to > 400 ms (necessary for  
some modems). Interruption up to 400 ms of modem tone does  
not cause enabling of canceller.  
'1': drop out time for tone disabler < 400 ms according ITU  
SPPROT Speech protection for 2100 Hz tone detection:  
'0': normal speech protection  
'1': Increased Speech protection

## Register Description

**VDFCTRL[7:0]** (Addr.: 76H): **V**oice **D**etection **F**reeze **C**ontrol,  
write protected, Reset value = B4H

| VDF<br>RELEN | VDF<br>REL[2] | VDF<br>REL[1] | VDF<br>REL[0] | VD<br>FSOL[3] | VD<br>FSOL[2] | VD<br>FSOL[1] | VD<br>FSOL[0] |
|--------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
|--------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

|              |                                                                                                                                                                                                                                                                                                                                          |  |  |  |  |  |  |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|
| VDFRELEN     | '0': No freeze of H-Register on no voice detection when combined loss (ERL+ERLE) > VDFREL<br>'1': Freeze of H-Register on no voice detection when combined loss (ERL+ERLE) > VDFREL                                                                                                                                                      |  |  |  |  |  |  |
| VDFREL[2:0]: | Threshold for total echo loss (ERL+ERLE) at which H-Register are frozen on a no voice signal detection if VDFRELEN = '1'<br>"000": 27 dB                      "001": 28.5 dB<br>"010": 30 dB                      "011": 31.5 dB<br>"100": 33 dB                      "101": 34.5 dB<br>"110": 36 dB                      "111": 37.5 dB |  |  |  |  |  |  |
| VDFSOL[3:0]  | Threshold for residual echo level at Send Out below which the H-Register are frozen on a 'no voice' signal.<br>"0000": minus infinite: no freezing for periodic signals<br>"0001": -66 dBm0<br>"0010": -63 dBm0<br>"0011": -60 dBm0<br>"0100": -57 dBm0<br>...<br>"1101": -30 dBm0<br>"1110": -27 dBm0<br>"1111": -24 dBm0               |  |  |  |  |  |  |

**CONFPSD[7:0]** (Addr.: 1CH): **C**onfiguration of 2100 Hz tone **p**hase **s**hift **d**etector,  
write protected, Reset value = 43H

| DT30DIS | DEP[1] | DEP[0] | DBP<br>MIN[1] | DBP<br>MIN[0] | DBP<br>MAX[2] | DBP<br>MAX[1] | DBP<br>MAX[0] |
|---------|--------|--------|---------------|---------------|---------------|---------------|---------------|
|---------|--------|--------|---------------|---------------|---------------|---------------|---------------|

|             |                                                                                                                                                                                                                |  |  |  |  |  |  |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|
| DT30DIS     | '0': disable evaluation if phase shift detection of >30 ms is identified<br>'1': enable phase shift detection >30 ms                                                                                           |  |  |  |  |  |  |
| DEP[1:0]    | Evaluation time:<br>If no phase shift is detected in the time interval below the evaluation is terminated.<br>"00": 749 ms                      "01": 833 ms<br>"10": 916 ms                      "11": 999 ms |  |  |  |  |  |  |
| DBPMIN[1:0] | Minimum interruption time that results in response:                                                                                                                                                            |  |  |  |  |  |  |

## Register Description

|             |                                                              |                |
|-------------|--------------------------------------------------------------|----------------|
| DBPMAX[2:0] | "00": 1.125 ms                                               | "01": 2.250 ms |
|             | "10": 3.375 ms                                               | "11": 4.500 ms |
|             | Maximum interruption time that results in response:          |                |
|             | "000": 27 ms                                                 | "001": 28 ms   |
|             | "010": 29 ms                                                 | "011": 30 ms   |
|             | "100": 32 ms                                                 | "101": 33 ms   |
|             | "110": 34 ms                                                 | "111": 35 ms   |
|             | DBPMIN[1:0] and DBPMAX[2:0] determine the evaluation window. |                |

**CONFSS7[7:0]** (Addr.: 1DH): **Configuration of SS7 continuity check tone detection**, write protected, Reset value = 00H

| DIS<br>NR7[3] | DIS<br>NR7[2] | DIS<br>NR7[1] | DIS<br>NR7[0] | BY<br>NR7[3] | BY<br>NR7[2] | BY<br>NR7[1] | BY<br>NR7[0] |
|---------------|---------------|---------------|---------------|--------------|--------------|--------------|--------------|
|---------------|---------------|---------------|---------------|--------------|--------------|--------------|--------------|

If CONFSS7[7:0] = 00H the 2010 Hz tone detection is disabled.

**DISNR7[3:0]** protection time for reset of H-register after SS7 continuity check tone detection. For this time the 2010 Hz signal must be applied to the SIDEC to reset the H-Register.

|                  |               |
|------------------|---------------|
| "0000": no reset | "0001": 8ms   |
| "0010": 16ms     | "0011": 24ms  |
| "0100": 32ms     | "0101": 40ms  |
| "0110": 48ms     | "0111": 56ms  |
| "1000": 64ms     | "1001": 72ms  |
| "1010": 80ms     | "1011": 88ms  |
| "1100": 96ms     | "1101": 104ms |
| "1110": 112ms    | "1111": 120ms |

**BYNR7[3:0]** protection for bypass of the canceller after SS7 continuity check tone detection. For this time the 2010 Hz signal must be applied to the SIDEC to bypass the Echo Cancellor.

|                   |               |
|-------------------|---------------|
| "0000": no bypass | "0001": 8ms   |
| "0010": 16ms      | "0011": 24ms  |
| "0100": 32ms      | "0101": 40ms  |
| "0110": 48ms      | "0111": 56ms  |
| "1000": 64ms      | "1001": 72ms  |
| "1010": 80ms      | "1011": 88ms  |
| "1100": 96ms      | "1101": 104ms |
| "1110": 112ms     | "1111": 120ms |

## Register Description

**CONFCC[6:0]** (Addr.: 0BH) **C**onfiguration of **C**lock **C**ontrol unit, write protected,  
Reset value = 00H

| - | INV<br>CTRL32 | SYNC<br>ACT | SYNCO<br>DUR | SSCLK<br>EDGE | DIS<br>CTRL32 | DIS<br>SCLKO | DIS<br>CLK4O |
|---|---------------|-------------|--------------|---------------|---------------|--------------|--------------|
|---|---------------|-------------|--------------|---------------|---------------|--------------|--------------|

|           |                                                                                                                                                                                                                                                                                |  |  |  |  |  |  |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|
| INVCTRL32 | '1': Inverts the control voltage signal for the 32MHz VCO at pin CTRL32 (see <a href="#">Figure 23</a> )<br>'0': no inversion of the control voltage signal for the 32MHz VCO at pin CTRL32 (see <a href="#">Figure 23</a> )                                                   |  |  |  |  |  |  |
| SYNCACT   | '1': SYNCI/SYNCO is active high (active edge is the rising edge)<br>'0': SYNCI/SYNCO is active low (active edge is the falling edge)                                                                                                                                           |  |  |  |  |  |  |
| SYNCODUR  | '1': SYNCO duration is 2 SCLK periods<br>'0': SYNCO duration is 1 SCLK period                                                                                                                                                                                                  |  |  |  |  |  |  |
| SSCLKEDGE | '1': SYNCI is sampled with the rising edge of SCLKI, SYNCO is output with the falling edge of SCLKI (see <a href="#">Figure 21</a> ).<br>'0': SYNCI is sampled with the falling edge of SCLKI, SYNCO is output with the rising edge of SCLKI (see <a href="#">Figure 21</a> ). |  |  |  |  |  |  |
| DISCTRL32 | '1': disables (constantly set to '1') the output of the control voltage signal for the 32MHz VCO at pin CTRL32<br>'0': enables the output of the control voltage signal for the 32MHz VCO at pin CTRL32                                                                        |  |  |  |  |  |  |
| DISSCLKO  | '1': disables (constantly set to '1') the output of the system clock at pin SCLKO<br>'0': enables the output of the system clock at pin SCLKO                                                                                                                                  |  |  |  |  |  |  |
| DISCLK4O  | '1': disables (constantly set to '1') the output of the clock at pin CLK4O<br>'0': enables the output of the clock at pin CLK4O                                                                                                                                                |  |  |  |  |  |  |

**FSLIPV[6:0]** (Addr.: 0CH) **F**rame **slip** safety **i**nterval, write protected,  
Reset value = 28H

| - | RF<br>CLKEX | RFN | FSLIP<br>IV[4] | FSLIP<br>IV[3] | FSLIP<br>IV[2] | FSLIP<br>IV[1] | FSLIP<br>IV[0] |
|---|-------------|-----|----------------|----------------|----------------|----------------|----------------|
|---|-------------|-----|----------------|----------------|----------------|----------------|----------------|

|         |                                                                                                                                                                                                                                                                                                    |  |  |  |  |  |  |
|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|
| RFCLKEX | '1': Selects RFCLKEX as reference clock for the 16MHz PLL<br>'0': Selects RFCLKN or RFCLKF (depending on bit RFN )as reference clock for the 16MHz PLL                                                                                                                                             |  |  |  |  |  |  |
| RFN     | '1': Selects RFCLKN as reference clock for the 16MHz PLL if bit RFCLKEX = '0', and $\overline{\text{RFSPN}}$ as external data buffer sync pulse<br>'0': Selects RFLCKF as reference clock for the 16MHz PLL if bit RFCLKEX = '0', and $\overline{\text{RFSPF}}$ as external data buffer sync pulse |  |  |  |  |  |  |

## Register Description

**FSLIPV[4:0]** Determines the safety interval around the SYNCO pulse, which represents the minimum allowed distance between SYNCO and  $\overline{\text{RFSPN}}$  or  $\overline{\text{RFSPF}}$  in 2  $\mu\text{s}$  steps. If the distance between  $\overline{\text{RFSPN}}$ / $\overline{\text{F}}$  and SYNCO becomes smaller than  $\text{FSLIPV}[4:0] * 2 \mu\text{s}$ , SYNCO will jump to the optimal distance of 62.5  $\mu\text{s}$  with respect to  $\overline{\text{RFSPN}}$ / $\overline{\text{F}}$  (frame slip). The default value is "01000".

**RIALIGN[7:0]** (Addr.: 0DH): **Receive input frame alignment**, write protected, Reset value = 00H.

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| RI<br>ALIGN[7] | RI<br>ALIGN[6] | RI<br>ALIGN[5] | RI<br>ALIGN[4] | RI<br>ALIGN[3] | RI<br>ALIGN[2] | RI<br>ALIGN[1] | RI<br>ALIGN[0] |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**RIALIGN[7:0]** Determines the valid frame bit of the receive input PCM frame (starting with bit 7 channel 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. (00H = bit 7, channel 0; FFH = bit 0, channel 31). For explanation see [Figure 19](#).

**SIALIGN[7:0]** (Addr.: 0EH): **Send input frame alignment**, write protected, Reset value = 00H.

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| SI<br>ALIGN[7] | SI<br>ALIGN[6] | SI<br>ALIGN[5] | SI<br>ALIGN[4] | SI<br>ALIGN[3] | SI<br>ALIGN[2] | SI<br>ALIGN[1] | SI<br>ALIGN[0] |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**SIALIGN[7:0]** Determines the valid frame bit of the send input PCM frame (starting with bit 7 channel 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. (00H = bit 7, channel 0; FFH = bit 0, channel 31). For explanation see [Figure 19](#).

**SOALIGN[7:0]** (Addr.: 0FH): **Send output frame alignment**, write protected, Reset value = 00H.

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| SO<br>ALIGN[7] | SO<br>ALIGN[6] | SO<br>ALIGN[5] | SO<br>ALIGN[4] | SO<br>ALIGN[3] | SO<br>ALIGN[2] | SO<br>ALIGN[1] | SO<br>ALIGN[0] |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**SOALIGN[7:0]** Determines the valid frame bit of the send output PCM frame (starting with bit 7 channel 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. (00H = bit 7, channel 0; FFH = bit 0, channel 31). For explanation see [Figure 19](#).

## Register Description

**UCCALIGN[7:0]** (Addr.: 10H): **UCC** frame **alignment**, write protected, Reset value = 00H

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| UCC<br>ALIGN[7] | UCC<br>ALIGN[6] | UCC<br>ALIGN[5] | UCC<br>ALIGN[4] | UCC<br>ALIGN[3] | UCC<br>ALIGN[2] | UCC<br>ALIGN[1] | UCC<br>ALIGN[0] |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

UCCALIGN[7:0] Determines the valid frame bit of the UCC frame (starting with bit 7 channel 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. (00H = bit 7, channel 0; FFH = bit 0, channel 31). For explanation see [Figure 25](#).

**PHALIGN[7:0]** (Addr. 11H): Bit **Phase alignment** for RI, SI, SO and UCC, write protected, Reset value = 00H,

|                   |                   |                  |                  |                  |                  |                  |                  |
|-------------------|-------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| UCCPH<br>ALIGN[1] | UCCPH<br>ALIGN[0] | SOPH<br>ALIGN[1] | SOPH<br>ALIGN[0] | SIPH<br>ALIGN[1] | SIPH<br>ALIGN[0] | RIPH<br>ALIGN[1] | RIPH<br>ALIGN[0] |
|-------------------|-------------------|------------------|------------------|------------------|------------------|------------------|------------------|

UCCPHALIGN[1:0] Determines the valid bit phase of the UCC frame bit (starting with phase 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. ("00" = bit phase 0, "11" = bit phase 3)  
For explanation see [Figure 25](#).

SOPHALIGN[1:0] Determines the valid bit phase of the send output frame bit (starting with phase 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. ("00" = bit phase 0, "11" = bit phase 3)  
For explanation see [Figure 19](#).

SIPHALIGN[1:0] Determines the valid bit phase of the send input frame bit (starting with phase 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. ("00" = bit phase 0, "11" = bit phase 3)  
For explanation see [Figure 19](#).

RIPHALIGN[1:0] Determines the valid bit phase of the receive input frame bit (starting with phase 0) at the first falling SCLKI edge, with which an active SYNCI impulse is detected. ("00" = bit phase 0, "11" = bit phase 3)  
For explanation see [Figure 19](#).

**ASTOC[7:0]** (Addr.: 70H): **AFI Saw-Tooth and Offset Characteristic**, write protected, Reset value = 00H

|               |               |               |               |               |               |         |         |
|---------------|---------------|---------------|---------------|---------------|---------------|---------|---------|
| ST<br>RISE[2] | ST<br>RISE[1] | ST<br>RISE[0] | ST<br>FALL[2] | ST<br>FALL[1] | ST<br>FALL[0] | AMPL[1] | AMPL[0] |
|---------------|---------------|---------------|---------------|---------------|---------------|---------|---------|

Low frequency components are superimposed to the Receive In AFI input signal to increase stability. Under normal conditions this superimposition is not necessary.

STRISE[2:0] Saw-tooth rising clock frequency

## Register Description

**STFALL[2:0]** Saw-tooth falling clock frequency  
The clock for the increasing a decreasing saw tooth offset voltage is:  

|                |                 |
|----------------|-----------------|
| "000": 4 kHz   | "001": 2 kHz    |
| "010": 1 kHz   | "011": 500 Hz   |
| "100": 250 Hz  | "101": 125 Hz   |
| "110": 62.5 Hz | "111": 31.25 Hz |

 If STRISE[2:0] and STFALL[2:0] are set to "000", the clock will be switched off.

**AMPL[1:0]** Saw-tooth and offset amplitude:  
The maximum values of the saw tooth characteristic or offset (clock is switched off) are:  

|          |           |
|----------|-----------|
| "00": 15 | "01": 31  |
| "10": 63 | "11": 127 |

 These values will be added to the linearized receive path signals.  
The max. linearized value in A/μLaw Code is 8064/8031

**AFSTC[6:4,2:0]** (Addr.:71H): **AFI Filter Spring Timer Configuration**, write protected, Reset value = 44H,

|   |              |              |              |   |             |             |             |
|---|--------------|--------------|--------------|---|-------------|-------------|-------------|
| - | AC<br>SPT[2] | AC<br>SPT[1] | AC<br>SPT[0] | - | C<br>SPT[2] | C<br>SPT[1] | C<br>SPT[0] |
|---|--------------|--------------|--------------|---|-------------|-------------|-------------|

Additional damping of the Coefficients. This feature is disabled as soon as the coefficients are frozen.

**ACSPT[2:0]** Aux. coefficients spring timer  
**CSPT[2:0]** Coefficients spring timer  
The period for ACSPT[2:0] and CSPT[2:0] is:  

|               |               |
|---------------|---------------|
| "000": 250 μs | "001": 500 μs |
| "010": 1 ms   | "011": 2 ms   |
| "100": 4ms    | "101": 8 ms   |
| "110": 16 ms  | "111": 32 ms  |

**AEEPDP[3:0]** (Addr.: 72H): **AFI End Echo Path Delay**, write protected, Reset value = 0FH

|   |   |   |   |              |              |              |              |
|---|---|---|---|--------------|--------------|--------------|--------------|
| - | - | - | - | DELAY<br>[3] | DELAY<br>[2] | DELAY<br>[1] | DELAY<br>[0] |
|---|---|---|---|--------------|--------------|--------------|--------------|

**DELAY[3:0]** End echo path delay:  
Depending on the presumed delay in the end echo path, this register is set to DELAY := <echo\_delay> / 8 ms -1. Thus, the AFI handles end echo path delays in the range 8 ms to 128 ms. For end echo

## Register Description

delays > 128 ms, a tandem configuration of two SIDEC ASICs has to be used in which a single SIDEC chip processes only every other four channels:

Master: 0,1,2,3, 8,9,10,11, 16,17,18,19, 24,25,26,27

Slave: 4,5,6,7, 12,13,14,15, 20,21,22,23, 28,29,30,31

If the 128 ms mode is not selected (pins MODE0 and MODE1),

any DELAYs > 64 ms in register AEEPDP are interpreted as 64 ms.

"0000": 8 ms "0001": 16 ms

"0010": 24 ms "0011": 32 ms

"0100": 40 ms "0101": 48 ms

"0110": 56 ms "0111": 64 ms

"1000": 72 ms "1001": 80 ms

"1010": 88 ms "1011": 96 ms

"1100": 104 ms "1101": 112 ms

"1110": 120 ms "1111": 128 ms

**AVDDI[7:0]** (Addr.: 73H): **AFI Voice Detection, Detection Intervals**, write protected, Reset value = 77H

|                          |                          |                          |                          |                       |                       |                       |                       |
|--------------------------|--------------------------|--------------------------|--------------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| VDMAX<br>INTER<br>VAL[3] | VDMAX<br>INTER<br>VAL[2] | VDMAX<br>INTER<br>VAL[1] | VDMAX<br>INTER<br>VAL[0] | VD<br>INTER<br>VAL[3] | VD<br>INTER<br>VAL[2] | VD<br>INTER<br>VAL[1] | VD<br>INTER<br>VAL[0] |
|--------------------------|--------------------------|--------------------------|--------------------------|-----------------------|-----------------------|-----------------------|-----------------------|

### VDMAXINTERVAL[3:0]

Time interval for detecting maximum value for "no-voice" detection: VDMAXINTERVAL defines the time range over which the maximum of the received values for "no-voice"-detection is determined.

"0000": 8 ms "0001": 16 ms

"0010": 24 ms "0011": 32 ms

"0100": 40 ms "0101": 48 ms

"0110": 56 ms "0111": 64 ms

"1000": 72 ms "1001": 80 ms

"1010": 88 ms "1011": 96 ms

"1100": 104 ms "1101": 112 ms

"1110": 120 ms "1111": 128 ms

### VDINTERVAL[3:0]

Time interval for voice detection:

VDINTERVAL defines the time range over which received values are checked for "no-voice"-detection. The coding is the same as for AEEPDP.DELAY.

"0000": 8 ms "0001": 16 ms

"0010": 24 ms "0011": 32 ms

## Register Description

|                |                        |
|----------------|------------------------|
| "0100": 40 ms  | "0101": 48 ms          |
| "0110": 56 ms  | " <b>0111</b> ": 64 ms |
| "1000": 72 ms  | "1001": 80 ms          |
| "1010": 88 ms  | "1011": 96 ms          |
| "1100": 104 ms | "1101": 112 ms         |
| "1110": 120 ms | "1111": 128 ms         |

**AVDHG[7:0]** (Addr.: 74H): **A**FI **V**oice **D**etection, **H**ysteresis and **G**ap, write protected, Reset value = 74H

| VDSO<br>DELAY<br>[3] | VDSO<br>DELAY<br>[2] | VDSO<br>DELAY<br>[1] | VDSO<br>DELAY<br>[0] | VD<br>DIFF[3] | VD<br>DIFF[2] | VD<br>DIFF[1] | VD<br>DIFF[0] |
|----------------------|----------------------|----------------------|----------------------|---------------|---------------|---------------|---------------|
|----------------------|----------------------|----------------------|----------------------|---------------|---------------|---------------|---------------|

VDSODELAY[3:0] Delay for switching off "no-voice" after last detection

|                |                        |
|----------------|------------------------|
| "0000": 8 ms   | "0001": 16 ms          |
| "0010": 24 ms  | "0011": 32 ms          |
| "0100": 40 ms  | "0101": 48 ms          |
| "0110": 56 ms  | " <b>0111</b> ": 64 ms |
| "1000": 72 ms  | "1001": 80 ms          |
| "1010": 88 ms  | "1011": 96 ms          |
| "1100": 104 ms | "1101": 112 ms         |
| "1110": 120 ms | "1111": 128 ms         |

VDDIFF[3:0] VDDIFF defines the criterion for deciding whether a received value contributes to the "no-voice"-counting or not. A value does contribute if its amplitude differs by less than VDDIFF from the maximum in the interval AVDDI.VDMAXINTERVAL.

VDSODELAY defines the "hang-over" time of "no-voice" after it has been detected for the last time. This delay time is only evaluated if hysteresis is enabled for "no-voice" detection in ACONF.VDHYST.  
Difference between max. and current value for voice detection:

|                        |               |
|------------------------|---------------|
| "0000": 0 dB           | "0001": 3 dB  |
| "0010": 6 dB           | "0011": 9 dB  |
| " <b>0100</b> ": 12 dB | "0101": 15 dB |
| "0110": 18 dB          | "0111": 21 dB |
| "1000": 24 dB          | "1001": 27 dB |
| "1010": 30 dB          | "1011": 33 dB |
| "1100": 36 dB          | "1101": 39 dB |
| "1110": 42 dB          | "1111": 45 dB |

## Register Description

**AVDCI[7:0]** (Addr.: 75H): **AFI Voice Detection Count Init**, write protected,  
Reset value = 85H

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| VDCI<br>[7] | VDCI<br>[6] | VDCI<br>[5] | VDCI<br>[4] | VDCI<br>[3] | VDCI<br>[2] | VDCI<br>[1] | VDCI<br>[0] |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

VDCI[7:0]

Voice Detection Counter Init value:

A counter is used to count the number of values within the VDINTERVAL which fulfill the "no-voice"-criterion. "no-voice" is detected, if the counter ends up with a value that is greater or equal to 512 (64 ms mode) or 1024 (128 ms mode), respectively. The init-value for this counter is determined by VDCI in the following way:

64 ms Mode:  $\langle \text{init-value} \rangle = \text{VDCI}[7..0] * 2$

128 ms Mode:  $\langle \text{init-value} \rangle = \text{VDCI}[7..0] * 4$

The reset value of 85H requires that 48% of the values must fulfill the "no-voice" criterion in case the default VDINTERVAL (64 ms) is set)

**ATMAT[3:0]** (Addr.: 77H): **AFI Turbo Mode Activation Threshold**, write protected,  
Reset value = 08H

|   |   |   |   |                |                |                |                |
|---|---|---|---|----------------|----------------|----------------|----------------|
| - | - | - | - | TURBO<br>TH[3] | TURBO<br>TH[2] | TURBO<br>TH[1] | TURBO<br>TH[0] |
|---|---|---|---|----------------|----------------|----------------|----------------|

TURBOTH[3:0]

Turbo Threshold:

This register specifies the threshold for activating the AFI turbo mode (turbo-on indicates that the AFI is adapting to a new end echo path). Turbo mode is activated if the absolute value of one or more auxiliary coefficients is greater than  $351 + 4 * \text{TURBOTH}$ .

The default threshold is 383.

**AACSC[7:0]** (Addr.: 78H): **AFI Auxiliary Coefficient Supervision Configuration**, write protected, Reset value = 00H,

|               |               |               |               |               |               |              |              |
|---------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| ACS<br>EFFECT | ACSC<br>TH[4] | ACSC<br>TH[3] | ACSC<br>TH[2] | ACSC<br>TH[1] | ACSC<br>TH[0] | ACS<br>TH[1] | ACS<br>TH[0] |
|---------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|

To improve handling of periodic signals, two thresholds are used to determine when - probably due to a periodic signal - most of the auxiliary coefficients are becoming quite large. In that case, coefficient update should be slowed down. The slow down mode condition is described by ACSCTH[4:0] and ACSTH[1:0]. The effect of the slow down mode can be configured via the bit ACSEFFECT.

## Register Description

|             |                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ACSEFFECT   | ACSEFFECT specifies the effect of slow-down mode. If set to '1', coefficient update is limited to increasing/decreasing by at most 1. If set to '0', coefficient increment/decrement takes place in the normal way of operation, but turbo mode is disabled. Per default (after reset) it is not active.<br>'0': normal operation<br>'1': Disable turbo mode, Coeff. update limited to +/- 1 |
| ACSCTH[4:0] | Aux. Coeff. Supervision Count Threshold:<br>ACSCTH specifies the threshold for activating the slow-down mode of operation. Slow-down mode is active if at least 8 * ACSCTH auxiliary coefficients are "large". The default value ACSCTH[4:0]="00000" switches off supervision.                                                                                                               |
| ACSTH[1:0]  | Aux. Coeff. Supervision Threshold:<br>ACSTH specifies the threshold above which the absolute value of an auxiliary coefficient is considered "large". It refers to TURBOTH in register ATMAT:<br>"00": ATMAT.TURBOTH - 32<br>"01": ATMAT.TURBOTH - 16<br>"10": ATMAT.TURBOTH - 8<br>"11": ATMAT.TURBOTH                                                                                      |

**ACONF[6:0]** (Addr.: 79H): **AFI Configuration**, write protected, Reset value = 10H

|   |      |            |           |             |             |             |             |
|---|------|------------|-----------|-------------|-------------|-------------|-------------|
| - | EMAF | VD<br>HYST | VD<br>IHA | VD<br>AT[3] | VD<br>AT[2] | VD<br>AT[1] | VD<br>AT[0] |
|---|------|------------|-----------|-------------|-------------|-------------|-------------|

|           |                                                                                                                                                                                                                                                                                                                                                                                            |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EMAF      | Echo, Minimum Attenuation Factor for end echo path<br>'0': Attenuation 0 dB (no attenuation)<br>'1': Attenuation 6 dB                                                                                                                                                                                                                                                                      |
| VDHYST    | Voice Detection, Hysteresis On/Off:<br>VDHYST selects whether a hysteresis is used for switching off "no-voice".<br>'0': means that "no-voice" is active only if the set of received values currently in the detection set (AVDDI.VDINTERVAL) fulfill the "no-voice" criterion.<br>'1': means that "no-voice" - once activated - remains active for the time specified in AVDHG.VDSODELAY. |
| VDIHA     | Voice Detection, Ignore High Amplitude:<br>'1': received values with an amplitude above 126 (logarithmic) are ignored for "no-voice" detection.<br>'0': all values are taken into account, no values are ignored                                                                                                                                                                           |
| VDAT[3:0] | Specifies a lower limit on the amplitude of received                                                                                                                                                                                                                                                                                                                                       |

## Register Description

values that are considered for "no-voice"-detection. It is configured in the range from -42 dBm0 (VDAT[3:0] = "0001") to 0 dBm0 (VDAT[3:0] = "1111") in steps of 3 dBm0. With VDAT set to the default value "0000", no lower limit on the amplitude is in effect for "no-voice"-detection.

|                    |                 |
|--------------------|-----------------|
| "0000": - infinity | "0001": -42 dBm |
| "0010": -39 dBm    | "0011": -36 dBm |
| "0100": -33 dBm    | "0101": -30 dBm |
| "0110": -27 dBm    | "0111": -24 dBm |
| "1000": -21 dBm    | "1001": -18 dBm |
| "1010": -15 dBm    | "1011": -12 dBm |
| "1100": -9 dBm     | "1101": -6 dBm  |
| "1110": -3 dBm     | "1111": 0 dBm   |

**AFCMC[7,4:0]** (Addr.: 7AH): **AFI Filter Coefficients Monitoring Control**,  
Reset value = 00H

|           |   |   |              |              |              |              |              |
|-----------|---|---|--------------|--------------|--------------|--------------|--------------|
| MON<br>ON | - | - | CH<br>SEL[4] | CH<br>SEL[3] | CH<br>SEL[2] | CH<br>SEL[1] | CH<br>SEL[0] |
|-----------|---|---|--------------|--------------|--------------|--------------|--------------|

To successively read out all coefficients of a channel's filter, the processor writes the channel number and a set MONON bit to this register. The coefficients and aux. coefficients of the channel are delivered in ascending order via the registers AFCD1 thru AFCD3. The SIDECD interrupt request "Monitored coefficient available" indicates availability of the next coefficient. A running readout procedure stops immediately if the processor writes the AFCMC register again.

**MONON** Monitoring on/off:  
If MON\_ON is cleared, coefficient readout is completely reset immediately. If '1' is written to an already set MONON bit, MONON is first cleared to reset the readout procedure and then set to start readout for the new channel. If coefficient readout is not stopped explicitly by the processor, readout ends after delivery of the channel's last coefficient which resets the MONON bit.

**CHSEL[4:0]** Channel selection:  
In 128 ms mode the ASIC does not respond to requests for data channels it does not process (e.g. in master mode the chip responds only to requests for channels 0 to 3, 8 to 11, 16 to 19 and 24 to 27).

## Register Description

### 5.1.4 Read Register

**CLKSTAT[5:0]** (Addr.: 09H): **Clock-Status**

|   |   |             |            |            |       |       |       |
|---|---|-------------|------------|------------|-------|-------|-------|
| - | - | RF<br>CLKEX | RF<br>CLKN | RF<br>CLKF | SCLKI | CLK16 | CLK32 |
|---|---|-------------|------------|------------|-------|-------|-------|

|         |                                                    |
|---------|----------------------------------------------------|
| RFCLKEX | '1': no valid 2 MHz clock available at pin RFCLKEX |
| RFCLKN  | '1': no valid 2 MHz clock available at pin RFCLKN  |
| RFCLKF  | '1': no valid 2 MHz clock available at pin RFCLKF  |
| SCLKI   | '1': no valid 8 MHz clock available at pin SCLKI   |
| CLK16   | '1': no valid 16MHz clock available at pin CLK16   |
| CLK32   | '1': no valid 32 MHz clock available at pin CLK32  |

**IRREQ[6:0]** (Addr.: 08H): **Interrupt-Request**

|   |      |       |    |    |    |     |     |
|---|------|-------|----|----|----|-----|-----|
| - | WDOG | SYNCI | CA | TT | TE | UCC | TSM |
|---|------|-------|----|----|----|-----|-----|

|       |                                                                         |
|-------|-------------------------------------------------------------------------|
| WDOG  | '1': Watchdog interrupt                                                 |
| SYNCI | '1': SYNCI interrupt (no valid SYNCI detected)                          |
| CA    | '1': H-register coefficient available for readout interrupt             |
| TT    | '1': Test termination because of enabled test timeslot interrupt        |
| TE    | '1': Timer expired interrupt                                            |
| UCC   | '1': UCC interrupt                                                      |
| TSM   | '1': Timeslot monitor interrupt, reset when accessing<br>CTRLTSMON.MVAL |

Note: Each bit of this register will generate an interrupt at pin INT if activated (internally set to '1'). The bits and the pin  $\overline{\text{INT}}$  are cleared after read. Setting of these bits by activated source can be inhibited by masking in register IRMASK.

**STATUS[6:0]** (Addr.: 6EH): **Status**

|   |              |               |            |            |            |             |             |
|---|--------------|---------------|------------|------------|------------|-------------|-------------|
| - | WDOG<br>POLL | SYNCI<br>POLL | CA<br>POLL | TT<br>POLL | TE<br>POLL | UCC<br>POLL | TSM<br>POLL |
|---|--------------|---------------|------------|------------|------------|-------------|-------------|

Bits are reset when the interrupt source is no longer valid

|            |                                                               |
|------------|---------------------------------------------------------------|
| WDOG POLL  | '1': Watchdog status                                          |
| SYNCI POLL | '1': SYNCI status (no valid SYNCI detected)                   |
| CA POLL    | '1': H-register coefficient available for readout status      |
| TT POLL    | '1': Test termination because of enabled test timeslot status |
| TE POLL    | '1': Timer expired status                                     |

## Register Description

UCCPOLL        '1': UCC status  
TSMPOLL        '1': Timeslot monitor status

**SFATSES[2:0]** (Addr.: 36H): **S**uper frame **a**larm and requested **t**imeslot **e**n/disable status

|   |   |   |   |   |               |      |     |
|---|---|---|---|---|---------------|------|-----|
| - | - | - | - | - | TSEN<br>VALID | TSEN | SFA |
|---|---|---|---|---|---------------|------|-----|

TSENVALID    '1': TSEN value for the requested TS in register ATE is valid  
                  '0': TSEN value not valid since channel defined in register ATE is not detected yet

TSEN            '1': requested TS in register ATE is enabled, no test recommended  
                  '0': requested TS in register ATE is disabled, test permissible

SFA             '1': alarm, because not synchronized to PCM30 superframe  
                  '0': no alarm, because either synchronization to PCM superframe or TS16 CAS evaluation is deactivated (Bit CONF16.ENTS16 = '0')

**SOTP[6:0]** (Addr.: 3DH): **S**end path **o**utput **t**est **p**attern

|   |         |         |         |         |         |         |         |
|---|---------|---------|---------|---------|---------|---------|---------|
| - | SOTP[6] | SOTP[5] | SOTP[4] | SOTP[3] | SOTP[2] | SOTP[1] | SOTP[0] |
|---|---------|---------|---------|---------|---------|---------|---------|

SOTP[6:0]        Result of background test of timeslot defined in register ATE, amplitude A-/μ-Law encoded

**TESTSTAT[7:0]** (Addr.: 3EH): Background **t**est **s**tatus signals

|       |     |     |        |        |     |     |              |
|-------|-----|-----|--------|--------|-----|-----|--------------|
| DISPS | DIS | NLP | FREEZE | HRESET | ERL | FCM | NO<br>SPEECH |
|-------|-----|-----|--------|--------|-----|-----|--------------|

This register contains results of background test of timeslot defined in register ATE

DISPS            '1': 2100 Hz tone with phase shift detected  
                  '0': no 2100 Hz tone with phase shift detected

DIS               '1': 2100 Hz tone detected  
                  '0': no 2100 Hz tone detected

NLP               '1': NLP active  
                  '0': NLP disabled (bypassed)

FREEZE           '1': H-Register frozen  
                  '0': H-Register not frozen

HRESET           '1': H-Register reset

## Register Description

|          |                                                 |
|----------|-------------------------------------------------|
|          | '0': H-Register not reset                       |
| ERL      | '1': echo return loss > value of BYPTH[4:0]     |
|          | '0': echo return loss not > value of BYPTH[4:0] |
| FCM      | '1': fast convergence mode                      |
|          | '0': normal convergence mode                    |
| NOSPEECH | '1': no speech detected                         |
|          | '0': speech detected                            |

**DIRAM[7:0]** (Addr.: 67H): requested **Data Input RAM** value

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| DIRAM<br>[7] | DIRAM<br>[6] | DIRAM<br>[5] | DIRAM<br>[4] | DIRAM<br>[3] | DIRAM<br>[2] | DIRAM<br>[1] | DIRAM<br>[0] |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

DIRAM[7:0] Requested UCC input data for UCC frame defined in WRUCC.AR[4:0]

**UCCOLD[7:0]** (Addr.: 68H): Changed **UCC** input data **old** value

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| UCC<br>OLD[7] | UCC<br>OLD[6] | UCC<br>OLD[5] | UCC<br>OLD[4] | UCC<br>OLD[3] | UCC<br>OLD[2] | UCC<br>OLD[1] | UCC<br>OLD[0] |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

UCCOLD[7:0] Data prior to the modification of the modified UCC frame that caused the UCC interrupt. The corresponding frame number of the modified frame value is stored in UCCSTAT.AFR[4:0].

**UCCNEW[7:0]** (Addr.: 69H): Changed **UCC** input data **new** value

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| UCC<br>NEW[7] | UCC<br>NEW[6] | UCC<br>NEW[5] | UCC<br>NEW[4] | UCC<br>NEW[3] | UCC<br>NEW[2] | UCC<br>NEW[1] | UCC<br>NEW[0] |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

UCCNEW[7:0] Modified data of the changed UCC frame that caused the UCC interrupt. The corresponding frame number of the modified frame value is stored in UCCSTAT.AFR[4:0].

**UCCSTAT[6:0]** (Addr.: 6AH): **UCC status**

|  |         |            |        |        |        |        |        |
|--|---------|------------|--------|--------|--------|--------|--------|
|  | INVALID | NO<br>SYNC | AFR[4] | AFR[3] | AFR[2] | AFR[1] | AFR[0] |
|--|---------|------------|--------|--------|--------|--------|--------|

INVALID '1': possible data loss, because old interrupt has not yet been processed

## Register Description

'0': modified data valid  
NOSYNC '1': UCC unit is not synchronized to SYNCI pulse, i.e. the SYNCI pulse period is not an integer multiple of 32 UCC frames (4ms).  
'0': UCC unit is synchronized to SYNCI pulse, i.e. a SYNC pulse with a period of an integer multiple of 32 UCC frames (4ms) was detected  
AFR[4:0] value corresponds to the UCC frame that was modified

Note: Read access to this register is identified as acknowledge for the UCC interrupt and should be read after UCCOLD and UCCNEW. This access resets the bit STATUS.UCCPOLL and enables a new UCC interrupt.

### AFCD1[7:0] (Addr.: 7BH): AFI Filter Coefficient Data 1

| COEF<br>[13] | COEF<br>[12] | COEF<br>[11] | COEF<br>[10] | COEF<br>[9] | COEF<br>[8] | COEF<br>[7] | COEF<br>[6] |
|--------------|--------------|--------------|--------------|-------------|-------------|-------------|-------------|
|--------------|--------------|--------------|--------------|-------------|-------------|-------------|-------------|

Read access to this register is identified as acknowledgment for the coefficient availability (CA) interrupt. If an additional access to register AFCD2 and (or) AFCD3 is necessary, register AFCD1 should be read after AFCD2 and (or) AFCD3. This access resets the bit STATUS.CAPOLL and enables a new CA interrupt. The conversion from the 14 bit register value to the linear value is depicted in [Table 37](#).

COEF[13:6] MSB of monitored filter coefficient

### AFCD2[7:0] (Addr.: 7CH): AFI Filter Coefficient Data 2

| ISLAST | - | COEF<br>[5] | COEF<br>[4] | COEF<br>[3] | COEF<br>[2] | COEF<br>[1] | COEF<br>[0] |
|--------|---|-------------|-------------|-------------|-------------|-------------|-------------|
|--------|---|-------------|-------------|-------------|-------------|-------------|-------------|

ISLAST '1': COEF is last coefficient for channel readout  
COEF[5:0] LSB of monitored coefficient. The conversion from the 14 bit register value to the linear value is depicted in [Table 37](#).

**Table 37 AFI Coefficients to Absolute Linear Value Conversion**

| AFI Coefficient Register Value |   |   |   |   |   |   |   |   |   |   |   |   |   | Linear Value |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1                              | 1 | 1 | 1 |   | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 1            | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 3                              | 2 | 1 | 0 | 9 |   |   |   |   |   |   |   |   |   | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |
| S                              | 0 | 0 | 0 | A | B | C | D | E | F | G | H | I | J | S            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | B | C | D | E | F | G | H | I | J |
| S                              | 0 | 0 | 1 | A | B | C | D | E | F | G | H | I | J | S            | 0 | 0 | 0 | 0 | 0 | 0 | 1 | A | B | C | D | E | F | G | H | I | J |
| S                              | 0 | 1 | 0 | A | B | C | D | E | F | G | H | I | J | S            | 0 | 0 | 0 | 0 | 0 | 1 | A | B | C | D | E | F | G | H | I | J | 0 |
| S                              | 0 | 1 | 1 | A | B | C | D | E | F | G | H | I | J | S            | 0 | 0 | 0 | 0 | 1 | A | B | C | D | E | F | G | H | I | J | 0 | 0 |

## Register Description

**Table 37 AFI Coefficients to Absolute Linear Value Conversion**

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | 1 | 0 | 0 | A | B | C | D | E | F | G | H | I | J | S | 0 | 0 | 0 | 1 | A | B | C | D | E | F | G | H | I | J | 0 | 0 | 0 |
| S | 1 | 0 | 1 | A | B | C | D | E | F | G | H | I | J | S | 0 | 0 | 1 | A | B | C | D | E | F | G | H | I | J | 0 | 0 | 0 | 0 |
| S | 1 | 1 | 0 | A | B | C | D | E | F | G | H | I | J | S | 0 | 1 | A | B | C | D | E | F | G | H | I | J | 0 | 0 | 0 | 0 | 0 |
| S | 1 | 1 | 1 | A | B | C | D | E | F | G | H | I | J | S | 1 | A | B | C | D | E | F | G | H | I | J | 0 | 0 | 0 | 0 | 0 | 0 |

### AFCD3[7:0] (Addr.: 7DH): AFI Filter Coefficient Data 3

|                    |                    |                    |                    |                    |                    |                    |                    |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| AUX<br>COEF<br>[9] | AUX<br>COEF<br>[8] | AUX<br>COEF<br>[7] | AUX<br>COEF<br>[6] | AUX<br>COEF<br>[5] | AUX<br>COEF<br>[4] | AUX<br>COEF<br>[3] | AUX<br>COEF<br>[2] |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|

AUXCOEF[9:2] Most significant bits of the auxiliary coefficient monitored

**The following read registers contain channel individual values. The channel number defined in register CTRLTSMON.MCH[4:0]**

Since MVAL is the interrupt source indicating an update of the monitor registers it must be reset after the monitor registers are read out in order to avoid an unwanted interrupt.

### MONSI[7:0] (Addr.: 29H): Monitor send input signal (A-/μ-Law encoded)

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| MON<br>SI[7] | MON<br>SI[6] | MON<br>SI[5] | MON<br>SI[4] | MON<br>SI[3] | MON<br>SI[2] | MON<br>SI[1] | MON<br>SI[0] |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

The content of this register is PCM encoded.

### MONSO[7:0] (Addr.: 2AH): Monitor send output signal (A-/μ-Law encoded)

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| MON<br>SO[7] | MON<br>SO[6] | MON<br>SO[5] | MON<br>SO[4] | MON<br>SO[3] | MON<br>SO[2] | MON<br>SO[1] | MON<br>SO[0] |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

The content of this register is PCM encoded.

### MONRI[7:0] (Addr.: 2BH): Monitor of receive input signal (A-/μ-Law encoded)

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| MON<br>RI[7] | MON<br>RI[6] | MON<br>RI[5] | MON<br>RI[4] | MON<br>RI[3] | MON<br>RI[2] | MON<br>RI[1] | MON<br>RI[0] |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

## Register Description

The content of this register is PCM encoded

**MONSIL[7:0]** (Addr.: 1EH): **Monitor send input level**

| MON<br>SIL[7] | MON<br>SIL[6] | MON<br>SIL[5] | MON<br>SIL[4] | MON<br>SIL[3] | MON<br>SIL[2] | MON<br>SIL[1] | MON<br>SIL[0] |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

The content of this register is encoded logarithmically. The maximum value of 191 corresponds to 3 dBm0. A decrease of 16 is equivalent to a decrease of 6 dB. The following table displays the relation between the register value and the dBm0 value.

| Register Value |        | Level [dBm0]/[dB] | Register Value |        | Level [dBm0]/[dB] |
|----------------|--------|-------------------|----------------|--------|-------------------|
| HEX            | linear |                   | HEX            | linear |                   |
| C0             | 191    | +3                | 58             | 88     | -36               |
| B8             | 184    | 0                 | 50             | 80     | -39               |
| B0             | 176    | -3                | 48             | 72     | -42               |
| A8             | 168    | -6                | 40             | 64     | -45               |
| A0             | 160    | -9                | 38             | 56     | -48               |
| 96             | 152    | -12               | 30             | 48     | -51               |
| 90             | 144    | -15               | 28             | 40     | -54               |
| 88             | 136    | -18               | 20             | 32     | -57               |
| 80             | 128    | -21               | 18             | 24     | -60               |
| 78             | 120    | -24               | 10             | 16     | -63               |
| 70             | 112    | -27               | 08             | 8      | -66               |
| 68             | 104    | -30               | 1              | 1      | -69               |
| 60             | 96     | -33               | 0              | 0      | - infinity        |

**Table 38 Conversion of Monitor Register Values to dBm0 Values**

**MONSOL[7:0]** (Addr.: 1FH): **Monitor send output level**

| MON<br>SOL[7] | MON<br>SOL[6] | MON<br>SOL[5] | MON<br>SOL[4] | MON<br>SOL[3] | MON<br>SOL[2] | MON<br>SOL[1] | MON<br>SOL[0] |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

The content of this register is encoded logarithmically. For conversion to dBm0 see [Table 38](#) .

## Register Description

**MONRIL[7:0]** (Addr.: 20H): **Monitor of receive input level**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| MON<br>RIL[7] | MON<br>RIL[6] | MON<br>RIL[5] | MON<br>RIL[4] | MON<br>RIL[3] | MON<br>RIL[2] | MON<br>RIL[1] | MON<br>RIL[0] |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

The content of this register is encoded logarithmically. For conversion to dBm0 see [Table 38](#) .

**MONOFSI[5:0]** (Addr.: 21H): **Monitor offset in send path input**

|   |   |                |                |                |                |                |                |
|---|---|----------------|----------------|----------------|----------------|----------------|----------------|
| - | - | MON<br>OFSI[5] | MON<br>OFSI[4] | MON<br>OFSI[3] | MON<br>OFSI[2] | MON<br>OFSI[1] | MON<br>OFSI[0] |
|---|---|----------------|----------------|----------------|----------------|----------------|----------------|

The content of this register is a linear value in "1 complement" notation.

**MONOFSO[5:0]** (Addr.: 22H): **Monitor offset in send path output**

|   |   |                |                |                |                |                |                |
|---|---|----------------|----------------|----------------|----------------|----------------|----------------|
| - | - | MON<br>OFSO[5] | MON<br>OFSO[4] | MON<br>OFSO[3] | MON<br>OFSO[2] | MON<br>OFSO[1] | MON<br>OFSO[0] |
|---|---|----------------|----------------|----------------|----------------|----------------|----------------|

The content of this register is a linear value in "1 complement" notation.

**MONAEL[7:0]** (Addr.: 23H): **Monitor artificial echo level**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| MON<br>AEL[7] | MON<br>AEL[6] | MON<br>AEL[5] | MON<br>AEL[4] | MON<br>AEL[3] | MON<br>AEL[2] | MON<br>AEL[1] | MON<br>AEL[0] |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

The content of this register is encoded logarithmically. For conversion to dBm0 see [Table 38](#) .

**MONBNL[6:0]** (Addr. 24H): **Monitor background noise level**

|   |               |               |               |               |               |               |               |
|---|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| - | MON<br>BNL[6] | MON<br>BNL[5] | MON<br>BNL[4] | MON<br>BNL[3] | MON<br>BNL[2] | MON<br>BNL[1] | MON<br>BNL[0] |
|---|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

The content of this register is encoded logarithmically. For conversion to dBm0 see [Table 38](#) .

## Register Description

**MONERL[7:0]** (Addr.: 25H): **Monitor Echo return loss**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| MON<br>ERL[7] | MON<br>ERL[6] | MON<br>ERL[5] | MON<br>ERL[4] | MON<br>ERL[3] | MON<br>ERL[2] | MON<br>ERL[1] | MON<br>ERL[0] |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

The content of this register is encoded logarithmically. For conversion to dB see [Table 38](#).

**MONCL[7:0]** (Addr.: 26H): **Monitor combined loss without NLP**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| MON<br>CL[7] | MON<br>CL[6] | MON<br>CL[5] | MON<br>CL[4] | MON<br>CL[3] | MON<br>CL[2] | MON<br>CL[1] | MON<br>CL[0] |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

The content of this register is encoded logarithmically. For conversion to dB see [Table 38](#).

**MONNLPTH[7:0]** (Addr.: 27H): **Monitor NLP threshold level**

|                      |                      |                      |                      |                      |                      |                      |                      |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| MON<br>NLP<br>THL[7] | MON<br>NLP<br>THL[6] | MON<br>NLP<br>THL[5] | MON<br>NLP<br>THL[4] | MON<br>NLP<br>THL[3] | MON<br>NLP<br>THL[2] | MON<br>NLP<br>THL[1] | MON<br>NLP<br>THL[0] |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|

The content of this register is encoded logarithmically. For conversion to dBm0 see [Table 38](#).

**MONOCDT[7:0]** (Addr.: 28H): **Monitor overcompensation and double talk hang-over time**

|               |               |               |               |                     |                     |                     |                     |
|---------------|---------------|---------------|---------------|---------------------|---------------------|---------------------|---------------------|
| MON<br>OCE[3] | MON<br>OCE[2] | MON<br>OCE[1] | MON<br>OCE[0] | MON<br>DTHOT<br>[3] | MON<br>DTHOT<br>[2] | MON<br>DTHOT<br>[1] | MON<br>DTHOT<br>[0] |
|---------------|---------------|---------------|---------------|---------------------|---------------------|---------------------|---------------------|

MONOCE[3:0] Overcompensation evaluation

MONDTHOT[3:0] Double talk hang-over time

**MONSTAT1[7:0]** (Addr.: 2CH): **Monitor of internal/external control states 1**

|     |                  |          |            |           |             |          |           |
|-----|------------------|----------|------------|-----------|-------------|----------|-----------|
| MNS | M<br>DIS<br>NOSP | M<br>DIS | M<br>DISPS | M<br>HRES | M<br>FREEZE | M<br>NLP | M<br>ECBP |
|-----|------------------|----------|------------|-----------|-------------|----------|-----------|

## Register Description

|          |                                                             |
|----------|-------------------------------------------------------------|
| MNS      | '1': "no-voice" detected                                    |
| MDISNOSP | '1': 2100Hz detected but without speech protection          |
| MDIS     | '1': 2100Hz detected with speech protection                 |
| MDISPS   | '1': 2100Hz with phase shift and speech protection detected |
| MHRES    | '1': H-Register reset                                       |
| MFREEZE  | '1': H-Register frozen                                      |
| MNLP     | '1': NLP active                                             |
| MECBP    | '1': Entire echo cancellation path bypassed                 |

### MONSTAT2[7:0] (Addr.: 2DH): **Monitor of internal/external control states 2**

|            |         |          |           |                  |                 |                |           |
|------------|---------|----------|-----------|------------------|-----------------|----------------|-----------|
| M<br>ERLBP | M<br>DT | M<br>FCM | M<br>CSPR | M<br>NR7<br>NOSP | M<br>NR7<br>DIS | M<br>NR7<br>BY | M<br>IDLE |
|------------|---------|----------|-----------|------------------|-----------------|----------------|-----------|

The contents of individual bits of this register can also be output at pin FLEXMON1 or FLEXMON2 if configured in register CONFLEXMON.

|          |                                                                                   |
|----------|-----------------------------------------------------------------------------------|
| MERLBP   | '1': Subtractor bypassed because ERL > value of BYPTH[4:0]                        |
| MDT      | '1': near end subscriber is louder than the far end subscriber (true double talk) |
| MFCM     | '1': Fast convergence mode active                                                 |
| MCSPR    | '1': Convergence stability protection for non-speech signals active               |
| MNR7NOSP | '1': 2010Hz (SS Nr.7) detected but without speech protection                      |
| MNR7DIS  | '1': 2010Hz speech protection: second level reached (H-Register reset)            |
| MNR7BY   | '1': 2010Hz speech protection: first level reached (bypass of entire canceller)   |
| MIDLE    | '1': Idle channel detected                                                        |

### MONSTAT3[7:0] (Addr.: 2EH): **Monitor of internal/external control states 3**

|           |           |            |            |                |               |                    |               |
|-----------|-----------|------------|------------|----------------|---------------|--------------------|---------------|
| M<br>TS16 | M<br>UCCD | M<br>UCCFX | M<br>SCDIS | MSC<br>NLDPDIS | MSC<br>FREEZE | MSC<br>CONV<br>DIS | MFLEX<br>SCTR |
|-----------|-----------|------------|------------|----------------|---------------|--------------------|---------------|

|            |                                              |
|------------|----------------------------------------------|
| MTS16      | '1': channel disabled by TS16 CAS evaluation |
| MUCCD      | '1': disable by UCC-DIS-Bit active           |
| MUCCFX     | '1': UCC-FX bit active                       |
| MSCDIS     | '1': serial control signal DIS active        |
| MSCNLDPDIS | '1': serial control signal NLDPDIS active    |
| MSCFREEZE  | '1': serial control signal FREEZE active     |

---

**Register Description**

|            |                                            |
|------------|--------------------------------------------|
| MSCCONVDIS | '1': serial control signal CONVDIS active  |
| MFLEXSCTR  | '1': serial control signal FLEXSCTR active |

## 6 Electrical Characteristics

### 6.1 Absolute Maximum Ratings

| Parameter                                                                                            |     | Symbol        | Limit Values | Unit |
|------------------------------------------------------------------------------------------------------|-----|---------------|--------------|------|
| Ambient temperature under bias                                                                       | PEB | $T_A$         | 0 to 70      | °C   |
|                                                                                                      | PEF | $T_A$         | – 40 to 85   | °C   |
| Storage temperature                                                                                  |     | $T_{stg}$     | – 65 to 125  | °C   |
| IC supply voltage                                                                                    |     | $V_{DD}$      | 0 to 3.6     | V    |
| Voltage on any functional pin ( <b>not</b> $V_{DD}$ and <b>not</b> $V_{SS}$ ) with respect to ground |     | $V_S$         | -0.4 to 5.5  | V    |
| ESD robustness <sup>1)</sup><br>HBM: 1.5 kΩ, 100 pF                                                  |     | $V_{ESD,HBM}$ | 2000         | V    |

<sup>1)</sup> According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

**Note:** Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 6.2 Operating Range

| Parameter                      | Symbol   | Limit Values |      | Unit | Test Condition |
|--------------------------------|----------|--------------|------|------|----------------|
|                                |          | min.         | max. |      |                |
| Ambient temperature PEB<br>PEF | $T_A$    | 0            | 70   | °C   |                |
|                                | $T_A$    | -40          | 85   | °C   |                |
| Supply voltage                 | $V_{DD}$ | 3.0          | 3.6  | V    |                |
| Ground                         | $V_{SS}$ | 0            | 0    | V    |                |

**Note:** In the operating range, the functions given in the circuit description are fulfilled.

## Electrical Characteristics

### 6.3 DC Characteristics

| Parameter                 | Symbol                | Limit Values |                   | Unit          | Notes                                                                                          |
|---------------------------|-----------------------|--------------|-------------------|---------------|------------------------------------------------------------------------------------------------|
|                           |                       | min.         | max.              |               |                                                                                                |
| Input low voltage         | $V_{IL}$              | - 0.4        | 0.8               | V             | <sup>1)</sup>                                                                                  |
| Input high voltage        | $V_{IH}$              | 2.0          | 5.5               | V             |                                                                                                |
| Output low voltage        | $V_{OL}$              |              | 0.45              | V             | $I_{OL} = 4 \text{ mA}$ <sup>2)</sup><br>$I_{OL} = 2.5 \text{ mA}$ <sup>3)</sup>               |
| Output high voltage       | $V_{OH}$              | 2.4          |                   | V             | $I_{OH} = - 1.0 \text{ mA}$                                                                    |
| Avg. power supply current | $I_{CC} \text{ (AV)}$ |              | 350 <sup>4)</sup> | mA            | $V_{DD} = 3.3 \text{ V}$ ,<br>$T_A = 25^\circ \text{C}$ :                                      |
| Input leakage current     | $I_{IL}$              |              | 5                 | $\mu\text{A}$ | $V_{DD} = 3.3 \text{ V}$ ,<br>GND = 0 V; all other pins are floating; $V_{IN} = 0 \text{ V}$ , |
| Output leakage current    | $I_{OZ}$              |              | 5                 | $\mu\text{A}$ | $V_{DD} = 3.3 \text{ V}$ ,<br>GND = 0 V;<br>$V_{OUT} = 0 \text{ V}$ ,                          |

<sup>1)</sup> Permanent exposure to negative input voltages may result in minor degradation of lifetime

<sup>2)</sup> Apply to the following O or I/O pins:  
UUPIO0, UPIO1, UPIO2, UPIO3, AD[0:6],  $\overline{\text{RDY}}$ , UPRES,  $\overline{\text{UPRES}}$ ,  $\overline{\text{INT}}$ , RO, SO, TMFBO, CLK4O, SYNCO, SCLKO, SDECO, UCCO,  $\overline{\text{TUCCO}}$

<sup>3)</sup> Apply to all the I/O and O pins that do not appear in the list in note [Figure 2](#))

*The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25^\circ \text{C}$  and the given supply voltage.*

<sup>4)</sup> Not subject to production test - verified by design/characterization.

## 6.4 AC Characteristics

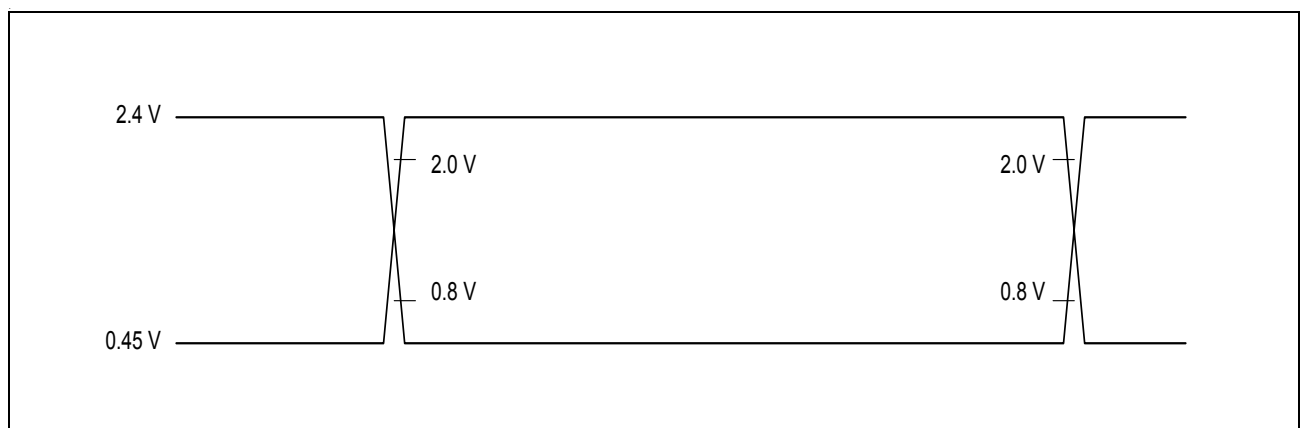
| Parameter           | Symbol   | Limit Values |      | Unit | Notes                                                                            |
|---------------------|----------|--------------|------|------|----------------------------------------------------------------------------------|
|                     |          | min.         | max. |      |                                                                                  |
| Input low voltage   | $V_{il}$ |              | 0.45 | V    | <sup>1)</sup>                                                                    |
| Input high voltage  | $V_{ih}$ | 2.4          |      | V    |                                                                                  |
| Output low voltage  | $V_{ol}$ |              | 0.8  | V    | $I_{ol} = 4 \text{ mA}$ <sup>2)</sup><br>$I_{ol} = 2.5 \text{ mA}$ <sup>3)</sup> |
| Output high voltage | $V_{oh}$ | 2.0          |      | V    | $I_{ol} = -1.0 \text{ mA}$                                                       |

<sup>1)</sup> Permanent exposure to negative input voltages may result in minor degradation of lifetime

<sup>2)</sup> Apply to the following O or I/O pins:  
UPIO0, UPIO1, UPIO2, UPIO3, AD[0:6],  $\overline{\text{RDY}}$ ,  $\overline{\text{UPRES}}$ ,  $\overline{\text{INT}}$ , RO, SO, TMFBO, CLK40, SYNCO, SCLKO, SDECO, UCCO,  $\overline{\text{TUCCO}}$

<sup>3)</sup> Apply to all the I/O and O pins that do not appear in the list in note [Figure 2\)](#)

*The listed characteristics are ensured over the operating range of the integrated circuit.  
Typical characteristics specify mean values expected over the production spread.  
If not otherwise specified, typical characteristics apply at  $T_A = 25^\circ\text{C}$  and the given supply voltage*



**Figure 29 Input/Output Waveforms for AC-Tests**

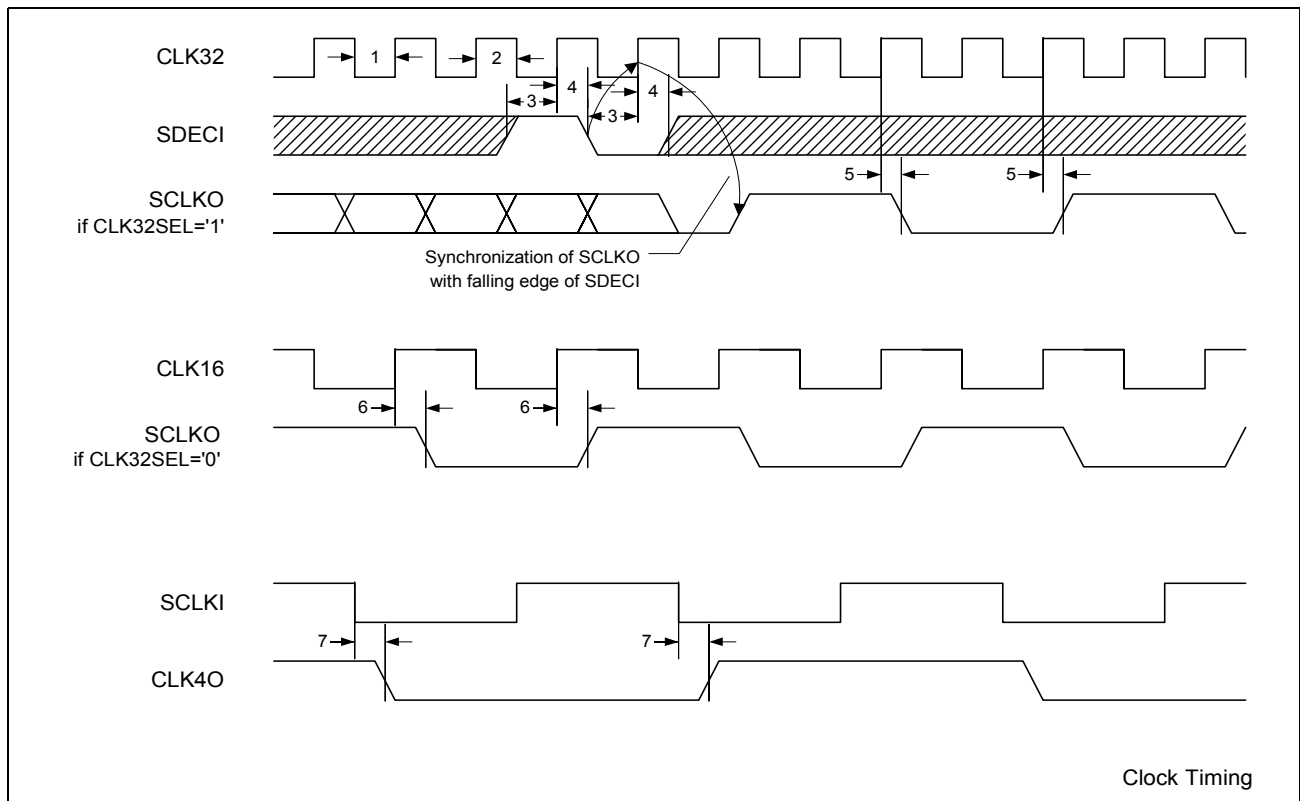
## 6.5 Capacitances

| Parameter                | Symbol     | Limit Values |      | Unit | Notes                                                                             |
|--------------------------|------------|--------------|------|------|-----------------------------------------------------------------------------------|
|                          |            | min.         | max. |      |                                                                                   |
| Clock input capacitance  | $C_{XIN}$  |              | 10   | pF   | $f_C = 1 \text{ MHz}$<br>The pins, which are not under test, are connected to GND |
| Clock output capacitance | $C_{XOUT}$ |              | 10   | pF   |                                                                                   |
| Input capacitance        | $C_{IN}$   |              | 10   | pF   |                                                                                   |
| Output capacitance       | $C_{OUT}$  |              | 10   | pF   |                                                                                   |

## 6.6 Timing Diagrams

*Note: All timing parameters are no subject to production tests. These parameters are verified by design/characterization only.*

### 6.6.1 Clock Timing



**Figure 30 Clock Timing**

**Table 39 Clock Timing Characteristics (preliminary)**

| No. | Name                | Parameter                       | Limit Values |      | Unit |
|-----|---------------------|---------------------------------|--------------|------|------|
|     |                     |                                 | min.         | max. |      |
| 1   | t_clk32_low         | CLK32 low time                  | 12           |      | ns   |
| 2   | t_clk32_high        | CLK32 high time                 | 12           |      | ns   |
| 3   | t_sdeci_setup       | SDECI setup time before CLK32Y  | 10           |      | ns   |
| 4   | t_sdeci_hold        | SDECI hold time after CLK 32Y   | 15           |      | ns   |
| 5   | t_sclko_delay_clk32 | SCLKO output delay after CLK32Y |              | 30   | ns   |

## Electrical Characteristics

**Table 39 Clock Timing Characteristics (preliminary) (cont'd)**

| No. | Name                | Parameter                        | Limit Values |      | Unit |
|-----|---------------------|----------------------------------|--------------|------|------|
|     |                     |                                  | min.         | max. |      |
| 6   | t_sclko_delay_clk16 | SCLKO output delay after CLK16Y  | 0            | 30   | ns   |
| 7   | t_clk4o_delay       | CLK4O output delay after SCLKI Z | 0            | 30   | ns   |

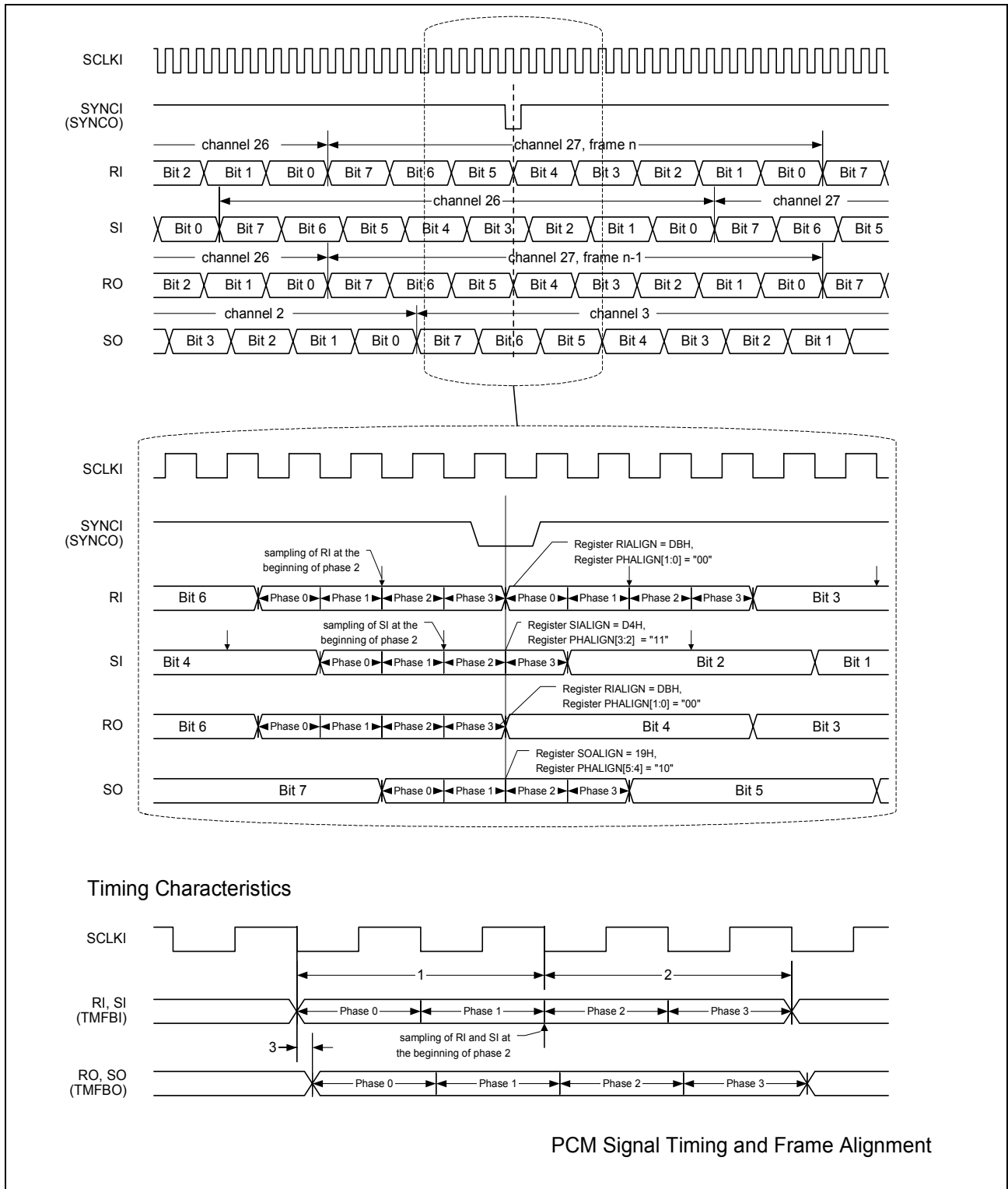
**Table 40 Periods of Clock Signals**

| No. | Parameter | min. | nom.   | Unit |
|-----|-----------|------|--------|------|
|     | CLK32     | 30   | 30.52  | ns   |
|     | CLK16     |      | 61.04  | ns   |
|     | SCLKI     |      | 122.07 | ns   |
|     | CLK4O     |      | 244.14 | ns   |

### 6.6.2 PCM Signal Timing and Frame Alignment

The SIDEC requires the MSB (bit7) first and the LSB (bit0) last as input.

## Electrical Characteristics



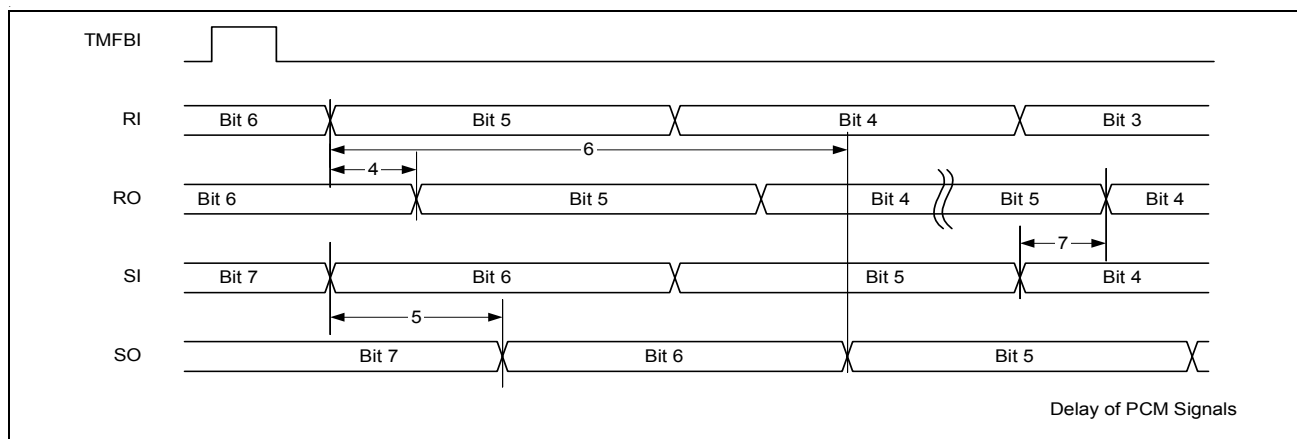
**Figure 31 PCM Signal Timing and Frame Alignment**

**Note:** Above values are examples only. PCM frame alignment with respect to the first detection of an active SYNCl (or SYNCO: If no SYNCl is applied, SYNCO takes over the part and role of SYNCl) with the falling edge of SCLKI can be configured by writing to the

## Electrical Characteristics

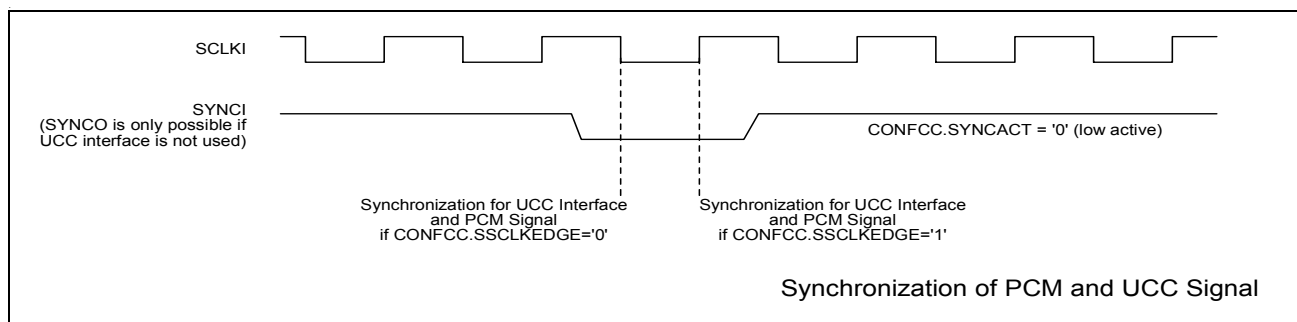
registers RIALIGN, SIALIGN and SOALIGN. For finer adjustments, the valid bit phase of the PCM signals at the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the register PHALIGN. The configured frame and bit phase alignment always denotes the beginning of the ideal bit phase (no signal delay) at the falling edge of SCLKI.

PCM inputs are always sampled with the falling edge of SCLKI at the beginning of bit phase 2, outputs are clocked with the falling edge of SCLKI at the beginning of bit phase 0. Unless not bypassed the PCM output RO has a fixed delay of one PCM frame (125  $\mu$ s) with respect to RI.



**Figure 32 Delay of PCM Signals**

**Figure 33** illustrates the synchronization of the 2048 kBit/s PCM and UCC signal for a low active SYNCI signal with respect to the internal 8192 kHz SCLKI signal. If SYNCI is sampled with the falling edge of SCLKI (CONFCC.SSCLKEDGE='0') this edge is the synchronization point for PCM and UCC signals. If SYNCI is sampled with the rising edge of SCLKI (CONFCC.SSCLKEDGE='1') the next falling SCLKI edge is the synchronization point for PCM and UCC signals. The SYNCO signal may only be used instead of the SYNCI signal if the UCC Interface is not used



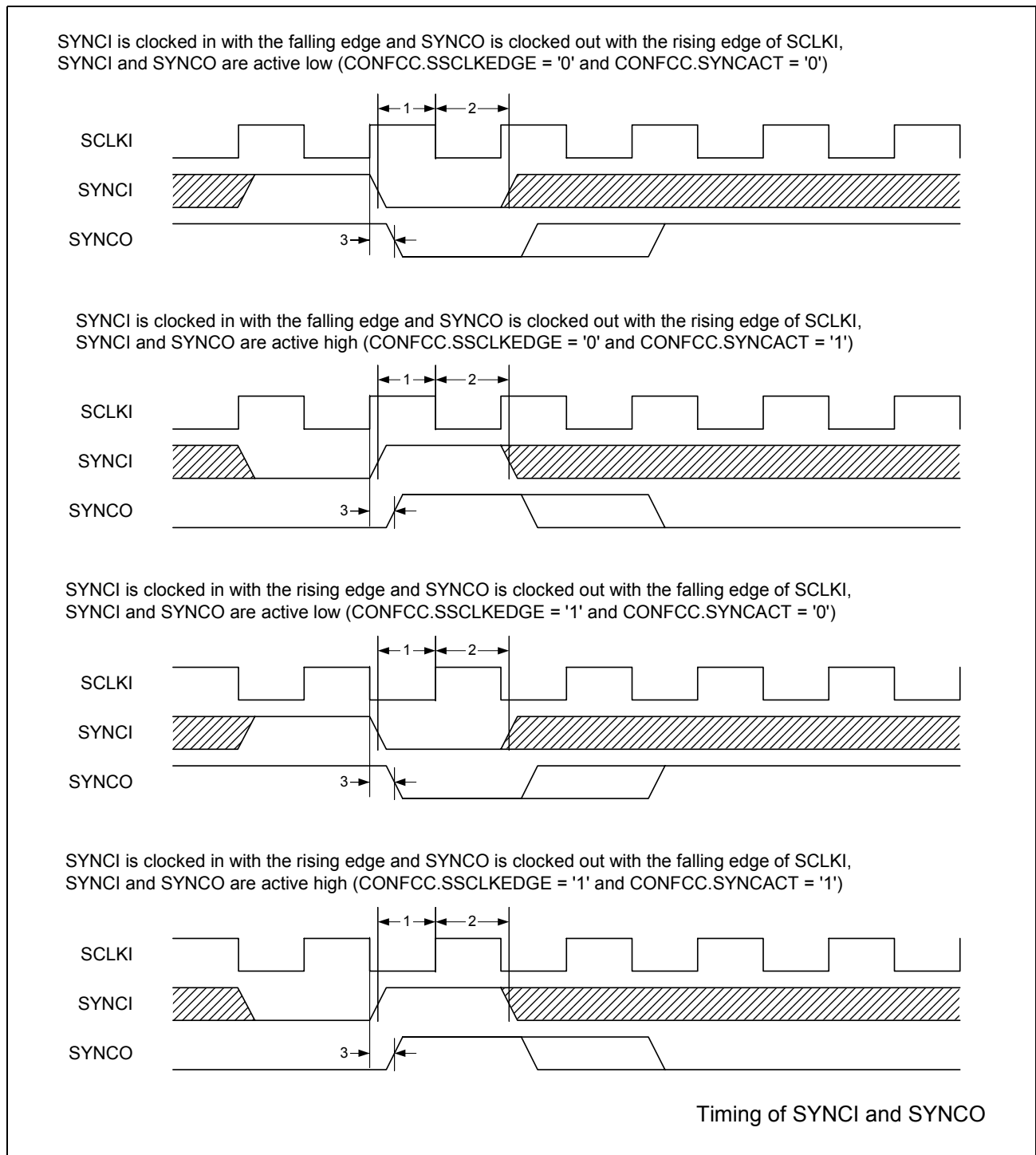
**Figure 33 PCM and UCC Signal synchronization to SCLKI and SYNCI**

Electrical Characteristics

**Table 41 PCM Signal Timing and Frame Characteristics (preliminary)**

| No. |                   | Parameter                                                            | Limit Values |      | Unit |
|-----|-------------------|----------------------------------------------------------------------|--------------|------|------|
|     |                   |                                                                      | min.         | max. |      |
| 1   | t_pcm_setup       | PCM input (RI,SI)<br>input setup time before<br>sampling with SCLKIZ | 15           |      | ns   |
| 2   | t_pcm_hold        | PCM input (RI,SI)<br>input hold time after<br>sampling with SCLKIZ   | 15           |      | ns   |
| 3   | t_pcm_delay       | PCM output (RO,SO)<br>delay after SCLKIZ                             | 0            | 30   | ns   |
| 4   | t_pcm_ri2ro_delay | delay for bypass RI to<br>RO                                         | 0            | 30   | ns   |
| 5   | t_pcm_si2so_delay | delay for bypass SI to<br>SO                                         | 0            | 30   | ns   |
| 6   | t_pcm_ri2so_delay | delay for bypass RI to<br>SO                                         | 0            | 30   | ns   |
| 7   | t_pcm_si2ro_delay | delay for bypass SI to<br>RO                                         | 0            | 30   | ns   |

### 6.6.3 Timing of SYNCI and SYNCO



**Figure 34** Timing of SYNCI and SYNCO

**Figure 34** shows the timing of the synchronization pulses for different configurations.

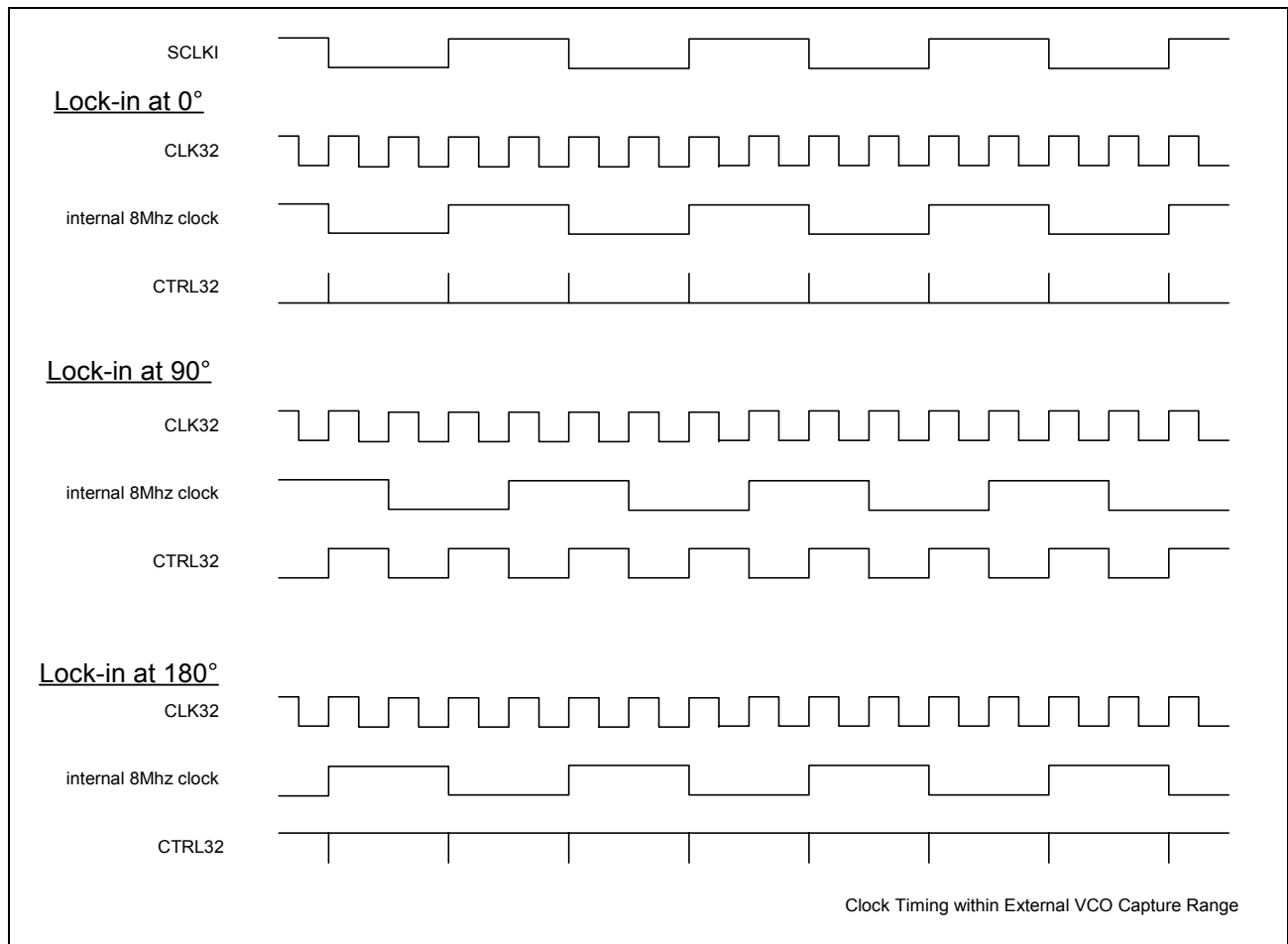
**Note:** The duration of SYNCO pulse can be configured by register CONFCC.SYNCODUR to either one or two SCLKI (8.192 MHz) periods.

Electrical Characteristics

**Table 42 Characteristics of Timing of SYNCI and SYNCO (preliminary)**

| No. | Name          | Parameter                                             | Limit Values |      | Unit |
|-----|---------------|-------------------------------------------------------|--------------|------|------|
|     |               |                                                       | min.         | max. |      |
| 1   | t_synci_setup | SYNCI setup time before active sampling edge of SCLKI | 10           |      | ns   |
| 2   | t_synci_hold  | SYNCI hold time after active sampling edge of SCLKI   | 10           |      | ns   |
| 3   | t_synco_delay | SYNCO delay after active output edge of SCLKI         | 0            | 30   | ns   |

#### 6.6.4 Clock Timing within External VCO Capture Range

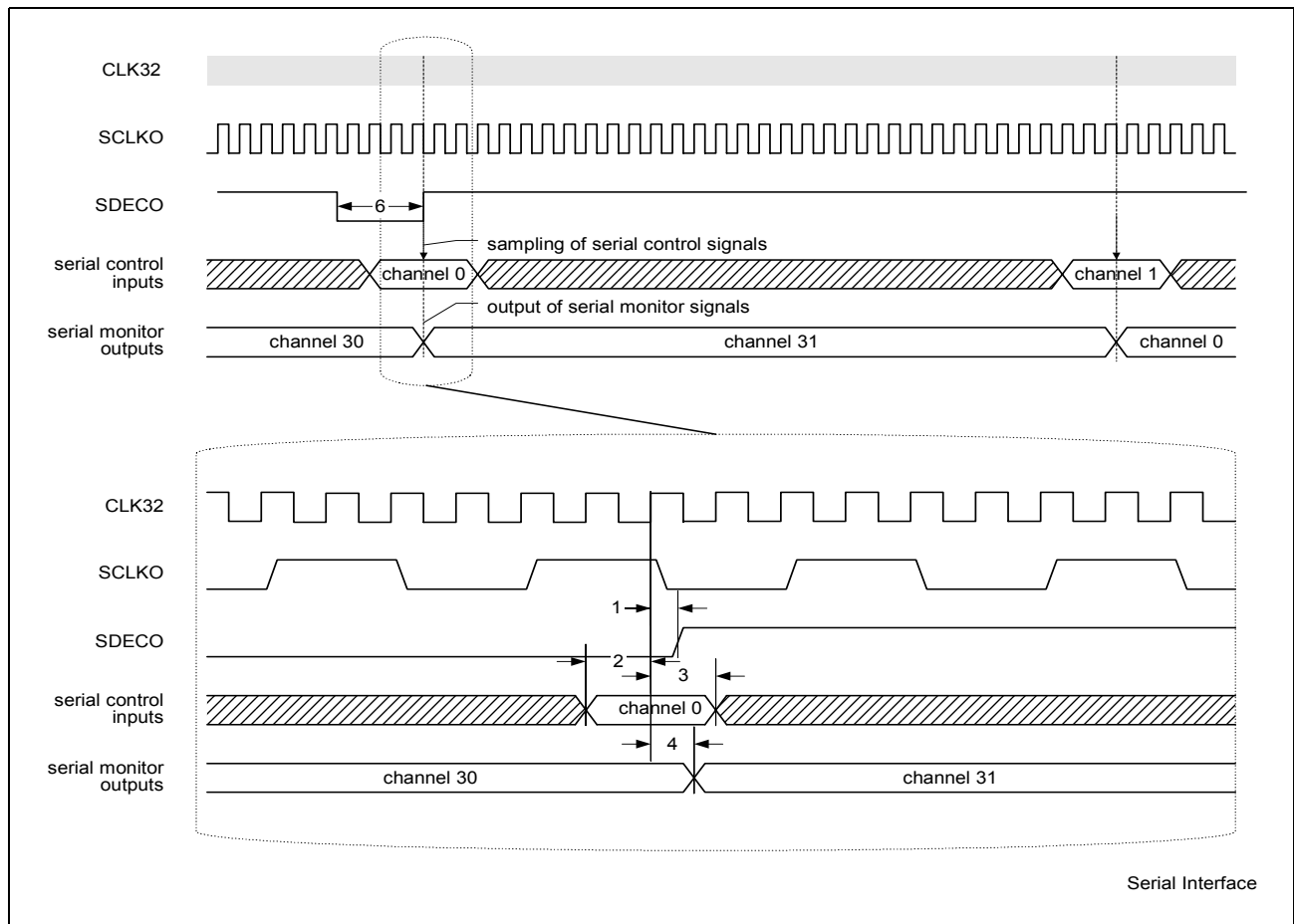


**Figure 35 Clock Timing within External VCO Capture Range**

In case a 32.768 MHz clock has to be generated and synchronized to the system clock at SCLKI, the signal at pin CTRL32 can be used to control an external VCO. The output at CTRL32 is the signal at SCLKI that is internally 'xored' with an internal 8.192 MHz clock that is derived from the signal pin CLK32 by division by 4. For proper operation of the SIDEDEC the system clock SCLKI and the internal 8.192 MHz clock must lock in within the capture range from 0° to 180°. CTRL32 can be inverted by bit CONFCC.INVCTRL32 for use of VCOs that increase the frequency with falling voltage.

The internal 8.192 MHz clock can be monitored at pin SCLKO with a delay of three CLK32 periods plus internal signal delay if pin CLK32SEL is set to logic '1'.

## 6.6.5 Serial Interface (Controlling and Monitoring) Timing



**Figure 36** Serial Interface (Controlling and Monitoring) Timing

**Table 43** Serial Interface (Controlling and Monitoring) Timing (preliminary)

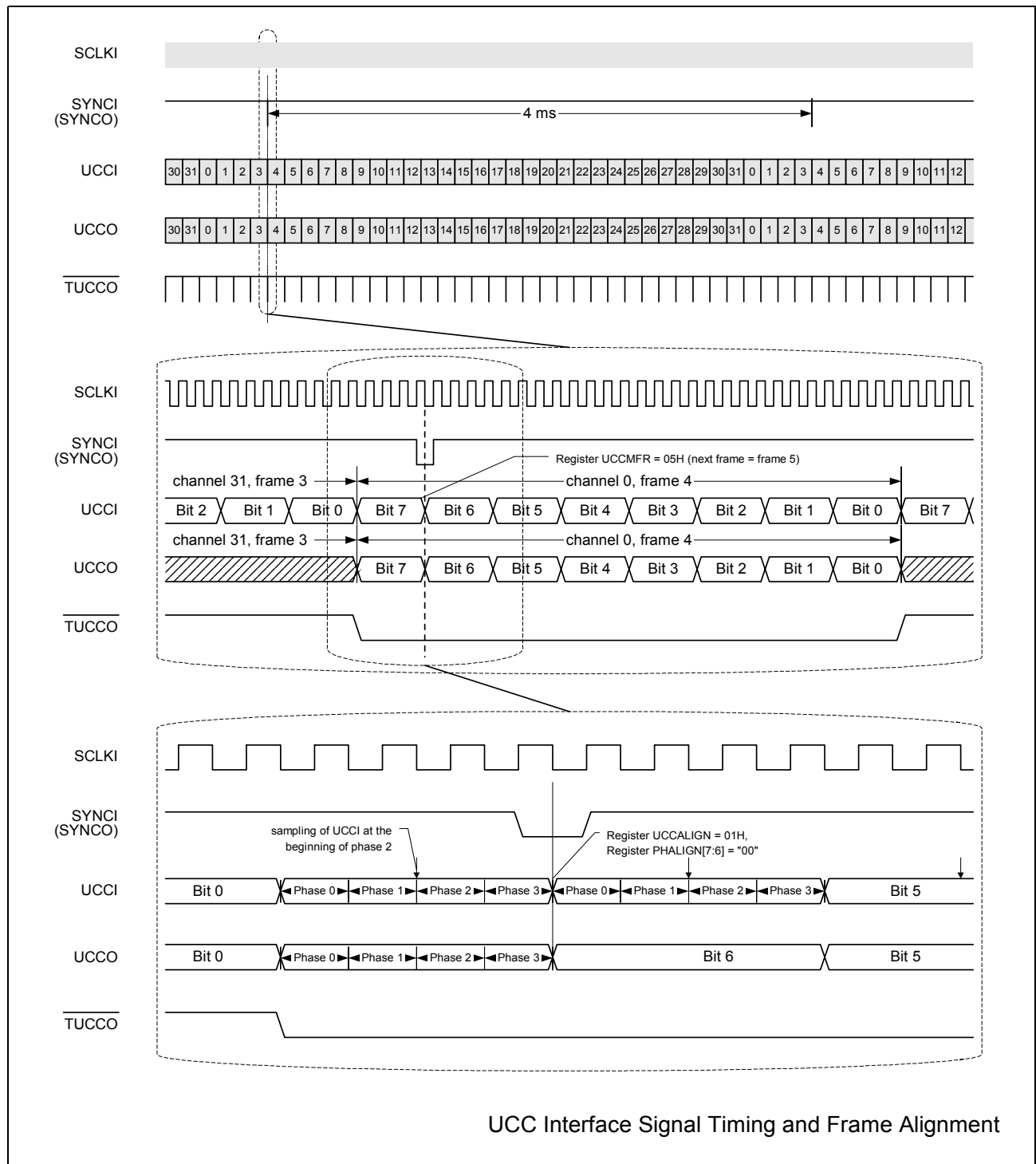
| No. | Name          | Parameter                                                    | Limit Values |      | Unit |
|-----|---------------|--------------------------------------------------------------|--------------|------|------|
|     |               |                                                              | min.         | max. |      |
| 1   | t_sdeco_delay | SDECO output delay after CLK32Y                              | 0            | 30   | ns   |
| 2   | t_sctr_setup  | Serial control signal setup time before sampling with CLK32Y | 15           |      | ns   |
| 3   | t_sctr_hold   | Serial control signal hold time after sampling with CLK32Y   | 15           |      | ns   |

Electrical Characteristics

**Table 43 Serial Interface (Controlling and Monitoring) Timing (preliminary)**

| No. | Name         | Parameter                                       | Limit Values      |      | Unit |
|-----|--------------|-------------------------------------------------|-------------------|------|------|
|     |              |                                                 | min.              | max. |      |
| 4   | t_smon_delay | Serial monitor signal output delay after CLK32Y | 0                 | 33   | ns   |
| 5   |              | SDECO duration                                  | 16 * CLK32 period |      |      |

## 6.6.6 UCC Interface Signal Timing and Frame Alignment



**Figure 37 UCC Interface Signal Timing and Frame Alignment**

**Note:** Above values are examples only. For the use of the UCC Interface a SYNCI signal with a period of 4 ms (equivalent to one multiframe) must be applied to the SIDECD. UCC frame and multiframe alignment with respect to the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the registers UCCALIGN

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## Electrical Characteristics

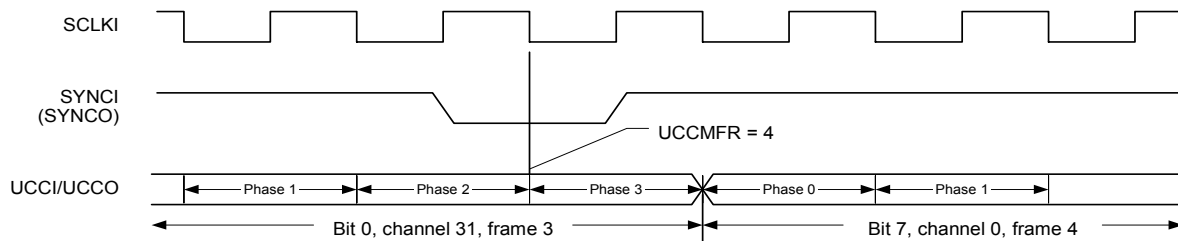
and UCCMFR. For finer adjustments, the valid bit phase of the UCC signals at the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the two MSBs of register PHALIGN.

The configured frame and bit phase alignment always denotes the beginning of the ideal bit phase (no signal delay) at the falling edge of SCLKI. If SYNCI is sampled with the falling edge of SCLKI (CONFCC.SSCLKEDGE='0') this edge is the synchronization point for PCM and UCC signals. If SYNCI is sampled with the rising edge of SCLKI (CONFCC.SSCLKEDGE='1') the next falling SCLKI edge is the synchronization point for PCM and UCC signals. This behavior is identical to the PCM signal behavior and illustrated in [Figure 33](#) in [Chapter 6.6.2](#)

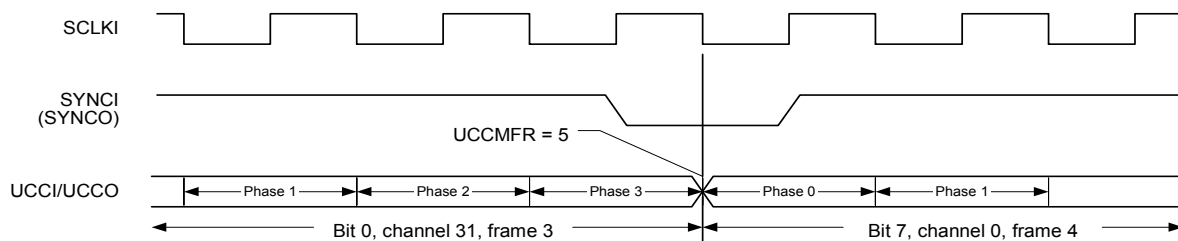
UCC inputs are always sampled with the falling edge of SCLKI at the beginning of bit phase 2, UCCO and  $\overline{\text{TUCCO}}$  are clocked out with the falling edge of SCLKI at the beginning of bit phase 0. The value of register UCCMFR denotes the frame number of the next complete frame that starts with phase 0, bit 7, channel 0 **after** the first detection of an active SYNCI with the falling edge of SCLKI (see figure below).

### Special Cases for Multiframe Alignment

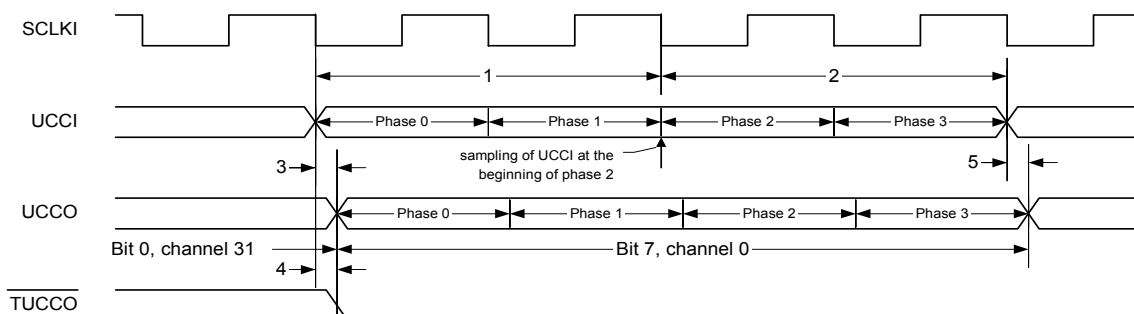
#### Case 1: SYNCI at channel 31, bit 0, phase 3



#### Case 2: SYNCI at channel 0, bit 7, phase 0



### Timing Characteristics



Special Case for Multiframe Alignment

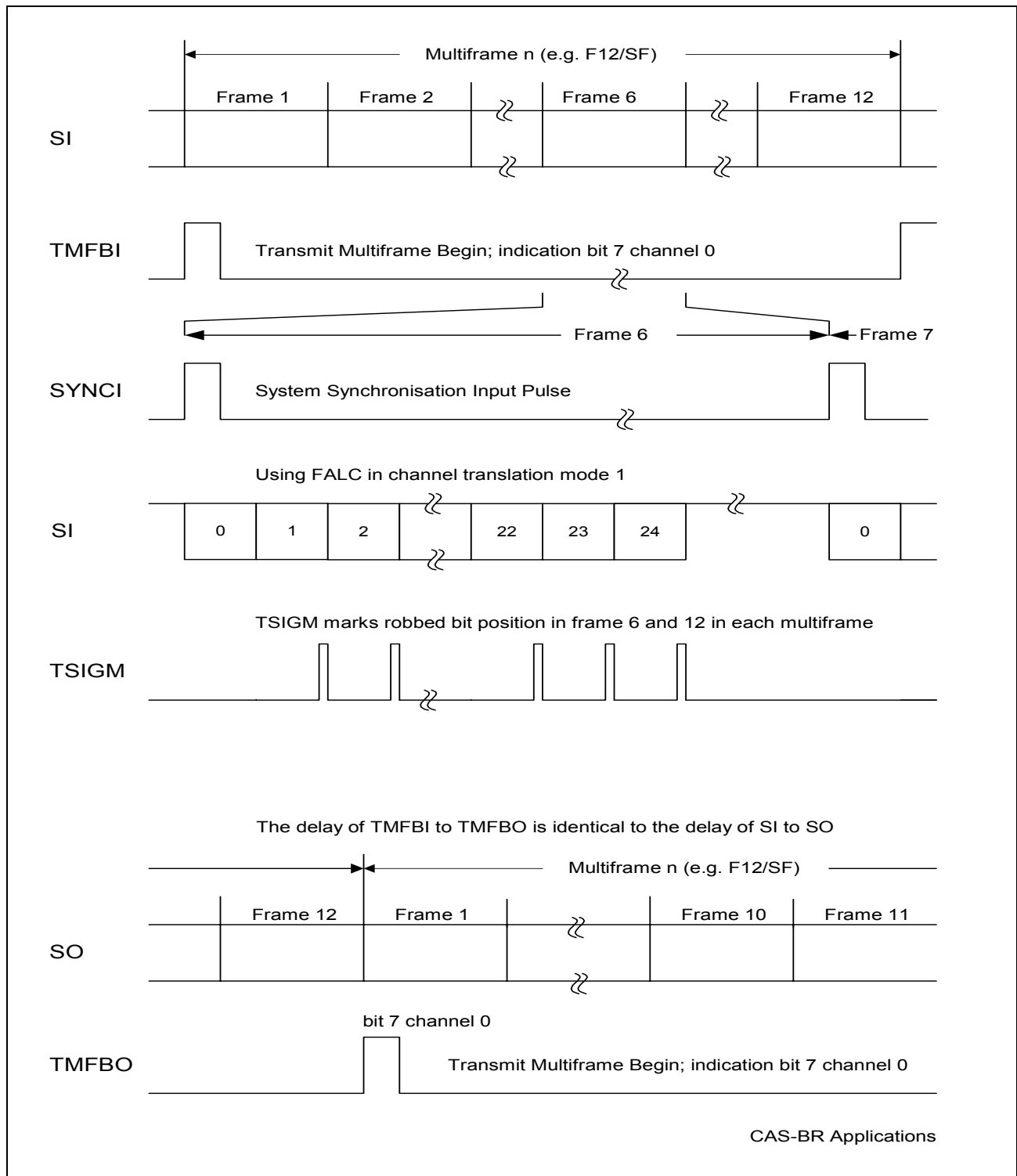
Figure 38 Special Cases for Multiframe Alignment and Timing Characteristics

## Electrical Characteristics

**Table 44 UCC Interface Signal Timing and Frame Alignment (preliminary)**

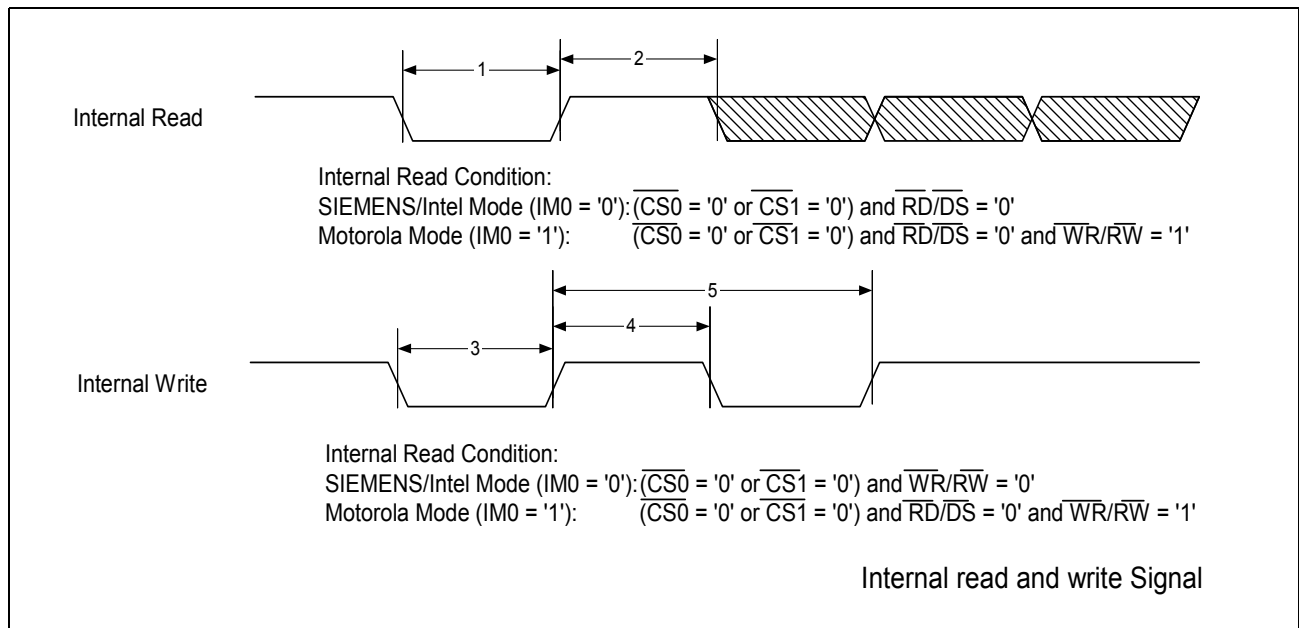
| No. | Name                | Parameter                                                | Limit Values |      | Unit |
|-----|---------------------|----------------------------------------------------------|--------------|------|------|
|     |                     |                                                          | min.         | max. |      |
| 1   | t_ucci_setup        | UCCI input setup time before sampling with SCLKIZ        | 15           |      | ns   |
| 2   | t_ucci_hold         | UCCI input hold time after sampling with SCLKIZ          | 15           |      | ns   |
| 3   | t_ucco_delay        | UCCO output delay after SCLKIZ                           | 0            | 30   | ns   |
| 4   | t_tucco_delay       | $\overline{\text{TUCCO}}$ output delay after SCLKIZ      | 0            | 30   | ns   |
| 5   | t_ucc_reflect_delay | Propagation delay from UCCI to UCCO for UCC reflect mode | 0            | 30   | ns   |

## 6.6.7 Speech Highway Control Signals for CAS in T1 Systems



**Figure 39 Timing of Supporting signals for CAS-BR Applications**

## 6.6.8 Microprocessor Interface



**Figure 40 Internal Read Signal and Internal Write Signal**

**Table 45 Preliminary Internal Read and Write Signal Timing**

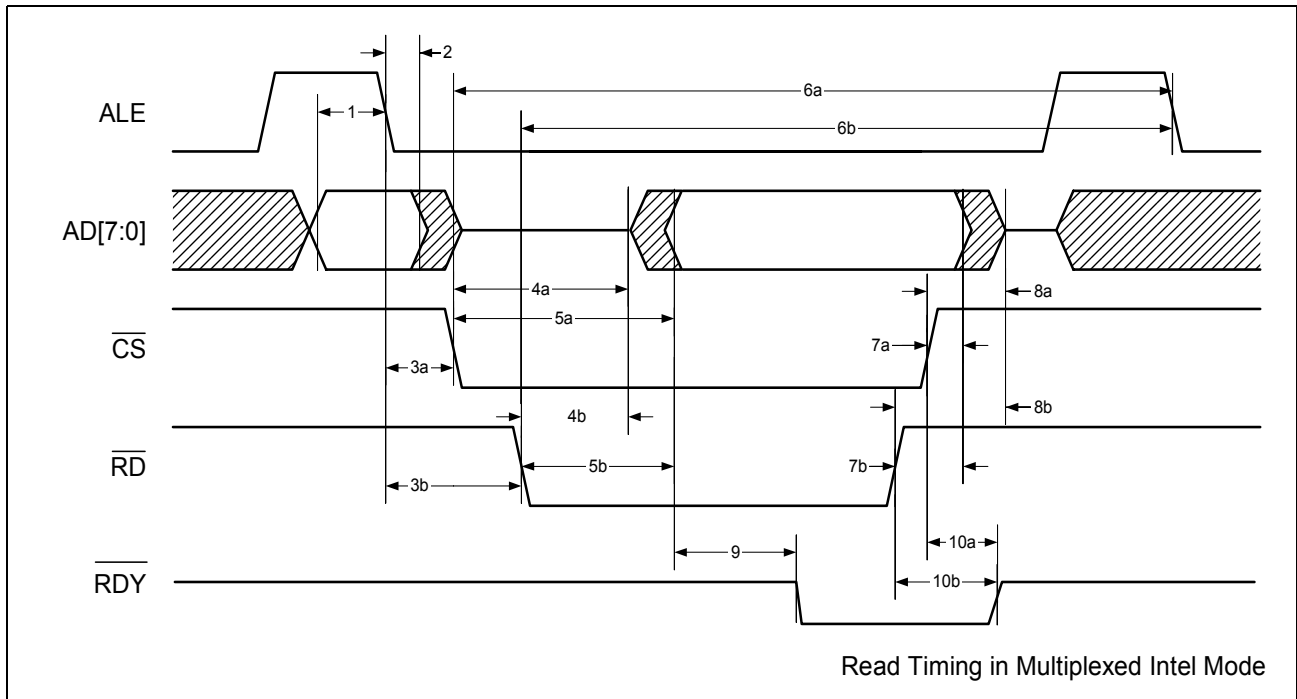
| No. | Parameter                                      | Limit Values |      | Unit |
|-----|------------------------------------------------|--------------|------|------|
|     |                                                | min.         | max. |      |
| 1   | Active time                                    | 40           |      | ns   |
| 2   | Inactive time                                  | 40           |      | ns   |
| 3   | Active time                                    | 40           |      | ns   |
| 4   | Inactive time                                  | 40           |      | ns   |
| 5   | Interval between two active rising write edges | 120          |      | ns   |

The written value of a register will be valid for read back 120 ns after rising edge of the  $\overline{WR/RW}$  signal.

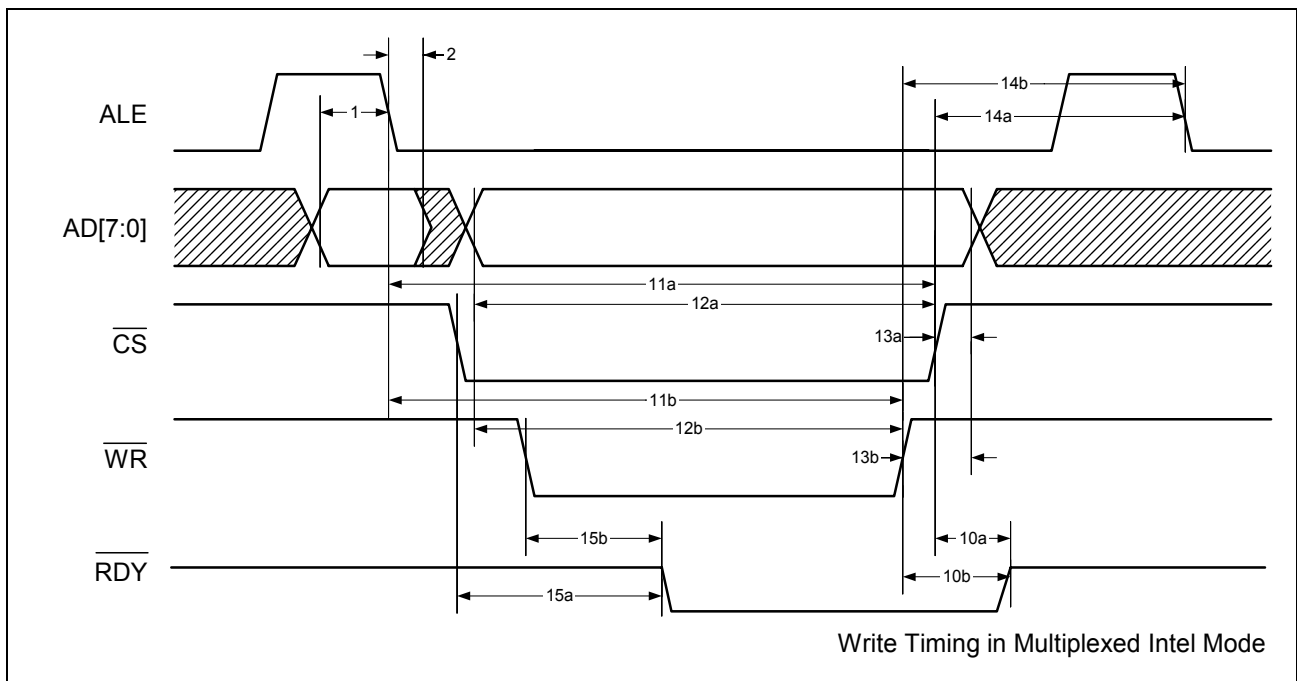
## Electrical Characteristics

### 6.6.8.1 Intel Mode (IM0='0')

#### a) Multiplexed Mode (IM1='0')



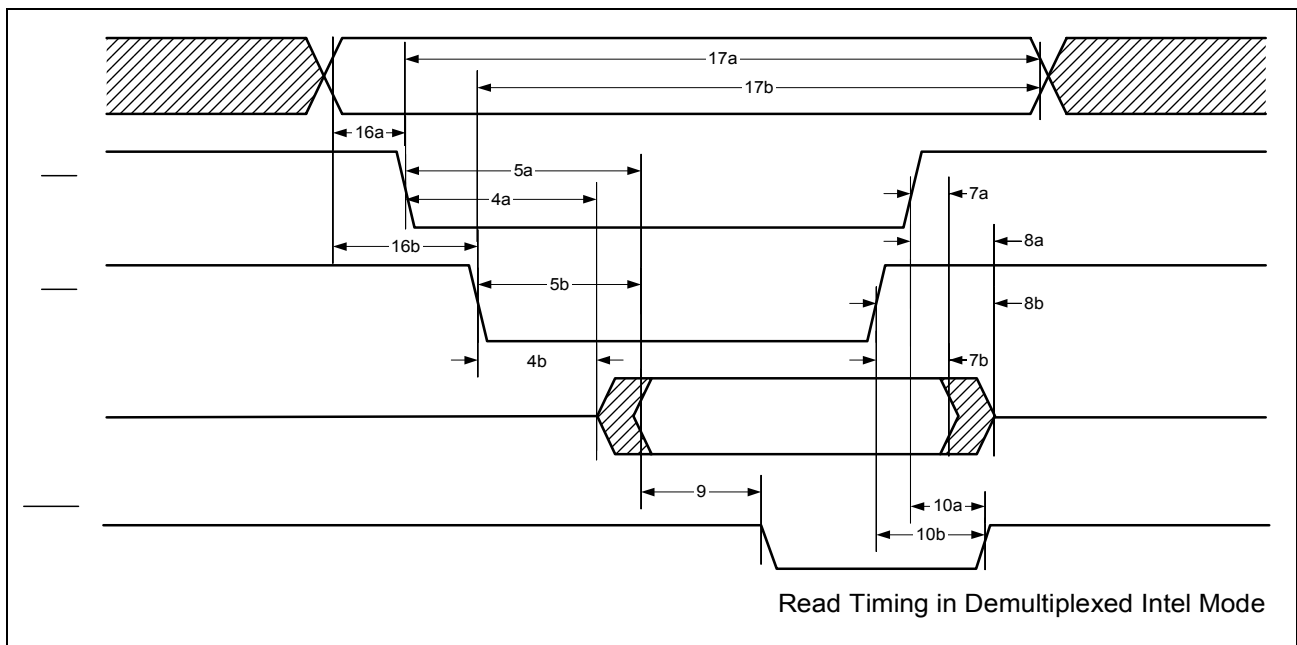
**Figure 41** Read Timing in Multiplexed Intel Mode (IM0='0', IM1='0')



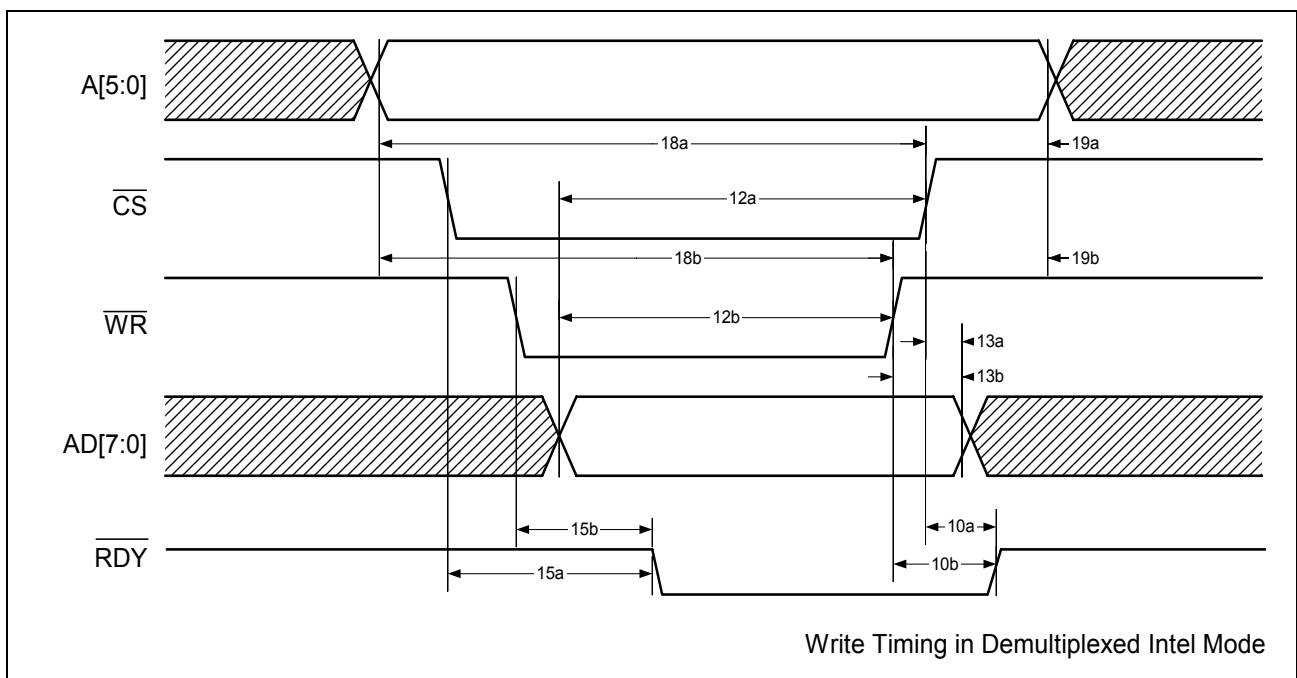
**Figure 42** Write Timing in Multiplexed Intel Mode (IM0='0', IM1='0')

## Electrical Characteristics

### b) Demultiplexed Mode (IM1='1')



**Figure 43** Read Timing in Demultiplexed Intel Mode (IM0='0', IM1='1')

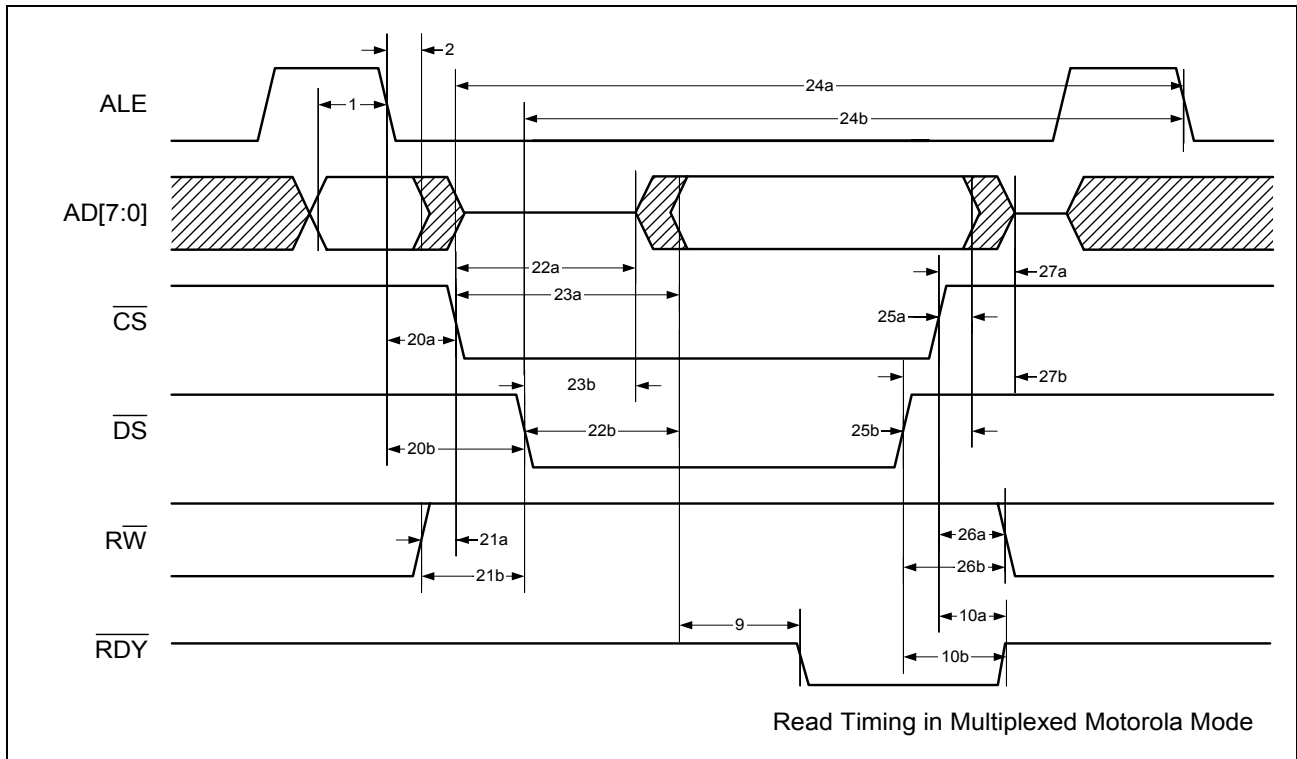


**Figure 44** Write Timing in Demultiplexed Intel Mode (IM0='0', IM1='1')

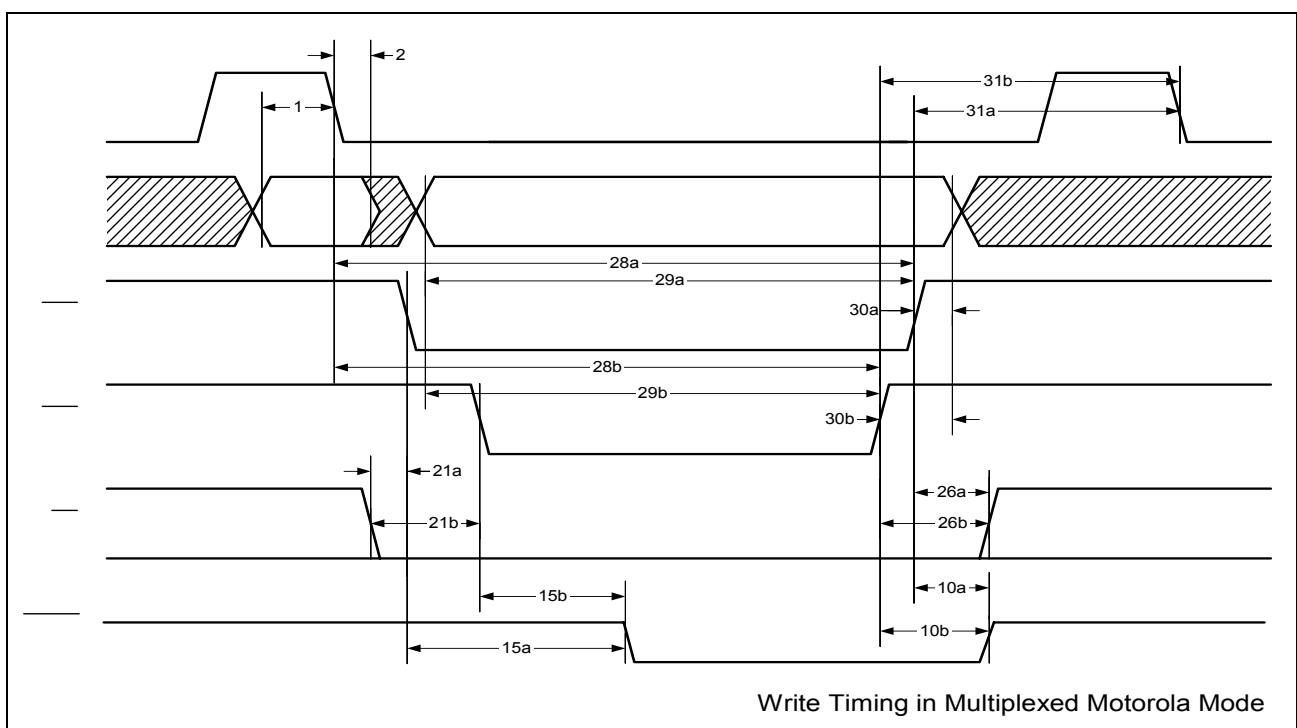
## Electrical Characteristics

### 6.6.8.2 Motorola Mode (IM0='1')

#### a) Multiplexed Mode (IM1='0')



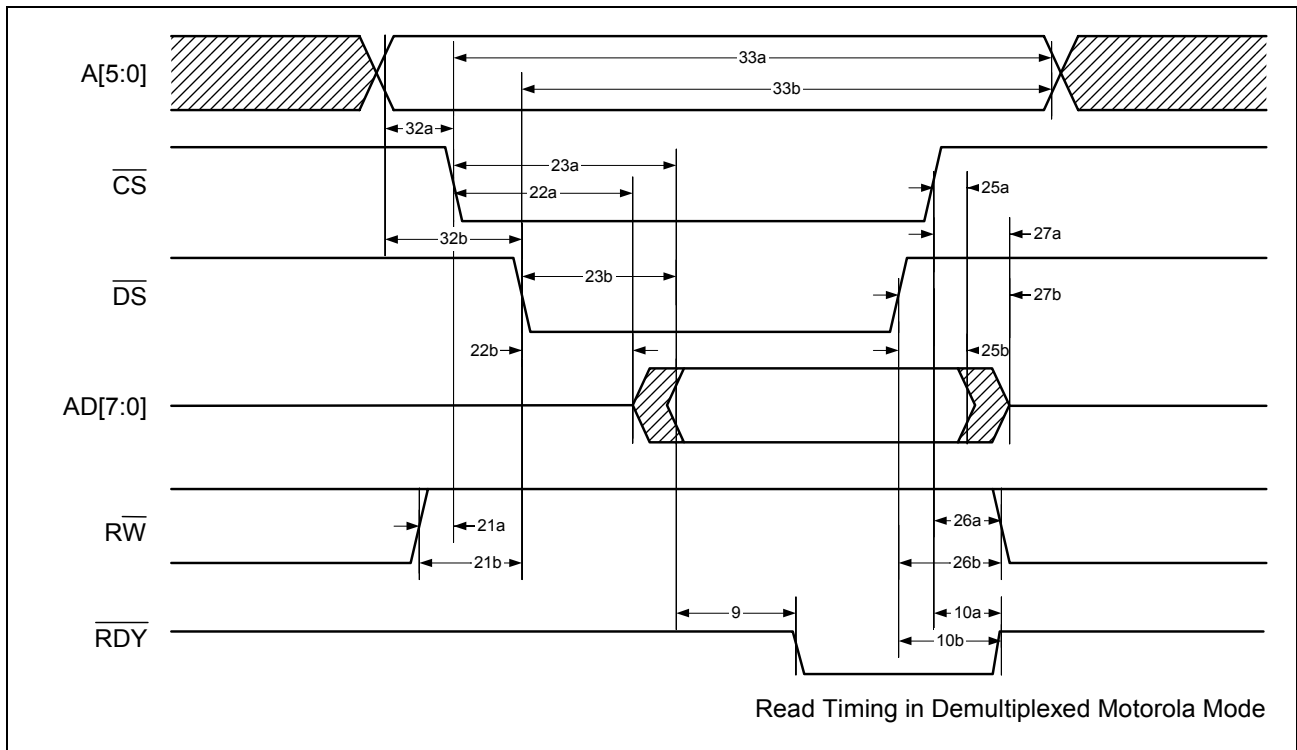
**Figure 45 Read Timing in Multiplexed Motorola Mode (IM0='1', IM1='0')**



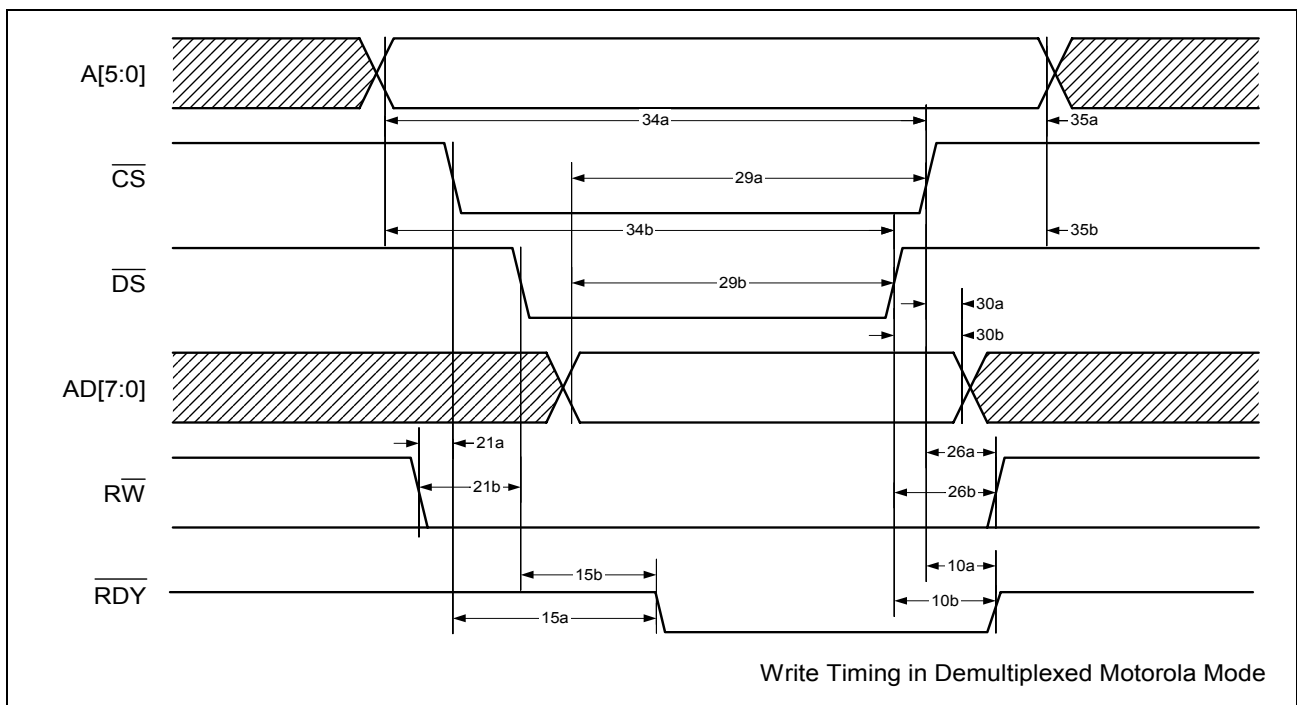
**Figure 46 Write Timing in Multiplexed Motorola Mode (IM0='1', IM1='0')**

## Electrical Characteristics

### b) Demultiplexed Mode (IM1='1')



**Figure 47** Read Timing in Demultiplexed Motorola Mode (IM0='1', IM1='1')



**Figure 48** Write Timing in Demultiplexed Motorola Mode (IM0='1', IM1='1')

## Electrical Characteristics

**Table 46 Preliminary Microprocessor Interface Timing Values**

| No. | Parameter                                               | Limit Values |      | Unit |
|-----|---------------------------------------------------------|--------------|------|------|
|     |                                                         | min.         | max. |      |
| 1   | Address setup before ALE falling edge                   | 15           |      | ns   |
| 2   | Address hold after ALE falling edge                     | 10           |      | ns   |
| 3a  | ALE falling edge before CS active if RD asserted        | 0            |      | ns   |
| 3b  | ALE falling edge before RD active if CS asserted        | 0            |      | ns   |
| 4a  | AD output after CS active if RD asserted                | 30           | 90   | ns   |
| 4b  | AD output after RD active if CS asserted                | 30           | 90   | ns   |
| 5a  | Read data valid after CS active if RD asserted          | 30           | 90   | ns   |
| 5b  | Read data valid after RD active if CS asserted          | 30           | 90   | ns   |
| 6a  | ALE rising edge after CS active if RD asserted          | 100          |      | ns   |
| 6b  | ALE rising edge after CS active if RD asserted          | 100          |      | ns   |
| 7a  | Read data hold after CS inactive if RD asserted         | 0            |      | ns   |
| 7b  | Read data hold after RD inactive if CS asserted         | 0            |      | ns   |
| 8a  | AD tristate after CS inactive if RD asserted            | 0            | 25   | ns   |
| 8b  | AD tristate after RD inactive if CS asserted            | 0            | 25   | ns   |
| 9   | RDY asserted after read data valid                      | 15           | 50   | ns   |
| 10a | RDY tristate after CS inactive if RD, WR or DS asserted | 0            | 20   | ns   |
| 10b | RDY tristate after RD, WR or DS inactive if CS asserted | 0            | 20   | ns   |
| 11a | ALE falling edge before CS rising edge if WR asserted   | 25           |      | ns   |
| 11b | ALE falling edge before WR rising edge if CS asserted   | 25           |      | ns   |

## Electrical Characteristics

**Table 46 Preliminary Microprocessor Interface Timing Values (cont'd)**

| No. | Parameter                                                             | Limit Values |      | Unit |
|-----|-----------------------------------------------------------------------|--------------|------|------|
|     |                                                                       | min.         | max. |      |
| 12a | Write data setup before CS rising edge if WR asserted                 | 25           |      | ns   |
| 12b | Write data setup before WR rising edge if CS asserted                 | 25           |      | ns   |
| 13a | Write data hold after CS rising edge if WR asserted                   | 20           |      | ns   |
| 13b | Write data hold after WR rising edge if CS asserted                   | 20           |      | ns   |
| 14a | CS rising edge before ALE falling edge if WR asserted                 | 20           |      | ns   |
| 14b | WR rising edge before ALE falling edge if CS asserted                 | 20           |      | ns   |
| 15a | RDY asserted after CS active if WR asserted or DS asserted and RW='0' | 30           | 90   | ns   |
| 15b | RDY asserted, if CS asserted, after WR active or DS active and RW='0' | 30           | 90   | ns   |
| 16a | Address valid before CS active if RD asserted                         | 0            |      | ns   |
| 16b | Address valid before RD active if CS asserted                         | 0            |      | ns   |
| 17a | Address hold after CS active if RD asserted                           | 100          |      | ns   |
| 17b | Address hold after RD active if CS asserted                           | 100          |      | ns   |
| 18a | Address setup before CS rising edge if WR asserted                    | 25           |      | ns   |
| 18b | Address setup before WR rising edge if CS asserted                    | 25           |      | ns   |
| 19a | Address hold after CS rising edge if WR asserted                      | 20           |      | ns   |
| 19b | Address hold after WR rising edge if CS asserted                      | 20           |      | ns   |
| 20a | ALE falling edge before CS active if DS asserted and RW = '1'         | 0            |      | ns   |

## Electrical Characteristics

**Table 46 Preliminary Microprocessor Interface Timing Values (cont'd)**

| No. | Parameter                                                                       | Limit Values |      | Unit |
|-----|---------------------------------------------------------------------------------|--------------|------|------|
|     |                                                                                 | min.         | max. |      |
| 20b | ALE falling edge before DS active if CS asserted and $\overline{RW} = '1'$      | 0            |      | ns   |
| 21a | $\overline{RW}$ setup before CS active if DS asserted                           | 10           |      | ns   |
| 21b | $\overline{RW}$ setup before DS active if CS asserted                           | 10           |      | ns   |
| 22a | AD output after CS active if DS asserted and $\overline{RW} = '1'$              | 30           | 90   | ns   |
| 22b | AD output after DS active if CS asserted and $\overline{RW} = '1'$              | 30           | 90   | ns   |
| 23a | Read data valid after CS active if DS asserted and $\overline{RW} = '1'$        | 30           | 90   | ns   |
| 23b | Read data valid after DS active if CS asserted and $\overline{RW} = '1'$        | 30           | 90   | ns   |
| 24a | ALE rising edge after CS active if DS asserted and $\overline{RW} = '1'$        | 100          |      | ns   |
| 24b | ALE rising edge after DS active if CS asserted and $\overline{RW} = '1'$        | 100          |      | ns   |
| 25a | Read data hold after CS inactive if DS asserted and $\overline{RW} = '1'$       | 0            |      | ns   |
| 25b | Read data hold after DS inactive if CS asserted and $\overline{RW} = '1'$       | 0            |      | ns   |
| 26a | $\overline{RW}$ hold after CS inactive if DS asserted                           | 10           |      | ns   |
| 26b | $\overline{RW}$ hold after DS inactive if CS asserted                           | 10           |      | ns   |
| 27a | AD tristate after CS inactive if DS asserted and $\overline{RW} = '1'$          | 0            | 25   | ns   |
| 27b | AD tristate after DS inactive if CS asserted and $\overline{RW} = '1'$          | 0            | 25   | ns   |
| 28a | ALE falling edge before CS rising edge if DS asserted and $\overline{RW} = '0'$ | 25           |      | ns   |
| 28b | ALE falling edge before DS rising edge if CS asserted and $\overline{RW} = '0'$ | 25           |      | ns   |
| 29a | Write data setup before CS rising edge if DS asserted and $\overline{RW} = '0'$ | 20           |      | ns   |

## Electrical Characteristics

**Table 46 Preliminary Microprocessor Interface Timing Values (cont'd)**

| No. | Parameter                                                                       | Limit Values |      | Unit |
|-----|---------------------------------------------------------------------------------|--------------|------|------|
|     |                                                                                 | min.         | max. |      |
| 29b | Write data setup before DS rising edge if CS asserted and $\overline{RW} = '0'$ | 20           |      | ns   |
| 30a | Write data hold after CS rising edge if DS asserted and $\overline{RW} = '0'$   | 20           |      | ns   |
| 30b | Write data hold after DS rising edge if CS asserted and $\overline{RW} = '0'$   | 20           |      | ns   |
| 31a | CS rising edge before ALE falling edge if DS asserted and $\overline{RW} = '0'$ | 20           |      | ns   |
| 31b | DS rising edge before ALE falling edge if CS asserted and $\overline{RW} = '0'$ | 20           |      | ns   |
| 32a | Address valid before CS active if DS asserted and $\overline{RW} = '1'$         | 0            |      | ns   |
| 32b | Address valid before DS active if CS asserted and $\overline{RW} = '1'$         | 0            |      | ns   |
| 33a | Address hold after CS active if DS asserted and $\overline{RW} = '1'$           | 100          |      | ns   |
| 33b | Address hold after DS active if CS asserted and $\overline{RW} = '1'$           | 100          |      | ns   |
| 34a | Address setup before CS rising edge if DS asserted and $\overline{RW} = '0'$    | 25           |      | ns   |
| 34b | Address setup before DS rising edge if CS asserted and $\overline{RW} = '0'$    | 25           |      | ns   |
| 35a | Address hold after CS rising edge if DS asserted and $\overline{RW} = '0'$      | 20           |      | ns   |
| 35b | Address hold after DS rising edge if CS asserted and $\overline{RW} = '0'$      | 20           |      | ns   |

## 6.6.9 JTAG Timing

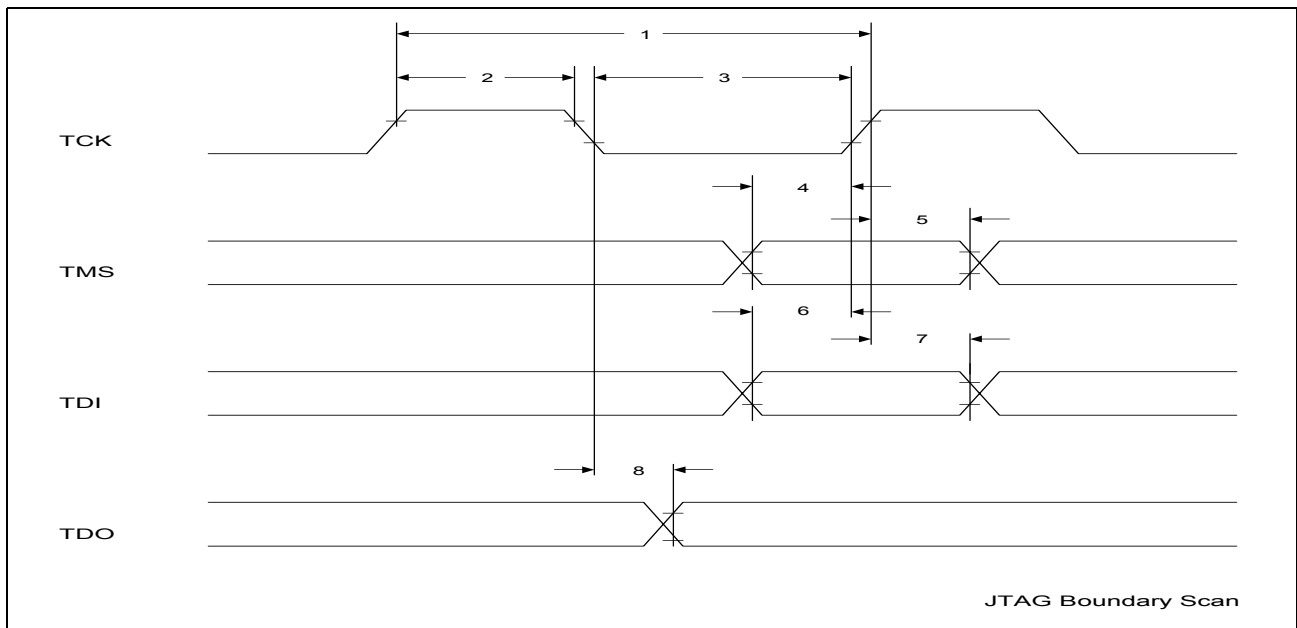


Figure 49 JTAG Boundary Scan Timing

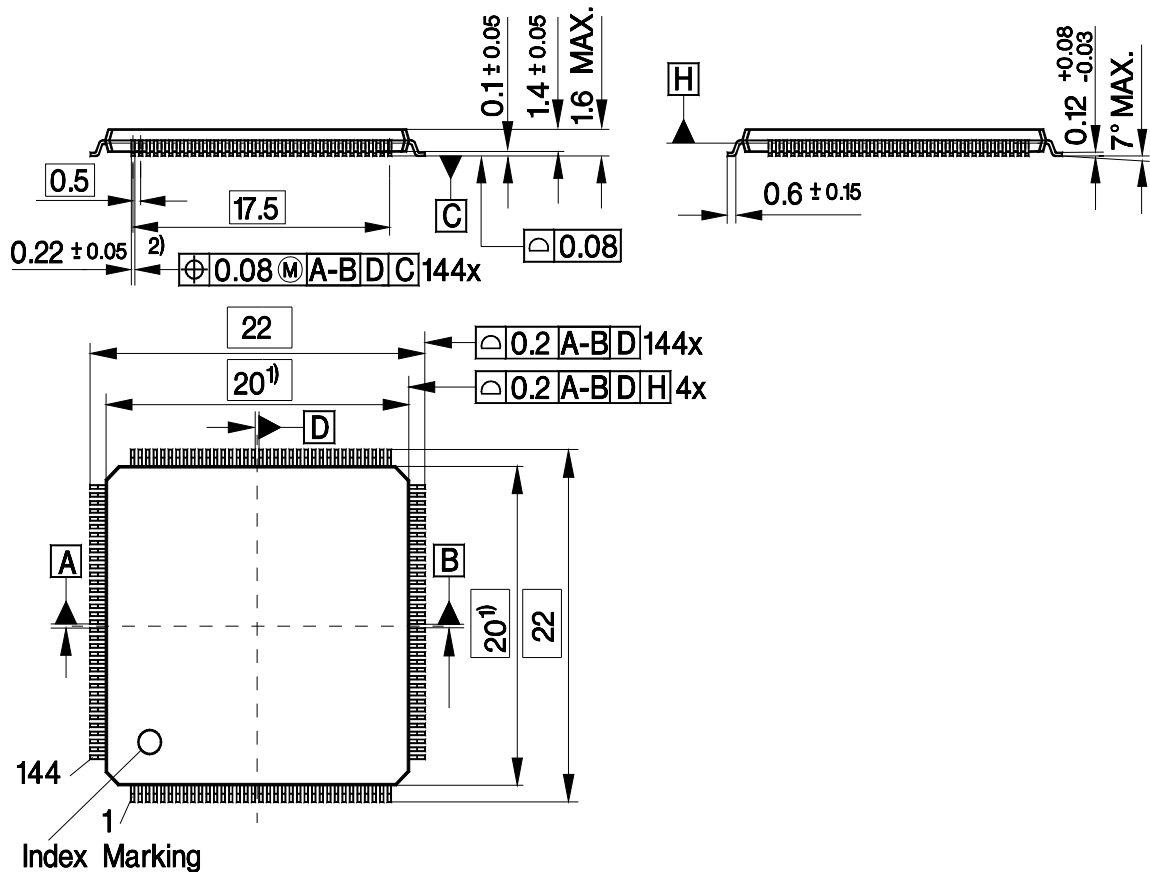
Table 47 JTAG Boundary Scan Timing

| No. | Name           | Parameter       | Limit Values |      | Unit |
|-----|----------------|-----------------|--------------|------|------|
|     |                |                 | min.         | max. |      |
| 1   | t_tck_period   | TCK period      | 250          |      | ns   |
| 2   | t_tck_high     | TCK high time   | 80           |      | ns   |
| 3   | t_tck_low      | TCK low time    | 80           |      | ns   |
| 4   | t_tms_setup    | TMS setup time  | 40           |      | ns   |
| 5   | t_tms_hold     | TMS hold time   | 40           |      | ns   |
| 6   | t_tdi_setup    | TDI setup time  | 40           |      | ns   |
| 7   | t_tdi_hold     | TDI hold time   | 40           |      | ns   |
| 8   | t_tck_tdo_fall | TDO valid delay |              | 100  | ns   |

## 7 Package Outlines

**TQFP-144**

(144pin Thin Plastic Quad Flatpack



- 1) Does not include plastic or metal protrusion of 0.25 max. per side
- 2) Does not include dambar protrusion of 0.08 max. per side

## Sorts of Packing

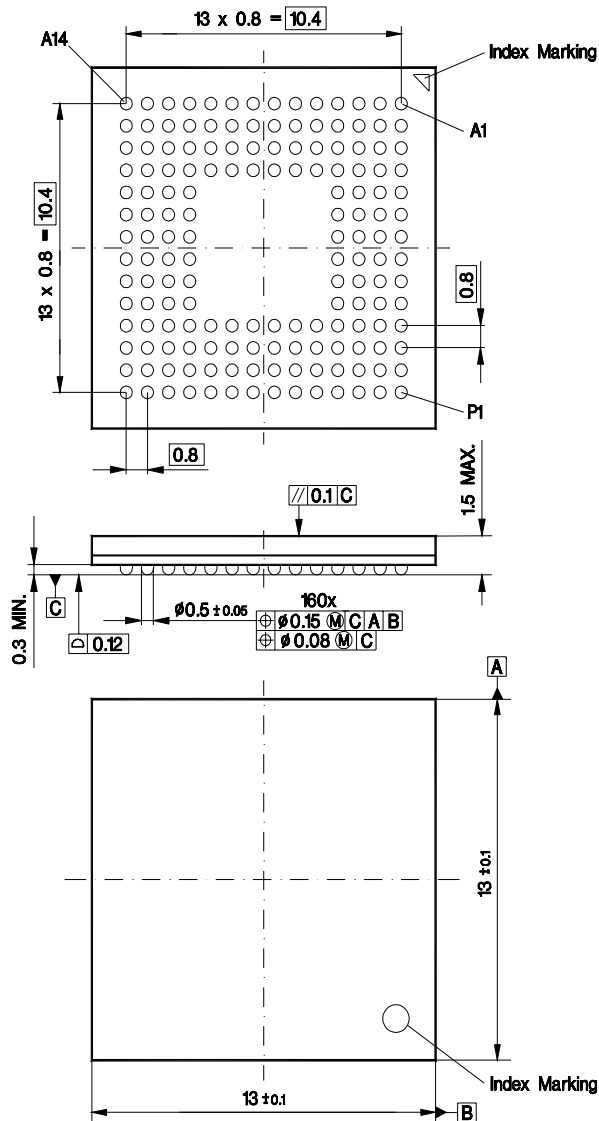
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

# P-LFBGA-160-2

(Plastic Metric Quad Flat Package)



GPM05249

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

SMD = Surface Mounted Device

Dimensions in mm

## 8 Glossary

### acoustic echo

Acoustic echoes consist of reflected signals caused by acoustic environments, e.g. hands-free phones which are connected with a 2-wire circuit to a hybrid. An echo path is introduced by the acoustic path from earphone to microphone.

### combined loss ( $A_{COM}$ )

The sum of echo return loss, echo return loss enhancement and non-linear processing loss (if present). This loss relates  $L_{Rin}$  to  $L_{RET}$  by:

$L_{RET} = L_{Rin} - A_{COM}$ , where:

$$A_{COM} = A_{ECHO} + A_{CANC} + A_{NLP}$$

### comfort noise

Insertion of pseudo-random noise during the silent interval when the NLP operates or allowance of some of the background or idle channel noise to pass through the NLP in order to prevent the annoyance of intervals of speech with background noise followed by intervals of silence.

### composite echo

Composite echoes consist of the electric echoes and acoustic echoes caused by reflected signals at hybrids and acoustic environments, e.g. hands-free telephones.

### convergence

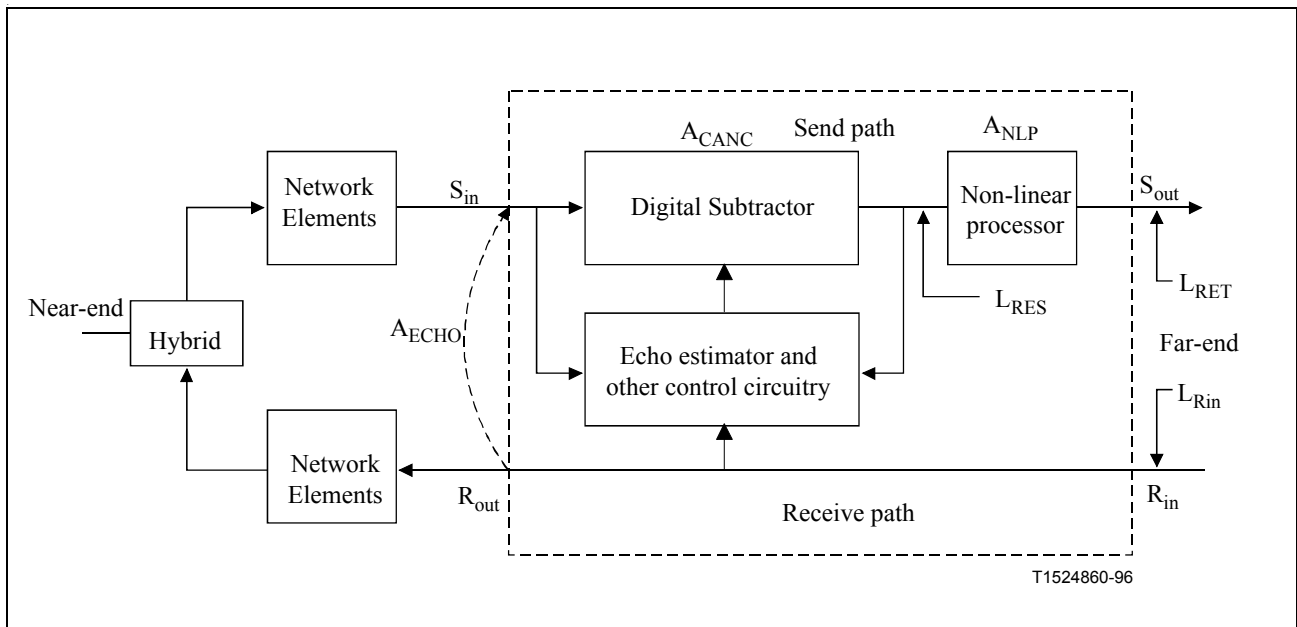
The process of developing a model of the echo path which will be used in the echo estimator to produce the estimate of the circuit echo.

### convergence time

For a defined echo path, the interval between the instant a defined test signal is applied to the receive-in port of an echo canceller with the estimated echo path impulse response initially set to zero, and the instant the returned echo level at the send-out port reaches a defined level.

### echo canceller

A voice-operated device placed in the 4-wire portion of a circuit and used for reducing near-end echo present on the send path by subtracting an estimation of that echo from the near-end echo (see [Figure 50](#))



**Figure 50** Location of levels and loss of an echo canceller

### echo path

The transmission path between  $R_{out}$  and  $S_{in}$  of an echo canceller. This term is intended to describe the signal path of the echo.

### echo path capacity

The maximum echo path delay for which an echo canceller is designed to operate.

### echo path delay ( $t_d$ )

The delay from the  $R_{out}$  port to the  $S_{in}$  port due to the delays inherent in the echo path transmission facilities including dispersion time due to the network elements. In case of multiple echo paths, all delays and dispersions of any individual echo path are included. The dispersion time, which varies with different networks, is required to accommodate the band-limiting, and hybrid transit effects.

### echo return loss (ERL) ( $A_{ECHO}$ )

The attenuation of a signal from the receive-out port ( $R_{out}$ ) to the send-in port ( $S_{in}$ ) of an echo canceller, due to transmission and hybrid loss, i.e. the loss in the (near-end) echo path.

**echo return loss enhancement (ERLE) ( $A_{\text{CANC}}$ )**

The attenuation of the echo signal as it passes through the send path of an echo canceller. This definition specifically excludes any non-linear processing on the output of the canceller to provide for further attenuation.

**electric echo**

Electric echoes consist of reflected signals caused by the near-end impedance mismatch, e.g. at a 2-wire/4-wire conversion unit (hybrid).

**far end**

The side of an echo canceller which does not contain the echo path on which the echo canceller is intended to operate.

**H register**

The register within the echo canceller which stores the impulse response model of the echo path.

**leak time**

The interval between the instant a test signal is removed from the receive-in port of a fully-converged echo canceller and the instant the echo path model in the echo canceller changes such that, when a test signal is reapplied to  $R_{\text{in}}$  with the convergence circuitry inhibited, the returned echo is at a defined level.

This definition refers to echo cancellers employing, for example, leaky integrators in the convergence circuitry.

**cancelled-end**

The side of an echo canceller which contains the echo path on which the echo canceller is intended to operate. This includes all transmission facilities and equipment (including the hybrid and terminating telephone set) which is included in the echo path.

**non-linear processor (NLP)**

A device having a defined suppression threshold level and in which:

- a) signals having a level detected as being below the threshold are suppressed; and
- b) signals having a level detected as being above the threshold are passed although the signal may be distorted.

NOTE 1 – The precise operation of a NLP depends upon the detection and control algorithm used.

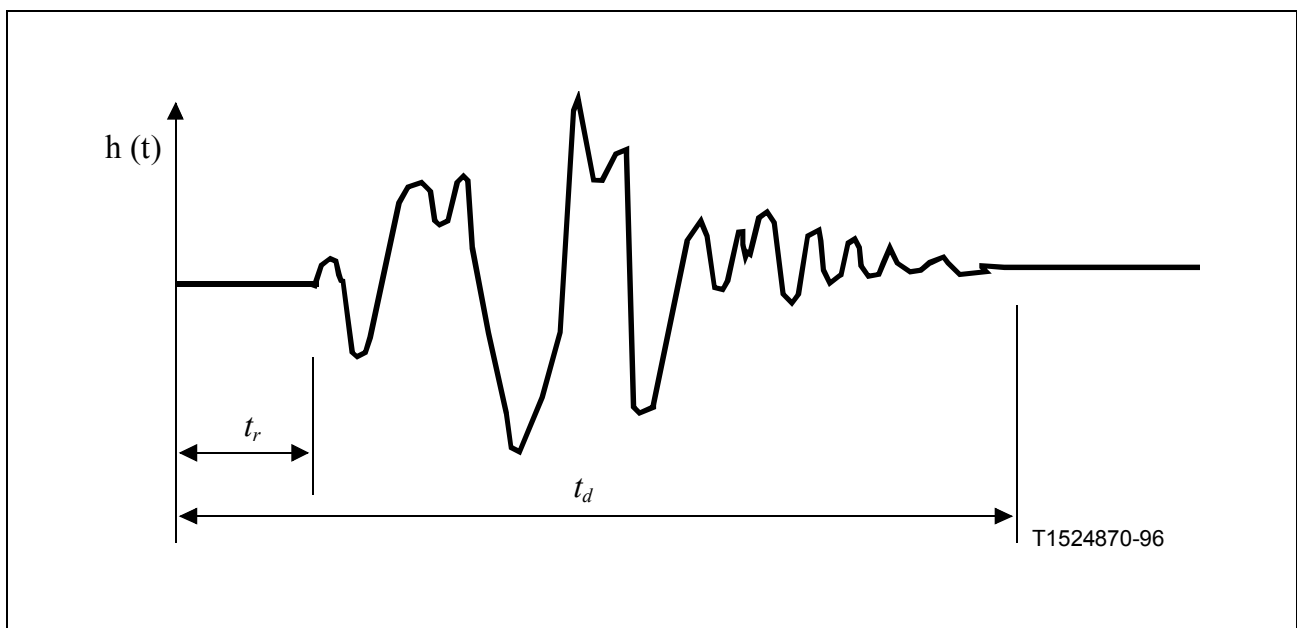
NOTE 2 – An example of a NLP is an analogue center clipper in which all signal levels below a defined threshold are forced to some minimum value.

### non-linear processing loss ( $A_{NLP}$ )

Additional attenuation of residual echo level by a NLP placed in the send path of an echo canceller.

### pure delay ( $t_r$ )

The delay from the  $R_{out}$  port to the Sin port due to the delays inherent in the near-end echo path transmission facilities, not including dispersion time due to the network elements. In this case, the transit time directly across the hybrid is assumed to be zero (see [Figure 51](#)).



**Figure 51** Example of an impulse response of an echo path

### residual echo level ( $L_{RES}$ )

The level of the echo signal which remains at the send-out port of an operating echo canceller after imperfect cancellation of the circuit echo. It is related to the receive-in signal  $L_{Rin}$  by:

$$L_{RES} = L_{RIN} - A_{ECHO} - A_{CANC}$$

Any non-linear processing is not included.

### returned echo level ( $L_{RET}$ )

The level of the signal at the send-out port of an operating echo canceller which will be returned to the talker. The attenuation of a NLP is included, if one is normally present.

$L_{RET}$  is related to  $L_{Rin}$  by:

$$L_{RET} = L_{RIN} - (A_{ECHO} + A_{CANC} + A_{NLP})$$

If non-linear processing is not present, note that  $L_{RES} = L_{RET}$ .

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