TPS3123 Ultra-Low Voltage Processor Supervisory Circuits

1 Features

- Minimum supply voltage of 0.9V
- Supply voltage supervision range:
  - 1.2V, 1.5V, 1.8V (TPS312x)
  - 3V (TPS3125 devices only)
  - Other versions on request
- Power-on reset generator with fixed delay time of 180ms
- Manual reset input (TPS3123/5/6/8)
- Watchdog timer retriggers the $\overline{\text{RESET}}$ output at $V_{DD} \geq V_{IT-}$
- Supply current of 14µA (typical)
- Small SOT23-5 package
- Temperature range of –40°C to +85°C
- Reset output available in Push-Pull (Active-Low and High) and Open-Drain (Active-Low)

2 Applications

- Portable / battery-powered equipment
- Wireless communication systems
- Industrial automation
- Servers
- Building automation

3 Description

The TPS312x family of voltage supervisory circuits provides voltage monitoring down to 1.2V rails and timing supervision, primarily for DSP and processor-based systems. All devices in the family monitor the power rail and assert $\overline{\text{RESET}}$ output when the power rail is under the threshold voltage target (V_{IT-}). The threshold voltage is programmed into the device to minimize external components. Built-in hysteresis prevents false triggering. The $\overline{\text{RESET}}$ output is not valid for supply voltage (V_{DD}) under 0.9V. The TPS312x family includes devices with active high output for use as disable during malfunction and active-low outputs for most systems where high output indicates properly functioning system.

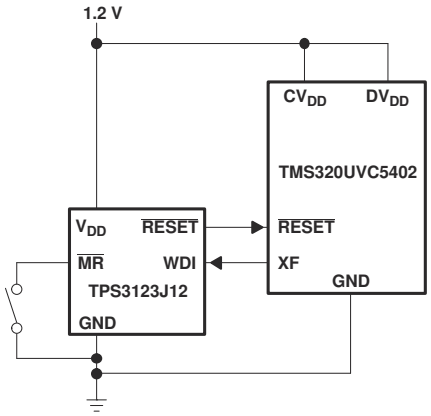
The TPS3123/3124/3128 also include the watchdog timer functionality to monitor timely digital pulses from the processor and issue an alert if the expected pulse does not arrive on time due to potential software freeze or hang. Such integration of supply rail monitoring and the watch dog timer feature is very helpful in always on systems, such as Factory Automation and Communications Infrastructure.

In addition the TPS3123/5/6/8 devices incorporate a manual reset input, MR, to force RESET triggered by an event unrelated to the voltage rail monitoring of the pulses monitored by the watch dog timer. A low level at MR causes RESET to become active. The TPS3124 devices do not have the input MR, but include a high-level output RESET same as the TPS3125 and TPS3126 devices.

All devices in the family are available in a 5-pin SOT23-5 package and are characterized for operation over a temperature range of –40°C to +85°C.

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TPS3123	SOT-23 (5)	2.90mm × 1.60mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Low-Voltage DSP Application

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4 Device Comparison

Figure 4-1 shows the device naming nomenclature to compare the different device variants. See Section 8.1 for ordering information on various variants of TPS3123/3124/3125/3126/ and TPS3128.

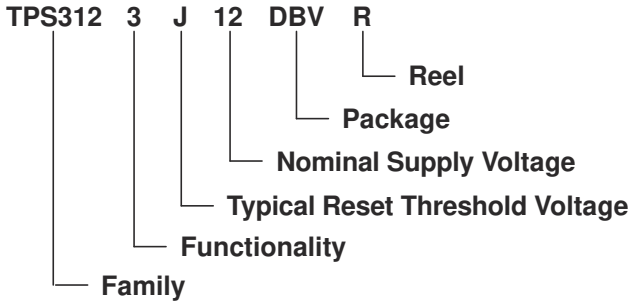


Figure 4-1. Device Naming Nomenclature

Table 4-1. Reset Output Topologies

DEVICES	OPEN DRAIN	PUSH-PULL
TPS3123		X
TPS3124		X
TPS3125		X
TPS3126	X	
TPS3128	X	

5 Pin Configuration and Functions

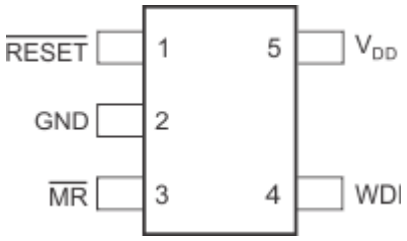


Figure 5-1. TPS3123 / TPS3128: DBV PACKAGE
5-Pin SOT-23
Top View

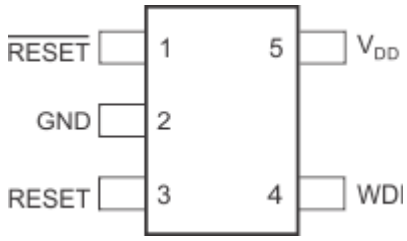


Figure 5-2. TPS3124: DBV PACKAGE
5-Pin SOT-23
Top View

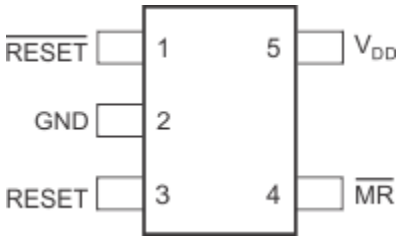


Figure 5-3. TPS3125 / TPS3126: DBV PACKAGE
5-Pin SOT-23
Top View

Table 5-1. Pin Functions

PIN				I/O	DESCRIPTION
PIN NUMBER	TPS3123 TPS3128	TPS3124	TPS3125 TPS3126		
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	O	**Active-Low Output Reset Signal:** This pin is driven to a logic low when VDD voltage falls below the negative voltage threshold (V_{IT-}). $\overline{\text{RESET}}$ remains low (asserted) for the delay time period (t_D) after VDD voltage rises above $V_{IT+} = V_{IT-} + V_{HYS}$.
2	GND	GND	GND	-	**GROUND**
3	$\overline{\text{MR}}$	-	-	I	**Manual Reset:** Pull this pin to a logic low to assert a reset signal in the $\overline{\text{RESET}}$ output pin. After $\overline{\text{MR}}$ pin is left floating or pulls to logic high, the $\overline{\text{RESET}}$ output deasserts to the nominal state after the reset delay time (t_D) expires.
3	-	RESET	RESET	O	**Active-High Output Reset Signal:** This pin is driven to a logic high when VDD voltage falls below the negative voltage threshold (V_{IT-}). RESET remains high (asserted) for the delay time period (t_D) after VDD voltage rises above $V_{IT+} = V_{IT-} + V_{HYS}$.
4	WDI	WDI	$\overline{\text{MR}}$	I	**Watchdog Timer Input:** If WDI remains high or low longer than the timeout period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge.
5	VDD	VDD	VDD	I	**Input Supply Voltage:** Supply voltage pin. Good analog design practice is to place a 0.1µF ceramic capacitor close to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Manual reset, $\overline{MR}$	–0.3	V_{DD} + 0.6	V
Voltage	$\overline{RESET}$	–0.3	V_{DD} + 0.6	V
Voltage	Open drain RESET output	–0.3	V_{DD} + 0.3	V
Voltage	Supply voltgae	–0.3	3.6	V
Voltage	Watchdog input, WDI	–0.3	V_{DD} + 0.6	V
Current	Maximum low output current, I_{OL}		5	mA
Current	Maximum high output current, I_{OL}		–5	mA
Current	Input clamp current (V_I < 0 or V_I > V_{DD}), I_{IK}	–10	10	mA
Current	Output clamp current (V_O < 0 or V_O > V_{DD}), I_{OK}	–10	10	mA
Temperature	Operating free-air temperature, T_A	–40	85	°C
Temperature	Storage temperature range, T_{stg}	–65	150	°C
Temperature	Soldering temperature		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	T_A = 0°C to 85°C	0.9		3.3	V
		T_A = –40°C to 85°C	0.9		3.3	
	Manual reset voltage		0		V_{DD} + 0.3	V
V_{WD1}	Watchdog input voltage		0		V_{DD} + 0.3	V
V_{IH}	High level input voltage		0.7 × V_{DD}			V
V_{IL}	Low level input voltage				0.3 × V_{DD}	V
Δt/ΔV	Input transition rise and fall rate at WDI				1	µs/V
T_A	Operating free-air temperature range		–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS312x DBV (SOT-23) 5 PINS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83.3
$R_{\theta JB}$	Junction-to-board thermal resistance	52.4
ψ_{JT}	Junction-to-top characterization parameter	20.4
ψ_{JB}	Junction-to-board characterization parameter	52.0
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (inless otherwise noted).

	PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
R_{MR}	$\overline{MR}$ pullup resistor (Internal)					90		kΩ
I_{IH}	High-level input current	WDI	WDI = V_{DD} = 3.3V		-1		1	µA
		$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 3.3V		7		19	µA
I_{IL}	Low-level input current	WDI	WDI = 0V, V_{DD} = 3.3V		-1		1	µA
	Low-level input current	$\overline{MR}$	$\overline{MR}$ = 0V, V_{DD} = 3.3V		24		61	µA
I_{OH}	High-level output current (leakage into $\overline{RESET}$ pin)	TPS3126-xx TPS3128-xx	V_{DD} = V_{OH} = 3.3V				200	nA
V_{OH}	High-level output voltage (TPS3123/4/5 only)	$\overline{RESET}$	V_{DD} = 1.5V, I_{OH} = –1mA		0.8 × V_{DD}			V
			V_{DD} = 3.3V, I_{OH} = –4.5mA					
		RESET	V_{DD} = 0.9V, I_{OH} = –8µA					
			V_{DD} = 1.5V, I_{OH} = –1mA					
V_{OL}	Low-level output voltage	$\overline{RESET}$	V_{DD} = 0.9V, I_{OL} = 15µA				0.2 × V_{DD}	V
			V_{DD} = 1.5V, I_{OL} = 1.4mA					
		RESET	V_{DD} = 1.5V, I_{OL} = 1.4mA					
			V_{DD} = 3.3V, I_{OL} = 3mA				0.4	
V_{IT-}	Negative-going input threshold voltage [1]	TPS312xJ12	T_A = –40°C to 85°C		1.04	1.08	1.12	V
		TPS312xG15			1.35	1.40	1.45	
		TPS312xJ18			1.56	1.62	1.68	
		TPS312xL30			2.57	2.64	2.71	
		TPS312xE12			1.10	1.14	1.18	
		TPS312xE15			1.38	1.43	1.48	
		TPS312xE18			1.65	1.71	1.77	
V_{HYS}	Hysteresis at V_{DD} input		1V < V_{IT-} < 1.4V			15		mV
			1.4V < V_{IT-} < 2V			20		
			2V < V_{IT-} < 3V			30		
I_{DD}	Supply current	TPS3123-xx TPS3124-xx TPS3128-xx	WDI = V_{DD}, $\overline{MR}$ unconnected	V_{DD} = 0.9V		14		µA
				V_{DD} = 3.3V		22	30	
		TPS3125-xx TPS3126-xx[2]	$\overline{MR}$ unconnected	V_{DD} = 0.9V		14		
				V_{DD} = 3.3V		18	25	
C_i	Input capacitance at $\overline{MR}$, WDI		V_I = 0V to 3.3V			5		pF

(1) To make sure best stability of the threshold voltage, place a bypass capacitor (ceramic, 0.1µF) near the supply terminal.
(2) The supply current during delay time td is typical 5µA higher.

6.6 Timing Requirements

at R_L = 1MΩ, C_L = 50pF, T_A = +25°C

	PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_W	Pulse width	At V_{DD}	$V_{IH} = V_{IT-} + 0.2V$, $V_{IL} = V_{IT-} - 0.2V$	6			µs
		At $\overline{MR}$	$V_{DD} \geq V_{IT-} + 0.2V$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	1			
		At WDI		0.1			

6.7 Switching Characteristics

at R_L = 1MΩ, C_L = 50pF, T_A = +25°C

	PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{tout}	Watchdog time out		$V_{DD} \geq V_{IT-} + 0.2V$, See timing diagram	0.8	1.4	2.1	s
t_d	Delay time		$V_{DD} \geq V_{IT-} + 0.2V$, See timing diagram	100	180	260	ms
t_{PHL}	Propagation delay time, high-to-low output	$\overline{MR}$ to $\overline{RESET}$ delay (TPS3123/5/6/8)	$V_{DD} \geq V_{IT-} + 0.2V$, VIL = $V_{DD} \times 0.2$, $V_{IH} = V_{DD} \times 0.8$			0.1	µs
t_{PLH}	Propagation delay time, low-to-high output	$\overline{MR}$ to RESET delay (TPS3125/6)				0.1	µs
t_{PHL}	Propagation delay time, high-to-low output	V_{DD} to $\overline{RESET}$ delay	$V_{IL} = V_{IT-} - 0.2V$, $V_{IH} = V_{IT-} + 0.2V$			17	µs
t_{PLH}	Propagation delay time, low-to-high output	V_{DD} to RESET delay (TPS3124/5/6)				17	µs

6.8 Timing Diagrams

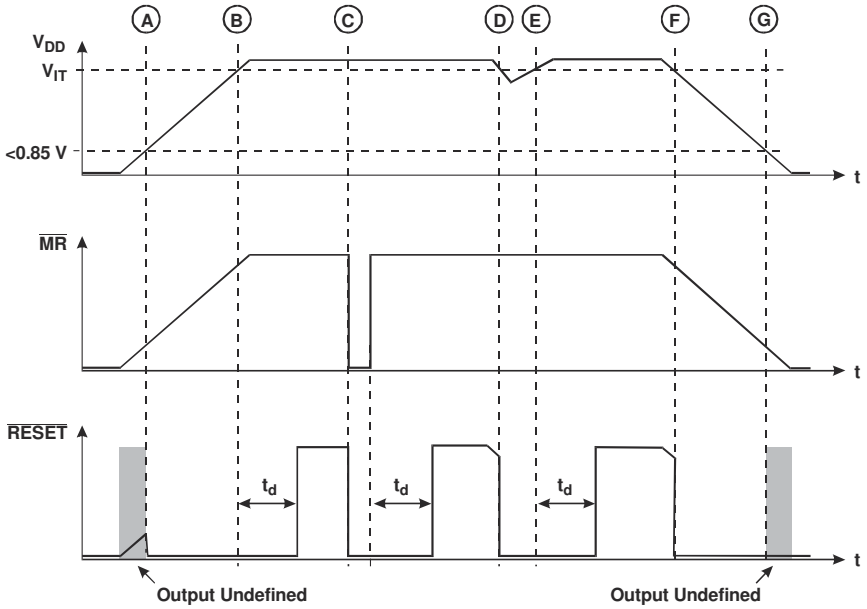


Figure 6-1. Timing Diagram TPS3123/5/6/8

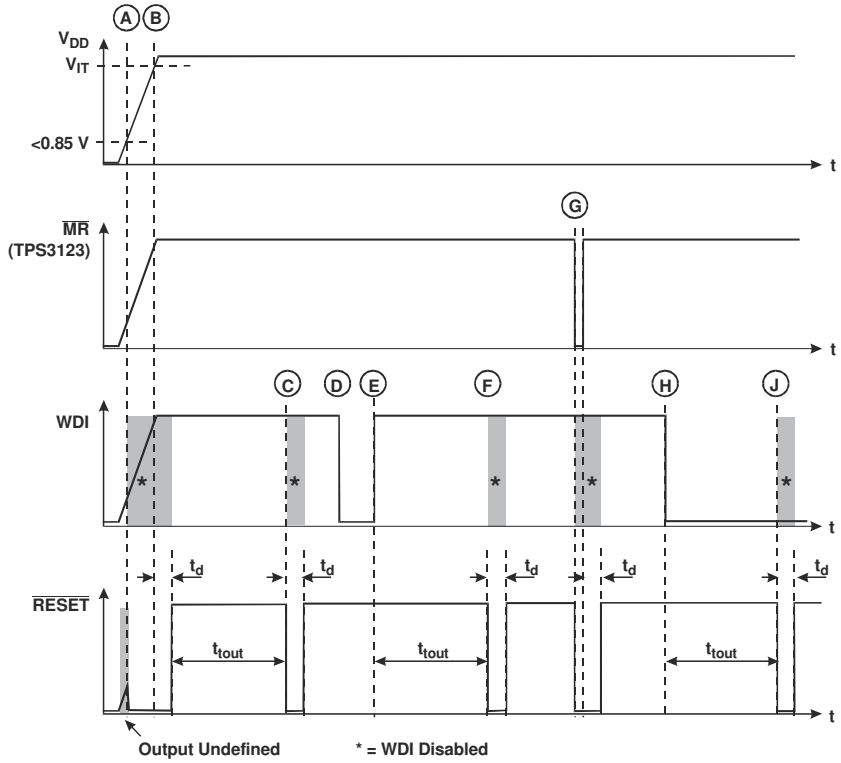


Figure 6-2. Timing Diagram TPS3123/4/8

Note

A=Min VDD, B=VDD threshold, C,F,J=Watch Dog timeout, D,E,H=Watch Dog retriggered, G=Manual Reset

6.9 Typical Characteristics

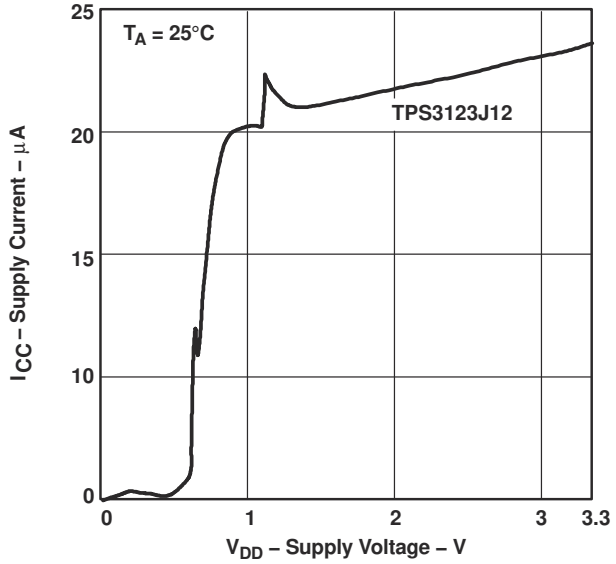


Figure 6-3. SUPPLY CURRENT vs SUPPLY VOLTAGE

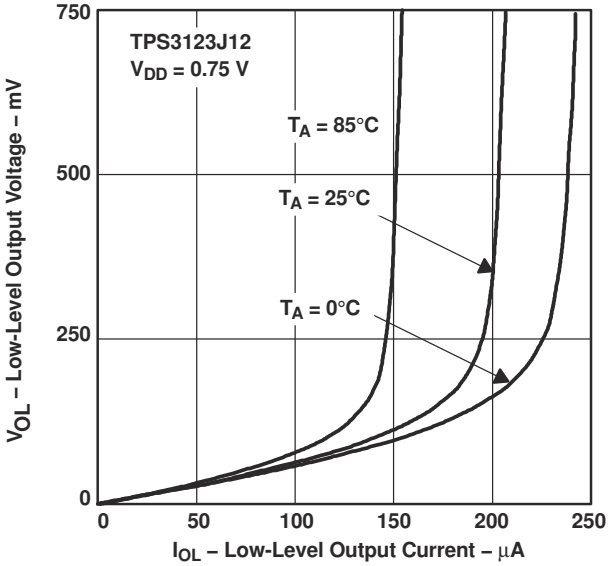


Figure 6-4. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

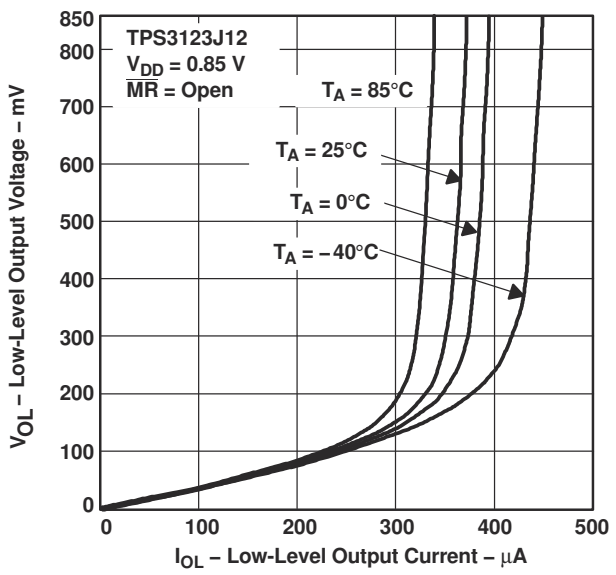


Figure 6-5. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

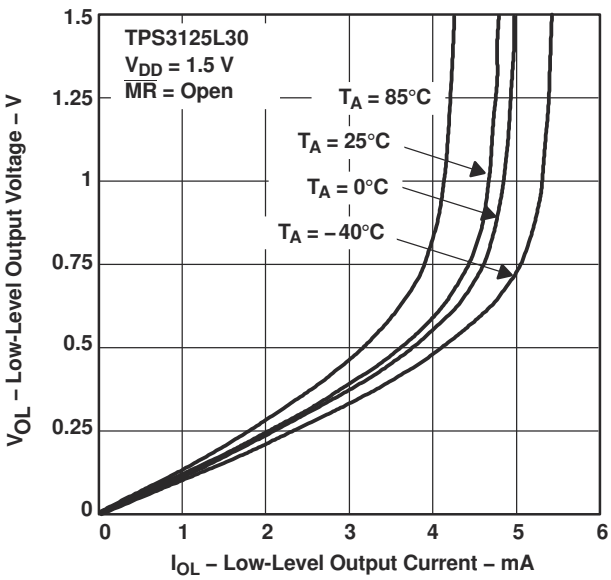


Figure 6-6. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

6.9 Typical Characteristics (continued)

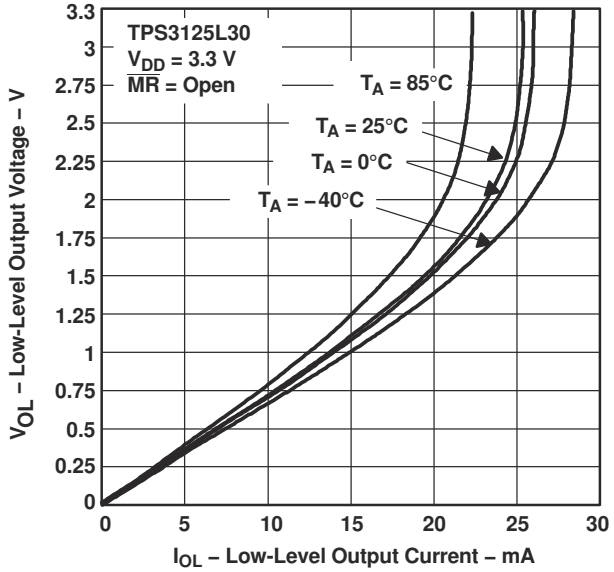


Figure 6-7. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

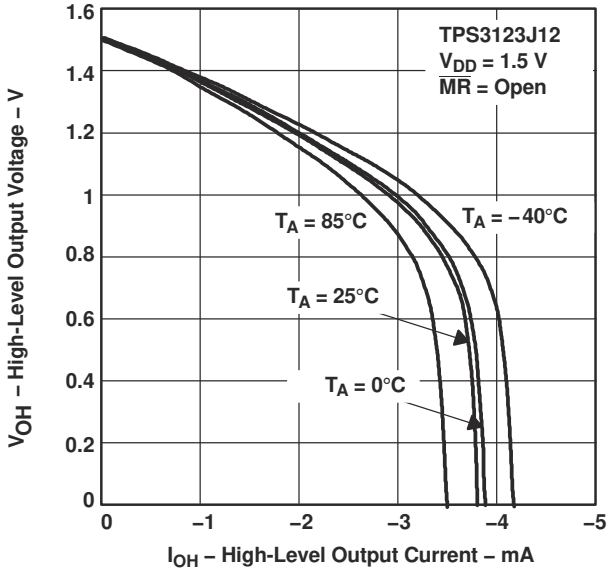


Figure 6-8. HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

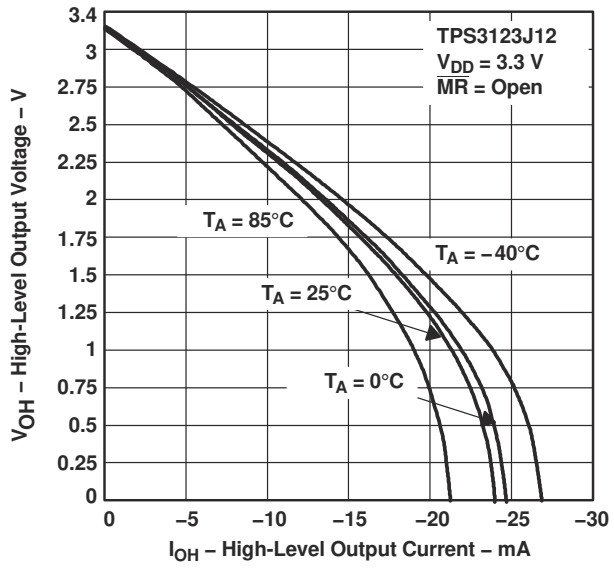


Figure 6-9. HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

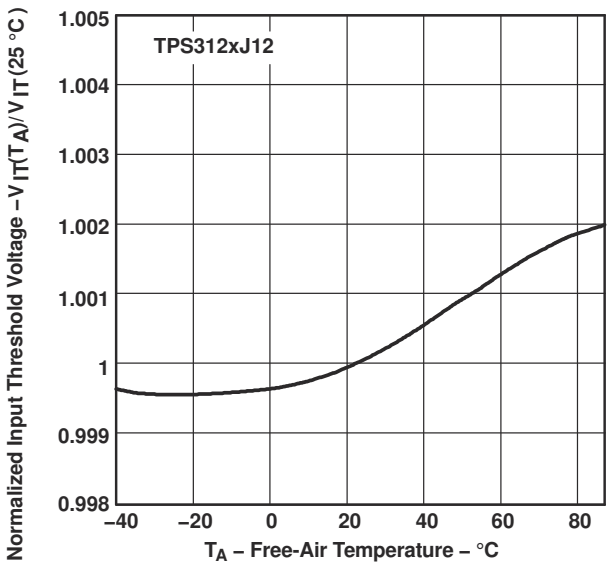


Figure 6-10. NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

6.9 Typical Characteristics (continued)

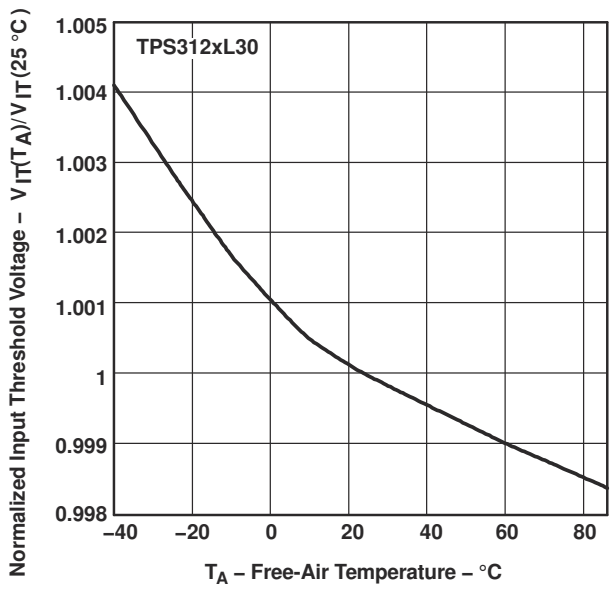


Figure 6-11. NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

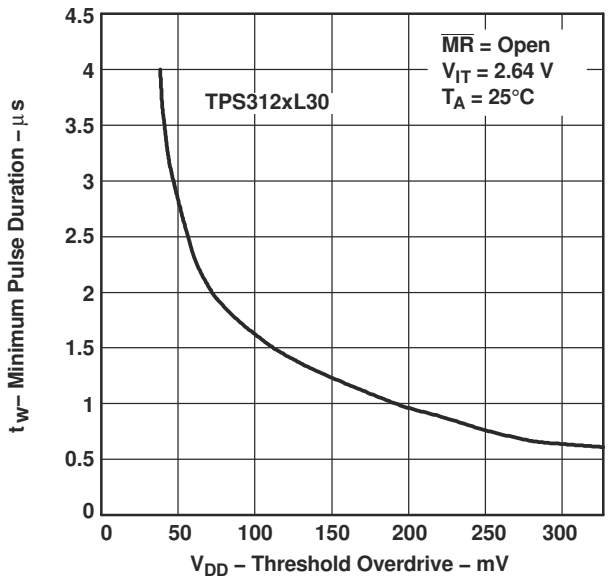


Figure 6-12. MINIMUM PULSE DURATION vs THRESHOLD OVERDRIVE

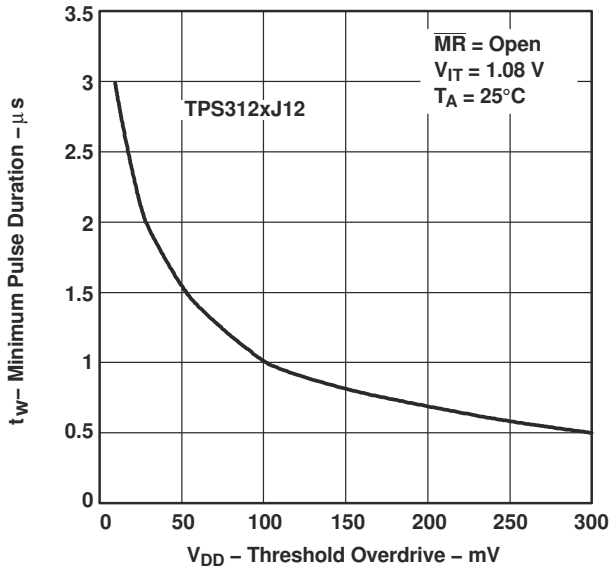


Figure 6-13. MINIMUM PULSE DURATION vs THRESHOLD OVERDRIVE

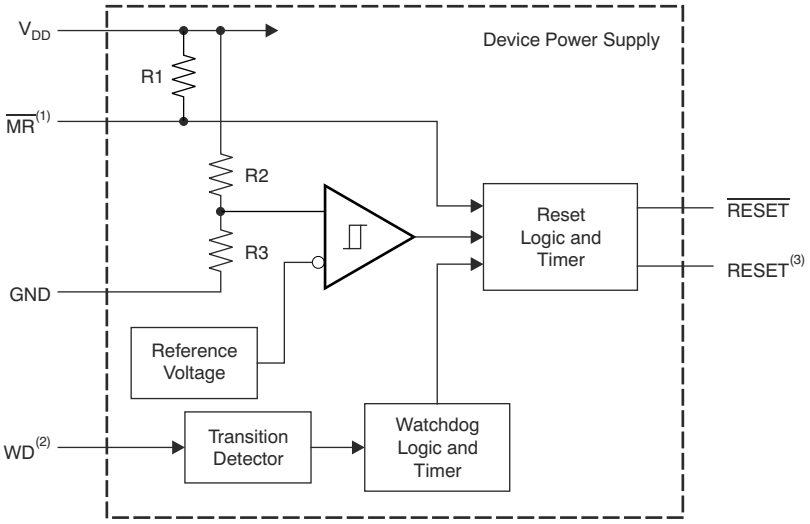
7 Detailed Description

7.1 Overview

The TPS312x family of supervisors provide circuit initialization and timing supervision. Optional configurations include devices with active-high and active-low output signals (TPS3124/3125/3126), devices with a watchdog timer (TPS3123/3124/3128), and devices with manual reset ($\overline{MR}$) pins (TPS3123/3125/3126/3128). $\overline{RESET}$ output is valid when the supply voltage, V_{DD}, is above 0.9V. For devices with active-low output logic, the device monitors V_{DD} and keeps $\overline{RESET}$ low as long as V_{DD} remains below the negative threshold voltage, V_{IT-}. For devices with active-high output logic, RESET remains high as long as V_{DD} remains below V_{IT-}. An internal timer delays the return of the output to the inactive state (high) to make sure proper system reset. The delay time, t_d, starts after V_{DD} rises above the positive threshold voltage (V_{IT-} + V_{HYS}). When the supply voltage drops below V_{IT-}, the output becomes active (low) again. All the devices of this family have a fixed-sense threshold voltage, V_{IT-}, set by an internal voltage divider, so no external components are required.

The TPS312x family is designed to monitor supply voltage. For devices with the manual reset functionality, a low level at $\overline{MR}$ causes $\overline{RESET}$ to become active. For devices with the watch dog timer functionality, when the supervising system fails to retrigger the watchdog circuit within the time-out interval t_{tout} = 0.8s, $\overline{RESET}$ output becomes active for the time period (t_d). This event also reinitializes the watchdog timer. The devices are available in a 5-pin SOT-23 package and are characterized for operation over a temperature range of −40°C to 85°C.

7.2 Functional Block Diagram



NOTES:
(1) TPS3123/5/6/8
(2) TPS3123/4/8
(3) TPS3124/5/6

Figure 7-1. FUNCTIONAL BLOCK DIAGRAM

7.3 Feature Description

7.3.1 Manual Reset ($\overline{MR}$)

The $\overline{MR}$ input allows an external logic signal from processors, logic circuits, and/or discrete sensors to force a reset signal regardless of V_{DD} with respect to V_{IT-} or the state of the watchdog timer. A low level at $\overline{MR}$ causes the reset signals to become active.

7.3.2 Active-High or Active-Low Output

All TPS312x devices have an active-low logic output ($\overline{\text{RESET}}$), while the TPS3124/3125/3126 devices also include an active-high logic output (RESET).

7.3.3 Push-Pull or Open-Drain Output

All TPS312x devices, except for TPS3126/3128, have push-pull outputs. TPS3126/3128 devices have an open-drain output.

7.3.4 Watchdog Timer (WDI)

The TPS3123, TPS3124, and TPS3128 devices have a watchdog timer that must be periodically triggered by either a positive or negative transition at WDI to avoid a reset signal being issued. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{tout}, $\overline{\text{RESET}}$ becomes active for the time period t_d. This event also reinitializes the watchdog timer.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the TPS312x devices.

Table 7-1. Device Functional Modes Table

TPS3123/8			TPS3124			TPS3125/6			
$\overline{\text{MR}}$	VDD > V_{IT-}	$\overline{\text{RESET}}$	VDD > V_{IT-}	$\overline{\text{RESET}}$	RESET	$\overline{\text{MR}}$	VDD > V_{IT-}	$\overline{\text{RESET}}$	RESET
L	0	L	0	L	H	L	0	L	H
L	1	L	1	H	L	L	1	L	H
H	0	L				H	0	L	H
H	1	H				H	1	H	L

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device and Documentation Support

Table 8-1. Ordering Information Application Specific Versions (1)

DEVICE NAME	NOMINAL SUPPLY VOLTAGE, V_{NOM}	DEVICE NAME	TYPICAL RESET THRESHOLD VOLTAGE–V_{IT-}
TPS312xx12DBV	1.2V	TPS312xAxxDBV	V_{NOM} –1%
TPS312xx15DBV	1.5V	TPS312xBxxDBV	V_{NOM} –2%
TPS312xx18DBV	1.8V	TPS312xCxxDBV	V_{NOM} –3%
TPS312xx30DBV	3.0V	TPS312xDxxDBV	V_{NOM} –4%
		TPS312xExxDBV	V_{NOM} –5%
		TPS312xFxxDBV	V_{NOM} –6%
		TPS312xGxxDBV	V_{NOM} –7%
		TPS312xHxxDBV	V_{NOM} –8%
		TPS312xIxxDBV	V_{NOM} –9%
		TPS312xJxxDBV	V_{NOM} –10%
		TPS312xKxxDBV	V_{NOM} –11%
		TPS312xLxxDBV	V_{NOM} –12%
		TPS312xMxxDBV	V_{NOM} –13%
		TPS312xNxxDBV	V_{NOM} –14%
		TPS312xOxxDBV	V_{NOM} –15%

1. For the application-specific versions contact Texas Instruments for availability, lead time, and minimum order quantities.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (June 2024) to Revision H (March 2025)	Page
• Rearrange table to meet latest data sheet guidelines	5
• Update VDD Min value to 0.9V	5
• Remove 'Dissipation Rating Table' and replace with 'Thermal Information'	6
• Remove Table 8-2.	14

Changes from Revision F (December 2020) to Revision G (June 2024)	Page
• Removed "If unused, the WDI connection must be high impedance to prevent device from causing a reset event." due to functionality not available	4
• Updated MR resistance typical value	6
• Updated tPHL and tPLH max specification	7

Changes from Revision E (August 2011) to Revision F (December 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the description to highlight benefits of the key features	1
• Moved table of the details on package, threshold and top mark to the device and documentation support section in the back, leaving only the nomenclature and the topology summary here in this device comparison table section	3
• Moved pin out figures from first page to this new pin configuration section and added pin function table	4
• Moved Timing Diagrams to new section and added legend for the letters on the diagrams	8
• Moved and updated device overview, block diagram and function mode table to this newly created section and added subsections for detailed feature descriptions for MR, output topology (active high/low, push-pull/ open-drain and watchdog timer)	12

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3123J12DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBNI
TPS3123J12DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBNI
TPS3123J12DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PBNI
TPS3123J18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBPI
TPS3123J18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBPI
TPS3123J18DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PBPI
TPS3124G15DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBRI
TPS3124G15DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBRI
TPS3124J12DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBQI
TPS3124J12DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBQI
TPS3124J12DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PBQI
TPS3124J18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBSI
TPS3124J18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBSI
TPS3124J18DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PBSI
TPS3125G15DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBUI
TPS3125G15DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBUI
TPS3125G15DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PBUI
TPS3125J12DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBTI
TPS3125J12DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBTI
TPS3125J12DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PBTI
TPS3125J18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBVI
TPS3125J18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBVI
TPS3125J18DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PBVI
TPS3125L30DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBXI
TPS3125L30DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PBXI
TPS3125L30DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PBXI
TPS3126E12DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFOI
TPS3126E12DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFOI
TPS3126E12DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PFOI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3126E15DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFPI
TPS3126E15DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFPI
TPS3126E15DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PFPI
TPS3126E18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFQI
TPS3126E18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFQI
TPS3126E18DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PFQI
TPS3128E12DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFRI
TPS3128E12DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFRI
TPS3128E15DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFSI
TPS3128E15DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFSI
TPS3128E15DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PFSI
TPS3128E18DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFTI
TPS3128E18DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFTI
TPS3128E18DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	PFTI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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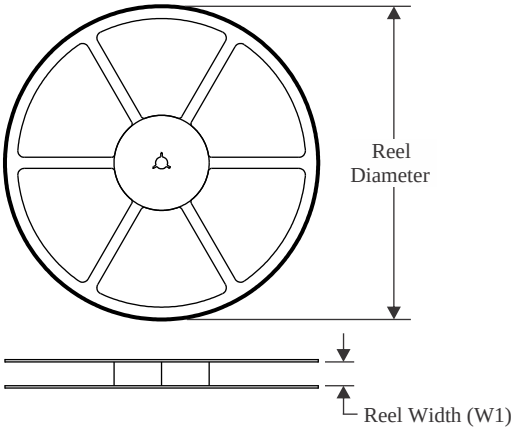
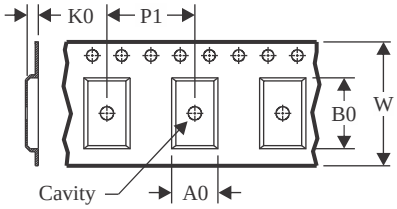
TAPE AND REEL INFORMATION

REEL DIMENSIONS

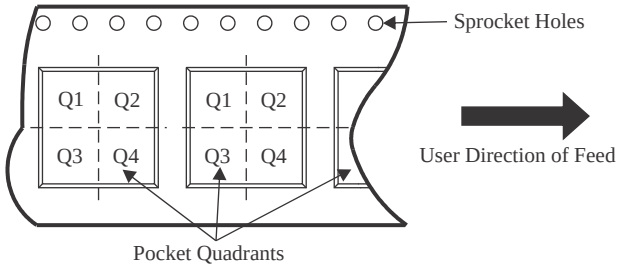


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

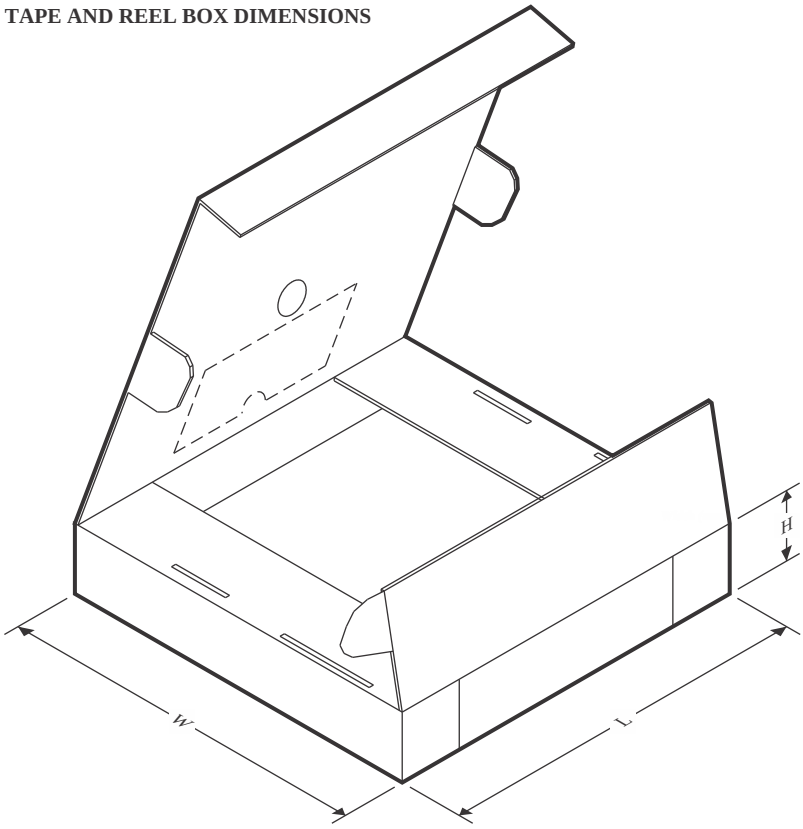
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3123J12DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3123J18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3124G15DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3124J12DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3124J18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3125G15DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3125J12DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3125J18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3125L30DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3126E12DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3126E15DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3126E18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3128E12DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3128E15DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3128E18DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

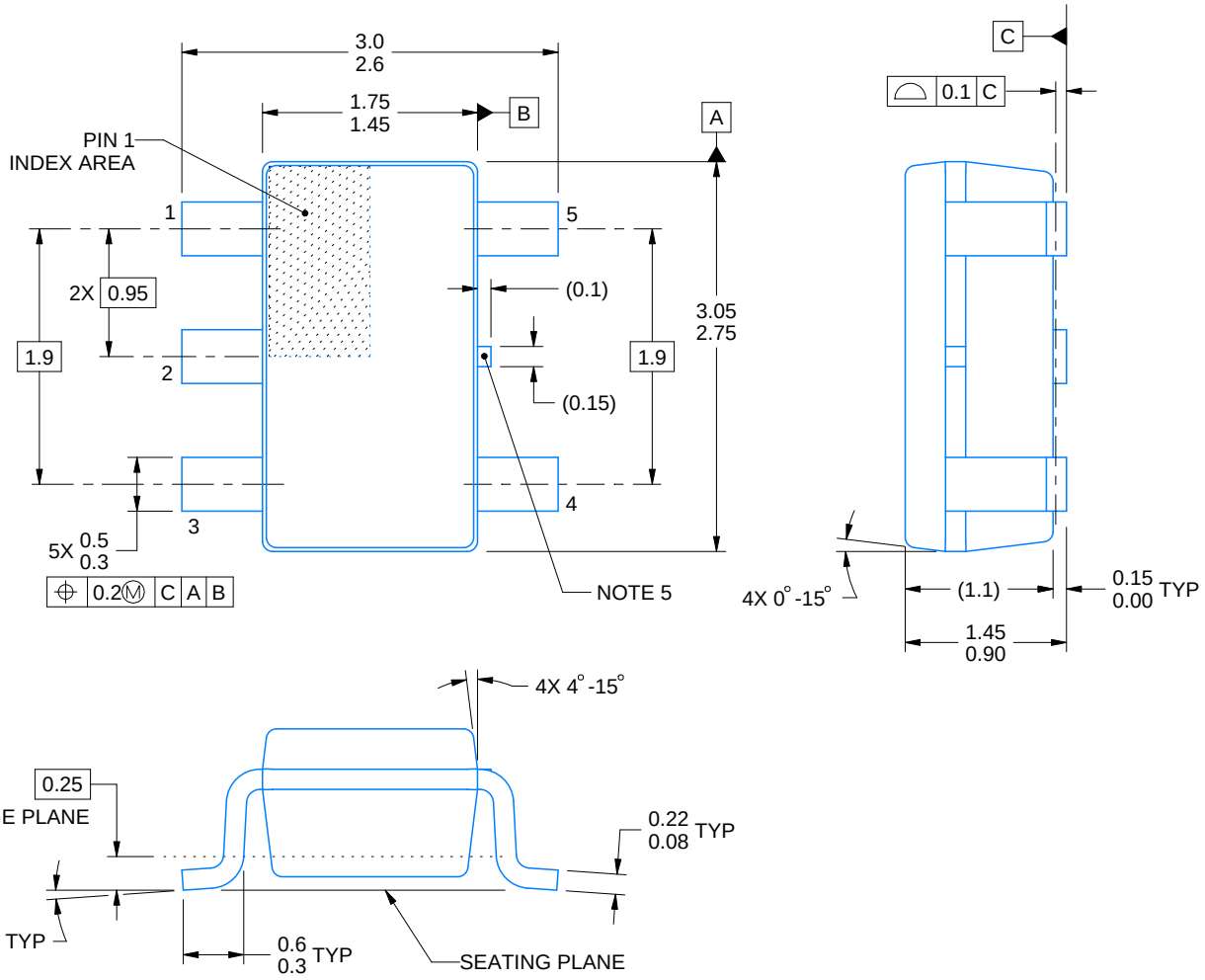
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3123J12DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3123J18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3124G15DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3124J12DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3124J18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3125G15DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3125J12DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3125J18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3125L30DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3126E12DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3126E15DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3126E18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3128E12DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TPS3128E15DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3128E18DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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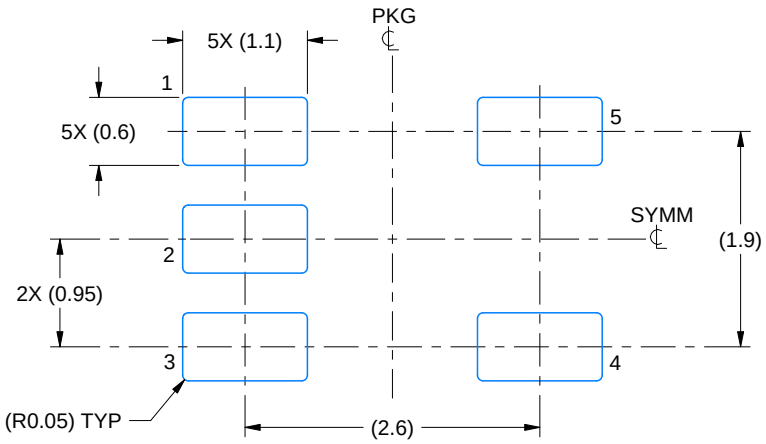
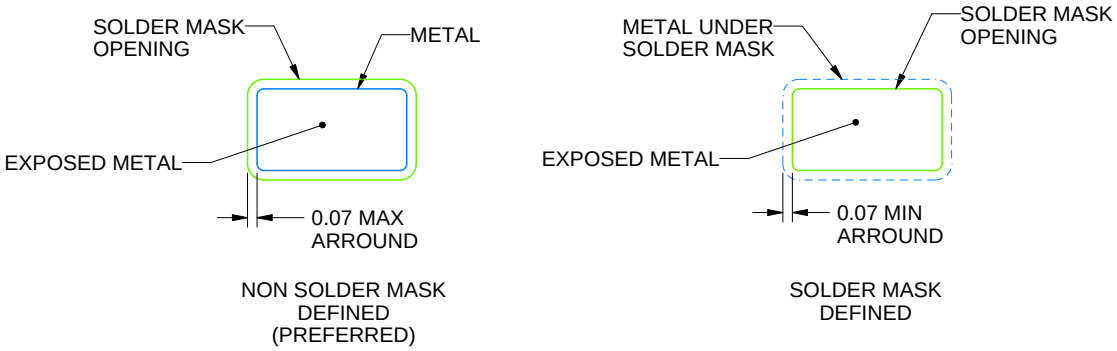
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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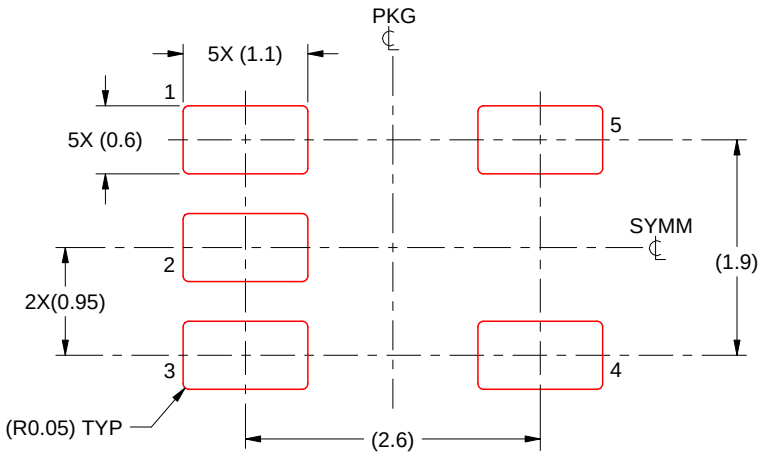
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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