

TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C TIBPAL20L8-20M, TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M HIGH-PERFORMANCE **IMPACT**™ **PAL**® CIRCUITS

SRPS021A – D2920, JUNE 1986 – REVISED DECEMBER 2010

- **High-Performance:** $f_{\max}$ (w/o feedback)
TIBPAL20R' -15C Series . . . 45 MHz
TIBPAL20R' -20M Series . . . 41.6 MHz
- **High-Performance . . . 45 MHz Min**
- **Reduced I_{CC} of 180 mA Max**
- **Functionally Equivalent, but Faster Than**
PAL20L8, PAL20R4, PAL20R6, PAL20R8
- **Power-Up Clear on Registered Devices (All**
Register Outputs are Set Low, but Voltage
Levels at the Output Pins Go High)
- **Preload Capability on Output Registers**
Simplifies Testing
- **Package Options Include Both Plastic and**
Ceramic Chip Carriers in Addition to Plastic
and Ceramic DIPs

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORT S
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

description

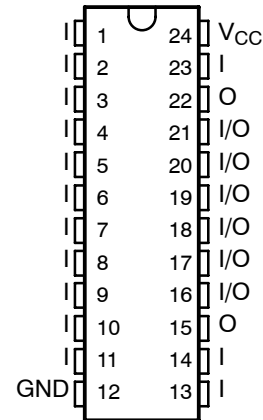
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These **IMPACT**™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C series is characterized from 0°C to 75°C. The TIBPAL20' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

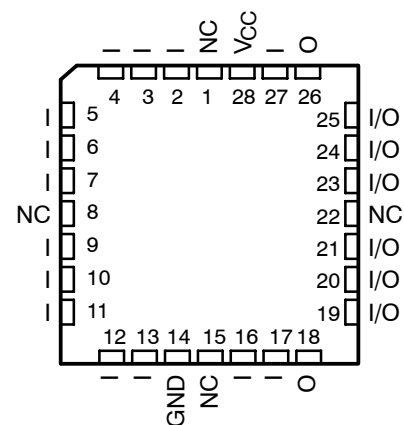
TIBPAL20L8'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE

(TOP VIEW)



TIBPAL20L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

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Products conform to specifications per the terms of Texas Instruments
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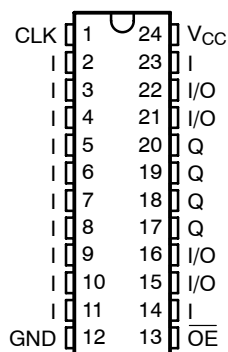
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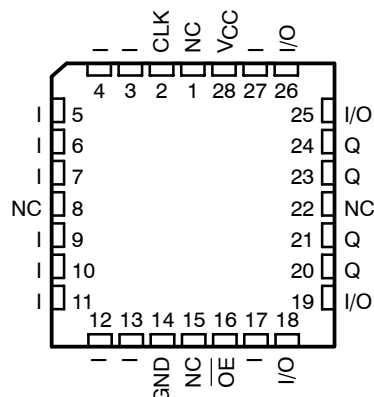
TIBPAL20R4'
C SUFFIX ... JT OR NT PACKAGE
M SUFFIX ... JT OR W PACKAGE

(TOP VIEW)



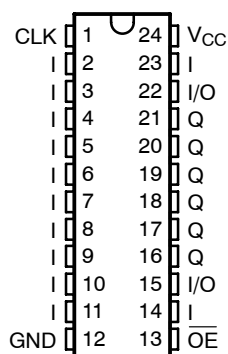
TIBPAL20R4'
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M SUFFIX ... FK PACKAGE

(TOP VIEW)



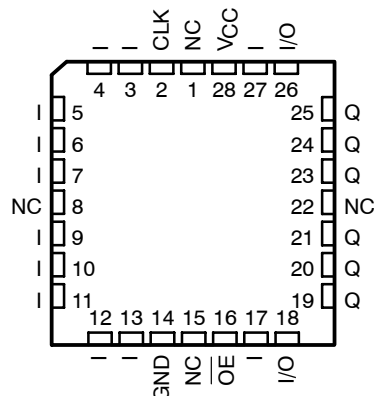
TIBPAL20R6'
C SUFFIX ... JT OR NT PACKAGE
M SUFFIX ... JT OR W PACKAGE

(TOP VIEW)



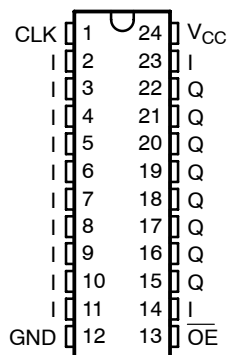
TIBPAL20R6'
C SUFFIX ... FN PACKAGE
M SUFFIX ... FK PACKAGE

(TOP VIEW)



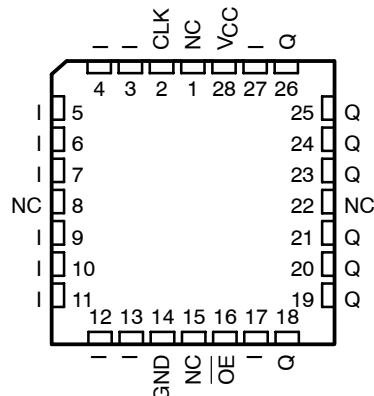
TIBPAL20R8'
C SUFFIX ... JT OR NT PACKAGE
M SUFFIX ... JT OR W PACKAGE

(TOP VIEW)



TIBPAL20R8'
C SUFFIX ... FN PACKAGE
M SUFFIX ... FK PACKAGE

(TOP VIEW)



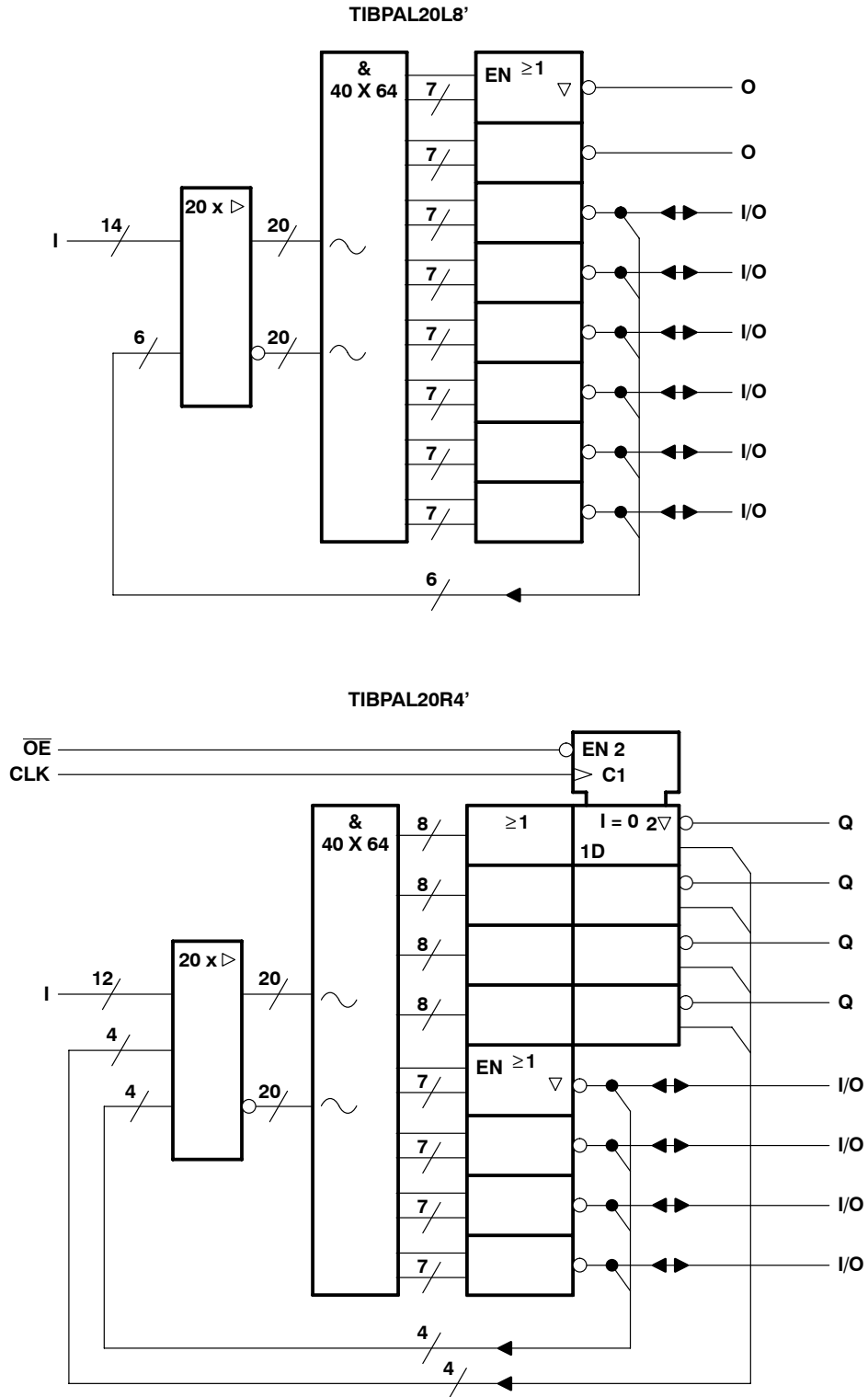
Pin assignments in operating mode

NC – No internal connection

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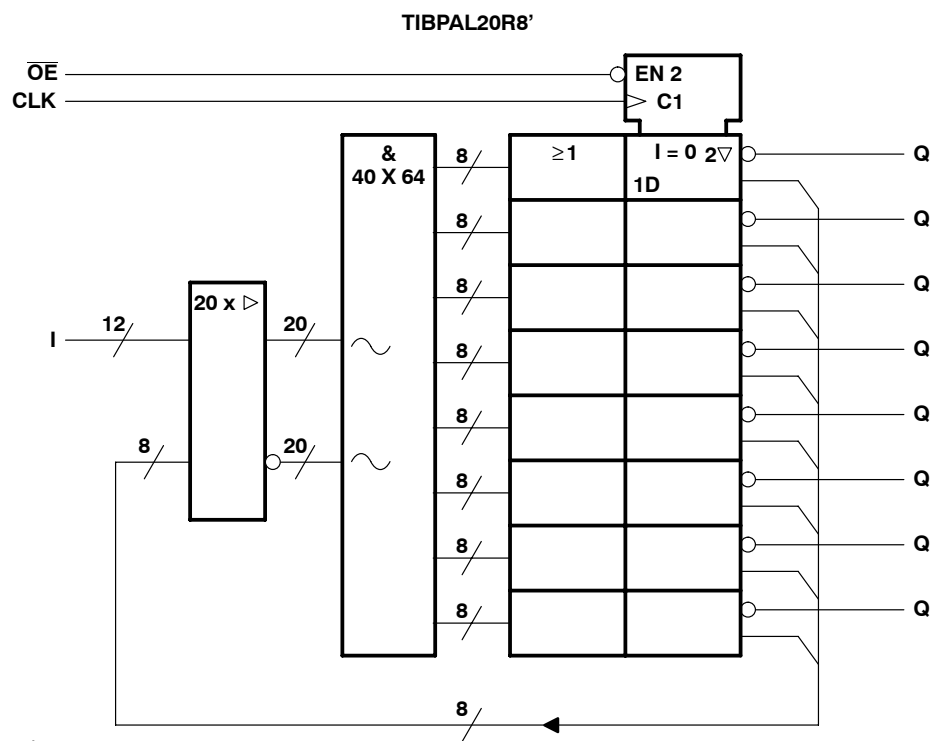
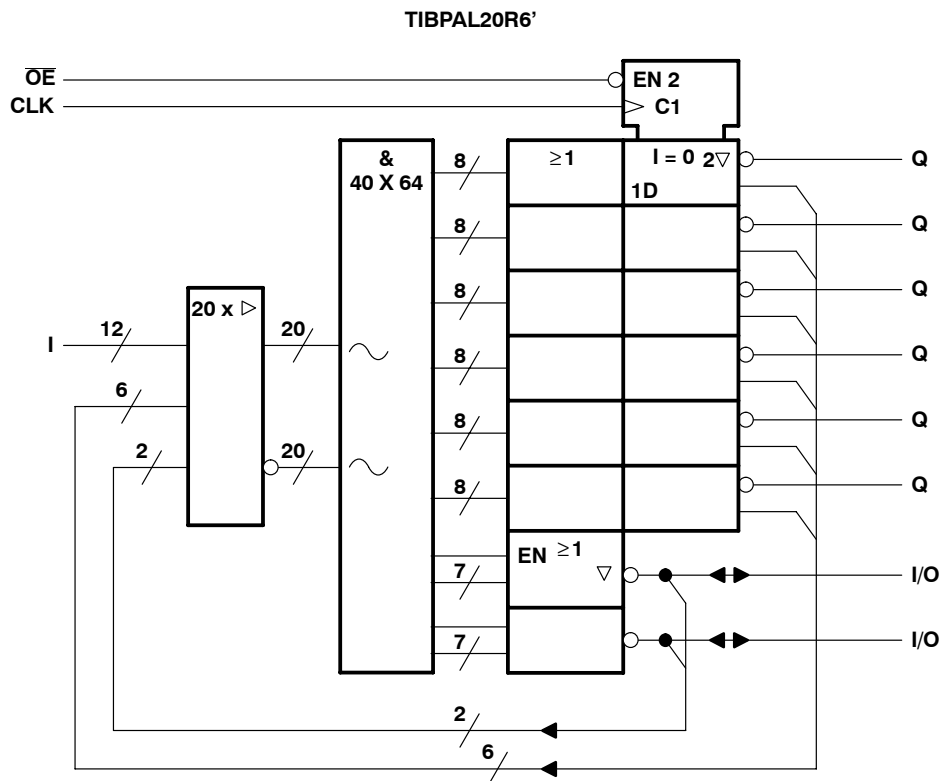
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functional block diagrams (positive logic)



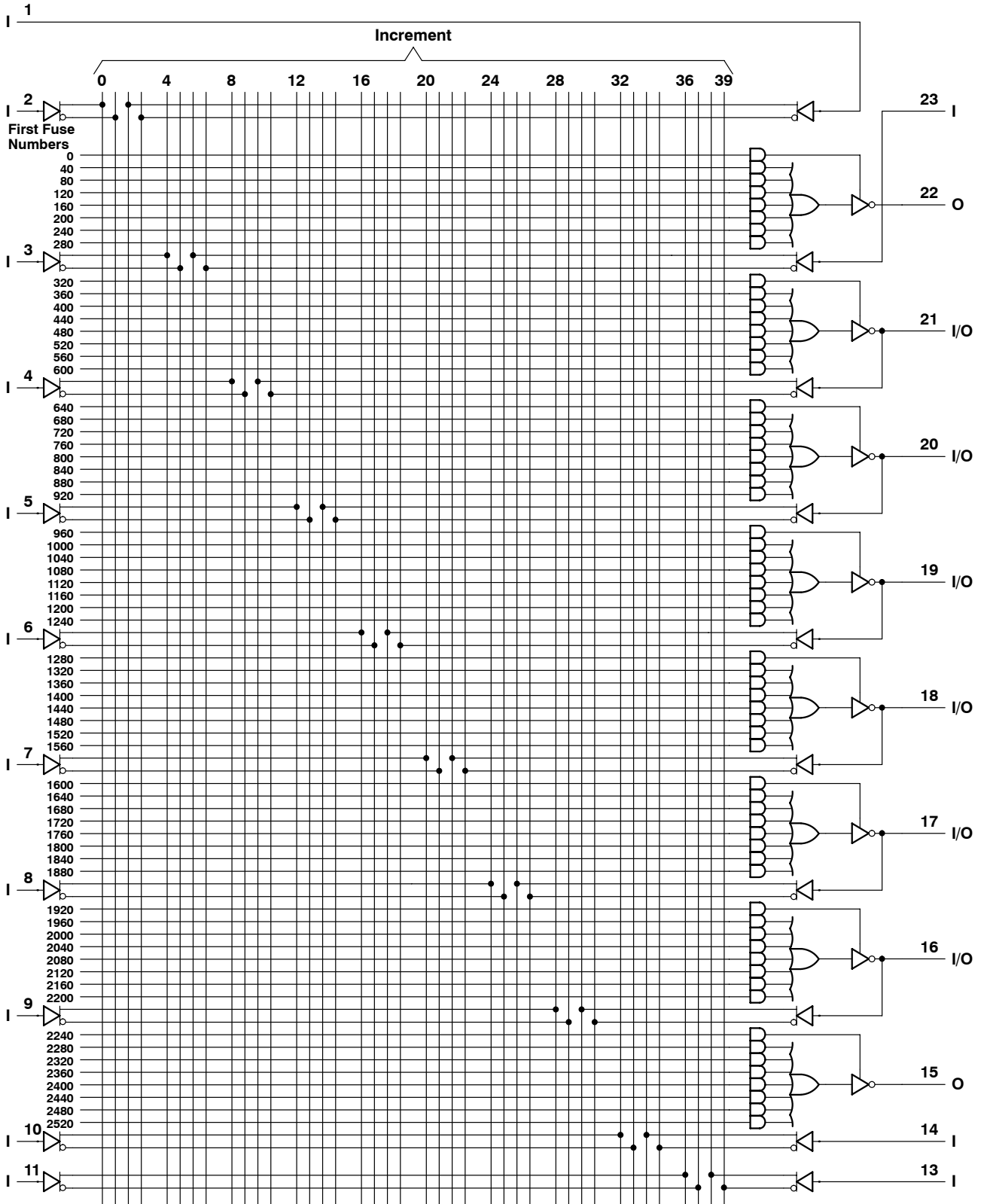
TIBPAL20R6-15C, TIBPAL20R8-15C
TIBPAL20R6-20M, TIBPAL20R8-20M
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functional block diagrams (positive logic)



~ denotes fused inputs

logic diagram (positive logic)

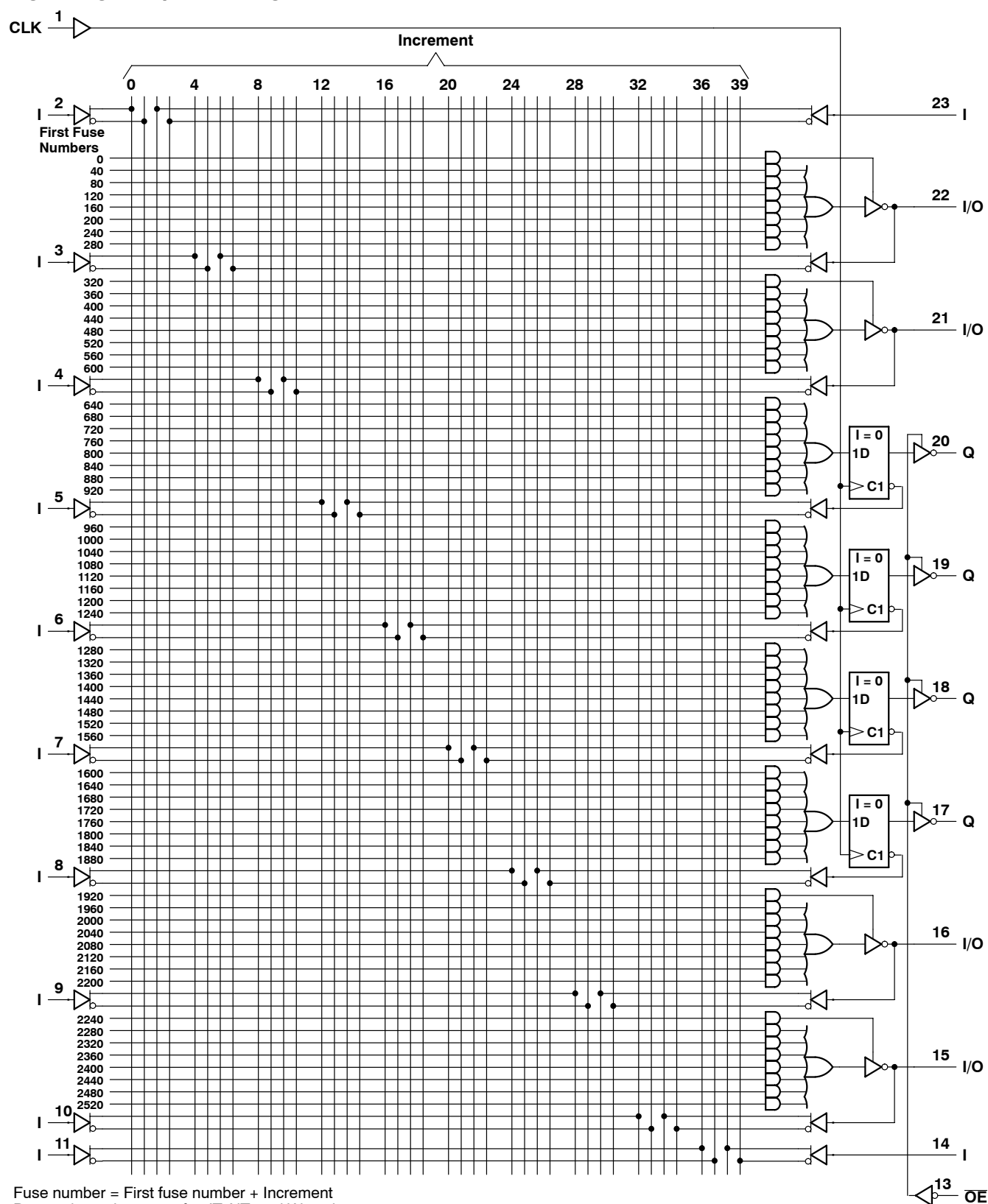


Fuse number = First fuse number + Increment
 Pin numbers shown are for JT, NT, and W packages.

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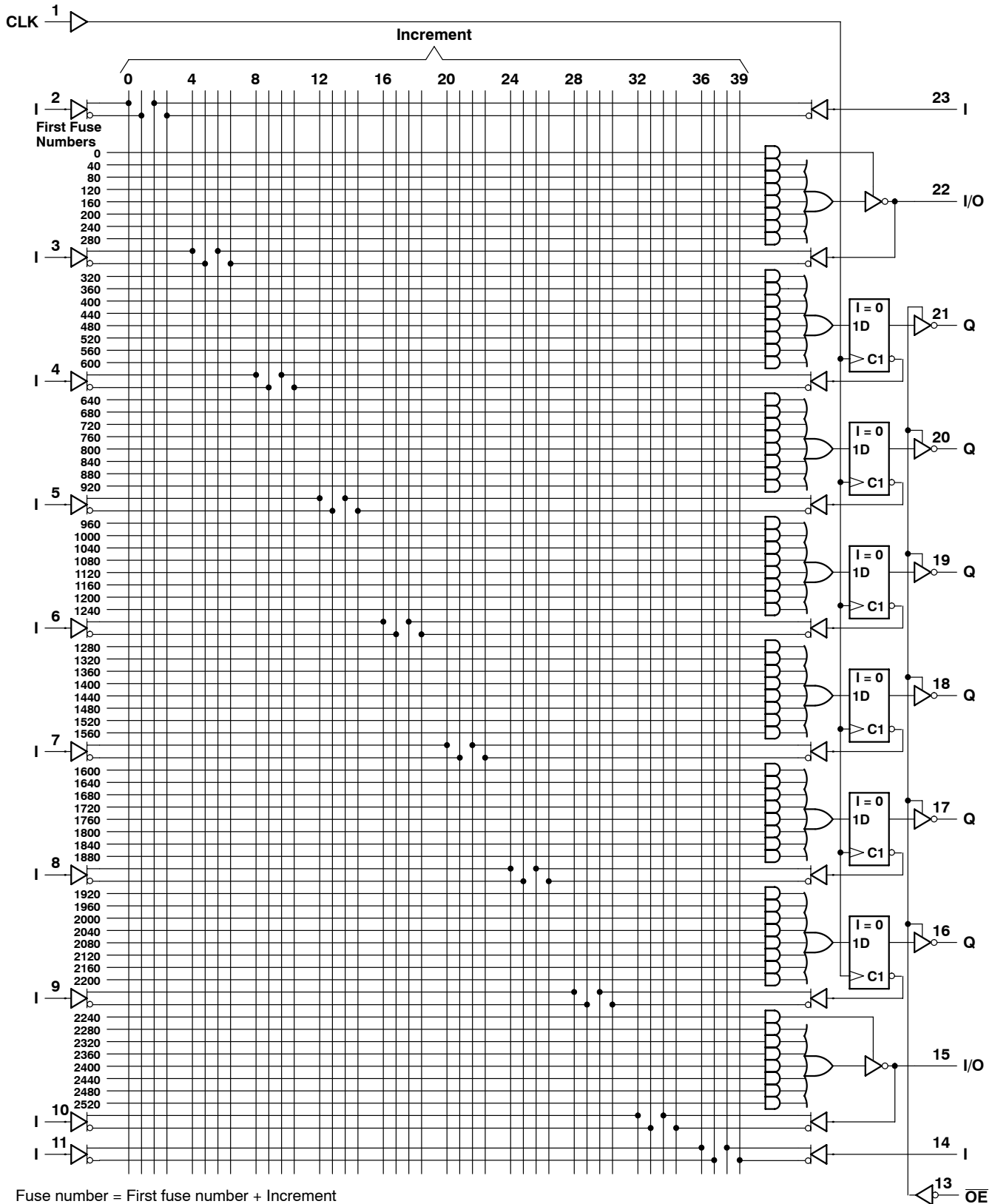
logic diagram (positive logic)



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logic diagram (positive logic)



Fuse number = First fuse number + Increment
 Pin numbers shown are for JT, NT, and W packages.

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Figure 10 is a detailed diagram of the 10K10K0-10 device, showing the internal structure and fuse map. The diagram is divided into three main sections: the top section for the clock and increment counter, the middle section for the fuse map, and the bottom section for the output logic.

Top Section: Clock and Increment Counter

- CLK 1**: The clock input, represented by a triangle symbol.
- Increment**: A counter that increments by 1 for each clock cycle. The output is labeled **Increment** and ranges from 0 to 39.

Middle Section: Fuse Map

The fuse map is a grid with **First Fuse Numbers** on the vertical axis (0 to 2520) and **Increment** on the horizontal axis (0 to 39). The grid shows the connections between the first fuse numbers and the increment counter. The connections are represented by dots on the grid lines.

Bottom Section: Output Logic

The output logic shows 10 outputs (Q13 to Q23) each with a 1D input and a C1 input. The outputs are labeled **Q13** through **Q23**. The logic for each output is shown as a block with inputs **I = 0**, **1D**, and **C1**. The output of each block is connected to the corresponding output pin.

Fuse Map Data

The fuse map shows the connections between the first fuse numbers and the increment counter. The connections are as follows:

First Fuse Number	Increment
0	0
40	0
80	0
120	0
160	0
200	0
240	0
280	0
320	0
360	0
400	0
440	0
480	0
520	0
560	0
600	0
640	0
680	0
720	0
760	0
800	0
840	0
880	0
920	0
960	0
1000	0
1040	0
1080	0
1120	0
1160	0
1200	0
1240	0
1280	0
1320	0
1360	0
1400	0
1440	0
1480	0
1520	0
1560	0
1600	0
1640	0
1680	0
1720	0
1760	0
1800	0
1840	0
1880	0
1920	0
1960	0
2000	0
2040	0
2080	0
2120	0
2160	0
2200	0
2240	0
2280	0
2320	0
2360	0
2400	0
2440	0
2480	0
2520	0

Output Logic

The output logic shows 10 outputs (Q13 to Q23) each with a 1D input and a C1 input. The outputs are labeled **Q13** through **Q23**. The logic for each output is shown as a block with inputs **I = 0**, **1D**, and **C1**. The output of each block is connected to the corresponding output pin.

Fuse number = First fuse number + Increment

Fuse number = First fuse number + Increment
Pin numbers shown are for JT, NT, and W packages.

TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–3.2	mA
I_{OL}	Low-level output current			24	mA
$f_{clock}^{\dagger}$	Clock frequency	0		45	MHz
$t_w^{\dagger}$	Pulse duration, clock	High		10	ns
		Low		12	
$t_{su}^{\dagger}$	Setup time, input or feedback before clock $\uparrow$	15			ns
$t_h^{\dagger}$	Hold time, input or feedback after clock $\uparrow$	0			ns
T_A	Operating free-air temperature	0	25	75	°C

$^{\dagger} f_{clock}$, t_w , t_{su} , and t_h do not apply for TIBPAL20L8'.



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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.75\text{ V}$,	$I_I = -18\text{ mA}$		-0.8	-1.5	V
V_{OH}		$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -3.2\text{ mA}$	2.4			V
V_{OL}		$V_{CC} = 4.75\text{ V}$,	$I_{OL} = 24\text{ mA}$		0.3	0.5	V
I_{OZH}	O, Q outputs	$V_{CC} = 5.25\text{ V}$,	$V_O = 2.7\text{ V}$			20	μA
	I/O ports					100	
I_{OZL}	O, Q outputs	$V_{CC} = 5.25\text{ V}$,	$V_O = 0.4\text{ V}$			-20	μA
	I/O ports					-250	
I_I		$V_{CC} = 5.25\text{ V}$,	$V_I = 5.5\text{ V}$			0.1	mA
$I_{IH}^\ddagger$		$V_{CC} = 5.25\text{ V}$,	$V_I = 2.7\text{ V}$			25	μA
$I_{IL}^\ddagger$		$V_{CC} = 5.25\text{ V}$,	$V_I = 0.4\text{ V}$			-0.25	mA
$I_{OS}^\S$		$V_{CC} = 5.25\text{ V}$,	$V_O = 0.5\text{ V}$	-30	-70	-130	mA
I_{CC}		$V_{CC} = 5.25\text{ V}$, Outputs open,	$V_I = 0$, $\overline{OE}$ at V_{IH}		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f _{max} [¶]	With feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 3	37	40		MHz
	Without feedback			45	50		
t _{pd}	I, I/O	O, I/O			12	15	ns
t _{pd}	CLK↑	Q			8	12	ns
t _{en}	OE	Q			10	15	ns
t _{dis}	OE↑	Q			8	12	ns
t _{en}	I, I/O	O, I/O			12	18	ns
t _{dis}	I, I/O	O, I/O			12	15	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

$$^\P f_{\max}(\text{with feedback}) = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}, \quad f_{\max}(\text{without feedback}) = \frac{1}{t_{w\text{ high}} + t_{w\text{ low}}},$$

$f_{\max}$ does not apply for TIBPAL20L8.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	–55°C to 125°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2	mA
I_{OL}	Low-level output current			12	mA
$f_{clock}^{\dagger}$	Clock frequency	0		41.6	MHz
$t_w^{\dagger}$	Pulse duration, clock	High		12	ns
		Low		12	
$t_{su}^{\dagger}$	Setup time, input or feedback before clock $\uparrow$	20			ns
$t_h^{\dagger}$	Hold time, input or feedback after clock $\uparrow$	0			ns
T_A	Operating free-air temperature	–55	25	125	°C

$^{\dagger} f_{clock}$, t_w , t_{su} , and t_h do not apply for TIBPAL20L8'.



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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$		-0.8	-1.5	V
V_{OH}		$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -2\text{ mA}$	2.4	3.2		V
V_{OL}		$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 12\text{ mA}$		0.3	0.5	V
I_{OZH}		$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$			100	μA
$I_{OZL}^\ddagger$	O, Q outputs	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$			-20	μA
	I/O ports					-250	
I_I		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$			1	mA
$I_{IH}^\ddagger$	I/O ports	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			100	μA
	All others					25	
$I_{IL}^\ddagger$		$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$			-0.25	mA
$I_{OS}^\S$		$V_{CC} = 5.5\text{ V}$,	$V_O = 0.5\text{ V}$	-30	-70	-250	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, Outputs open,	$V_I = 0$, $OE = V_{IH}$		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f _{max} [¶]	With feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 3	28.5	40		MHz
	Without feedback			41.6	50		
t _{pd}	I, I/O	O, I/O			12	20	ns
t _{pd}	CLK↑	Q			8	15	ns
t _{en}	$\overline{OE}$	Q			10	20	ns
t _{dis}	$\overline{OE}\uparrow$	Q			8	20	ns
t _{en}	I, I/O	O, I/O			12	25	ns
t _{dis}	I, I/O	O, I/O			12	20	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

$$^\parallel f_{\max}(\text{with feedback}) = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}, \quad f_{\max}(\text{without feedback}) = \frac{1}{t_{w\text{ high}} + t_{w\text{ low}}},$$

$f_{\max}$ does not apply for TIBPAL20L8.



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programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL} , raise Pin 13 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 13 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.

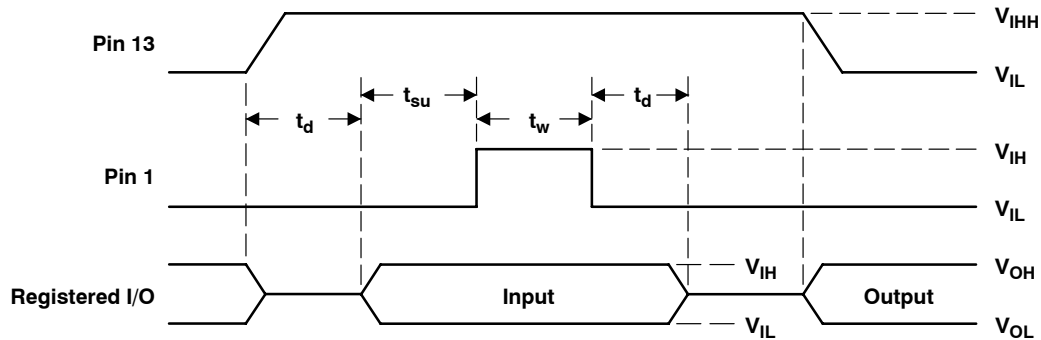


Figure 1. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT, NT, and W packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

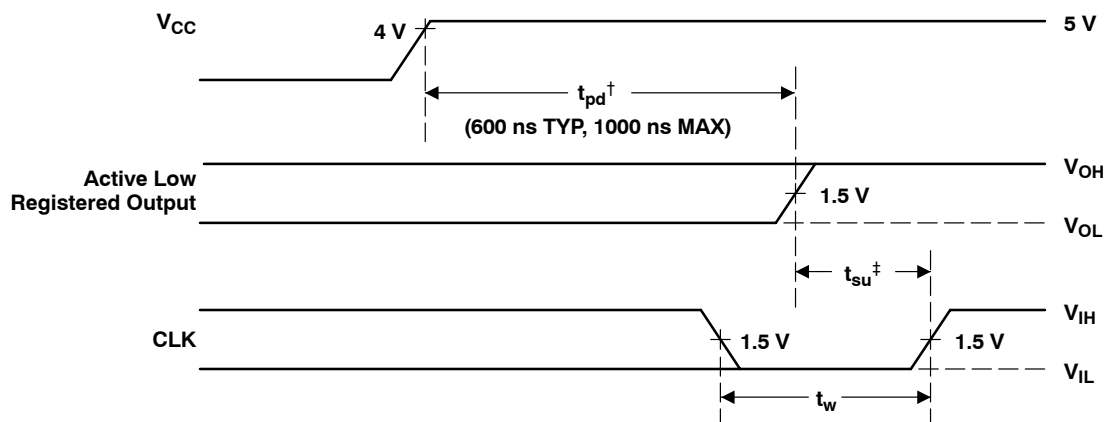
3. $t_d = t_{su} = t_h = 100$ ns to 1000 ns $V_{IHH} = 10.25$ V to 10.75 v

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power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

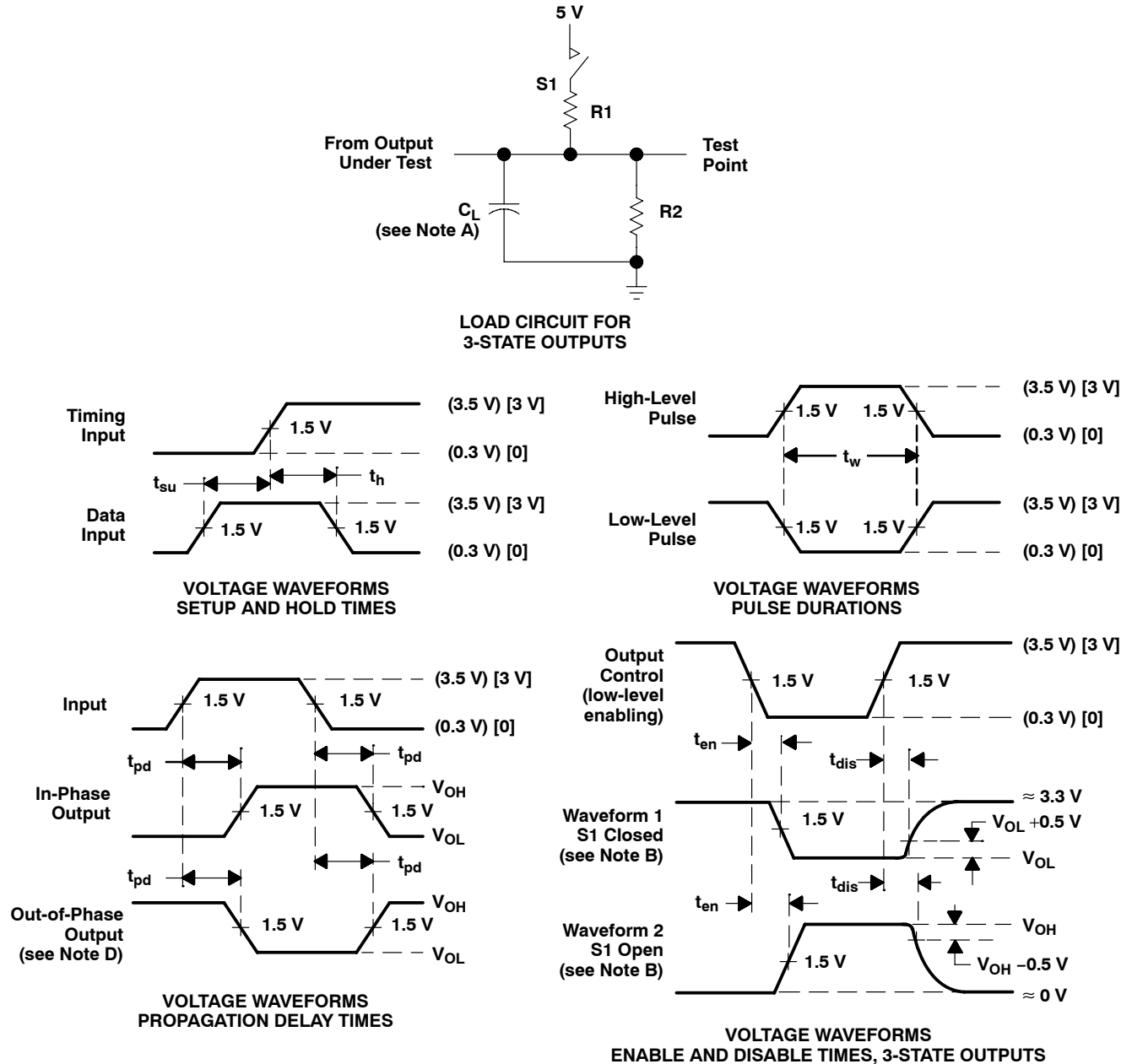


† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses (). PRR ≤ 1 MHz, t_r = t_f ≤ 2 ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets []. PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

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Elmo Semiconductor	(818) 768-7400
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D0892

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-87671013A	Active	Production	LCCC (FD) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87671013A TIBPAL20 L8-20MFDB
5962-87671013A.A	Active	Production	LCCC (FD) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87671013A TIBPAL20 L8-20MFDB
5962-87671043A	Active	Production	LCCC (FD) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87671043A TIBPAL20 R4-20MFDB
5962-87671043A.A	Active	Production	LCCC (FD) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87671043A TIBPAL20 R4-20MFDB
5962-8767104LA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8767104LA TIBPAL20R4-20M JTB
5962-8767104LA.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8767104LA TIBPAL20R4-20M JTB
8412901XA	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8412901XA TIBPAL20 L8-20MFKB
8412901XA.A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8412901XA TIBPAL20 L8-20MFKB
8412902LA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8412902LA TIBPAL20R8-20M JTB
8412902LA.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8412902LA TIBPAL20R8-20M JTB

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
8412904LA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8412904LA TIBPAL20R4-20M JTB
8412904LA.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8412904LA TIBPAL20R4-20M JTB
JM38510/50501BLA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 50501BLA
JM38510/50501BLA.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 50501BLA
JM38510/50502BLA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 50502BLA
JM38510/50502BLA.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 50502BLA
JM38510/50504BLA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 50504BLA
JM38510/50504BLA.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 50504BLA
M38510/50501BLA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 50501BLA
M38510/50502BLA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 50502BLA
M38510/50504BLA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 50504BLA
TIBPAL20R4-20MJT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TIBPAL20R4-20M JT
TIBPAL20R4-20MJT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TIBPAL20R4-20M JT
TIBPAL20R4-20MJTB	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8767104LA TIBPAL20R4-20M JTB
TIBPAL20R4-20MJTB.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8767104LA TIBPAL20R4-20M JTB

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TIBPAL20R8-20MJTB	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8767102LA TIBPAL20R8-20M JTB
TIBPAL20R8-20MJTB.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8767102LA TIBPAL20R8-20M JTB

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

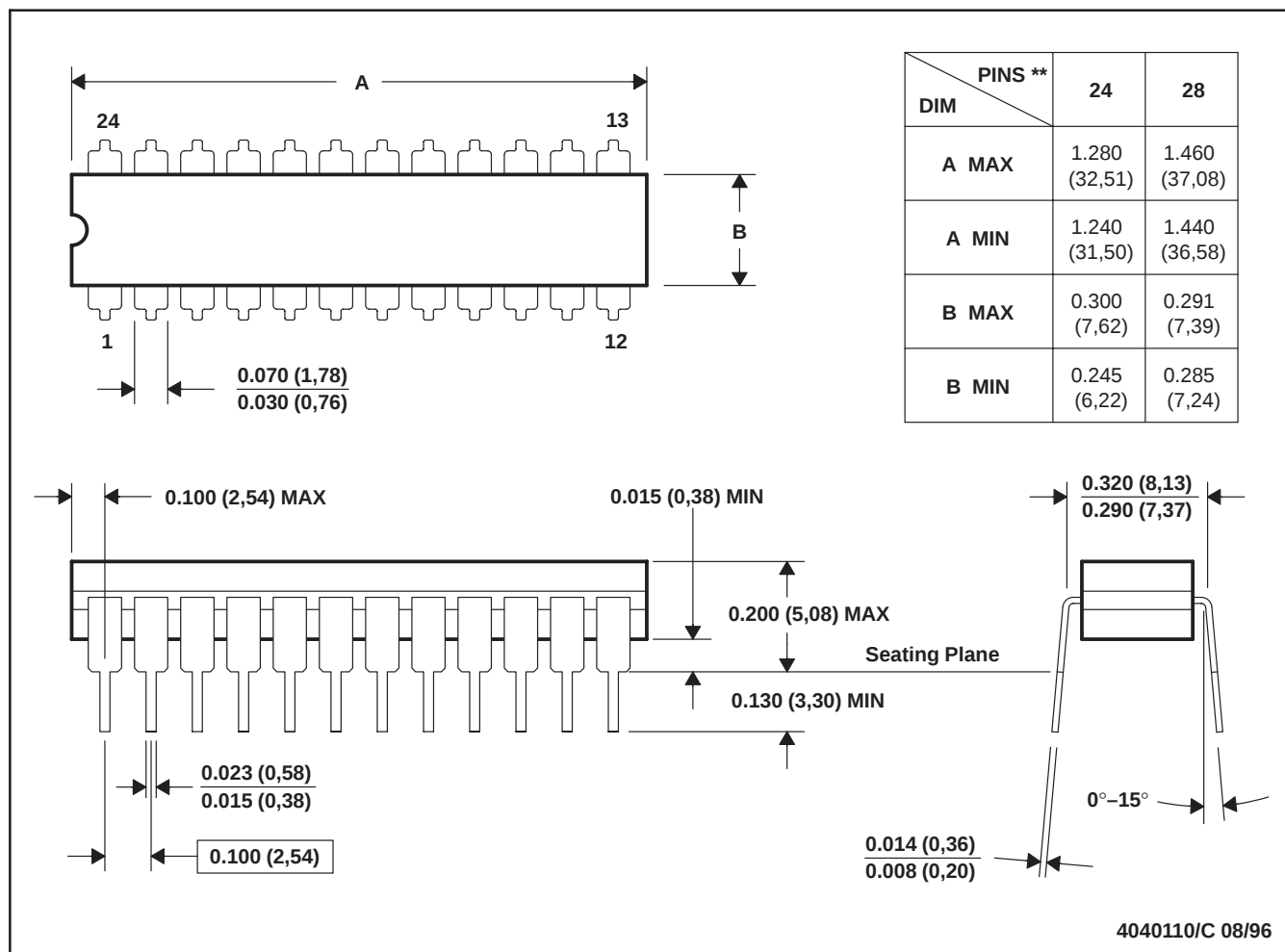
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JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



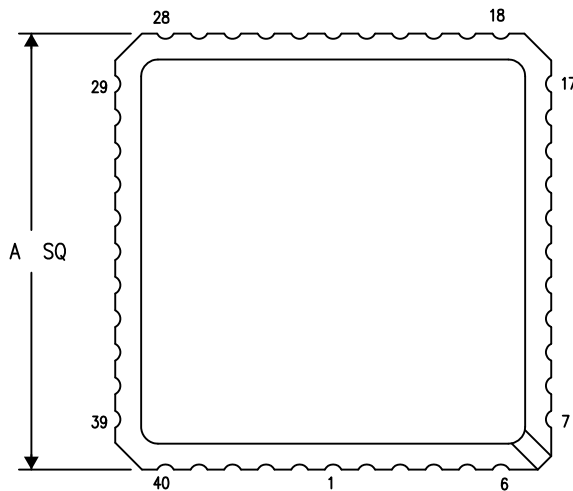
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

MECHANICAL DATA

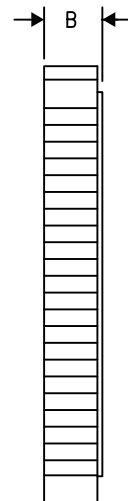
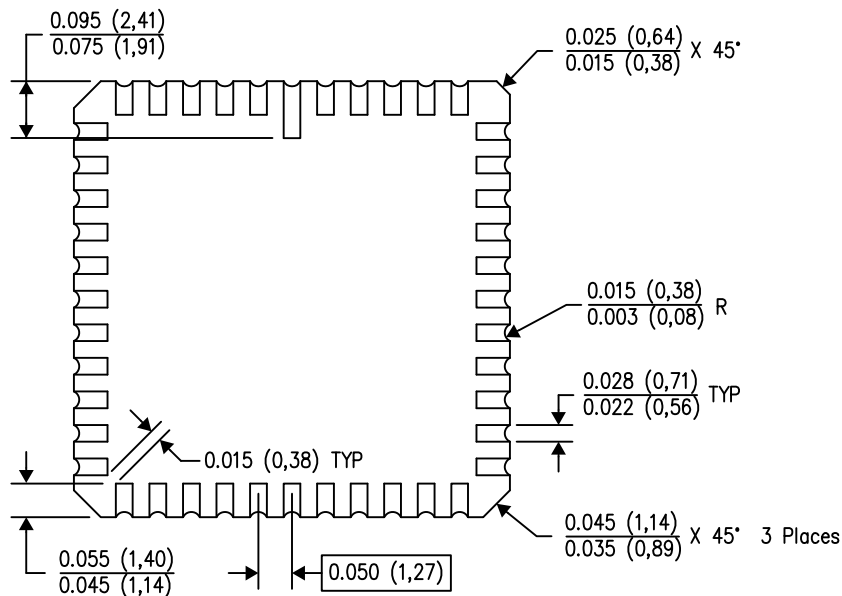
FD (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

44 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.064 (1,63)	0.080 (2,03)
28	0.442 (11,23)	0.458 (11,63)	0.064 (1,63)	0.080 (2,03)
44	0.640 (16,26)	0.660 (16,76)	0.069 (1,75)	0.120 (3,05)
52	0.739 (18,78)	0.761 (19,33)	0.082 (2,08)	0.120 (3,05)
68	0.938 (23,83)	0.962 (24,43)	0.082 (2,08)	0.120 (3,05)
84	1.135 (28,83)	1.165 (29,59)	0.082 (2,08)	0.120 (3,05)



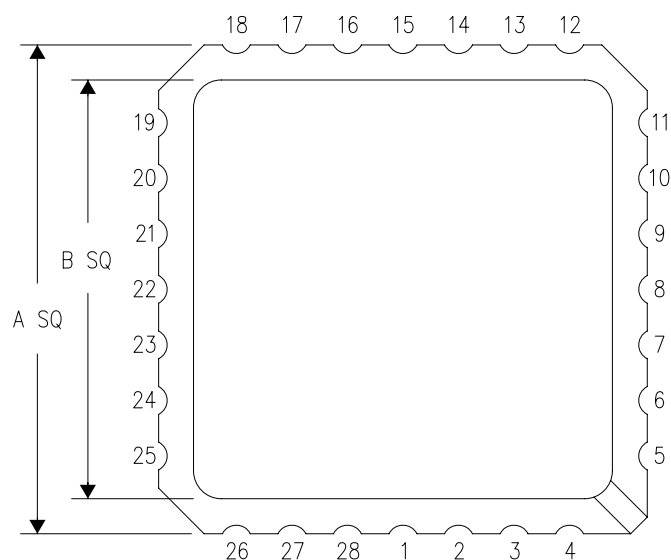
4040136/C 08/12

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals will be gold plated.
 - Falls within JEDEC MS-004.

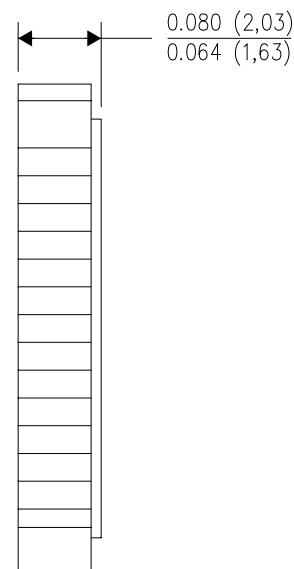
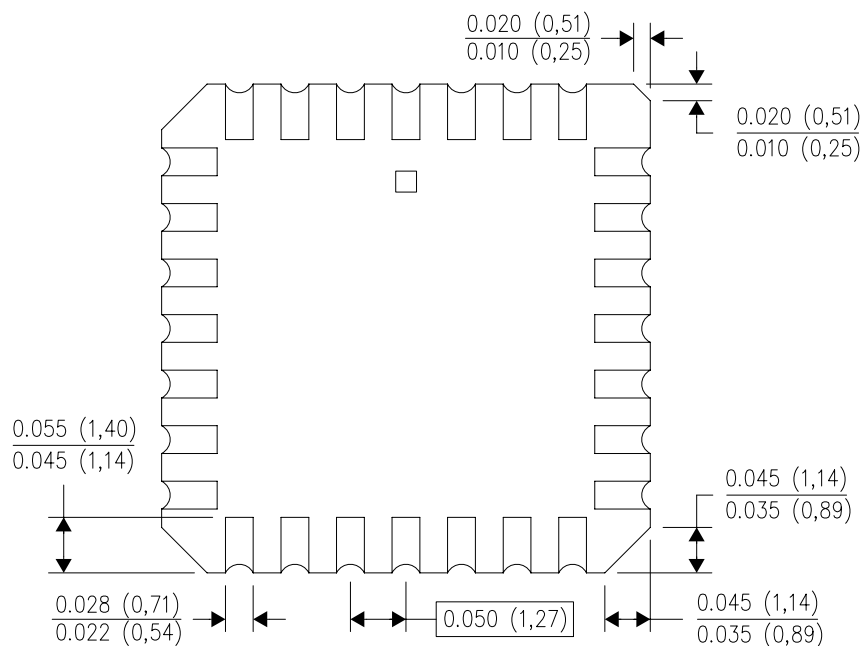
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

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