

# MC10135

## Dual J-K Master-Slave Flip-Flop

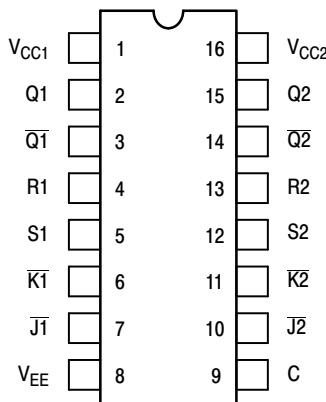
The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate  $\bar{J}$ - $\bar{K}$  inputs. When the clock is static, the  $\bar{J}$ - $\bar{K}$  inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.

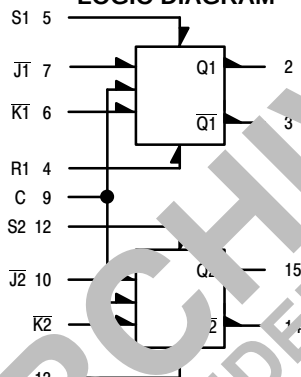
- $P_D = 280$  mW typ/pkg (No Load)
- $f_{Tog} = 140$  MHz typ
- $t_{pd} = 3.0$  ns typ
- $t_r, t_f = 2.5$  ns typ (20%–80%)

### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Configuration Tables on page 18 of the ON Semiconductor ECL Data Book (DL122/D).

### LOGIC DIAGRAM



$V_{CC1} = \text{PIN 1}$   
 $V_{CC2} = \text{PIN 16}$   
 $V_{EE} = \text{PIN 8}$

### R-S TRUTH TABLE

| R | S | $Q_{n+1}$ |
|---|---|-----------|
| L | L | $Q_n$     |
| L | H | H         |
| H | L | L         |
| H | H | N.D.      |

N.D. = Not Defined

### CLOCK J-K TRUTH TABLE\*

| $\bar{J}$ | $\bar{K}$ | $Q_{n+1}$   |
|-----------|-----------|-------------|
| L         | L         | $\bar{Q}_n$ |
| H         | L         | L           |
| L         | H         | H           |
| H         | H         | $Q_n$       |

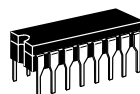
\*Output states change on positive transition of clock for  $\bar{J}$ - $\bar{K}$  input condition present.



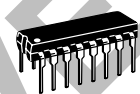
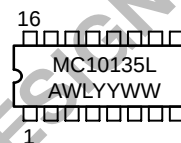
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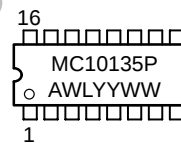
### MARKING DIAGRAMS



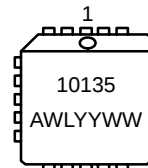
CDIP-16  
L SUFFIX  
CASE 620



PDIP-16  
P SUFFIX  
CASE 648



PLCC-20  
FN SUFFIX  
CASE 775



A = Assembly Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week

### ORDERING INFORMATION

| Device    | Package | Shipping        |
|-----------|---------|-----------------|
| MC10135L  | CDIP-16 | 25 Units / Rail |
| MC10135P  | PDIP-16 | 25 Units / Rail |
| MC10135FN | PLCC-20 | 46 Units / Rail |

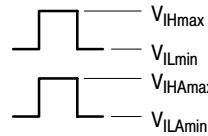
## ELECTRICAL CHARACTERISTICS

| Characteristic                            | Symbol                            | Pin Under Test            | Test Limits      |                  |                  |     |                  |                  |                  | Unit |
|-------------------------------------------|-----------------------------------|---------------------------|------------------|------------------|------------------|-----|------------------|------------------|------------------|------|
|                                           |                                   |                           | −30°C            |                  | +25°C            |     |                  | +85°C            |                  |      |
|                                           |                                   |                           | Min              | Max              | Min              | Typ | Max              | Min              | Max              |      |
| Power Supply Drain Current                | I <sub>E</sub>                    | 8                         |                  | 75               |                  | 54  | 68               |                  | 75               | mAdc |
| Input Current                             | I <sub>inH</sub>                  | 6,7,9,10,11<br>4,5,12,13  |                  | 425<br>620       |                  |     | 265<br>390       |                  | 265<br>390       | μAdc |
|                                           | I <sub>inL</sub>                  | 4,5,6,7,9,<br>10,11,12,13 | 0.5<br>0.5       |                  | 0.5<br>0.5       |     |                  | 0.3<br>0.3       |                  | μAdc |
| Output Voltage      Logic 1               | V <sub>OH</sub>                   | 2<br>2 (3.)               | −1.060<br>−1.060 | −0.890<br>−0.890 | −0.960<br>−0.960 |     | −0.810<br>−0.810 | −0.890<br>−0.890 | −0.700<br>−0.700 | Vdc  |
| Output Voltage      Logic 0               | V <sub>OL</sub>                   | 3<br>3 (3.)               | −1.890<br>−1.890 | −1.675<br>−1.675 | −1.850<br>−1.850 |     | −1.650<br>−1.650 | −1.825<br>−1.825 | −1.615<br>−1.615 | Vdc  |
| Threshold Voltage    Logic 1              | V <sub>OHA</sub>                  | 2<br>2 (4.)               | −1.080<br>−1.080 |                  | −0.980<br>−0.980 |     |                  | −0.910<br>−0.910 |                  | Vdc  |
| Threshold Voltage    Logic 0              | V <sub>OLA</sub>                  | 3<br>3 (4.)               |                  | −1.655<br>−1.655 |                  |     | −1.630<br>−1.630 |                  | −1.595<br>−1.595 | Vdc  |
| Switching Times (50Ω Load)<br>Clock Input |                                   |                           |                  |                  |                  |     |                  |                  |                  | ns   |
| Propagation Delay                         | t <sub>9+2+</sub>                 | 2                         | 1.8              | 5.0              | 1.8              | 3.0 | 4.5              | 1.8              | 4.6              |      |
|                                           | t <sub>9+2−</sub>                 | 2                         | 1.8              | 5.0              | 1.8              | 3.0 | 4.5              | 1.8              | 4.6              |      |
| Rise Time            (20 to 80%)          | t <sub>2+</sub> , t <sub>3+</sub> | 2, 3                      | 1.1              | 4.8              | 1.1              | 2.0 | 4.5              | 1.1              | 4.7              |      |
| Fall Time            (20 to 80%)          | t <sub>2−</sub> , t <sub>3−</sub> | 2, 3                      | 1.1              | 4.8              | 1.1              | 2.0 | 4.5              | 1.1              | 4.7              |      |
| Set Input                                 |                                   |                           |                  |                  |                  |     |                  |                  |                  | ns   |
| Propagation Delay                         | t <sub>5+2+</sub>                 | 2                         | 1.8              | 5.6              | 1.8              | 3.0 | 5.0              | 1.8              | 5.2              |      |
|                                           | t <sub>12+15+</sub>               | 15                        | 1.8              | 5.6              | 1.8              | 3.0 | 5.0              |                  | 5.2              |      |
|                                           | t <sub>5+3−</sub>                 | 3                         | 1.8              | 5.6              | 1.8              | 3.0 | 5.0              |                  | 5.2              |      |
|                                           | t <sub>12+14−</sub>               | 14                        | 1.8              | 5.6              | 1.8              | 3.0 | 5.0              |                  | 5.2              |      |
| Reset Input                               |                                   |                           |                  |                  |                  |     |                  |                  |                  | ns   |
| Propagation Delay                         | t <sub>4+2−</sub>                 | 2                         | 1.8              | 5.6              | 1.8              | 3.0 | 5.0              | 1.8              | 5.2              |      |
|                                           | t <sub>4+3−</sub>                 | 3                         | 1.8              | 5.6              | 1.8              | 3.0 | 5.0              | 1.8              | 5.2              |      |
|                                           | t <sub>13+15−</sub>               | 15                        | 1.8              | 5.6              | 1.8              | 3.0 | 5.0              | 1.8              | 5.2              |      |
|                                           | t <sub>13+14+</sub>               | 14                        | 1.8              | 5.6              | 1.8              | 3.0 | 5.0              | 1.8              | 5.2              |      |
| Setup Time                                | t <sub>setup</sub>                | 7                         | 2.5              |                  | 2.5              | 1.0 |                  | 2.5              |                  | ns   |
| Hold Time                                 | t <sub>hold</sub>                 | 7                         | 1.5              |                  | 1.5              | 1.0 |                  | 2.5              |                  | ns   |
| Toggle Frequency (Max)                    | f <sub>tog</sub>                  | 2                         | 125              |                  | 125              | 140 |                  | 125              |                  | MHz  |

1. Individually test each input; apply  $V_{IHmax}$  to pin under test.

2. Individually test each input; apply  $V_{ILmin}$  to pin under test.

3. Output level to be measured after a clock pulse has been applied to the  $\overline{C_E}$  Input (Pin 6)



4. Output level to be measured after a clock pulse has been applied to the  $\overline{C_E}$  Input (Pin 6)

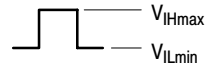
## ELECTRICAL CHARACTERISTICS (continued)

| @ Test Temperature                        |                                                                                      |                                  | TEST VOLTAGE VALUES (Volts)               |                    |                     |                    |                 | (V <sub>CC</sub> )<br>Gnd |
|-------------------------------------------|--------------------------------------------------------------------------------------|----------------------------------|-------------------------------------------|--------------------|---------------------|--------------------|-----------------|---------------------------|
|                                           |                                                                                      |                                  | V <sub>IHmax</sub>                        | V <sub>ILmin</sub> | V <sub>IHAmin</sub> | V <sub>ILAmx</sub> | V <sub>EE</sub> |                           |
|                                           |                                                                                      |                                  | –30°C                                     | –0.890             | –1.890              | –1.205             | –1.500          | –5.2                      |
|                                           |                                                                                      |                                  | +25°C                                     | –0.810             | –1.850              | –1.105             | –1.475          | –5.2                      |
|                                           |                                                                                      |                                  | +85°C                                     | –0.700             | –1.825              | –1.035             | –1.440          | –5.2                      |
| Characteristic                            | Symbol                                                                               | Pin Under Test                   | TEST VOLTAGE APPLIED TO PINS LISTED BELOW |                    |                     |                    |                 | (V <sub>CC</sub> )<br>Gnd |
|                                           |                                                                                      |                                  | V <sub>IHmax</sub>                        | V <sub>ILmin</sub> | V <sub>IHAmin</sub> | V <sub>ILAmx</sub> | V <sub>EE</sub> |                           |
| Power Supply Drain Current                | I <sub>E</sub>                                                                       | 8                                |                                           |                    |                     |                    | 8               | 1, 16                     |
| Input Current                             | I <sub>inH</sub>                                                                     | 6, 7, 9, 10, 11<br>4, 5, 12, 13  | Note 1.<br>Note 1.                        |                    |                     |                    | 8<br>8          | 1, 16<br>1, 16            |
|                                           | I <sub>inL</sub>                                                                     | 4, 5, 6, 7, 9,<br>10, 11, 12, 13 |                                           | Note 2.<br>Note 2. |                     |                    | 8<br>8          | 1, 16<br>1, 16            |
| Output Voltage Logic 1                    | V <sub>OH</sub>                                                                      | 2                                | 5                                         |                    |                     |                    | 8               | 1, 16                     |
|                                           |                                                                                      | 2 (3.)                           | 6                                         |                    |                     |                    | 8               | 1, 16                     |
| Output Voltage Logic 0                    | V <sub>OL</sub>                                                                      | 3                                | 5                                         |                    |                     |                    | 8               | 1, 16                     |
|                                           |                                                                                      | 3 (3.)                           | 6                                         |                    |                     |                    | 8               | 1, 16                     |
| Threshold Voltage Logic 1                 | V <sub>OHA</sub>                                                                     | 2                                |                                           |                    | 5                   |                    | 8               | 1, 16                     |
|                                           |                                                                                      | 2 (4.)                           | 6                                         |                    |                     |                    | 8               | 1, 16                     |
| Threshold Voltage Logic 0                 | V <sub>OLA</sub>                                                                     | 3                                |                                           |                    | 5                   |                    | 8               | 1, 16                     |
|                                           |                                                                                      | 3 (4.)                           | 6                                         |                    |                     |                    | 8               | 1, 16                     |
| Switching Times (50Ω Load)<br>Clock Input |                                                                                      |                                  |                                           |                    | Pulse In            | Pulse Out          | –3.2 V          | +2.0 V                    |
| Propagation Delay                         | t <sub>9+2+</sub><br>t <sub>9+2–</sub>                                               | 2                                |                                           |                    | 9                   | 2                  | 8               | 1, 16                     |
|                                           |                                                                                      | 2                                |                                           |                    | 9                   | 2                  | 8               | 1, 16                     |
| Rise Time (20 to 80%)                     | t <sub>2+, t3+</sub>                                                                 | 2, 3                             |                                           |                    | 9                   | 2, 3               | 8               | 1, 16                     |
| Fall Time (20 to 80%)                     | t <sub>2–, t3–</sub>                                                                 | 2, 3                             |                                           |                    | 9                   | 2, 3               | 8               | 1, 16                     |
| Set Input<br>Propagation Delay            | t <sub>5+2+</sub><br>t <sub>12+15+</sub><br>t <sub>5+3–</sub><br>t <sub>12+14–</sub> | 2                                |                                           |                    | 5                   | 2                  | 8               | 1, 16                     |
|                                           |                                                                                      | 15                               |                                           |                    | 12                  | 15                 | 8               | 1, 16                     |
|                                           |                                                                                      | 3                                |                                           |                    | 5                   | 3                  | 8               | 1, 16                     |
|                                           |                                                                                      | 14                               |                                           |                    | 12                  | 14                 | 8               | 1, 16                     |
| Reset Input<br>Propagation Delay          | t <sub>4+2–</sub><br>t <sub>4+3–</sub><br>t <sub>13+15–</sub><br>t <sub>13+14+</sub> | 2                                |                                           |                    | 4                   | 2                  | 8               | 1, 16                     |
|                                           |                                                                                      | 3                                |                                           |                    | 4                   | 3                  | 8               | 1, 16                     |
|                                           |                                                                                      | 15                               |                                           |                    | 13                  | 15                 | 8               | 1, 16                     |
|                                           |                                                                                      | 14                               |                                           |                    | 13                  | 14                 | 8               | 1, 16                     |
| Setup Time                                | t <sub>setup</sub>                                                                   | 7                                |                                           |                    | 6, 9                | 2                  | 8               | 1, 16                     |
| Hold Time                                 | t <sub>hold</sub>                                                                    | 7                                |                                           |                    | 6, 9                | 2                  | 8               | 1, 16                     |
| Toggle Frequency (Max)                    | f <sub>tog</sub>                                                                     | 2                                |                                           |                    | 9                   | 2                  | 8               | 1, 16                     |

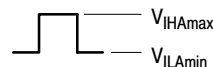
1. Individually test each input; apply V<sub>IHmax</sub> to pin under test.

2. Individually test each input; apply V<sub>ILmin</sub> to pin under test.

3. Output level to be measured after a clock pulse has been applied to the  $\overline{C_E}$  Input (Pin 6)



4. Output level to be measured after a clock pulse has been applied to the  $\overline{C_E}$  Input (Pin 6)

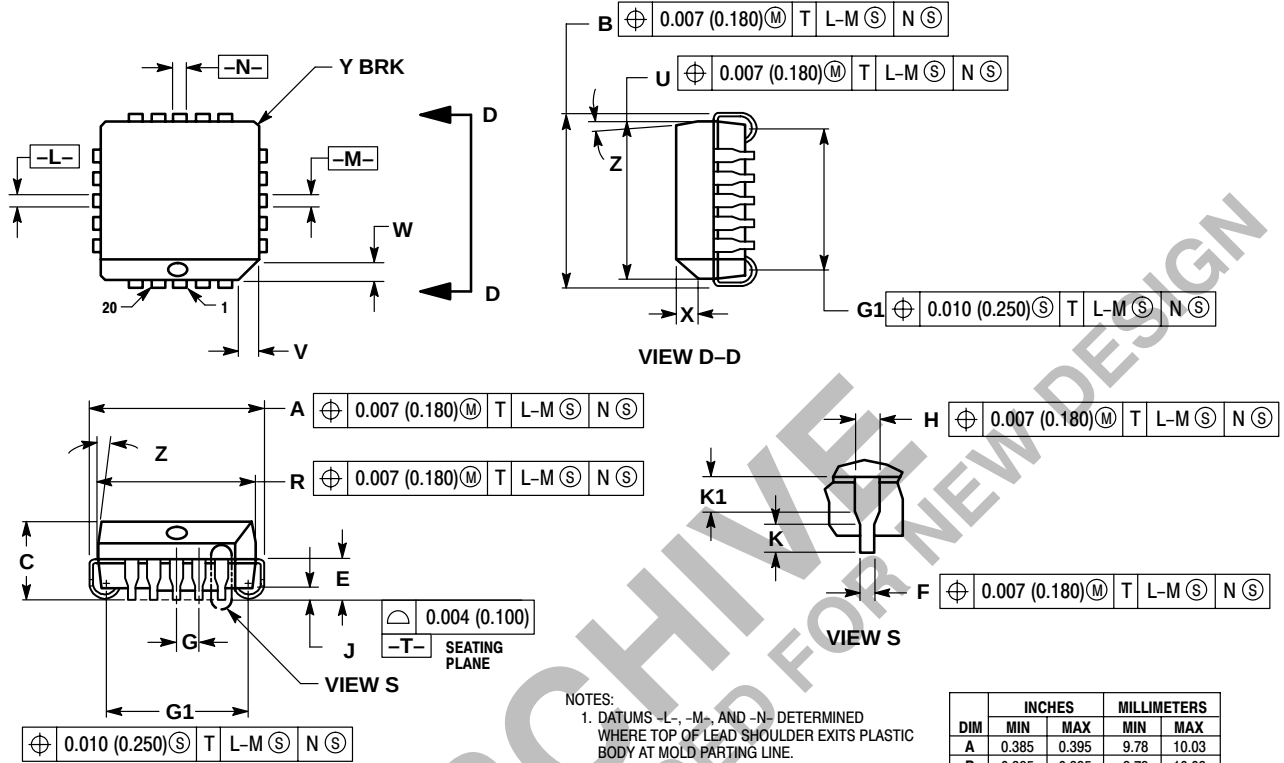


Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

# MC10135

## PACKAGE DIMENSIONS

PLCC-20  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.385     | 0.395 | 9.78        | 10.03 |
| B   | 0.385     | 0.395 | 9.78        | 10.03 |
| C   | 0.165     | 0.180 | 4.20        | 4.57  |
| E   | 0.090     | 0.110 | 2.29        | 2.79  |
| F   | 0.013     | 0.019 | 0.33        | 0.48  |
| G   | 0.050 BSC |       | 1.27 BSC    |       |
| H   | 0.026     | 0.032 | 0.66        | 0.81  |
| J   | 0.020     | ---   | 0.51        | ---   |
| K   | 0.025     | ---   | 0.64        | ---   |
| R   | 0.350     | 0.356 | 8.89        | 9.04  |
| U   | 0.350     | 0.356 | 8.89        | 9.04  |
| V   | 0.042     | 0.048 | 1.07        | 1.21  |
| W   | 0.042     | 0.048 | 1.07        | 1.21  |
| X   | 0.042     | 0.056 | 1.07        | 1.42  |
| Y   | ---       | 0.020 | ---         | 0.50  |
| Z   | 2 °       | 10 °  | 2 °         | 10 °  |
| G1  | 0.310     | 0.330 | 7.88        | 8.38  |
| K1  | 0.040     | ---   | 1.02        | ---   |

# MC10135

## PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.750     | 0.785 | 19.05       | 19.93 |
| B   | 0.240     | 0.295 | 6.10        | 7.49  |
| C   | ---       | 0.200 | ---         | 5.08  |
| D   | 0.015     | 0.020 | 0.39        | 0.50  |
| E   | 0.050 BSC |       | 1.27 BSC    |       |
| F   | 0.055     | 0.065 | 1.40        | 1.65  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.125     | 0.170 | 3.18        | 4.31  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 15°   | 0°          | 15°   |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

**Notes**

**ARCHIVE**  
DEVICE NOT RECOMMENDED FOR NEW DESIGN

**Notes**

**ARCHIVE**  
DEVICE NOT RECOMMENDED FOR NEW DESIGN

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