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Hitachi 4-Bit Single-Chip Microcomputers

HMCS43XX Family

HD404344R Series, HD404394 Series, HD404318 Series, HD404358 Series, HD404358R Series, HD404339 Series, HD404369 Series

Hardware Manual

ADE-602-081B
Rev.3.0
3/5/03
Hitachi, Ltd.

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List of Items Revised or Added for This Version

Page	Item	Description
—	Timer Function Overview	Prescaler W column amended
405	18.2.1 Timer Mode Register B1 (TMB1:$009)	Note amended
418	18.4 Interrupts	Series name amended
560	Table 25-21 Absolute Maximum Ratings (HD404358 and HD404358R Series)	Pin voltage HD404358 Series Rated Value amended
566	Table 25-25 AC Characteristics (HD404358 and HD404358R Series)	Oscillator stabilization period (crystal oscillator) Notes added
633	B.2 I/O Registers (2) $030—Data Control Register R0 DCR0	Series name amended
636	B.2 I/O Registers (2) $038—Data Control Register R8 DCR8	Series name amended

Preface

Introduction

The HMCS43XX Family of 4-bit microcomputers are built around the HMCS400 CPU core, which has a powerful architecture designed for efficient programming. All of these microcomputers include standard on-chip peripheral functions, including a multiple input channel A/D converter, a serial interface, and multi-function timers.

The peripheral functions are developed individually as modules, and connected using a standard interface.

This manual describes six product series in the HMCS43XX Family: the HD404344R, HD404394, HD404318, HD404358, HD404358R, HD404339, and HD404369 series. The products in these series form a fine-grained product line in which products are differentiated by their memory capacities, medium and high voltage pins, high current pins, low power modes, normal vs. high-speed versions, and other aspects. This allows an appropriate microcomputer to be selected for a wide range of applications.

All members of the HMCS43XX Family are available in both ROM and PROM (ZTAT™) versions. PROM versions can be programmed freely by the user with a general purpose PROM writer.

Note: ZTAT™ is a registered trademark of Hitachi, Ltd.

Manual Layout

The microcomputers in the HMCS43XX family differ in their memory capacities and peripheral functions. This table provides an overview of the differences between these products as they relate to the structure of this manual. Use this table to determine which sections are relevant to the product(s) of interest.

Organization		HD404344R Series	HD404394 Series	HD404318 Series	HD404358/ HD404358R Series	HD404339 Series	HD404369 Series
Section 1: Overview	Provides a brief overview of the features of the HMCS43XX Family.	●	●	●	●	●	●
Section 2: Memory	These sections describe the HMCS400 CPU and its internal states.	●	●	●	●	●	●
Section 3: CPU		●	●	●	●	●	●
Section 4: Exception Handling		●	●	●	●	●	●
Section 5: Low Power Modes		●	●	●	●	—	—
Section 6: Low Power Modes		—	—	—	—	●	●
Section 7: I/O Ports	These sections describe the peripheral functions used in the HMCS43XX Family. Note that the peripheral functions actually present differ between product series.	●	●	●	●	●	●
Section 8: I/O Ports		—	●	—	—	—	—
Section 9: I/O Ports		—	—	●	—	—	—
Section 10: I/O Ports		—	—	—	●	—	—
Section 11: I/O Ports		—	—	—	—	●	—
Section 12: I/O Ports		—	—	—	—	—	●
Section 13: Oscillator Circuits		●	●	●	●	—	—
Section 14: Oscillator Circuits		—	—	—	—	●	●
Section 15: A/D converter		●	●	●	●	●	●
Section 16: Prescaler		●	●	●	●	●	●
Section 17: Timer A		—	—	●	●	●	●
Section 18: Timer B		●	●	●	●	●	●
Section 19: Timer C		●	●	●	●	●	●
Section 20: Serial Interface		●	●	●	●	●	●
Section 21: Alarm Output		—	—	●	●	●	●
Section 22: ROM		●	●	●	●	●	●
Section 23: RAM		●	●	●	●	●	●

Organization		HD404344R Series	HD404394 Series	HD404318 Series	HD404358/ HD404358R Series	HD404339 Series	HD404369 Series
Section 24: Application Examples	Describes the use of the A/D converter and timer B. Refer to this section when developing software for any of these products.	●	●	●	●	●	●
Section 25: Electrical Characteristics		●	●	●	●	●	●
Appendices		●	●	●	●	●	●

Note on How to Use this Manual

Either <series name(s)> or <All Products> is printed at the top of each page in this manual to indicate that the page refers to one or more specific series or to all products, respectively. Since the peripheral functions actually present differ between products, care is required when reading this manual. Differences between products are specified in notes and by shading.

This manual describes seven product series, the HD404344R, HD404394, HD404318, HD404358, HD404358R, HD404339, and HD404369 series. To use this manual as the manual for a particular product be sure to read both the chapters that pertain to all products as well as the chapters that are related to the product being used.

Function Overview

Item		HD404344R Series	HD404394 Series	HD404318 Series	HD404358 Series	HD404358R Series	HD404339 Series	HD404369 Series
ROM	Capacity (words)	Mask ROM 1/2/4 k ZTAT™ 4 k	Mask ROM 1/2/4 k ZTAT™ 4 k	Mask ROM 4/6/8 k ZTAT™ 8 k	Mask ROM 4/6/8 k ZTAT™ 16 k	Mask ROM 4/6/8 k ZTAT™ 16 k	Mask ROM 4/6/8/12/16 k ZTAT™ 16 k	Mask ROM 4/8/12/16 k ZTAT™ 16 k
RAM	Capacity (digits)	256	256	384	384 (Mask ROM)/ 512 (ZTAT™)	512	512	512
I/O	Pins	22	21	34	34	34	54	54
	Medium voltage pins	—	3	—	4	—	—	8
	High voltage pins	—	—	22 (of which one is input-only)	—	—	31 (of which one is input-only)	—
		10	—	—	—	20	—	—
Interrupts	Priority High	$\overline{INT}_0$	$\overline{INT}_0$	$\overline{INT}_0$	$\overline{INT}_0$	$\overline{INT}_0$	$\overline{INT}_0$	$\overline{INT}_0$
		—	—	$\overline{INT}_1$	$\overline{INT}_1$	$\overline{INT}_1$	$\overline{INT}_1$	$\overline{INT}_1$
		—	—	Timer A	Timer A	Timer A	Timer A	Timer A
		Timer B	Timer B	Timer B	Timer B	Timer B	Timer B	Timer B
		Timer C	Timer C	Timer C	Timer C	Timer C	Timer C	Timer C
		A/D	A/D	A/D	A/D	A/D	A/D	A/D
	Low	Serial	Serial	Serial	Serial	Serial	Serial	Serial
Serial interface	Pins	1	1	1	1	1	1	1
	Clock selection	Prescaler output divided by 2 or 4	Prescaler output divided by 2 or 4	Prescaler output divided by 2 or 4	Prescaler output divided by 2 or 4	Prescaler output divided by 2 or 4	Prescaler output divided by 2 or 4	Prescaler output divided by 2 or 4
	Idle control	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Start instruction	STS instruction	STS instruction	STS instruction	STS instruction	STS instruction	STS instruction	STS instruction
A/D converter	Channels	4	3	8	8	8	12	12
	I_{AD} off	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	V_{ref} pin	—	Built-in	—	—	—	—	—

Note: * Under development

Item		HD404344R Series	HD404394 Series	HD404318 Series	HD404358 Series	HD404358R Series	HD404339 Series	HD404369 Series
Alarm output		—	—	On-chip	On-chip	On-chip	On-chip	On-chip
System clock oscillator	Oscillator	Ceramic, external, CR	Ceramic, external	Crystal, ceramic, external	Crystal, ceramic, external	Crystal, ceramic, CR, external	Crystal, ceramic, external	Crystal, ceramic, external
	Frequency	0.4 to 4.5 MHz 1.0 to 3.5 MHz (CR versions)	0.4 to 4.5 MHz	0.4 to 4.5 MHz	0.4 to 5.0 MHz (5 MHz versions) 0.4 to 8.5 MHz (8.5 MHz versions)	0.4 to 5.0 MHz (5 MHz versions) 0.4 to 8.5 MHz (8.5 MHz versions) 1.0 to 3.5 MHz (CR versions)	0.4 to 4.5 MHz	0.4 to 5.0 MHz (5 MHz versions) 0.4 to 8.5 MHz (8.5 MHz versions)
	Divisor	4	4	4	4	4	4/8/16/32 (software selectable)	4/8/16/32 (software selectable)
Sub-system clock oscillator	Frequency	—	—	—	—	—	32 kHz	32 kHz
	Divisor	—	—	—	—	—	4/8 (software selectable)	4/8 (software selectable)
	Stopping in stop mode	—	—	—	—	—	Yes	Yes
Low power modes	Watch mode	—	—	—	—	—	Yes	Yes
	Subactive mode	—	—	—	—	—	Yes	Yes
	Standby mode	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Stop mode	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Direct return to active mode from subactive mode		—	—	—	—	—	Yes	Yes

Timer Function Overview

Item		HD404344R/ HD404394 Series		HD404318/ HD404358/ HD404358R Series			HD404339/ HD404369 Series		
		B	C	A	B	C	A	B	C
Timer	Prescaler S	◯	◯	◯	◯	◯	◯	◯	◯
	Prescaler W	—	—	—	—	—	◯	—	—
	External event input (falling edge, rising edge, or double edge)	◯	—	—	◯	—	—	◯	—
	Free-running timer	◯	◯	◯	◯	◯	◯	◯	◯
	Time base	—	—	—	—	—	◯	—	—
	Event counter	◯	—	—	◯	—	—	◯	—
	Reload	◯	◯	—	◯	◯	—	◯	◯
	Watchdog	—	◯	—	—	◯	—	—	◯
	PWM	—	◯	—	—	◯	—	—	◯
	Input capture	—	—	—	◯	—	—	◯	—

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1.1 Overview

The products in the HMCS43XX Family are 4-bit microcomputers that include an on-chip A/D converter with multiple input channels. The HMCS43XX Family encompasses an extensive product line of microcomputers that include an on-chip A/D converter in packages with from 28 to 64 pins. Figure 1-1 shows the structure of the HMCS43XX Family.

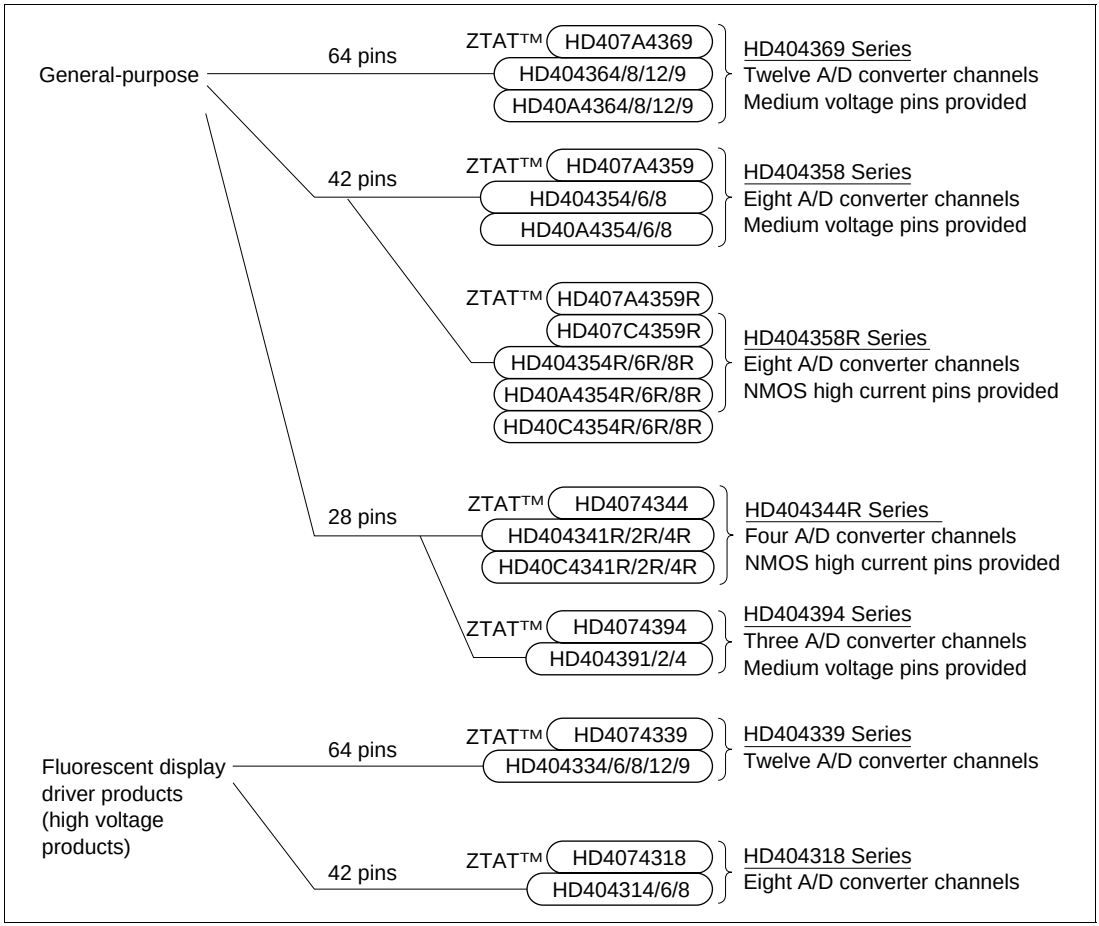


Figure 1-1 Structure of the HMCS43XX Family

Table 1-1 lists HMCS43XX Family product line, and table 1-2 lists the functions of those products.

Table 1-1 Product Lineup

Series	ROM Type		Product	Model	ROM (Words)	RAM (Digits)	Package
HD404344R Series	Mask ROM	Standard version	HD404341R	HD404341RS	1,024	256	DP-28S
				HD404341RFP			FP-28DA
				HD404341RFT			FP-30D
			HD404342R	HD404342RS	2,048	256	DP-28S
				HD404342RFP			FP-28DA
				HD404342RFT			FP-30D
			HD404344R	HD404344RS	4,096	256	DP-28S
				HD404344RFP			FP-28DA
				HD404344RFT			FP-30D
		CR version	HD40C4341R	HD40C4341RS	1,024	256	DP-28S
				HD40C4341RFP			FP-28DA
				HD40C4341RFT			FP-30D
			HD40C4342R	HD40C4342RS	2,048	256	DP-28S
				HD40C4342RFP			FP-28DA
				HD40C4342RFT			FP-30D
			HD40C4344R	HD40C4344RS	4,096	256	DP-28S
				HD40C4344RFP			FP-28DA
				HD40C4344RFT			FP-30D
	ZTAT™		HD4074344	HD4074344S	4,096	256	DP-28S
				HD4074344FP			FP-28DA
				HD4074344FT			FP-30D
HD404394 Series	Mask ROM		HD404391	HD404391S	1,024	256	DP-28S
				HD404391FP			FP-28DA
				HD404391FT			FP-30D
			HD404392	HD404392S	2,048	256	DP-28S
				HD404392FP			FP-28DA
				HD404392FT			FP-30D

Note: ZTAT™ is a registered trademark of Hitachi, Ltd.

Table 1-1 Product Lineup (cont)

Series	ROM Type		Product	Model	ROM (Words)	RAM (Digits)	Package
HD404394 Series	Mask ROM		HD404394	HD404394S	4,096	256	DP-28S
				HD404394FP			FP-28DA
				HD404394FT			FP-30D
	ZTAT™		HD4074394	HD4074394S	4,096	256	DP-28S
				HD4074394FP			FP-28DA
				HD4074394FT			FP-30D
HD404318 Series	Mask ROM		HD404314	HD404314S	4,096	384	DP-42S
				HD404314H			FP-44A
			HD404316	HD404316S	6,144	384	DP-42S
				HD404316H			FP-44A
			HD404318	HD404318S	8,192	384	DP-42S
				HD404318H			FP-44A
	ZTAT™		HD4074318	HD4074318S	8,192	384	DP-42S
				HD4074318H			FP-44A
HD404358 Series	Mask ROM	5 MHz version	HD404354	HD404354S	4,096	384	DP-42S
				HD404354H			FP-44A
			HD404356	HD404356S	6,144	384	DP-42S
				HD404356H			FP-44A
			HD404358	HD404358S	8,192	384	DP-42S
				HD404358H			FP-44A
		8.5 MHz version	HD40A4354	HD40A4354S	4,096	384	DP-42S
				HD40A4354H			FP-44A
			HD40A4356	HD40A4356S	6,144	384	DP-42S
				HD40A4356H			FP-44A
			HD40A4358	HD40A4358S	8,192	384	DP-42S
				HD40A4358H			FP-44A
	ZTAT™		HD407A4359	HD407A4359S	16,384	512	DP-42S
				HD407A4359H			FP-44A

Note: ZTAT™ is a registered trademark of Hitachi, Ltd

Series	ROM Type		Product	Model	ROM (Words)	RAM (Digits)	Package
HD404358R Series	Mask ROM	5 MHz version	HD404354R	HD404354RS	4,096	512	DP-42S
				HD404354RH			FP-44A
			HD404356R	HD404356RS	6,144	512	DP-42S
				HD404356RH			FP-44A
			HD404358R	HD404358RS	8,192	512	DP-42S
				HD404358RH			FP-44A
		8.5 MHz version	HD40A4354R	HD40A4354RS	4,096	512	DP-42S
				HD40A4354RH			FP-44A
			HD40A4356R	HD40A4356RS	6,144	512	DP-42S
				HD40A4356RH			FP-44A
			HD40A4358R	HD40A4358RS	8,192	512	DP-42S
				HD40A4358RH			FP-44A
		CR version	HD40C4354R	HD40C4354RS	4,096	512	DP-42S
				HD40C4354RH			FP-44A
			HD40C4356R	HD40C4356RS	6,144	512	DP-42S
				HD40C4356RH			FP-44A
			HD40C4358R	HD40C4358RS	8,192	512	DP-42S
				HD40C4358RH			FP-44A
	ZTAT™	8.5 MHz version	HD407A4359R	HD407A4359RS	16,384	512	DP-42S
				HD407A4359RH			FP-44A
		CR version	HD407C4359R	HD407C4359RS	16,384	512	DP-42S
				HD407C4359RH			FP-44A

Note: ZTAT™ is a registered trademark of Hitachi, Ltd.

Table 1-1 Product Lineup (cont)

Series	ROM Type		Product	Model	ROM (Words)	RAM (Digits)	Package
HD404339 Series	Mask ROM		HD404334	HD404334S	4,096	512	DP-64S
				HD404334FS			FP-64B
			HD404336	HD404336S	6,144	512	DP-64S
				HD404336FS			FP-64B
			HD404338	HD404338S	8,192	512	DP-64S
				HD404338FS			FP-64B
			HD4043312	HD4043312S	12,288	512	DP-64S
				HD4043312FS			FP-64B
			HD404339	HD404339S	16,384	512	DP-64S
				HD404339FS			FP-64B
	ZTAT™		HD4074339	HD4074339S	16,384	512	DP-64S
				HD4074339FS			FP-64B
HD404369 Series	Mask ROM	5 MHz version	HD404364	HD404364S	4,096	512	DP-64S
				HD404364F			FP-64B
			HD404368	HD404368S	8,192	512	DP-64S
				HD404368F			FP-64B
			HD4043612	HD4043612S	12,288	512	DP-64S
				HD4043612F			FP-64B
			HD404369	HD404369S	16,384	512	DP-64S
				HD404369F			FP-64B
		8.5 MHz version	HD40A4364	HD40A4364S	4,096	512	DP-64S
				HD40A4364F			FP-64B
			HD40A4368	HD40A4368S	8,192	512	DP-64S
				HD40A4368F			FP-64B
HD404369 Series	Mask ROM	8.5 MHz version	HD40A43612	HD40A43612S	12,288	512	DP-64S
				HD40A43612F			FP-64B
			HD40A4369	HD40A4369S	16,384	512	DP-64S
				HD40A4369F			FP-64B
	ZTAT™		HD407A4369	HD407A4369S	16,384	512	DP-64S
				HD407A4369F			FP-64B

Note: ZTAT™ is a registered trademark of Hitachi, Ltd.

Specifications

Item		HD404344R Series	HD404394 Series	HD404318 Series	HD404358 Series	HD404358R Series	HD404339 Series	HD404369 Series
CPU		• Three RAM addressing modes 1. Register indirect addressing 2. Direct addressing 3. Memory register addressing • Four ROM addressing modes and the P instruction 1. Direct addressing 2. Current addressing 3. Zero page addressing 4. Table data addressing 5. P instruction (ROM data reference instruction) • Simple and efficient instruction set All instructions are executed in one or two cycles, except for the return instruction, which requires three cycles.						
ROM (words: 1 word = 10 bits)	16 k	—	—	—	HD407A4359	HD407A4359R HD407C4359R	HD404339 HD4074339 HD407A4369	HD404369 HD40A4369
	12 k	—	—	—	—	—	HD4043312	HD4043612 HD40A43612
	8 k	—	—	HD404318 HD4074318	HD404358 HD40A4358	HD404358R HD40A4358R HD40C4358R	HD404338	HD404368 HD40A4368
	6 k	—	—	HD404316	HD404356 HD40A4356	HD404356R HD40A4356R HD40C4356R	HD404336	—
	4 k	HD404344R HD40C4344R HD4074344	HD404394 HD4074394	HD404314	HD404354 HD40A4354	HD404354R HD40A4354R HD40C4354R	HD404334	HD404364 HD40A4364
	2 k	HD404342R HD40C4342R	HD404392	—	—	—	—	—
	1 k	HD404341R HD40C4341R	HD404391	—	—	—	—	—

Specifications

Item	HD404344R Series	HD404394 Series	HD404318 Series	HD404358 Series	HD404358R Series	HD404339 Series	HD404369 Series
RAM (digits: 1 digit = 4 bits)	256	256	384	384 (Mask ROM)/ 512 (ZTAT™)	512	512	512
I/O ports	Total: 22 pins • Standard I/O pins: 22 pins (NMOS high current pins: 10 pins)	Total: 21 pins • Standard I/O pins: 13 pins • Medium voltage NMOS open drain I/O pins: 3 pins • Standard voltage NMOS open drain high current I/O pins: 5 pins	Total: 34 pins • Standard I/O pins: 12 pin • High voltage I/O pins: 21 pins • High voltage input pins: 1 pin	Total: 34 pins • Standard I/O pins: 29 pins • Medium voltage I/O pins: 4 pins • Standard input pins: 1 pin	Total: 34 pins • Standard I/O pins: 33 pins (NMOS high current pins: 20 pins) • Standard input pins: 1 pin	Total: 54 pins • Standard I/O pins: 23 pins • High voltage I/O pins: 30 pins • High voltage input pins: 1 pin	Total: 54 pins • Standard I/O pins: 45 pins • Medium voltage I/O pins: 8 pins • Standard input pins: 1 pin
A/D converter	• Resistor ladder successive approximations A/D converter • Resolution: 8 bits • Generates an interrupt at the end of the A/D conversion period						
	Analog inputs: 4 channels	Analog inputs: 3 channels plus V_{ref} pin	Analog inputs: 8 channels			Analog inputs: 12 channels	

Specifications

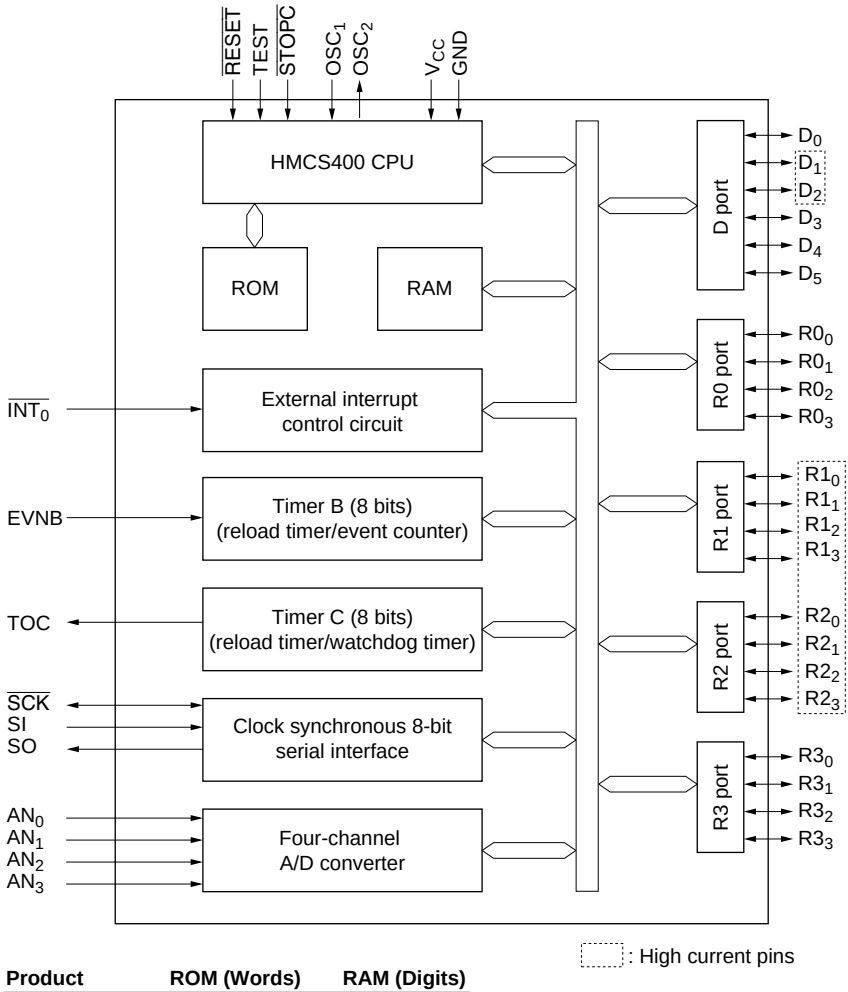
Item	HD404344R Series	HD404394 Series	HD404318 Series	HD404358 Series	HD404358R Series	HD404339 Series	HD404369 Series
Timer A	—	—	• Can be driven by any one of eight internal clocks generated by dividing the system clock. • Generates an interrupt on overflow.			• Can be driven by any one of eight internal clocks generated by dividing the system clock. • Can be driven by any one of five internal clocks generated by dividing the 32.768 kHz oscillator. (clock time base) • Generates an interrupt on overflow.	
Timer B	• Can be driven by any one of seven internal clocks generated by dividing the system clock or by event input. • Event input detection on rising edges, falling edges, or falling/rising edge pairs • Generates an interrupt on overflow.						
	—	—	Also supports input capture operation				
Timer C	• Can be driven by any one of eight internal clocks generated by dividing the system clock. • Supports PWM output. • Can also function as a watchdog timer. • Generates an interrupt on overflow.						
Serial interface	• Single channel 8-bit clock synchronization serial interface • One of 13 internal clocks or an external clock can be used as the transfer clock. • Can control the high/low level output state of the data transmission pin in idle mode. • Generates interrupts on transfer complete and transfer interrupted.						
Alarm output	—	—	• Outputs one of four frequencies generated by dividing the system clock.				
Interrupts	External interrupt pins: 1 pin Internal interrupt sources: 4 sources Interrupt vectors: 5 locations		External interrupt pins: 2 pins Internal interrupt sources: 5 sources Interrupt vectors: 7 locations				
Low power modes	• Standby mode • Stop mode (external stop mode clear input provided)						
	—	—	—	—	—	• Watch mode • Subactive mode	

Table 1-2 HMCS43XX Family Functional Overview (cont)

Item	Specifications						
	HD404344R Series	HD404394 Series	HD404318 Series	HD404358 Series	HD404358R Series	HD404339 Series	HD404369 Series
System clock	0.4 to 4.5 MHz 1.0 to 3.5 MHz	0.4 to 4.5 MHz 1.0 to 3.5 MHz	0.4 to 4.5 MHz	0.4 to 5.0 MHz, 0.4 to 8.5 MHz, 1.0 to 3.5 MHz	0.4 to 5.0 MHz, 0.4 to 8.5 MHz, 1.0 to 3.5 MHz	0.4 to 4.5 MHz	0.4 to 5.0 MHz, 0.4 to 8.5 MHz
Subsystem clock	—	—	—	—	—	32.768 kHz	32.768 kHz

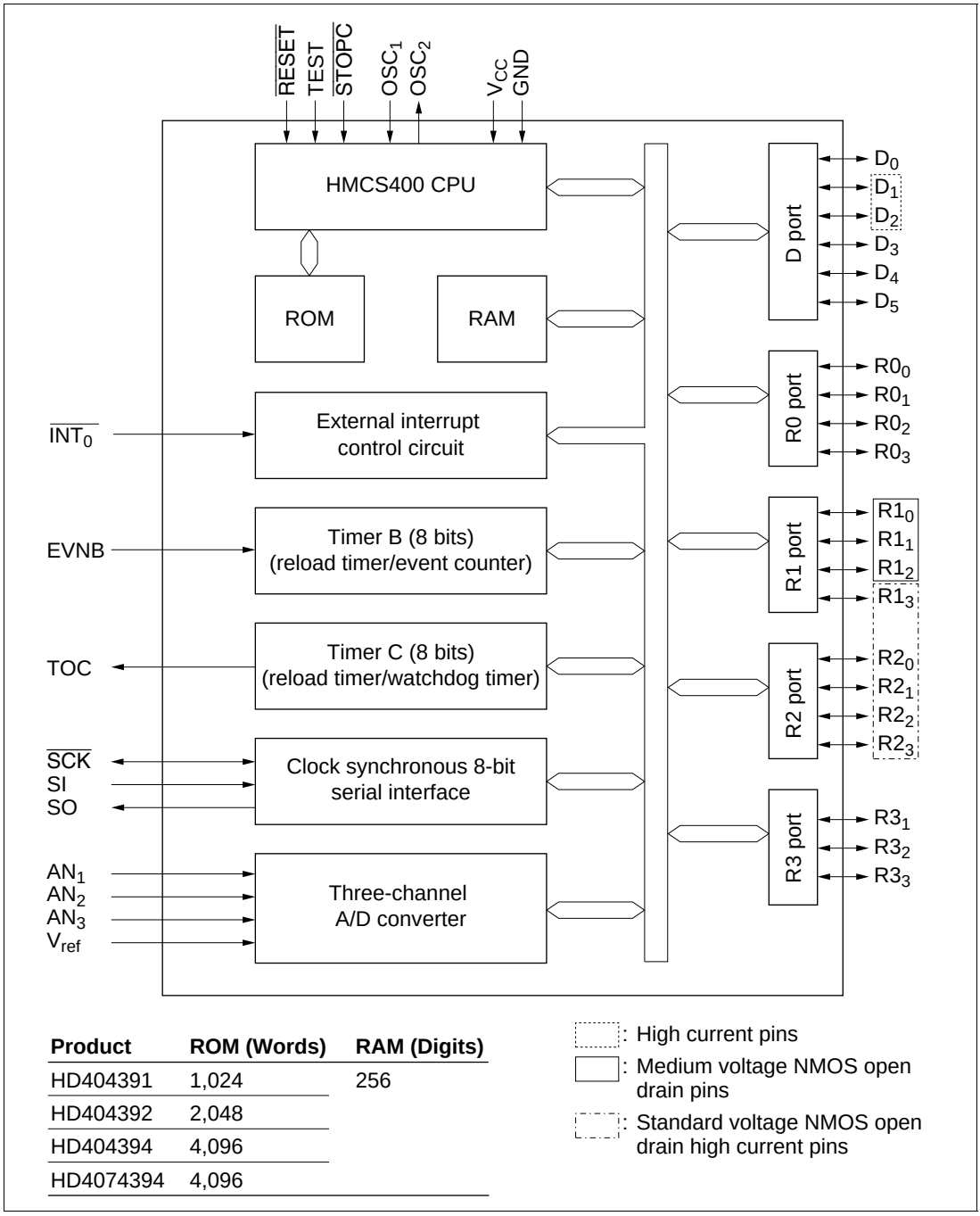
1.2 Internal Block Diagrams

Figures 1-2 to 1-8 show the internal block diagrams for the HD404344R, HD404394, HD404318, HD404358, HD404358R, HD404339, and HD404369 series microcomputers.



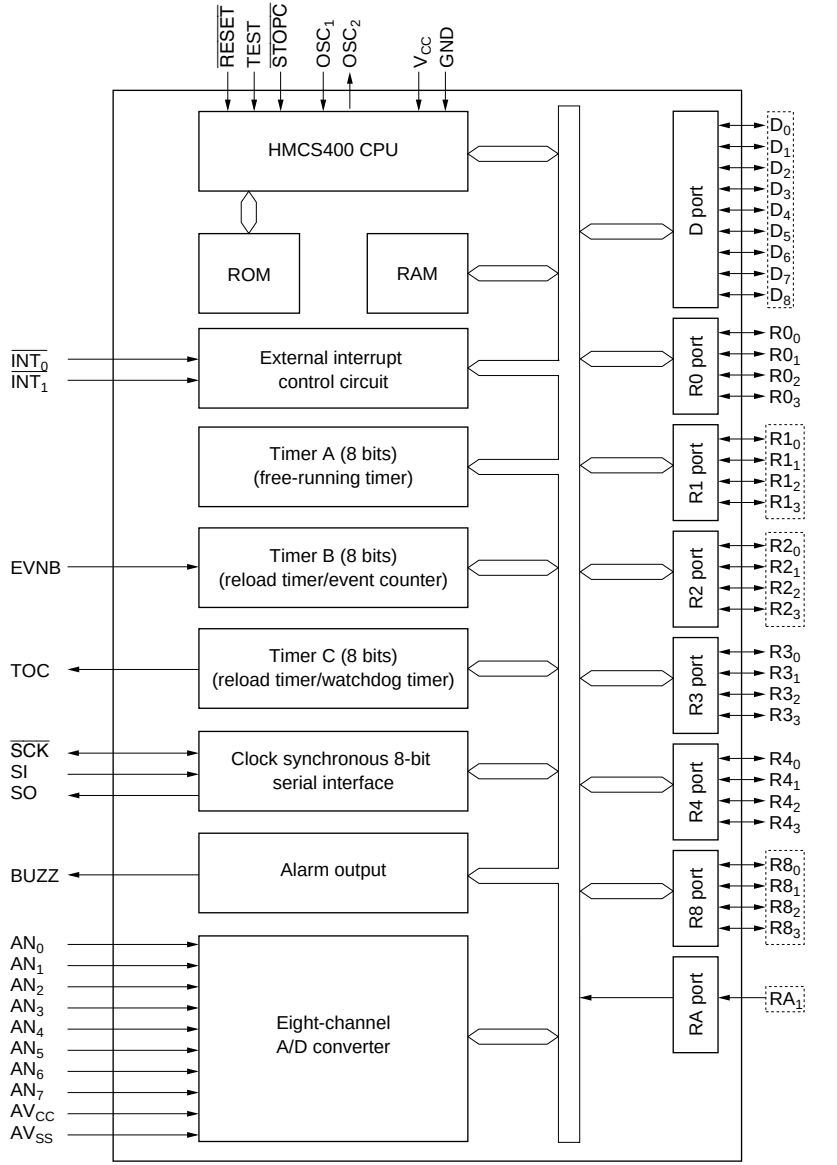
Product	ROM (Words)	RAM (Digits)
HD404341R	1,024	256
HD40C4341R		
HD404342R	2,048	
HD40C4342R		
HD404344R	4,096	
HD40C4344R		
HD4074344	4,096	

Figure 1-2 HD404344R Series Internal Block Diagram



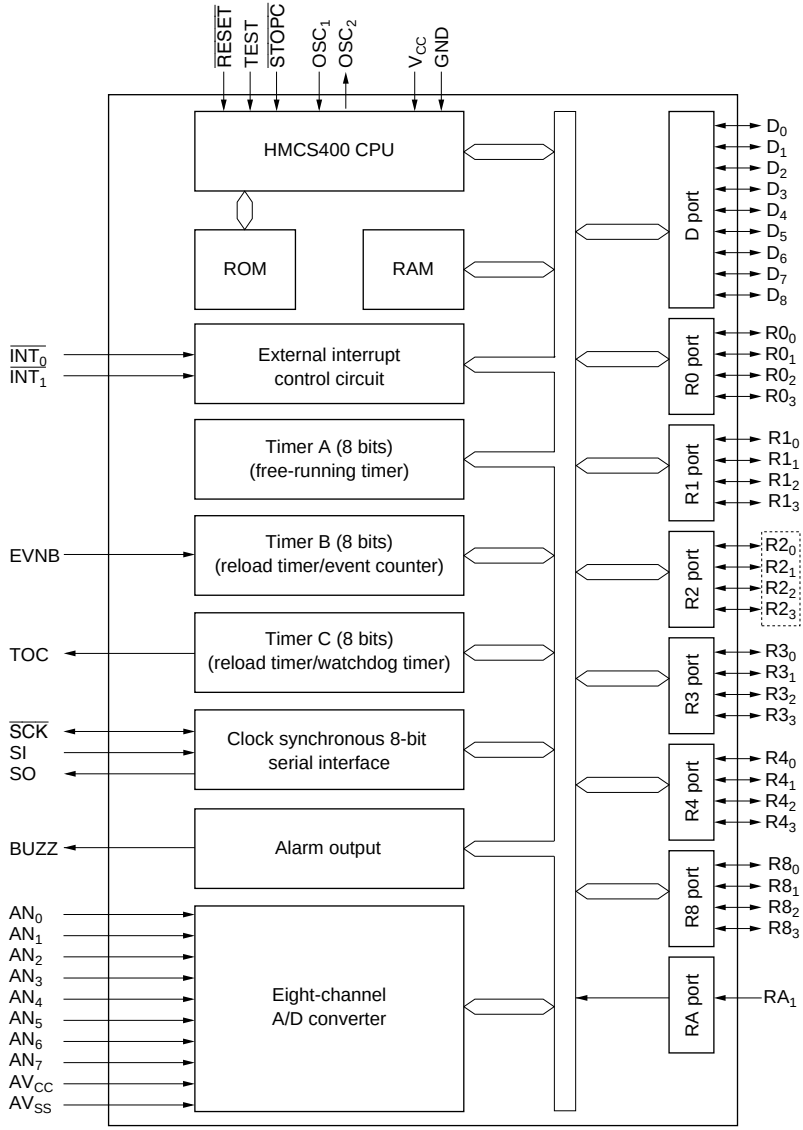
Product	ROM (Words)	RAM (Digits)
HD404391	1,024	256
HD404392	2,048	
HD404394	4,096	
HD4074394	4,096	

Figure 1-3 HD404394 Series Internal Block Diagram



Product	ROM (Words)	RAM (Digits)
HD404314	4,096	384
HD404316	6,144	
HD404318	8,192	
HD4074318	8,192	

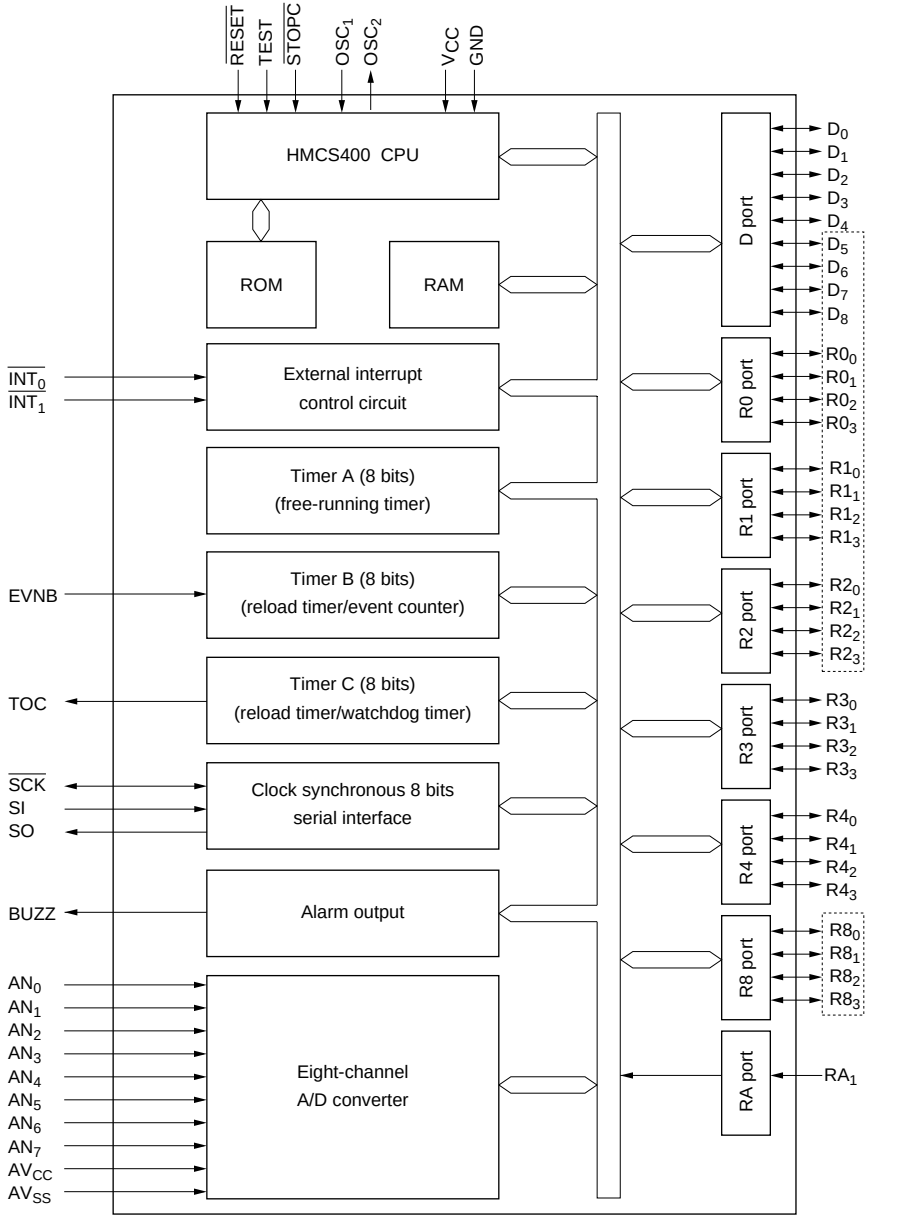
Figure 1-4 HD404318 Series Internal Block Diagram



Product	ROM (Words)	RAM (Digits)
HD404354/HD40A4354	4,096	384
HD404356/HD40A4356	6,144	
HD404358/HD40A4358	8,192	
HD407A4359	16,384	512

: Medium voltage NMOS open drain pins

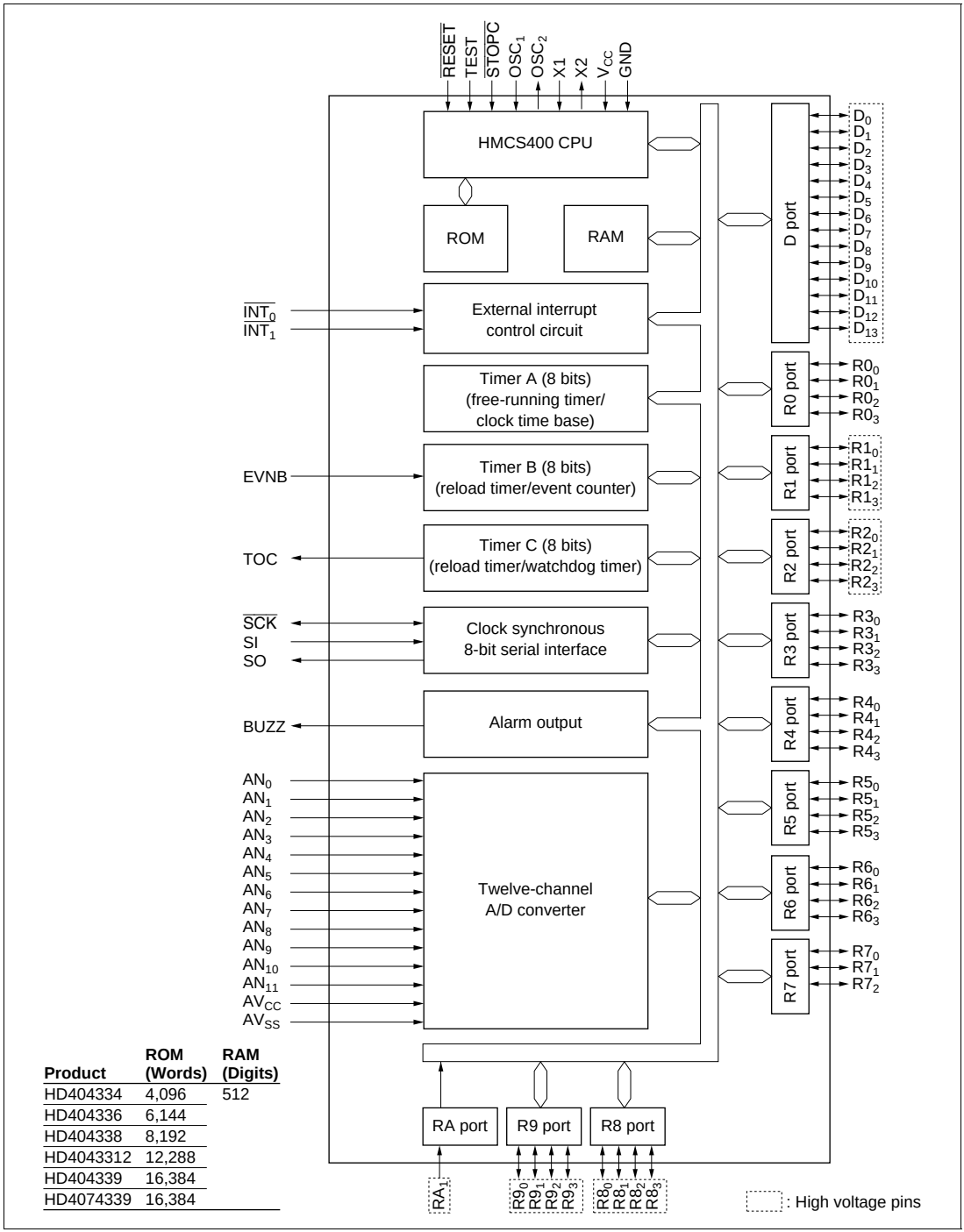
Figure 1-5 HD404358 Series Internal Block Diagram



Product	ROM (Words)	RAM (Digits)
HD404354R/HD40A4354R/HD40C4354R	4,096	512
HD404356R/HD40A4356R/HD40C4356R	6,144	
HD404358R/HD40A4358R/HD40C4358R	8,192	
HD407A4359R/HD407C4359R	16,384	

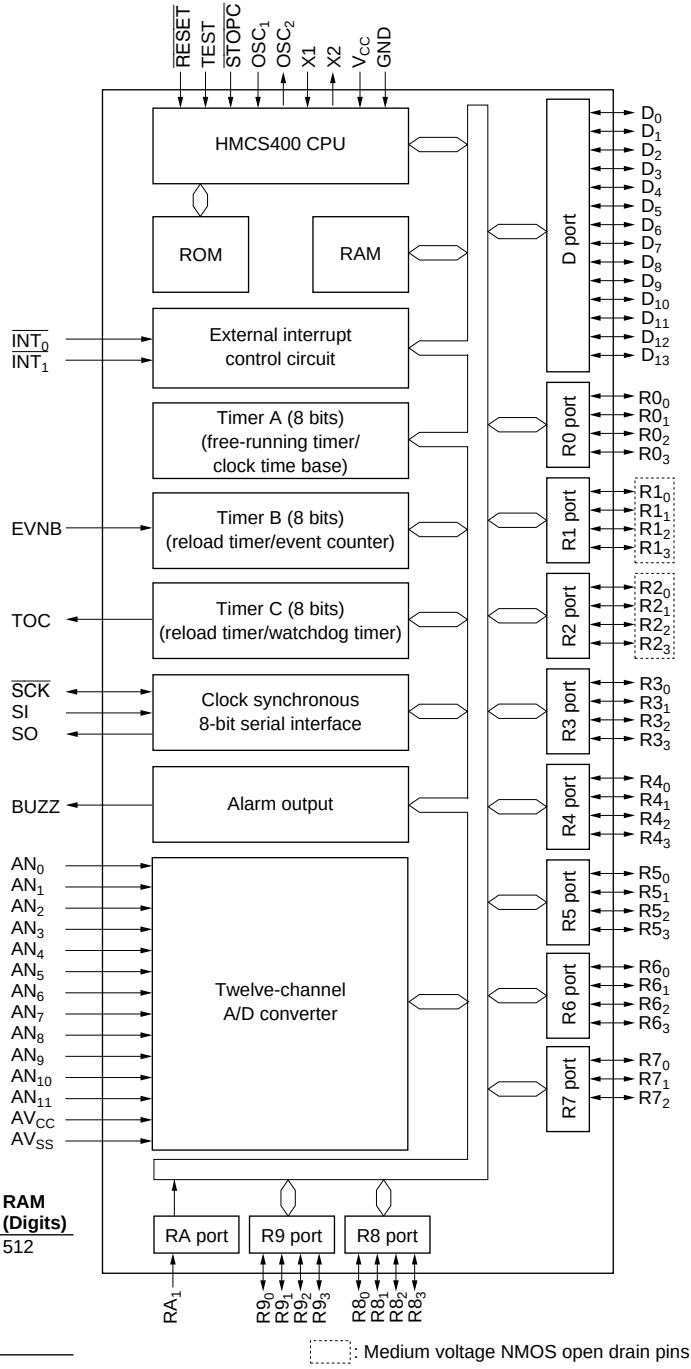
: NMOS high current pins

Figure 1-6 HD404358R Series Internal Block Diagram



Product	ROM (Words)	RAM (Digits)
HD404334	4,096	512
HD404336	6,144	
HD404338	8,192	
HD4043312	12,288	
HD404339	16,384	
HD4074339	16,384	

Figure 1-7 HD404339 Series Internal Block Diagram



Product	ROM (Words)	RAM (Digits)
HD404364/HD40A4364	4,096	512
HD404368/HD40A4368	8,192	
HD4043612/HD40A43612	12,288	
HD404369/HD40A4369	16,384	
HD407A4369	16,384	

Figure 1-8 HD404369 Series Internal Block Diagram

1.3 Pin Functions

1.3.1 HD404344R and HD404394 Series Pin Functions

Figures 1-9 and 1-10 show the pin arrangements for the HD404344R and HD404394 Series products in the DP-28S, FP-28DA, and FP-30D packages.

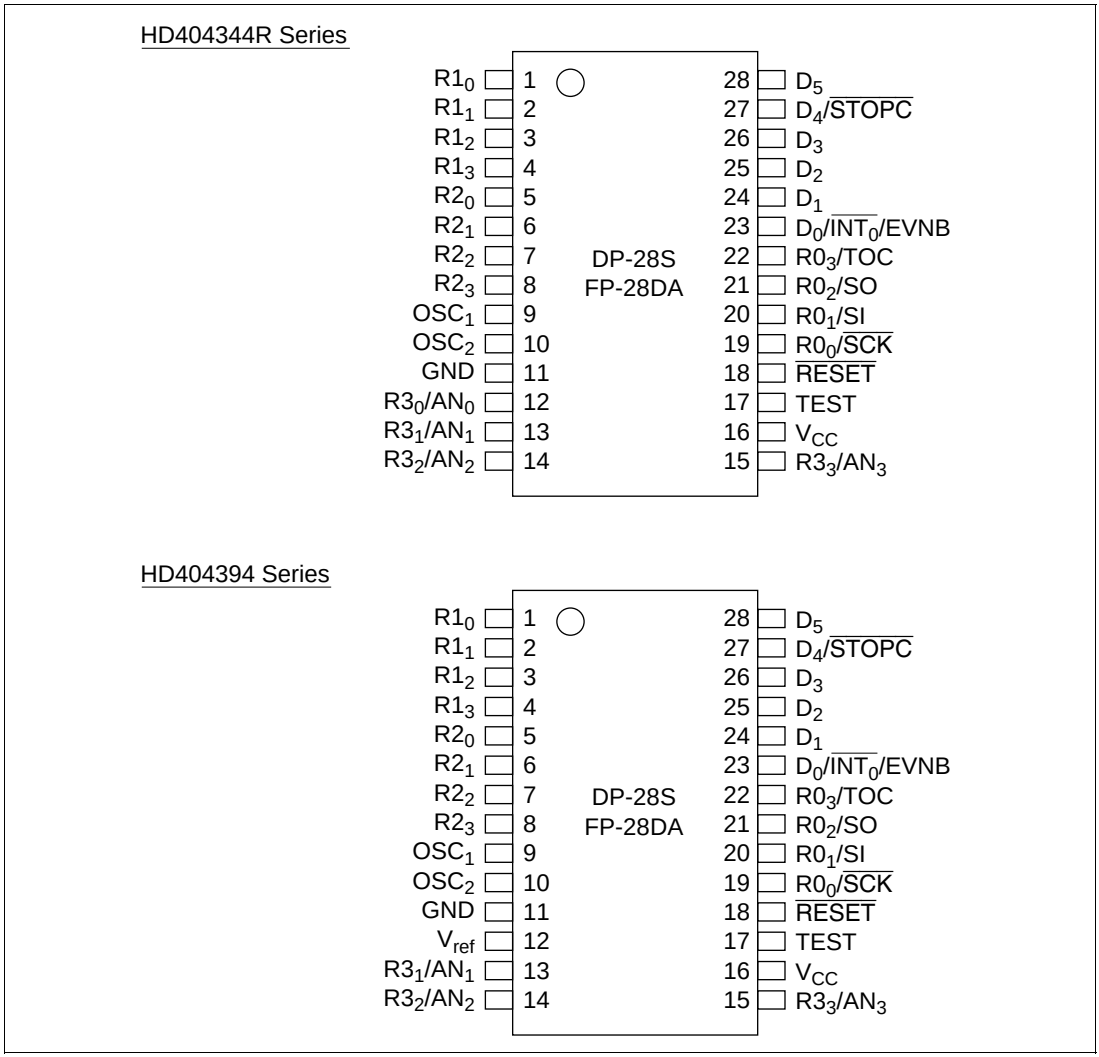
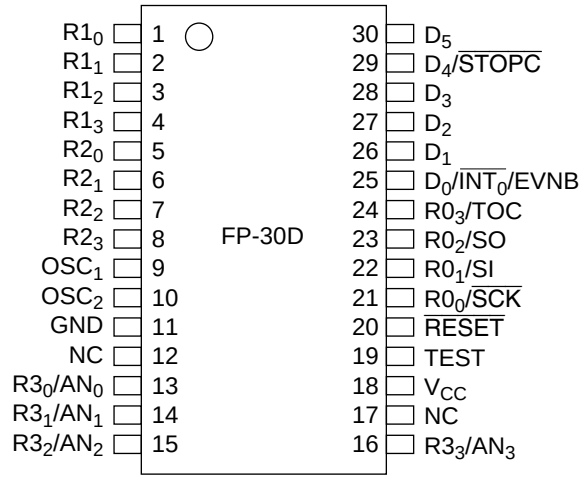


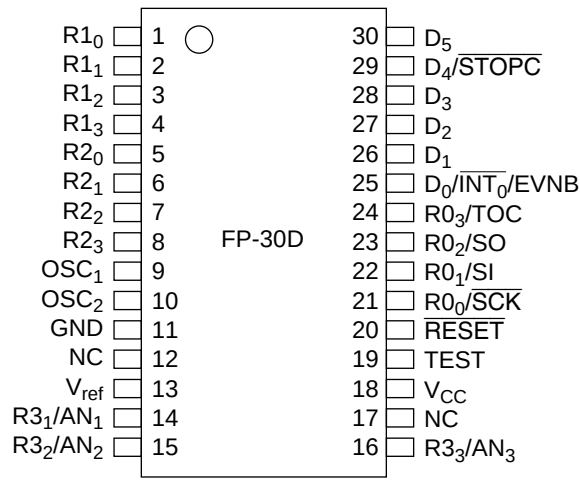
Figure 1-9 HD404344R and HD404394 Series Pin Arrangements (DP-28S and FP-28DA Packages: Top View)

HD404344R Series



Note: No connections should be made to NC pins.

HD404394 Series



Note: No connections should be made to NC pins.

Figure 1-10 HD404344R and HD404394 Series Pin Arrangements (FP-30D Package: Top View)

Table 1-3 lists the pin assignments for the HD404344R and HD404394 Series microcomputers.

Table 1-3 HD404344R and HD404394 Series Pin Assignments

Pin No.			Pin Function	
DP-28S, FP-28DA	FP-30D	Pin	HD404344R Series	HD404394 Series
1	1	$R1_0$	Standard voltage high current I/O port	Medium voltage I/O port
2	2	$R1_1$	Standard voltage high current I/O port	Medium voltage I/O port
3	3	$R1_2$	Standard voltage high current I/O port	Medium voltage I/O port
4	4	$R1_3$	Standard voltage high current I/O port	Standard voltage high current I/O port
5	5	$R2_0$	Standard voltage high current I/O port	Standard voltage high current I/O port
6	6	$R2_1$	Standard voltage high current I/O port	Standard voltage high current I/O port
7	7	$R2_2$	Standard voltage high current I/O port	Standard voltage high current I/O port
8	8	$R2_3$	Standard voltage high current I/O port	Standard voltage high current I/O port
9	9	OSC_1	System clock oscillator connection: input	
10	10	OSC_2	System clock oscillator connection: output	
11	11	GND	Ground	
12	13	$R3_0/AN_0$ (V_{ref})*	Standard voltage I/O port/ analog input channel	Analog reference voltage
13	14	$R3_1/AN_1$	Standard voltage I/O port/analog input channel	
14	15	$R3_2/AN_2$	Standard voltage I/O port/analog input channel	
15	16	$R3_3/AN_3$	Standard voltage I/O port/analog input channel	
16	18	V_{CC}	Power supply	
17	19	TEST	Test	
18	20	$\overline{RESET}$	Reset	
19	21	$R0_0/\overline{SCK}$	Standard voltage I/O port/serial transfer clock I/O	
20	22	$R0_1$/SI	Standard voltage I/O port/serial reception data input	

Note: * Items without parentheses apply to the HD404344R Series and items in parentheses apply to the HD404394 Series.

Table 1-3 HD404344R and HD404394 Series Pin Assignments (cont)

Pin No.			Pin Function	
DP-28S, FP-28DA	FP-30D	Pin	HD404344R Series	HD404394 Series
21	23	$R0_2$/SO	Standard voltage I/O port/serial transmission data output	
22	24	$R0_3$/TOC	Standard voltage I/O port/timer C output	
23	25	D_0/$\overline{INT}_0$/ EVNB	Standard voltage I/O port/external interrupt input/timer B event input	
24	26	D_1	Standard voltage high current I/O port	
25	27	D_2	Standard voltage high current I/O port	
26	28	D_3	Standard voltage I/O port	
27	29	D_4/$\overline{STOPC}$	Standard voltage I/O port/stop mode clear	
28	30	D_5	Standard voltage I/O port	
—	12	NC	—	—
—	17	NC	—	—

Note: No connections should be made to NC pins.

Table 1-4 lists the pin functions for the HD404344R and HD404394 Series microcomputers.

Table 1-4 HD404344R and HD404394 Series Pin Functions

Type	Symbol	I/O	Function
Power supply	V_{CC}	—	**Power supply:** Connect to the system power supply.
	GND	—	**Ground:** Connect to the system ground
	V_{ref}	—	**Analog reference voltage (HD404394 Series):** Connection for the A/D converter internal resistor ladder power supply.
Clock	OSC_1	Input	**System clock oscillator connection 1:** Connect a ceramic oscillator or an oscillator circuit to this pin. Alternately, for CR oscillation a resistor should be connected. Use an oscillator with a clock frequency between 400 kHz and 4.5 MHz. See section 13, “Oscillator Circuits,” for examples of the circuits used when connecting a ceramic oscillator or resistor, or when using an external clock input.
	OSC_2	Output	**System clock oscillator connection 2:** Connect a ceramic oscillator to this pin. Use an oscillator with a frequency of between 400 kHz and 4.5 MHz. Alternately, for CR oscillation a resistor should be connected. Leave this pin open if an external clock is input to the OSC_1 pin.
Port	D_0 to D_5	I/O	**D port:** I/O pins (CMOS three state) that can be accessed in 1-bit units. Pins D_1 and D_2 are high current pins that can accept influx currents of up to 15 mA.
	$R0_0$ to $R0_3$	I/O	**R0 port:** Standard I/O pins (CMOS three state) that can be accessed as a 4-bit unit.
	$R1_0$ to $R1_3$	I/O	**R1 port (HD404344R Series):** I/O pins (CMOS three state) that can be accessed as a 4-bit unit. Pins $R1_0$ to $R1_3$ are high current pins that can accept influx currents of up to 15 mA. **R1 port (HD404394 Series):** I/O pins that can be accessed as a 4-bit unit. Pins $R1_0$ to $R1_2$ are medium voltage I/O pins (NMOS open drain). Also, pin $R1_3$ is a standard voltage high current pin that can accept influx currents of up to 15 mA.

Table 1-4 HD404344R and HD404394 Series Pin Functions (cont)

Type	Symbol	I/O	Function
Port	$R2_0$ to $R2_3$	I/O	**R2 port (HD404344R Series):** I/O pins (CMOS three state) that can be accessed as a 4-bit unit. Pins $R2_0$ to $R2_3$ are high current pins that can accept influx currents of up to 15 mA.
			R2 port (HD404394 Series): I/O pins (NMOS open drain) that can be accessed as a 4-bit unit. Pins $R2_0$ to $R2_3$ are high current pins that can accept influx currents of up to 15 mA.
	$R3_0$ to $R3_3$, ($R3_1$ to $R3_3$)*	I/O	**R3 port:** Standard I/O pins (CMOS three state) that can be accessed as a 4-bit (3-bit)* unit.
System control	TEST	Input	**Test:** Connect to ground.
	$\overline{\text{RESET}}$	Input	**Reset:** The microcomputer goes to the reset state when a low level is applied to this pin.
	$\overline{\text{STOPC}}$	Input	**Stop mode clear:** Input pin for clearing stop mode. The microcomputer switches from stop mode to active mode when a low level is applied to this pin.
Interrupt	$\overline{\text{INT}_0}$	Input	**External interrupt input 0:** Falling edge detection external interrupt input.
8-bit timers	TOC	Output	**Timer C output:** The timer C output. Generates a PWM output signal.
	EVNB	Input	**Timer B event input:** The timer B event input. External events can be counted on falling edges, rising edges, or falling/rising edge pairs in this input.
Serial interface	$\overline{\text{SCK}}$	I/O	**Serial transfer clock I/O:** I/O pin for the serial interface clock.
	SI	Input	**Serial reception data input:** Data input pin for the serial interface.
	SO	Output	**Serial transmission output:** Data output pin for the serial interface.
A/D converter	AN_0 to AN_3 (AN_1 to AN_3)*	Input	**Analog input channels 0 to 3 (HD404344R Series):** Analog input channels for the A/D converter.
			Analog input channels 1 to 3 (HD404394 Series): Analog input channels for the A/D converter.

Note: * Items without parentheses apply to the HD404344R Series and items in parentheses apply to the HD404394 Series.

1.3.2 HD404318/HD404358/HD404358R Series Pin Functions

Figures 1-11 and 1-12 show the pin arrangements for the HD404318, HD404358 and HD404358R Series products in the DP-42S and FP-44A packages.

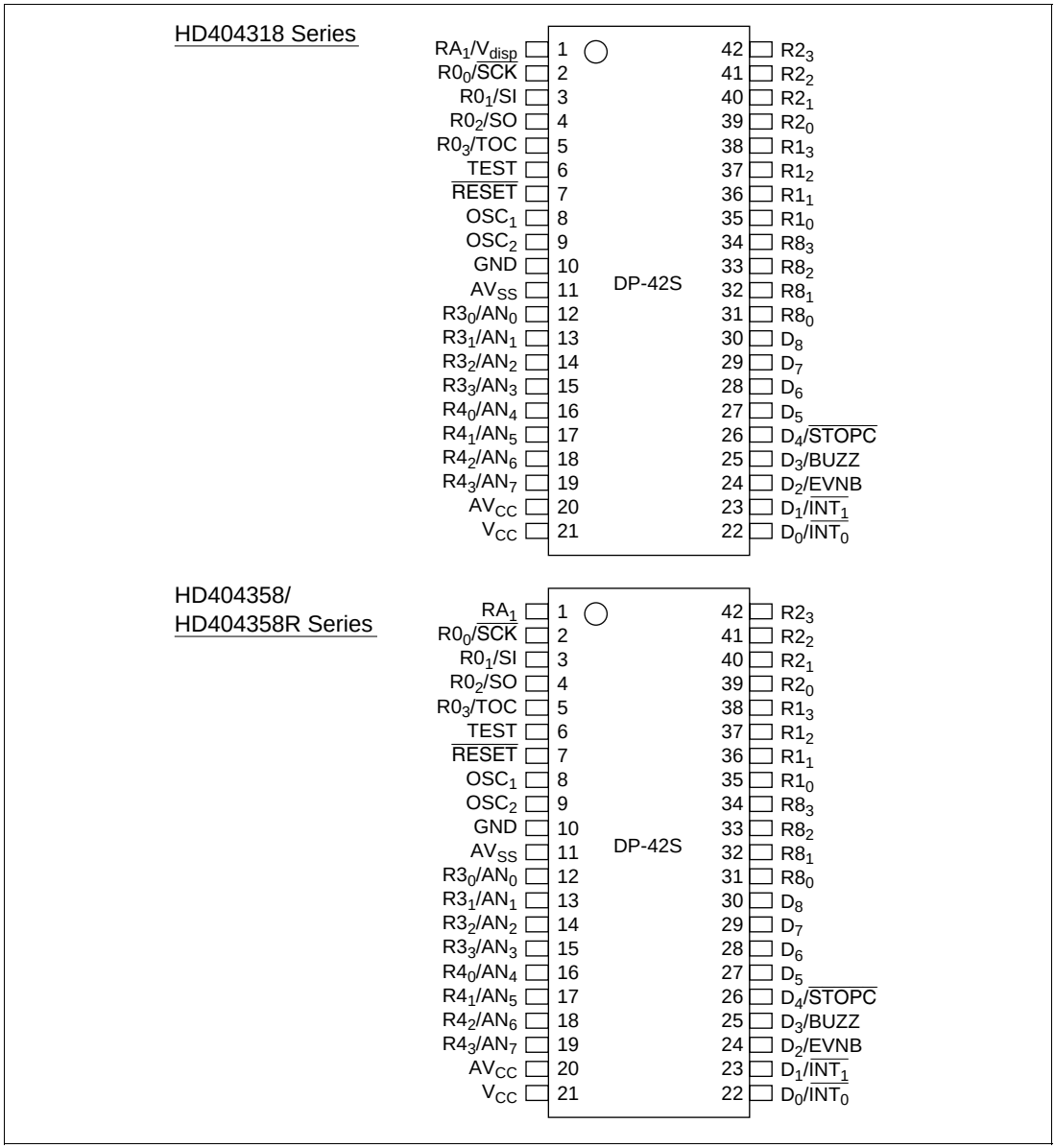


Figure 1-11 HD404318, HD404358 and HD404358R Series Pin Arrangements (DP-42S Package: Top View)

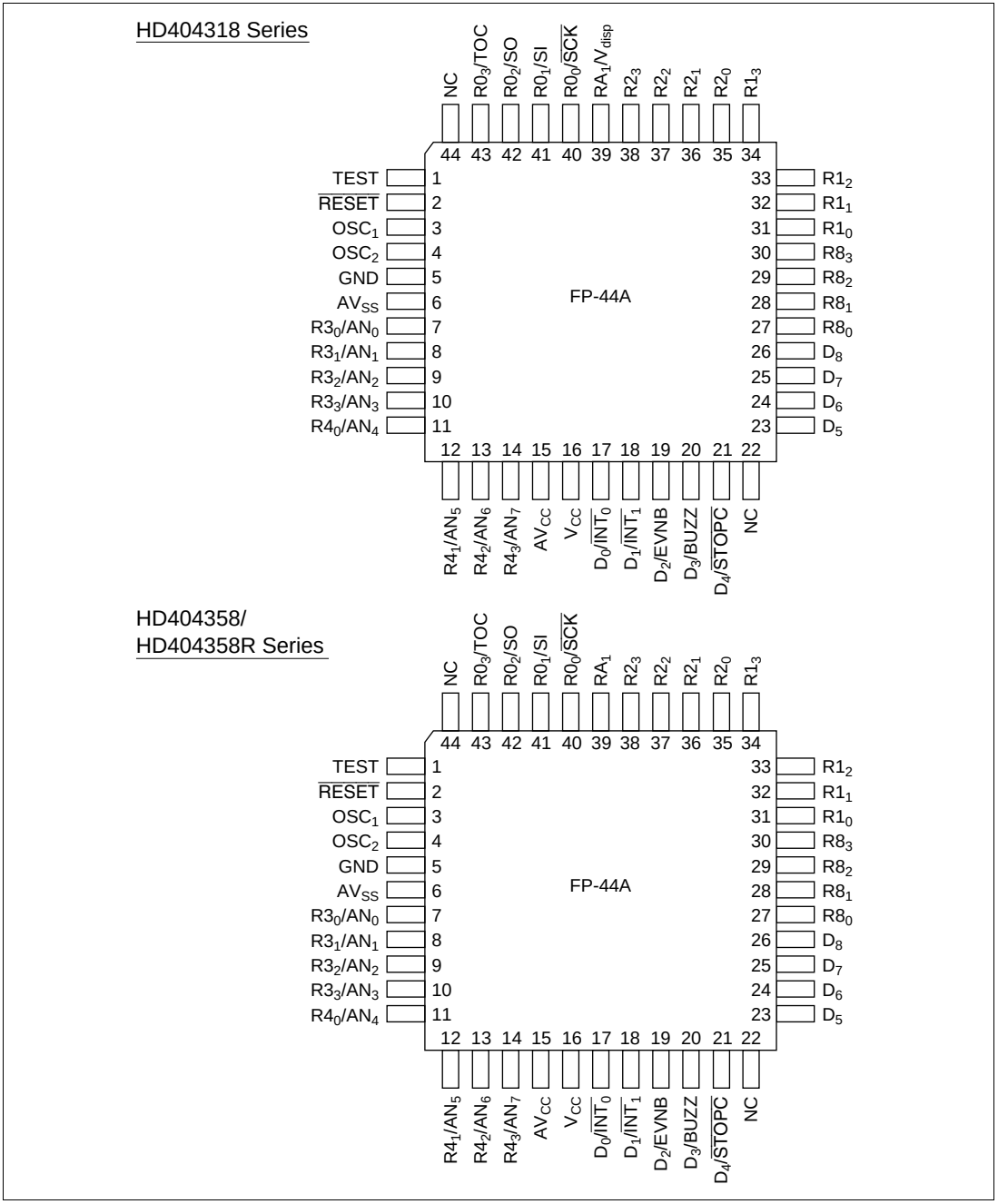


Figure 1-12 HD404318, HD404358 and HD404358R Series Pin Arrangements (FP-44A Package: Top View)

Table 1-5 lists the pin assignments for the HD404318, HD404358 and HD404358R Series microcomputers.

Table 1-5 HD404318, HD404358 and HD404358R Series Pin Assignments

Pin No.			Pin Function		
DP-42S	**FP-44A**	**Pin**	**HD404318 Series**	**HD404358 Series**	**HD404358R Series**
1	39	RA_1/(V_{disp})*	High voltage input port/high voltage pin output power supply	Standard voltage input port	
2	40	$R0_0/\overline{SCK}$	Standard voltage I/O port/serial transfer clock I/O		Standard voltage high current I/O port/serial transfer clock I/O
3	41	$R0_1$/SI	Standard voltage I/O port/serial reception data input		Standard voltage high current I/O port/serial reception data input
4	42	$R0_2$/SO	Standard voltage I/O port/serial transmission data output		Standard voltage high current I/O port/ serial transmission data output
5	43	$R0_3$/TOC	Standard voltage I/O port/timer C output		Standard voltage high current I/O port/ timer C output
6	1	TEST	Test		
7	2	$\overline{RESET}$	Reset		
8	3	OSC_1	System clock oscillator connection: input		
9	4	OSC_2	System clock oscillator connection: output		
10	5	GND	Ground		
11	6	AV_{SS}	Analog ground		
12	7	$R3_0/AN_0$	Standard voltage I/O port/analog input channel		
13	8	$R3_1/AN_1$	Standard voltage I/O port/analog input channel		
14	9	$R3_2/AN_2$	Standard voltage I/O port/analog input channel		
15	10	$R3_3/AN_3$	Standard voltage I/O port/analog input channel		
16	11	$R4_0/AN_4$	Standard voltage I/O port/analog input channel		
17	12	$R4_1/AN_5$	Standard voltage I/O port/analog input channel		
18	13	$R4_2/AN_6$	Standard voltage I/O port/analog input channel		
19	14	$R4_3/AN_7$	Standard voltage I/O port/analog input channel		
20	15	AV_{CC}	Analog power supply		

Note: * Items in parentheses apply only to the HD404318 Series.

Table 1-5 HD404318, HD404358 and HD404358R Series Pin Assignments (cont)

Pin No.			Pin Function		
DP-42S	FP-44A	Pin	HD404318 Series	HD404358 Series	HD404358R Series
21	16	V_{CC}	Power supply		
22	17	D_0/$\overline{INT}_0$	High voltage I/O port/ external interrupt input	Standard voltage I/O port/external interrupt input	
23	18	D_1/$\overline{INT}_1$	High voltage I/O port/ external interrupt input	Standard voltage I/O port/external interrupt input	
24	19	D_2/EVNB	High voltage I/O port/ timer B event input	Standard voltage I/O port/timer B event input	
25	20	D_3/BUZZ	High voltage I/O port/ alarm output	Standard voltage I/O port/alarm output	
26	21	D_4/ $\overline{STOPC}$	High voltage I/O port/ stop mode clear	Standard voltage I/O port/stop mode clear	
27	23	D_5	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
28	24	D_6	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
29	25	D_7	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
30	26	D_8	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
31	27	$R8_0$	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
32	28	$R8_1$	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
33	29	$R8_2$	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
34	30	$R8_3$	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
35	31	$R1_0$	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
36	32	$R1_1$	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
37	33	$R1_2$	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port
38	34	$R1_3$	High voltage I/O port	Standard voltage I/O port	Standard voltage high current I/O port

Note: No connections should be made to NC pins.

Table 1-5 HD404318, HD404358 and HD404358R Series Pin Assignments (cont)

Pin No.			Pin Function		
DP-42S	**FP-44A**	**Pin**	**HD404318 Series**	**HD404358 Series**	**HD404358R Series**
39	35	$R2_0$	High voltage I/O port	Medium voltage I/O port	Standard voltage high current I/O port
40	36	$R2_1$	High voltage I/O port	Medium voltage I/O port	Standard voltage high current I/O port
41	37	$R2_2$	High voltage I/O port	Medium voltage I/O port	Standard voltage high current I/O port
42	38	$R2_3$	High voltage I/O port	Medium voltage I/O port	Standard voltage high current I/O port
—	22	NC	—	—	—
—	44	NC	—	—	—

Note: No connections should be made to NC pins.

Table 1-6 lists the pin functions for the HD404318, HD404358 and HD404358R Series microcomputers.

Table 1-6 HD404318, HD404358 and HD404358R Series Pin Functions

Type	Symbol	I/O	Function
Power supply	V_{CC}	—	**Power supply:** Connect to the system power supply.
	GND	—	**Ground:** Connect to the system ground
	AV_{CC}	—	**Analog power supply:** The A/D converter power supply connection. Connect to a potential identical to that of V_{CC} at a point as close as possible to the V_{CC} pin. Note that a bypass capacitor (about 0.1 µF) should be connected between the AV_{CC} pin and the AV_{SS} pin if a power supply separate from the V_{CC} power supply is used for the A/D converter power supply. This capacitor is not required if the AV_{CC} pin is connected directly to the V_{CC} pin.
	AV_{SS}	—	**Analog ground:** The A/D converter ground connection. Connect to a potential identical to that of GND at a point as close as possible to the GND pin.
	V_{disp}	—	**High voltage pin output power supply (HD404318 Series):** Used as the output power supply by the high voltage pins.
Clock	OSC_1	Input	**System clock oscillator connection 1:** Connect a ceramic or crystal oscillator, or an external oscillator circuit. Use an oscillator or clock with a frequency of between 400 kHz and 4.5 MHz for the HD404318 and a frequency between 400 kHz and 8.5 MHz for the HD404358/HD404358R. Alternately, for CR oscillation* a resistor should be connected. See section 13, “Oscillator Circuits” for examples of the circuits used when a ceramic or crystal oscillator, a resistor, or an external clock is used.
	OSC_2	Output	**System clock oscillator connection 2:** Connect a ceramic or crystal oscillator to this pin. Use an oscillator with a frequency of between 400 kHz and 4.5 MHz for the HD404318 and a frequency between 400 kHz and 8.5 MHz for the HD404358/HD404358R. Alternately, for CR oscillation* a resistor should be connected. Leave this pin open if an external clock is input to the OSC_1 pin.

Table 1-6 HD404318, HD404358 and HD404358R Series Pin Functions (cont)

Type	Symbol	I/O	Function
Port	D_0 to D_8	I/O	**High voltage D port (HD404318 Series):** High voltage I/O pins (PMOS open drain) that can be accessed in 1-bit units. **D port (HD404358 Series):** Standard voltage I/O pins (CMOS three state) that can be accessed in 1-bit units. **D port (HD404358R Series):** Standard voltage I/O pins (CMOS three state) that can be accessed in 1-bit units. Pins D_5 to D_8 are high-current pins (CMOS three state) capable of handling current levels of up to 15 mA.
	$R0_0$ to $R0_3$	I/O	**R0 port:** Standard voltage I/O pins (CMOS three state) that can be accessed as a 4-bit unit. **R0 port (HD404358R Series):** Standard voltage high current I/O pins (CMOS three state) that can be accessed as a 4-bit unit. Pins $R0_0$ to $R0_3$ are high - current pins capable of handling current levels of up to 15 mA.
	$R1_0$ to $R1_3$	I/O	**High voltage R1 port (HD404318 Series):** High voltage I/O pins (PMOS open drain) that can be accessed as a 4-bit unit. **R1 port (HD404358 Series):** Standard voltage I/O pins (CMOS three state) that can be accessed as a 4-bit unit. **R1 port (HD404358R Series):** Standard voltage high current I/O pins that can be accessed as a 4-bit unit. Pins $R1_0$ to $R1_3$ are high-current pins (CMOS three state) capable of handling current levels of up to 15 mA.
	$R2_0$ to $R2_3$	I/O	**High voltage R2 port (HD404318 Series):** High voltage I/O pins (PMOS open drain) that can be accessed as a 4-bit unit. **Medium voltage R2 port (HD404358 Series):** Medium voltage I/O pins (NMOS open drain) that can be accessed as a 4-bit unit. **R2 port (HD404358R Series):** Standard voltage high current I/O pins that can be accessed as a 4-bit unit. Pins $R2_0$ to $R2_3$ are high-current pins (CMOS three state) capable of handling current levels of up to 15 mA.
	$R3_0$ to $R3_3$	I/O	**R3 port:** Standard voltage I/O pins (CMOS three state) that can be accessed as a 4-bit unit.
	$R4_0$ to $R4_3$	I/O	**R4 port:** Standard voltage I/O pins (CMOS three state) that can be accessed as a 4-bit unit.

Table 1-6 HD404318, HD404358 and HD404358R Series Pin Functions (cont)

Type	Symbol	I/O	Function
Port	$R8_0$ to $R8_3$	I/O	**High voltage R8 port (HD404318 Series):** High voltage I/O pins (PMOS open drain) that can be accessed as a 4-bit unit. **R8 port (HD404358 Series):** Standard voltage I/O pins (CMOS three state) that can be accessed as a 4-bit unit. **R8 port (HD404358R Series):** Standard voltage large current I/O pins that can be accessed as a 4-bit unit. Pins $R8_0$ to $R8_3$ are high-current pins (CMOS three state) capable of handling current levels of up to 15 mA.
	RA_1	Input	**High voltage RA port (HD404318 Series):** Single bit high voltage input pin. **RA port (HD404358/HD404358R Series):** Single bit standard input pin.
System control	TEST	Input	**Test:** Connect to ground.
	$\overline{RESET}$	Input	**Reset:** The microcomputer goes to the reset state when a low level is applied to this pin.
	$\overline{STOPC}$	Input	**Stop mode clear:** Input pin for clearing stop mode. The microcomputer switches from stop mode to active mode when a low level is applied to this pin.
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$	Input	**External interrupts 0 and 1:** Falling edge detection external interrupt inputs.
Alarm	BUZZ	Output	**Alarm output:** Output pin for the alarm output.
8-bit timers	TOC	Output	**Timer C output:** The timer C output.
	EVNB	Input	**Timer B event input:** The timer B event input. External events can be counted on falling edges, rising edges, or falling/rising edge pairs in this input. This pin can also be used as an input capture trigger.
Serial interface	$\overline{SCK}$	I/O	**Serial transfer clock I/O:** I/O pin for the serial interface clock.
	SI	Input	**Serial reception data input:** Data input pin for the serial interface.
	SO	Output	**Serial transmission output:** Data output pin for the serial interface.
A/D converter	AN_0 to AN_7	Input	**Analog input channels 0 to 7:** Analog input channels for the A/D converter.

Note: * Apply to the HD404358R Series.

1.3.3 HD404339/HD404369 Series Pin Functions

Figures 1-13 and 1-14 show the pin arrangements for the HD404339 and HD404369 Series products in the DP-64S, and FP-64B packages.

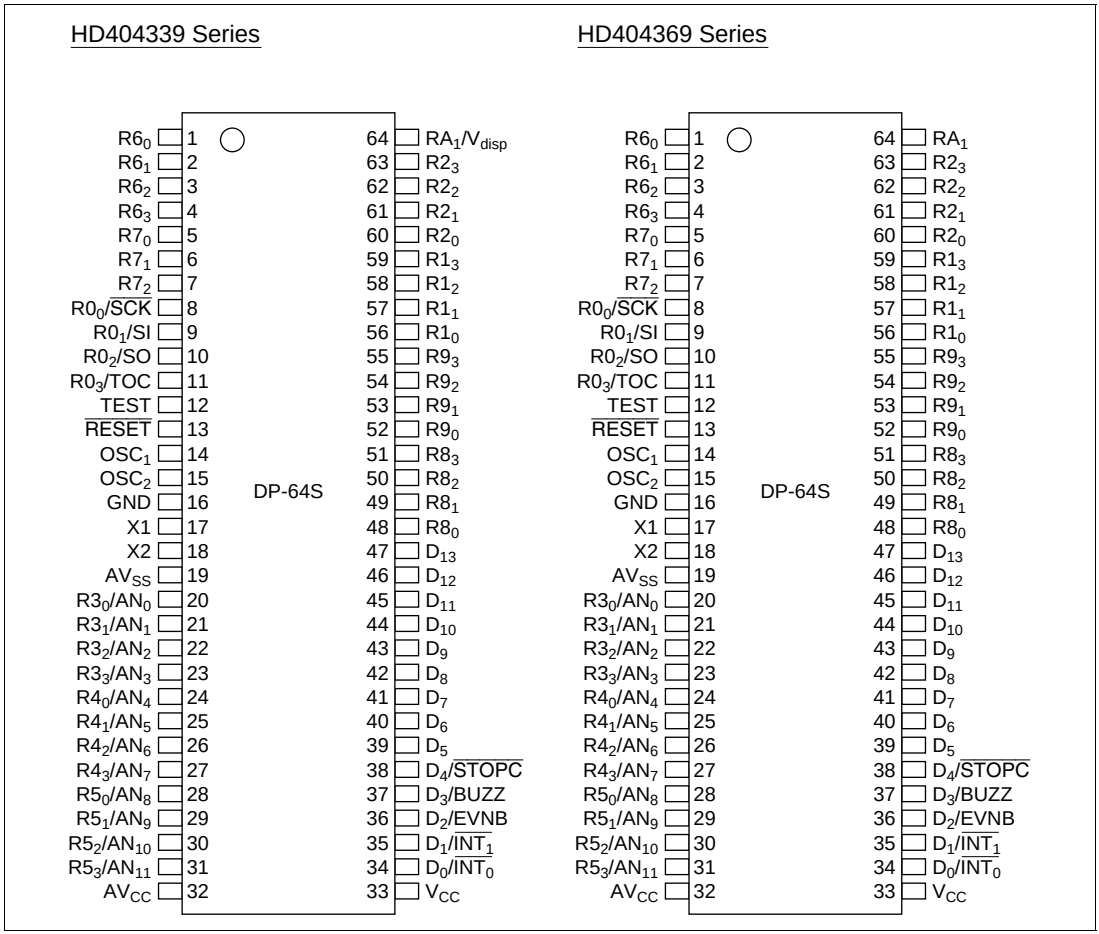
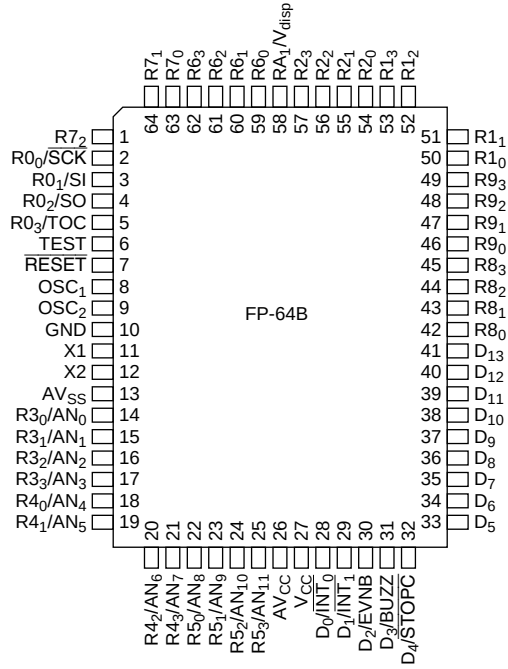


Figure 1-13 HD404339 and HD404369 Series Pin Arrangements (DP-64S Package: Top View)

HD404339 Series



HD404369 Series

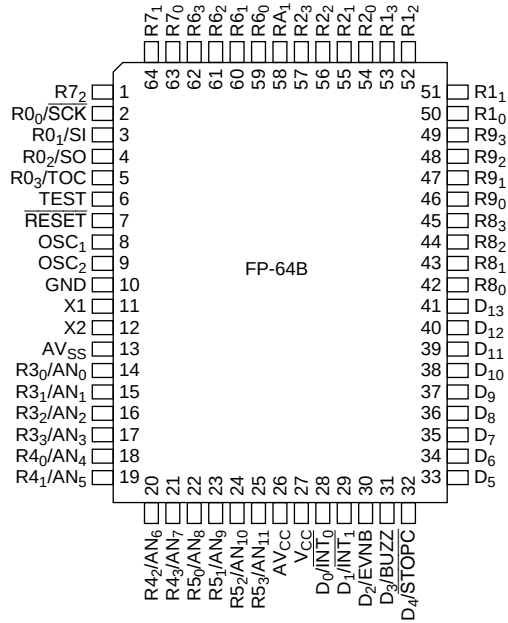


Figure 1-14 HD404339 and HD404369 Series Pin Arrangements (FP-64B Package: Top View)

Table 1-7 lists the pin assignments for the HD404339 and HD404369 Series microcomputers.

Table 1-7 HD404339 and HD404369 Series Pin Assignments

Pin No.			Pin Function	
DP-64S	FP-64B	Pin	HD404339 Series	HD404369 Series
1	59	$R6_0$	Standard voltage I/O port	
2	60	$R6_1$	Standard voltage I/O port	
3	61	$R6_2$	Standard voltage I/O port	
4	62	$R6_3$	Standard voltage I/O port	
5	63	$R7_0$	Standard voltage I/O port	
6	64	$R7_1$	Standard voltage I/O port	
7	1	$R7_2$	Standard voltage I/O port	
8	2	$R0_0/\overline{SCK}$	Standard voltage I/O port/serial transfer clock I/O	
9	3	$R0_1$/SI	Standard voltage I/O port/serial reception data input	
10	4	$R0_2$/SO	Standard voltage I/O port/serial transmission data output	
11	5	$R0_3$/TOC	Standard voltage I/O port/timer C output	
12	6	TEST	Test	
13	7	$\overline{RESET}$	Reset	
14	8	OSC_1	System clock oscillator connection: input	
15	9	OSC_2	System clock oscillator connection: output	
16	10	GND	Ground	
17	11	X1	Subsystem clock oscillator connection: input	
18	12	X2	Subsystem clock oscillator connection: output	
19	13	AV_{SS}	Analog ground	
20	14	$R3_0/AN_0$	Standard voltage I/O port/analog input channel	
21	15	$R3_1/AN_1$	Standard voltage I/O port/analog input channel	
22	16	$R3_2/AN_2$	Standard voltage I/O port/analog input channel	
23	17	$R3_3/AN_3$	Standard voltage I/O port/analog input channel	
24	18	$R4_0/AN_4$	Standard voltage I/O port/analog input channel	
25	19	$R4_1/AN_5$	Standard voltage I/O port/analog input channel	
26	20	$R4_2/AN_6$	Standard voltage I/O port/analog input channel	
27	21	$R4_3/AN_7$	Standard voltage I/O port/analog input channel	
28	22	$R5_0/AN_8$	Standard voltage I/O port/analog input channel	

Table 1-7 HD404339 and HD404369 Series Pin Assignments (cont)

Pin No.			Pin Function	
DP-64S	FP-64B	Pin	HD404339 Series	HD404369 Series
29	23	$R5_1/AN_9$	Standard voltage I/O port/analog input channel	
30	24	$R5_2/AN_{10}$	Standard voltage I/O port/analog input channel	
31	25	$R5_3/AN_{11}$	Standard voltage I/O port/analog input channel	
32	26	AV_{CC}	Analog power supply	
33	27	V_{CC}	Power supply	
34	28	$D_0/\overline{INT}_0$	High voltage I/O port/ external interrupt input	Standard voltage I/O port/ external interrupt input
35	29	$D_1/\overline{INT}_1$	High voltage I/O port/ external interrupt input	Standard voltage I/O port/ external interrupt input
36	30	D_2/EVNB	High voltage I/O port/ timer B event input	Standard voltage I/O port/ timer B event input
37	31	D_3/BUZZ	High voltage I/O port/ alarm output	Standard voltage I/O port/ alarm output
38	32	$D_4/\overline{STOPC}$	High voltage I/O port/ stop mode clear	Standard voltage I/O port/ stop mode clear
39	33	D_5	High voltage I/O port	Standard voltage I/O port
40	34	D_6	High voltage I/O port	Standard voltage I/O port
41	35	D_7	High voltage I/O port	Standard voltage I/O port
42	36	D_8	High voltage I/O port	Standard voltage I/O port
43	37	D_9	High voltage I/O port	Standard voltage I/O port
44	38	D_{10}	High voltage I/O port	Standard voltage I/O port
45	39	D_{11}	High voltage I/O port	Standard voltage I/O port
46	40	D_{12}	High voltage I/O port	Standard voltage I/O port
47	41	D_{13}	High voltage I/O port	Standard voltage I/O port
48	42	$R8_0$	High voltage I/O port	Standard voltage I/O port
49	43	$R8_1$	High voltage I/O port	Standard voltage I/O port
50	44	$R8_2$	High voltage I/O port	Standard voltage I/O port
51	45	$R8_3$	High voltage I/O port	Standard voltage I/O port
52	46	$R9_0$	High voltage I/O port	Standard voltage I/O port
53	47	$R9_1$	High voltage I/O port	Standard voltage I/O port
54	48	$R9_2$	High voltage I/O port	Standard voltage I/O port

Table 1-7 HD404339 and HD404369 Series Pin Assignments (cont)

Pin No.			Pin Function	
DP-64S	**FP-64B**	**Pin**	**HD404339 Series**	**HD404369 Series**
55	49	$R9_3$	High voltage I/O port	Standard voltage I/O port
56	50	$R1_0$	High voltage I/O port	Medium voltage I/O port
57	51	$R1_1$	High voltage I/O port	Medium voltage I/O port
58	52	$R1_2$	High voltage I/O port	Medium voltage I/O port
59	53	$R1_3$	High voltage I/O port	Medium voltage I/O port
60	54	$R2_0$	High voltage I/O port	Medium voltage I/O port
61	55	$R2_1$	High voltage I/O port	Medium voltage I/O port
62	56	$R2_2$	High voltage I/O port	Medium voltage I/O port
63	57	$R2_3$	High voltage I/O port	Medium voltage I/O port
64	58	RA_1/ (Vdisp)*	High voltage input port/ high voltage pin output power supply	Standard voltage input port

Note: * Items in parentheses apply only to the HD404339 Series.

Table 1-8 lists the pin functions for the HD404339 and HD404369 Series microcomputers.

Table 1-8 HD404339 and HD404369 Series Pin Functions

Type	Symbol	I/O	Function
Power supply	V_{CC}	—	**Power supply:** Connect to the system power supply.
	GND	—	**Ground:** Connect to the system ground
	AV_{CC}	—	**Analog power supply:** The A/D converter power supply connection. Connect to a potential identical to that of V_{CC} at a point as close as possible to the V_{CC} pin. Note that a bypass capacitor (about 0.1 µF) should be connected between the AV_{CC} pin and the AV_{SS} pin if a power supply separate from the V_{CC} power supply is used for the A/D converter power supply. This capacitor is not required if the AV_{CC} pin is connected directly to the V_{CC} pin.
	AV_{SS}	—	**Analog ground:** The A/D converter ground connection. Connect to a potential identical to that of GND at a point as close as possible to the GND pin.
	V_{disp}	—	**High voltage pin output power supply (HD404339 Series):** Used as the output power supply by the high voltage pins.
Clock	OSC_1	Input	**System clock oscillator connection 1:** Connect a ceramic or crystal oscillator to this pin. Alternatively, an external clock signal may be input to this pin. Use an oscillator or clock with a frequency of between 400 kHz and 4.5 MHz for the HD404339 and a frequency between 400 kHz and 8.5 MHz for the HD404369. See section 14, “Oscillator Circuits” for examples of the circuits used when a ceramic or crystal oscillator or an external clock is used.
	OSC_2	Output	**System clock oscillator connection 2:** Connect a ceramic or crystal oscillator to this pin. Use an oscillator with a frequency of between 400 kHz and 4.5 MHz for the HD404339 and a frequency between 400 kHz and 8.5 MHz for the HD404369. Leave this pin open if an external clock is input to the OSC_1 pin.
	X1	Input	**Subsystem clock oscillator connection 1:** Connect a 32.768 kHz crystal oscillator to this pin. Tie this pin to ground if the subsystem clock is not used.
	X2	Output	**Subsystem clock oscillator connection 2:** Connect a 32.768 kHz crystal oscillator to this pin. Leave this pin open if the subsystem clock is not used.

Table 1-8 HD404339 and HD404369 Series Pin Functions (cont)

Type	Symbol	I/O	Function
Port	D_0 to D_{13}	I/O	**High voltage D port (HD404339 Series):** High voltage I/O pins (PMOS open drain) that can be accessed in 1-bit units. **D port (HD404369 Series):** Standard I/O pins (CMOS three state) that can be accessed in 1-bit units.
	$R0_0$ to $R0_3$	I/O	**R0 port:** Standard I/O pins (CMOS three state) that can be accessed as a 4-bit unit.
	$R1_0$ to $R1_3$	I/O	**High voltage R1 port (HD404339 Series):** High voltage I/O pins (PMOS open drain) that can be accessed as a 4-bit unit. **Medium voltage R1 port (HD404369 Series):** Medium voltage I/O pins (NMOS open drain) that can be accessed as a 4-bit unit.
	$R2_0$ to $R2_3$	I/O	**High voltage R2 port (HD404339 Series):** High voltage I/O pins (PMOS open drain) that can be accessed as a 4-bit unit. **Medium voltage R2 port (HD404369 Series):** Medium voltage I/O pins (NMOS open drain) that can be accessed as a 4-bit unit.
	$R3_0$ to $R3_3$	I/O	**R3 port:** Standard I/O pins (CMOS three state) that can be accessed as a 4-bit unit.
	$R4_0$ to $R4_3$	I/O	**R4 port:** Standard I/O pins (CMOS three state) that can be accessed as a 4-bit unit.
	$R5_0$ to $R5_3$	I/O	**R5 port:** Standard I/O pins (CMOS three state) that can be accessed as a 4-bit unit.
	$R6_0$ to $R6_3$	I/O	**R6 port:** Standard I/O pins (CMOS three state) that can be accessed as a 4-bit unit.
	$R7_0$ to $R7_2$	I/O	**R7 port:** Three-bit standard I/O pins (CMOS three state).
	$R8_0$ to $R8_3$	I/O	**High voltage R8 port (HD404339 Series):** High voltage I/O pins (PMOS open drain) that can be accessed as a 4-bit unit. **R8 port (HD404369 Series):** Standard I/O pins (CMOS three state) that can be accessed as a 4-bit unit.
	$R9_0$ to $R9_3$	I/O	**High voltage R9 port (HD404339 Series):** High voltage I/O pins (PMOS open drain) that can be accessed as a 4-bit unit. **R9 port (HD404369 Series):** Standard I/O pins (CMOS three state) that can be accessed as a 4-bit unit.

Table 1-8 HD404339 and HD404369 Series Pin Functions (cont)

Type	Symbol	I/O	Function
Port	RA_1	Input	**High voltage RA port (HD404339 Series):** Single bit high voltage input pin. **RA port (HD404369 Series):** Single bit standard input pin.
System control	TEST	Input	**Test:** Connect to ground.
	$\overline{RESET}$	Input	**Reset:** The microcomputer goes to the reset state when a low level is applied to this pin.
	$\overline{STOPC}$	Input	**Stop mode clear:** Input pin for clearing stop mode. The microcomputer switches from stop mode to active mode when a low level is applied to this pin.
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$	Input	**External interrupts 0 and 1:** Falling edge detection external interrupt inputs.
Alarm	BUZZ	Output	**Alarm output:** Output pin for the alarm output.
8-bit timers	TOC	Output	**Timer C output:** The timer C output.
	EVNB	Input	**Timer B event input:** The timer B event input. External events can be counted on falling edges, rising edges, or falling/rising edge pairs in this input. This pin can also be used as an input capture trigger.
Serial interface	$\overline{SCK}$	I/O	**Serial transfer clock I/O:** I/O pin for the serial interface clock.
	SI	Input	**Serial reception data input:** Data input pin for the serial interface.
	SO	Output	**Serial transmission output:** Data output pin for the serial interface.
A/D converter	AN_0 to AN_{11}	Input	**Analog input channels 0 to 11:** Analog input channels for the A/D converter.

Section 2 Memory

2.1 Overview

Table 2-1 lists ROM and RAM capacities of the products in the HMCS43XX Family.

Table 2-1 ROM and RAM Capacities

Series	Product	ROM	RAM
HD404344R	HD404341R/HD40C4341R	1,024 words	256 digits
	HD404342R/HD40C4342R	2,048 words	
	HD404344R/HD40C4344R	4,096 words	
	HD4074344	4,096 words	
HD404394	HD404391	1,024 words	256 digits
	HD404392	2,048 words	
	HD404394	4,096 words	
	HD4074394	4,096 words	
HD404318	HD404314	4,096 words	384 digits
	HD404316	6,144 words	
	HD404318	8,192 words	
	HD4074318	8,192 words	
HD404358	HD404354/HD40A4354	4,096 words	384 digits
	HD404356/HD40A4356	6,144 words	
	HD404358/HD40A4358	8,192 words	
	HD407A4359	16,384 words	512 digits
HD404358R	HD404354R/HD40A4354R/HD40C4354R	4,096 words	512 digits
	HD404356R/HD40A4356R/HD40C4356R	6,144 words	
	HD404358R/HD40A4358R/HD40C4358R	8,192 words	
	HD407A4359R	16,384 words	
	HD407C4359R	16,384 words	

Note: 1 word: 10 bits
1 digit: 4 bits

Table 2-1 ROM and RAM Capacities (cont)

Series	Product	ROM	RAM
HD404339	HD404334	4,096 words	512 digits
	HD404336	6,144 words	
	HD404338	8,192 words	
	HD4043312	12,288 words	
	HD404339	16,384 words	
	HD4074339	16,384 words	
HD404369	HD404364/HD40A4364	4,096 words	512 digits
	HD404368/HD40A4368	8,192 words	
	HD4043612/HD40A43612	12,288 words	
	HD404369/HD40A4369	16,384 words	
	HD407A4369	16,384 words	

Note: 1 word: 10 bits
1 digit: 4 bits

2.2 ROM

2.2.1 Vector Address Area

The vector address area is allocated to ROM addresses $0000 to $000F. On a reset, when stop mode is cleared, or when an interrupt is handled, the processor executes the instruction at one of eight fixed vector addresses depending on the particular exception handling factor involved. Therefore, user software should specify a JMPL instruction (the unconditional long jump instruction: two words) that branches to the start of the appropriate reset, stop mode clear, or interrupt handling routine at each of these vector addresses. (See figures 2-1 and 2-2.)

2.2.2 Zero Page Subroutine Area

The zero page subroutine area is allocated to ROM addresses $0000 to $003F. User programs can make conditional subroutine calls to arbitrary addresses in this area with the CAL instruction.

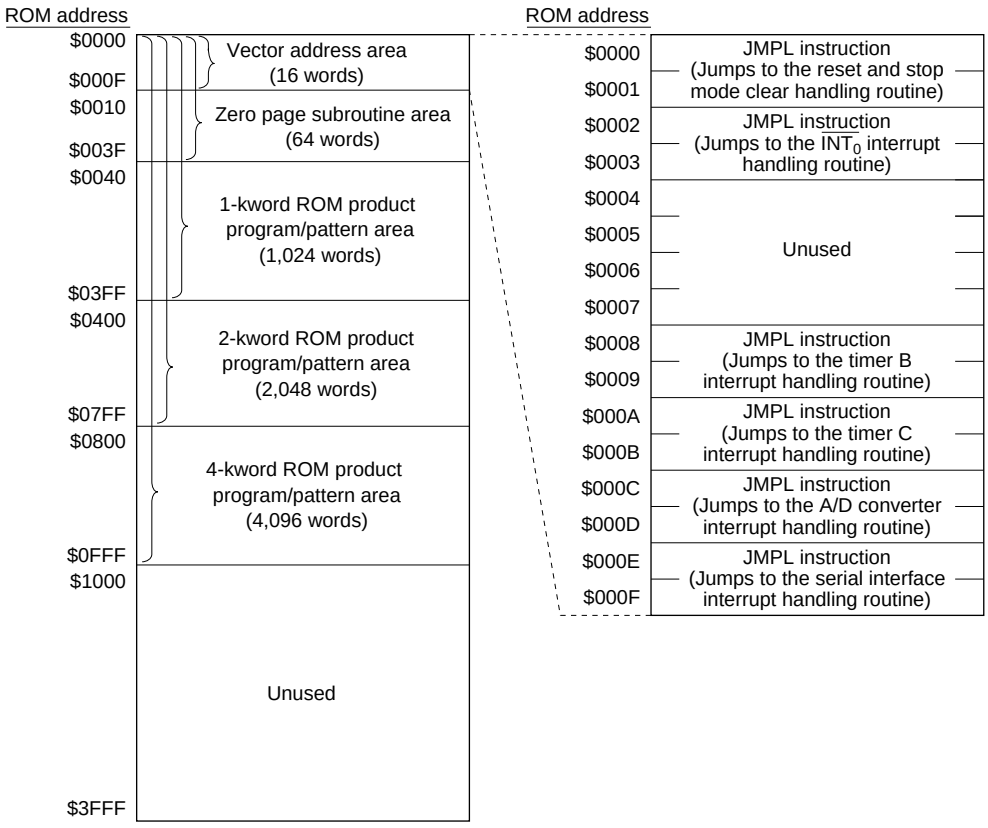
2.2.3 Pattern Area

The pattern area is allocated to ROM addresses $0000 to $0FFF. User programs can move ROM bit patterns (8 bits) in this area either to the R1 and R2 port data register pair or to the accumulator and B register pair with the P instruction.

2.2.4 Program Area

All of the ROM address space can be used as program area.

Figure 2-1 shows the ROM memory map for the microcomputers in the HD404344R and HD404394 Series.

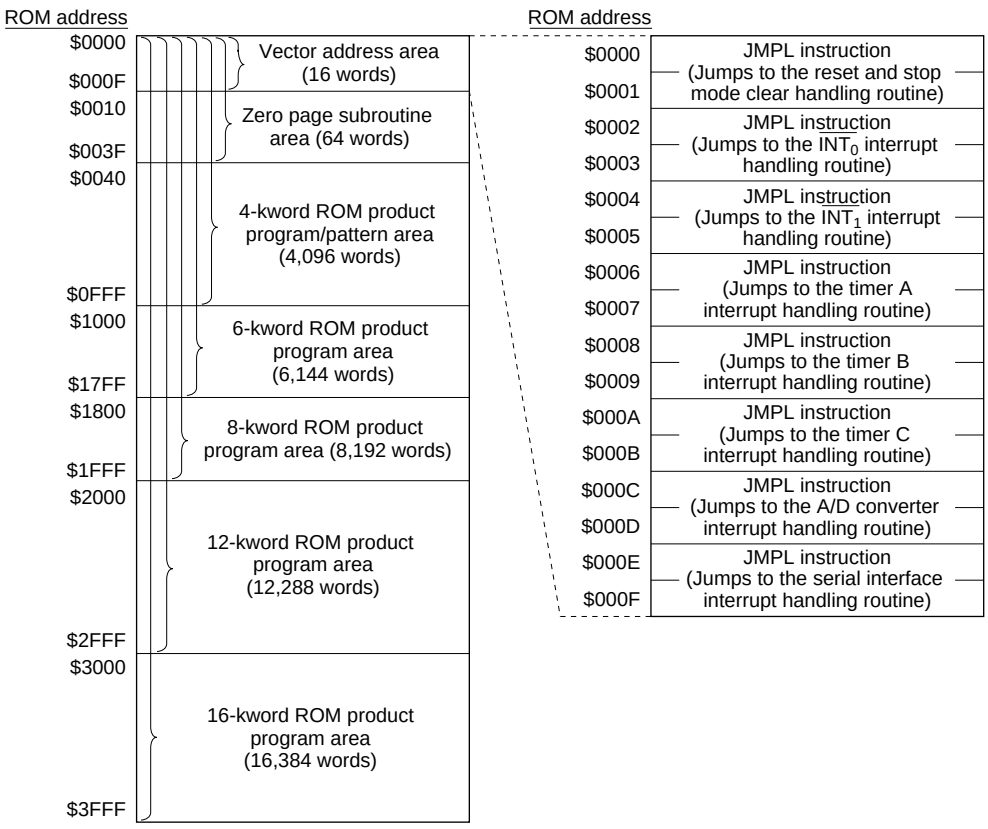


Note: The program/pattern area differs between different products in these series.

ROM Capacity	Product		Pattern Area		Program Area	
			Addresses	Capacity	Addresses	Capacity
1-kword	HD404341R HD40C4341R	HD404391	$0000 to $03FF	1,024 words	$0000 to $03FF	1,024 words
2-kword	HD404342R HD40C4342R	HD404392	$0000 to $07FF	2,048 words	$0000 to $07FF	2,048 words
4-kword	HD404344R HD40C4344R HD4074344	HD404394 HD4074394	$0000 to $0FFF	4,096 words	$0000 to $0FFF	4,096 words

Figure 2-1 HD404344R and HD404394 Series ROM Memory Map

Figure 2-2 shows the memory map for the microcomputers in the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series.



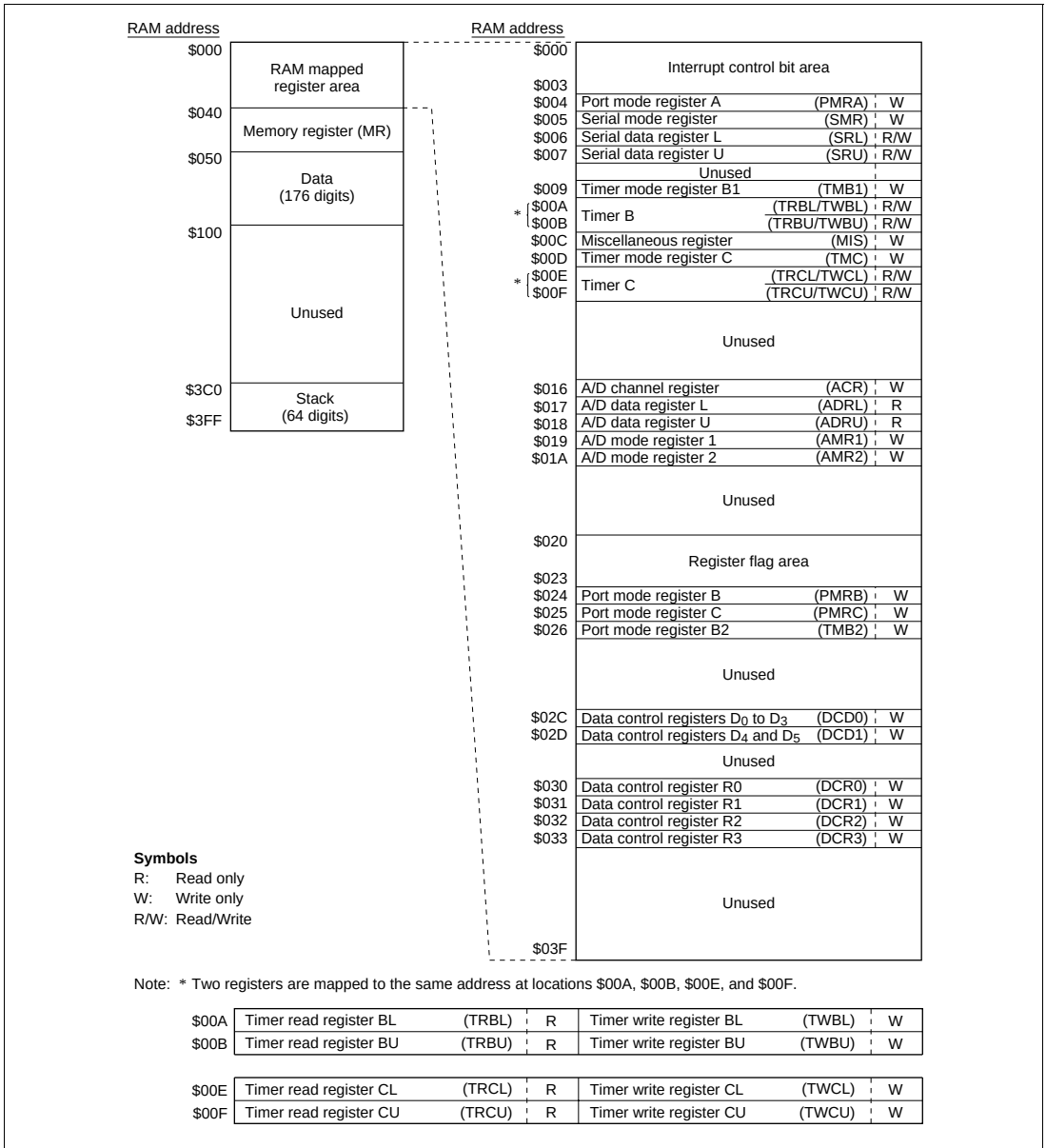
Note: The program area differs between different products in these series.

ROM Capacity	Product					Program Area	
						Addresses	Capacity
4-kword	HD404314	HD404354 HD40A4354	HD404354R HD40A4354R HD40C4354R	HD404334	HD404364 HD40A4364	$0000 to $0FFF	4,096 words
6-kword	HD404316	HD404356 HD40A4356	HD404356R HD40A4356R HD40C4356R	HD404336	—	$0000 to $17FF	6,144 words
8-kword	HD404318 HD4074318	HD404358 HD40A4358	HD404358R HD40A4358R HD40C4358R	HD404338	HD404368 HD40A4368	$0000 to $1FFF	8,192 words
12-kword	—	—	—	HD4043312	HD4043612 HD40A43612	$0000 to $2FFF	12,288 words
16-kword	—	HD407A4359	HD407A4359R HD407C4359R	HD404339 HD4074339	HD404369 HD40A4369 HD407A4369	$0000 to $3FFF	16,384 words

Figure 2-2 HD404318, HD404358, HD404358R, HD404339, and HD404369 Series ROM Memory Map

2.3 RAM

Figure 2-3 shows the RAM memory map for the microcomputers in the HD404344R and HD404394 Series.



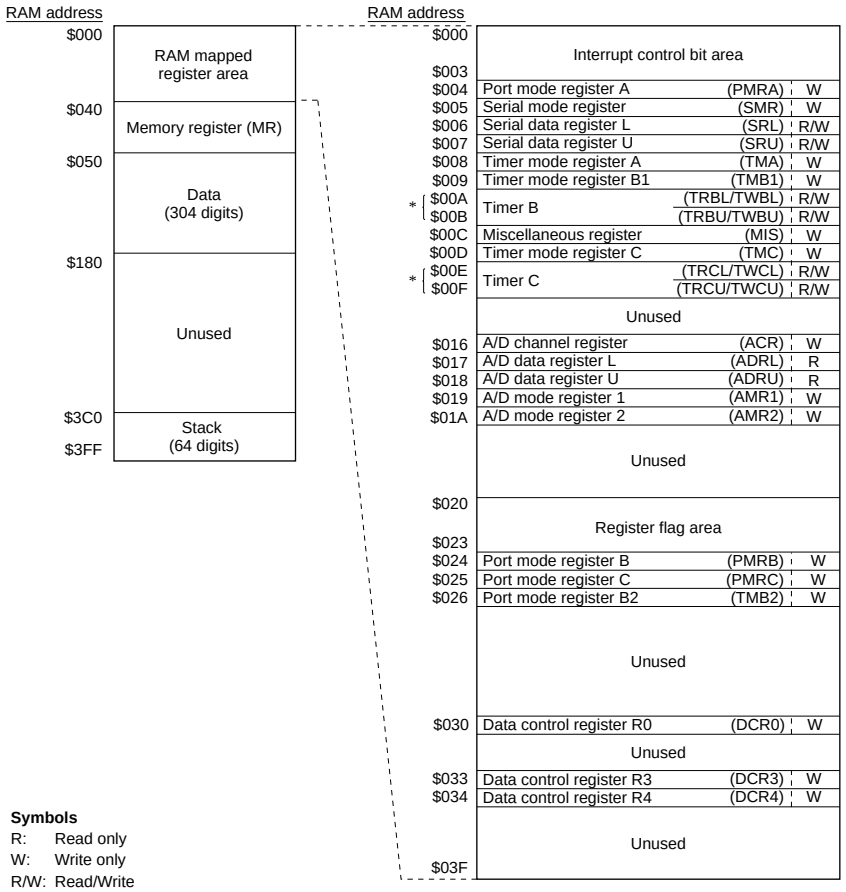
Note: * Two registers are mapped to the same address at locations $00A, $00B, $00E, and $00F.

$00A	Timer read register BL	(TRBL)	R	Timer write register BL	(TWBL)	W
$00B	Timer read register BU	(TRBU)	R	Timer write register BU	(TWBU)	W

$00E	Timer read register CL	(TRCL)	R	Timer write register CL	(TWCL)	W
$00F	Timer read register CU	(TRCU)	R	Timer write register CU	(TWCU)	W

Figure 2-3 HD404344R and HD404394 Series RAM Memory Map

Figure 2-4 shows the RAM memory map for the microcomputers in the HD404318 Series.

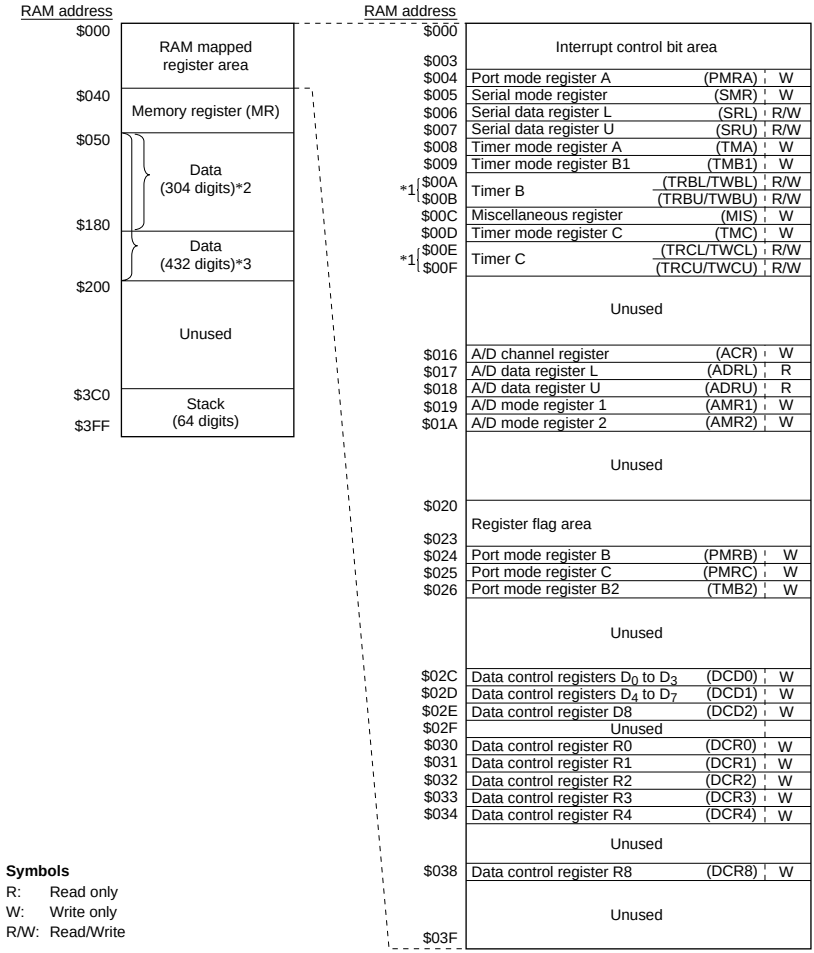


Note: * Two registers are mapped to the same address at locations $00A, $00B, $00E, and $00F.

$00A	Timer read register BL	(TRBL)	R	Timer write register BL	(TWBL)	W
$00B	Timer read register BU	(TRBU)	R	Timer write register BU	(TWBU)	W
$00E	Timer read register CL	(TRCL)	R	Timer write register CL	(TWCL)	W
$00F	Timer read register CU	(TRCU)	R	Timer write register CU	(TWCU)	W

Figure 2-4 HD404318 Series RAM Memory Map

Figure 2-5 shows the RAM memory map for the microcomputers in the HD404358/HD404358R Series.



Notes: 1. Two registers are mapped to the same address at locations $00A, $00B, $00E, and $00F.

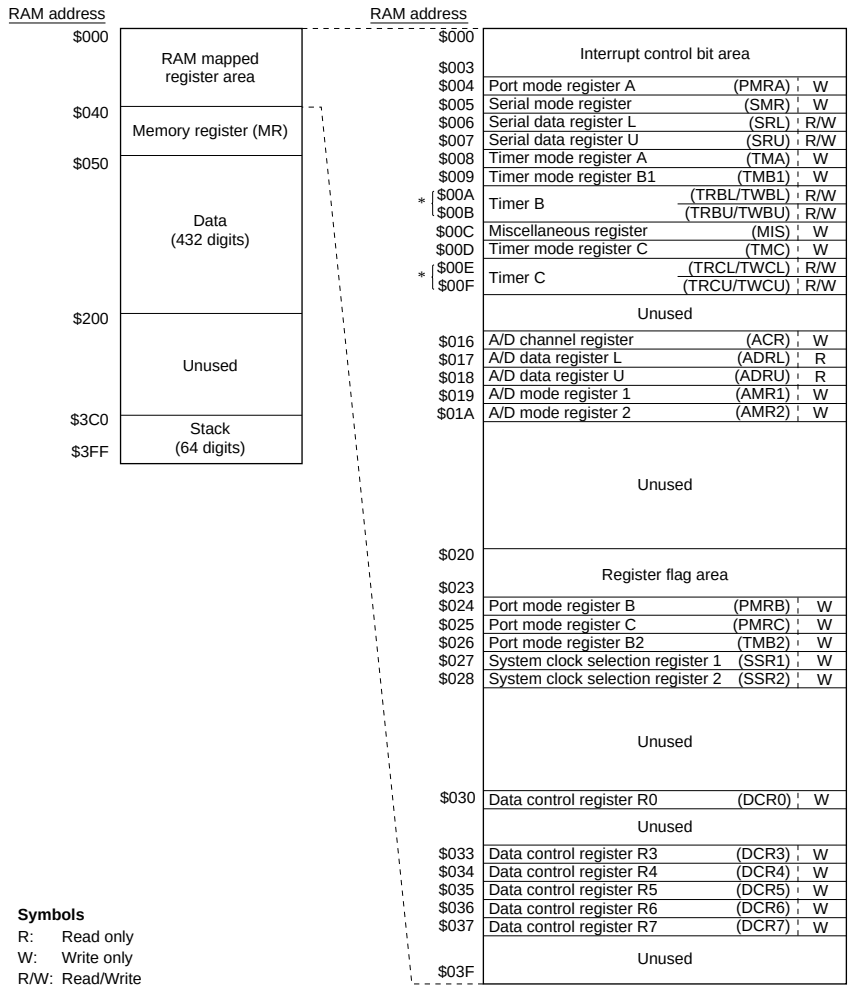
$00A	Timer read register BL	(TRBL)	R	Timer write register BL	(TWBL)	W
$00B	Timer read register BU	(TRBU)	R	Timer write register BU	(TWBU)	W

$00E	Timer read register CL	(TRCL)	R	Timer write register CL	(TWCL)	W
$00F	Timer read register CU	(TRCU)	R	Timer write register CU	(TWCU)	W

2. Applies to the HD404354, HD404356, HD404358, HD40A4354, HD40A4356, and HD40A4358.
3. Applies to the HD404354R, HD404356R, HD404358R, HD40A4354R, HD40A4356R, HD40A4358R, HD40C4354R, HD40C4356R, HD40C4358R, HD407A4359R, HD407C4359R, HD407A4359.

Figure 2-5 HD404358/HD404358R Series RAM Memory Map

Figure 2-6 shows the RAM memory map for the microcomputers in the HD404339 Series.



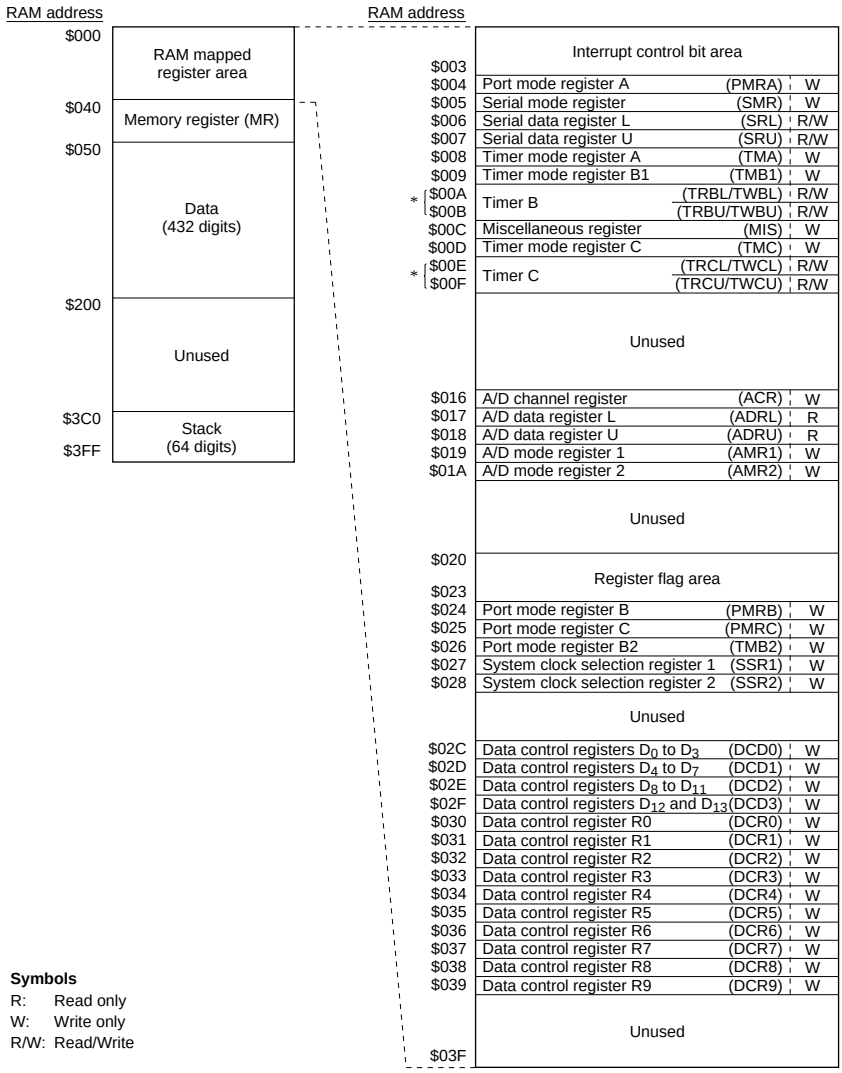
Note: * Two registers are mapped to the same address at locations $00A, $00B, $00E, and $00F.

$00A	Timer read register BL	(TRBL)	R	Timer write register BL	(TWBL)	W
$00B	Timer read register BU	(TRBU)	R	Timer write register BU	(TWBU)	W

$00E	Timer read register CL	(TRCL)	R	Timer write register CL	(TWCL)	W
$00F	Timer read register CU	(TRCU)	R	Timer write register CU	(TWCU)	W

Figure 2-6 HD404339 Series RAM Memory Map

Figure 2-7 shows the RAM memory map for the microcomputers in the HD404369 Series.



Note: * Two registers are mapped to the same address at locations $00A, $00B, $00E, and $00F.

$00A	Timer read register BL	(TRBL)	R	Timer write register BL	(TWBL)	W
$00B	Timer read register BU	(TRBU)	R	Timer write register BU	(TWBU)	W

$00E	Timer read register CL	(TRCL)	R	Timer write register CL	(TWCL)	W
$00F	Timer read register CU	(TRCU)	R	Timer write register CU	(TWCU)	W

Figure 2-7 HD404369 Series RAM Memory Map

2.3.1 RAM Mapped Register Area

The RAM mapped register area is allocated to RAM addresses $000 to $03F. It consists of three sub-areas: the interrupt control bit area ($000 to $003), the special register area ($004 to $01F, and $024 to $03F), and the register flag area ($020 to $023).

(1) Interrupt Control Bit Area ($000 to $003): The interrupt control bit area consists of the bits used for interrupt control. These bits can only be accessed by using the RAM bit manipulation instructions SEM, SEMD, REM, REMD, TM, and TMD. Figures 2-8 and 2-9 show the configurations of the interrupt control bit areas in each series in the HMCS43XX Family.

The bits in the interrupt control bit area can be set to 1 with a SEM or SEMD instruction and can be cleared to 0 with a REM or REMD instruction. The TM and TMD instructions can be used to test these bits. However, there are restrictions on the instructions that can be used with certain bits. Table 2-2 lists the instruction restrictions on the interrupt control bit area.

RAM address	Bit 3	Bit 2	Bit 1	Bit 0
$000	IM0 ($\overline{INT_0}$ interrupt mask)	IF0 ($\overline{INT_0}$ interrupt request flag)	RSP (Stack pointer reset)	IE (Interrupt enable flag)
$002	IMTC (Timer C interrupt mask)	IFTC (Timer C interrupt request flag)	IMTB (Timer B interrupt mask)	IFTB (Timer B interrupt request flag)
$003	IMS (Serial interrupt mask)	IFS (Serial interrupt request flag)	IMAD (A/D converter interrupt mask)	IFAD (A/D converter interrupt request flag)

: Shaded bits are unused

Figure 2-8 HD404344R and HD404394 Series Interrupt Control Bit Area Configuration

RAM address	Bit 3	Bit 2	Bit 1	Bit 0
$000	IM0 ($\overline{INT_0}$ interrupt mask)	IF0 ($\overline{INT_0}$ interrupt request flag)	RSP (Stack pointer reset)	IE (Interrupt enable flag)
$001	IMTA (Timer A interrupt mask)	IFTA (Timer A interrupt request flag)	IM1 ($\overline{INT_1}$ interrupt mask)	IF1 ($\overline{INT_1}$ interrupt request flag)
$002	IMTC (Timer C interrupt mask)	IFTC (Timer C interrupt request flag)	IMTB (Timer B interrupt mask)	IFTB (Timer B interrupt request flag)
$003	IMS (Serial interrupt mask)	IFS (Serial interrupt request flag)	IMAD (A/D converter interrupt mask)	IFAD (A/D converter interrupt request flag)

Figure 2-9 HD404318, HD404358, HD404358R, HD404339, and HD404369 Series Interrupt Control Bit Area Configuration

Table 2-2 Interrupt Control Bit Area Instruction Limitations

	Instruction		
Bit	**SEM/SEMD Instruction**	**REM/REMD Instruction**	**TM/TMD Instruction***
IE	○	○	○
IM	○	○	○
IF	△	○	○
RSP	△	○	X

Symbols

○: Allowed

△: The instruction will not be executed.

X: Unused

IF: Interrupt request flag

IM: Interrupt mask

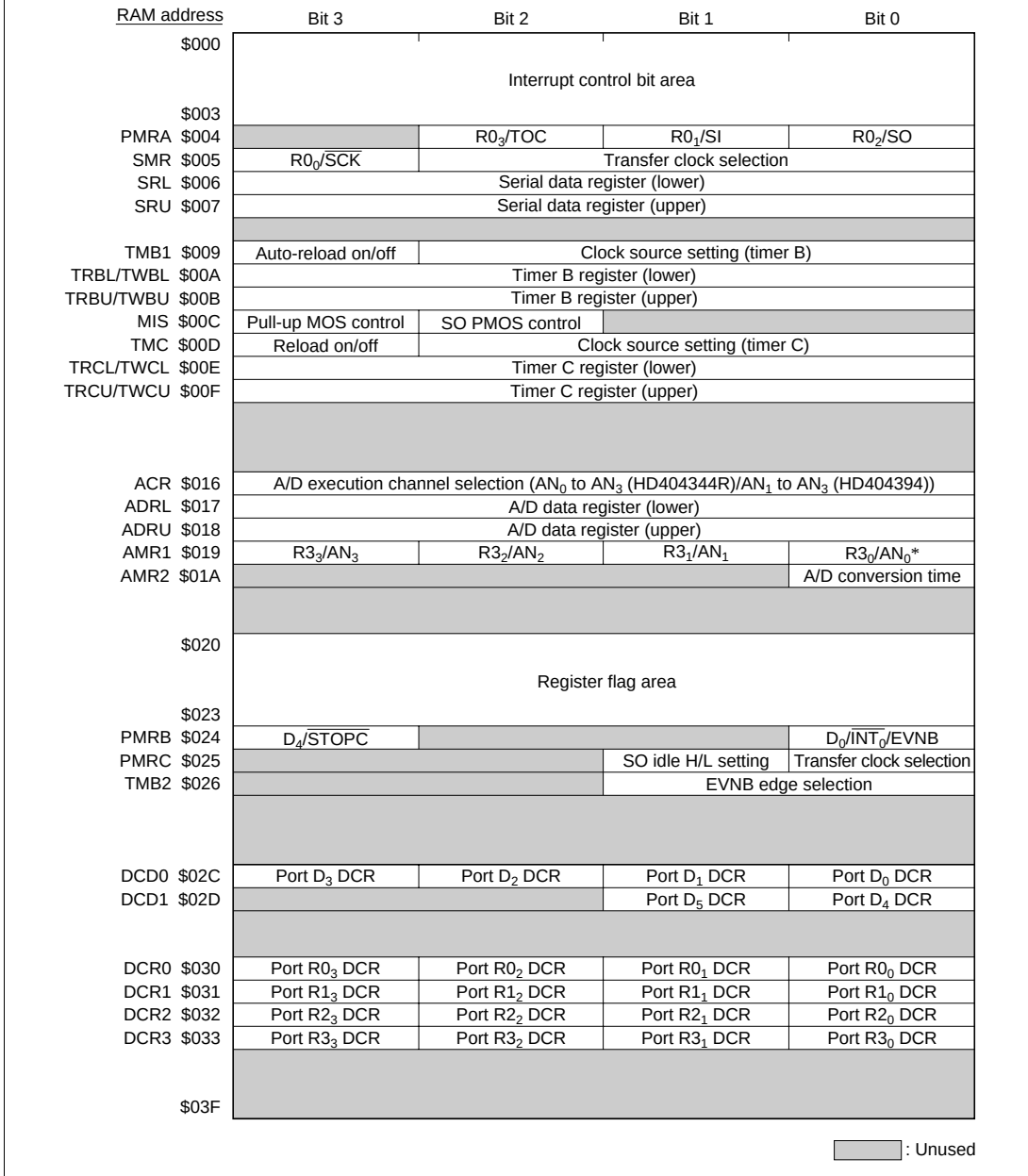
IE: Interrupt enable flag

RSP: Reset stack pointer

Note: * The microcomputer status is undefined if a TM or TMD instruction is executed for a nonexistent bit or for an unused bit.

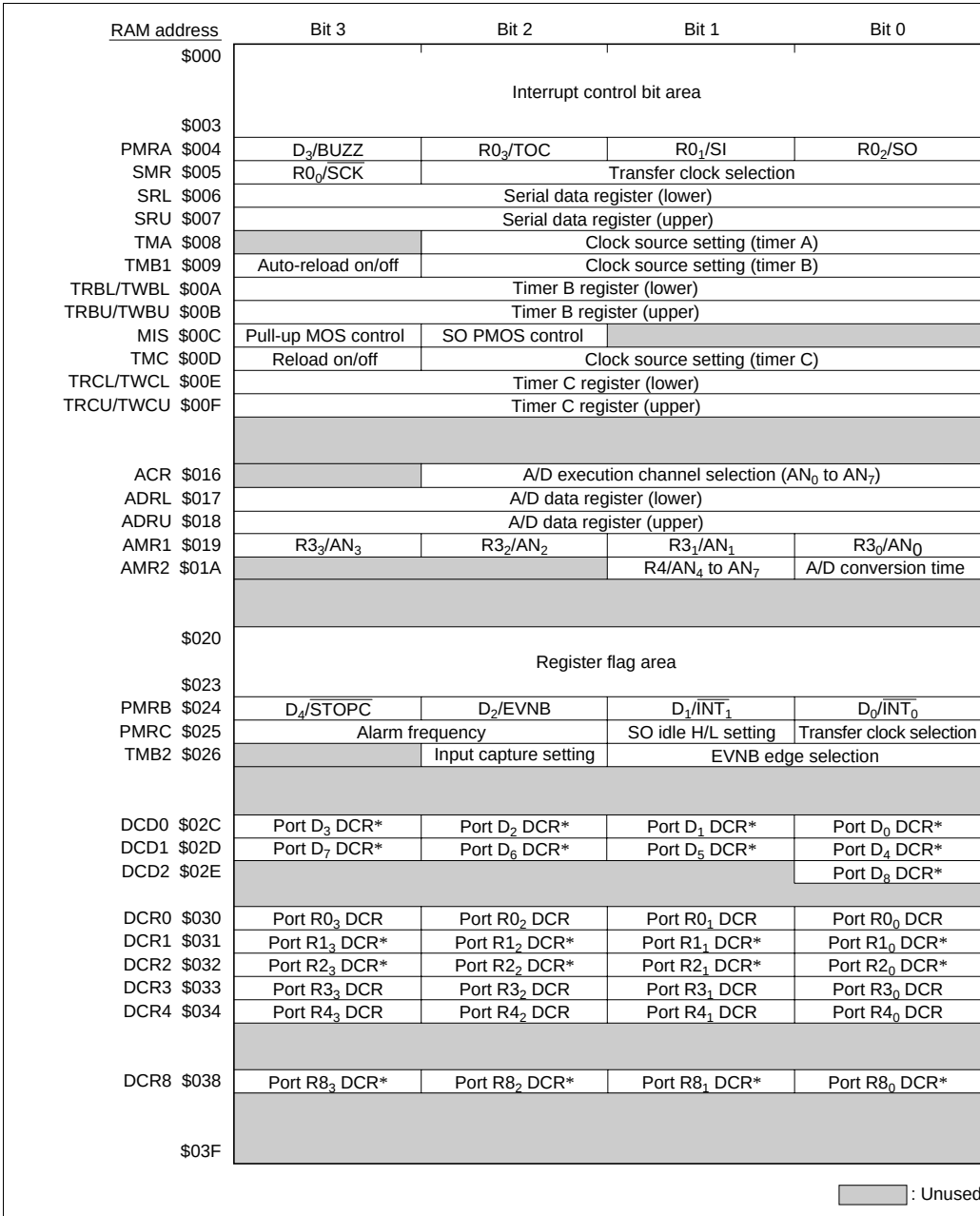
(2) Special Register Area ($004 to $01F, and $024 to $03F): The special register area consists of mode registers for external interrupts and peripheral functions, I/O port data control registers, and other registers. There are three types of registers allocated to the special register area: read-only registers, write-only registers, and read/write registers. These registers can be referenced by immediate instructions, RAM register instructions, arithmetic instructions, and comparison instructions.

Figures 2-10 to 2-12 show the structures of the special register areas.



Note: * Applies to the HD404344R Series. Unused in the HD404394 Series.

Figure 2-10 HD404344R and HD404394 Series Special Register Area Structure



Note: * Applies to the HD404358/HD404358R Series. Unused in the HD404318 Series.

Figure 2-11 HD404318, HD404358 and HD404358R Series Special Register Area Structure

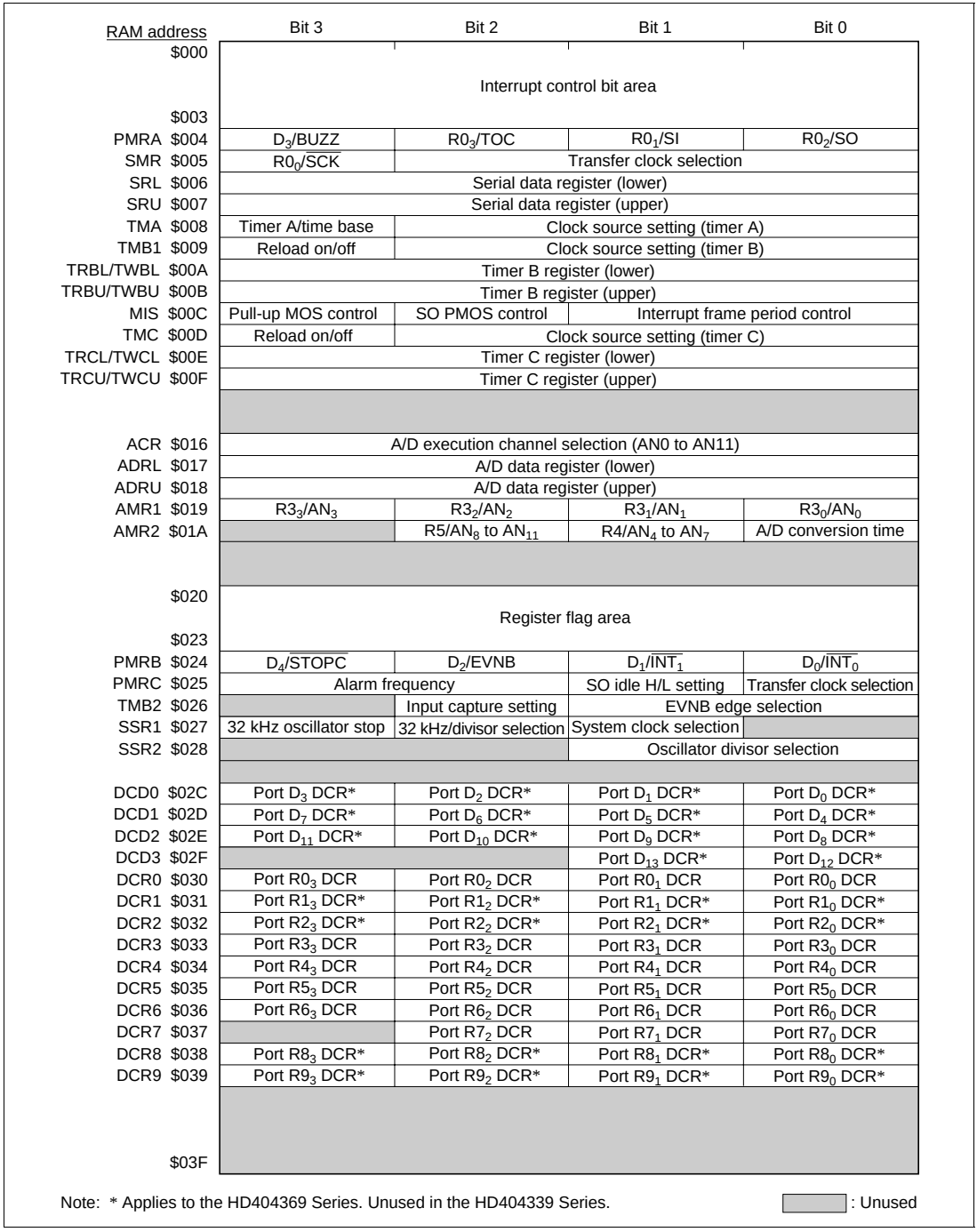


Figure 2-12 HD404339 and HD404369 Series Special Register Area Structure

(3) Register Flag Area ($020 to $023): The register flag area consists of the ADSF and WDON flags, interrupt control bits, and other bits. These bits can only be accessed by using the RAM bit manipulation instructions SEM, SEMD, REM, REMD, TM, and TMD. Figures 2-13 to 2-15 show the configurations of the register flag areas in each series in the HMCS43XX Family.

The bits in the register flag area can be set to 1 with a SEM or SEMD instruction and can be cleared to 0 with a REM or REMD instruction. The TM and TMD instructions can be used to test these bits. However, there are restrictions on the instructions that can be used with certain bits. Table 2-3 lists the instruction restrictions on the register flag area.

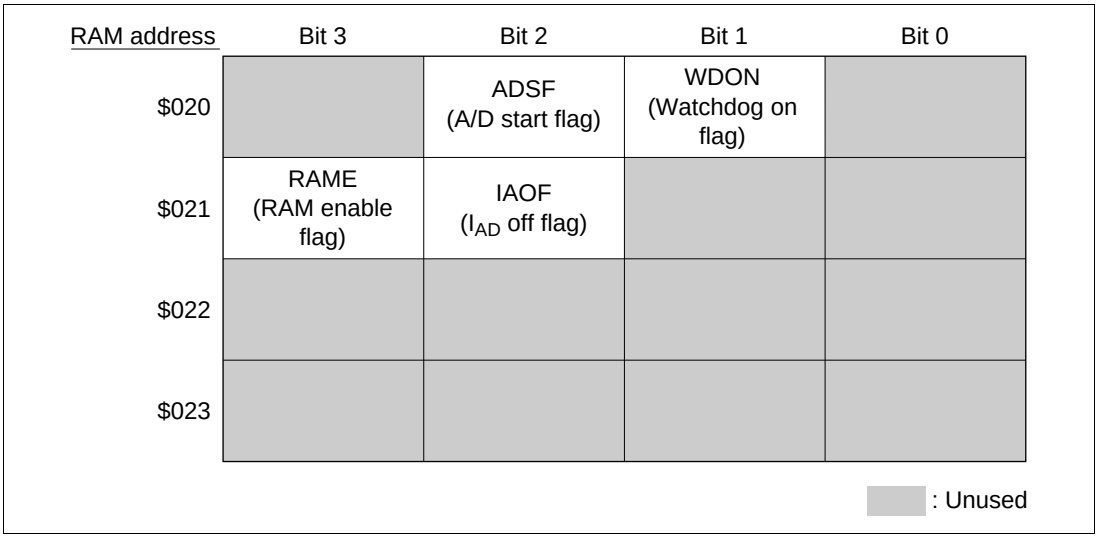


Figure 2-13 HD404344R and HD404394 Series Register Flag Area Configuration

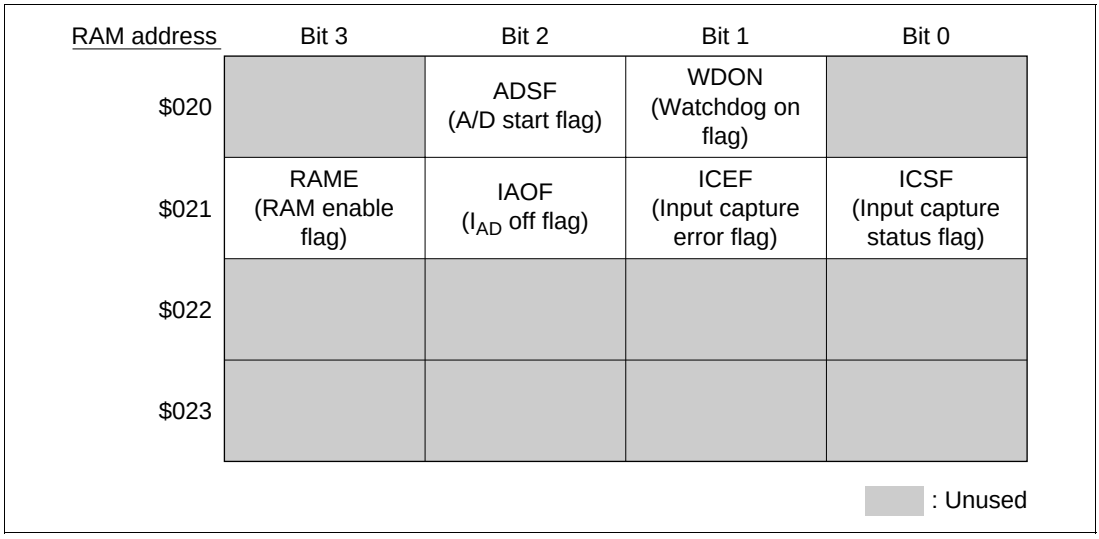


Figure 2-14 HD404318, HD404358 and HD404358R Series Register Flag Area Configuration

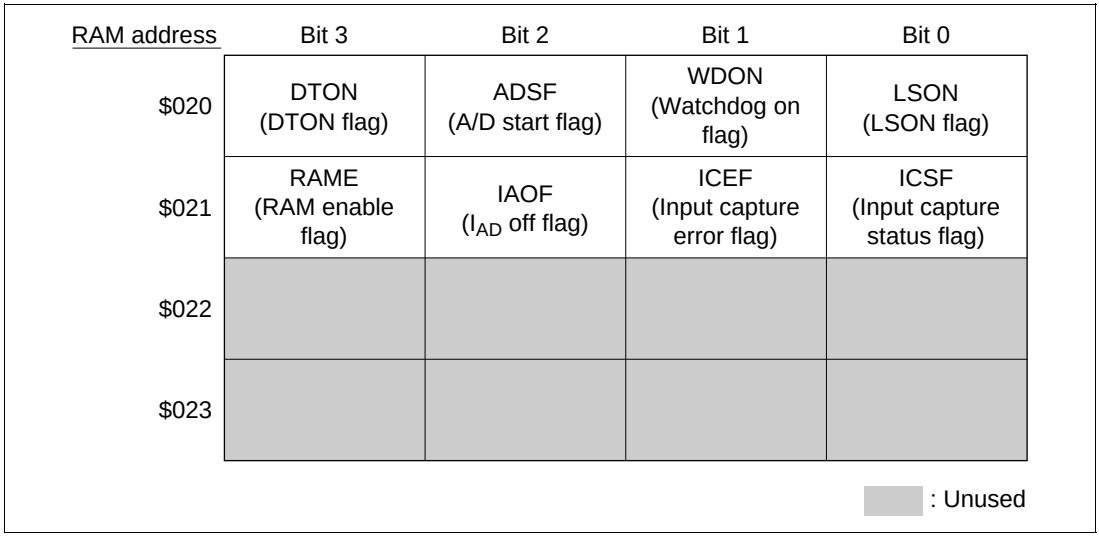


Figure 2-15 HD404339 and HD404369 Series Register Flag Area Configuration

Table 2-3 Register Flag Area Instruction Limitations

Bit	Instruction		
	SEM/SEMD Instruction	REM/REMD Instruction	TM/TMD Instruction*
IM	○	○	○
LSON			
IAOF			
IF	△	○	○
ICSF			
ICEF			
RAME			
RSP	△	○	X
WDON	○		X
ADSF	○	X	○
DTON	△ (active mode)	○	○
	○ (subactive mode)		
Unused	△	△	X

Symbols

○ : Allowed

△ : The instruction will not be executed.

X : Unused

DTON: Direct transfer on flag

IF : Interrupt request flag

IM : Interrupt mask

Note: * The microcomputer status is undefined if a TM or TMD instruction is executed for a nonexistent bit or for an unused bit.

2.3.2 Memory Register Area

The memory register (MR) area is allocated to RAM addresses $040 to $04F. Figure 2-16 shows the structure of the MR area. This area consists of 16 memory registers, and is a data area that can be accessed by the LAMR and XMRA register to register instructions in addition to the usual RAM access instructions.

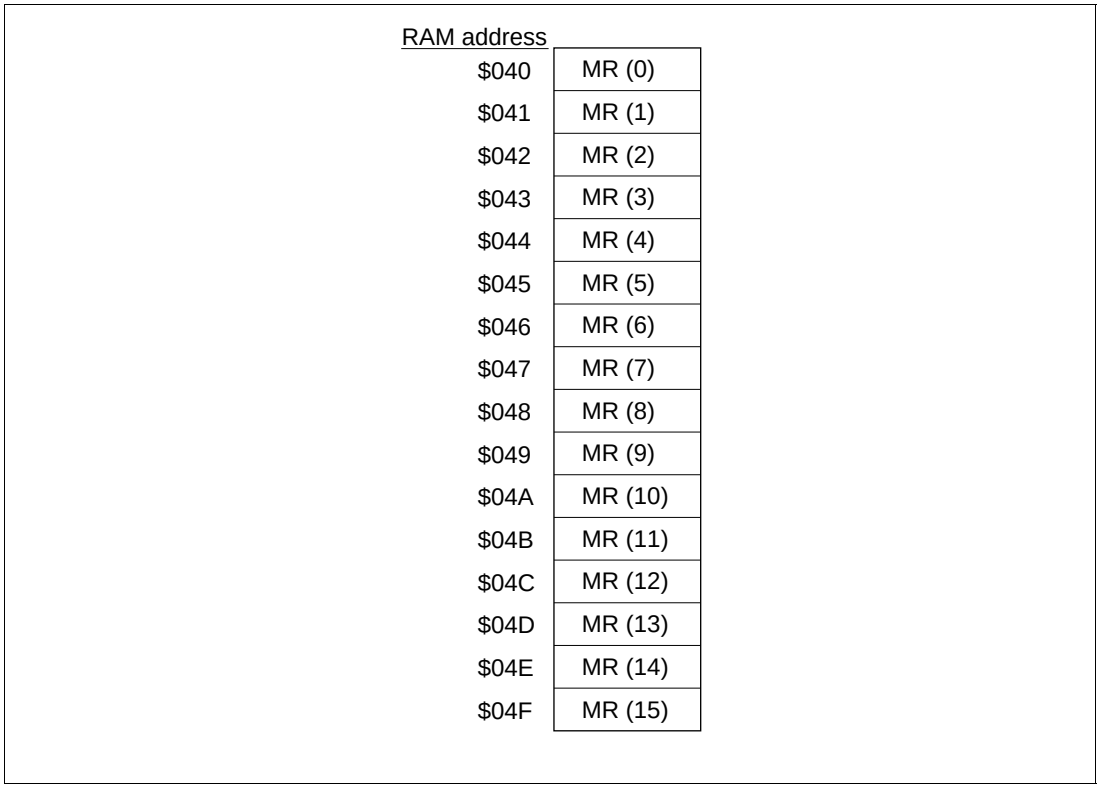


Figure 2-16 Memory Register Area Structure

2.3.3 Data Area

The data area is allocated to the whole of RAM. Note that the size differs between products. Table 2-4 shows the structure of the data areas in the different products in the HMCS43XX Family.

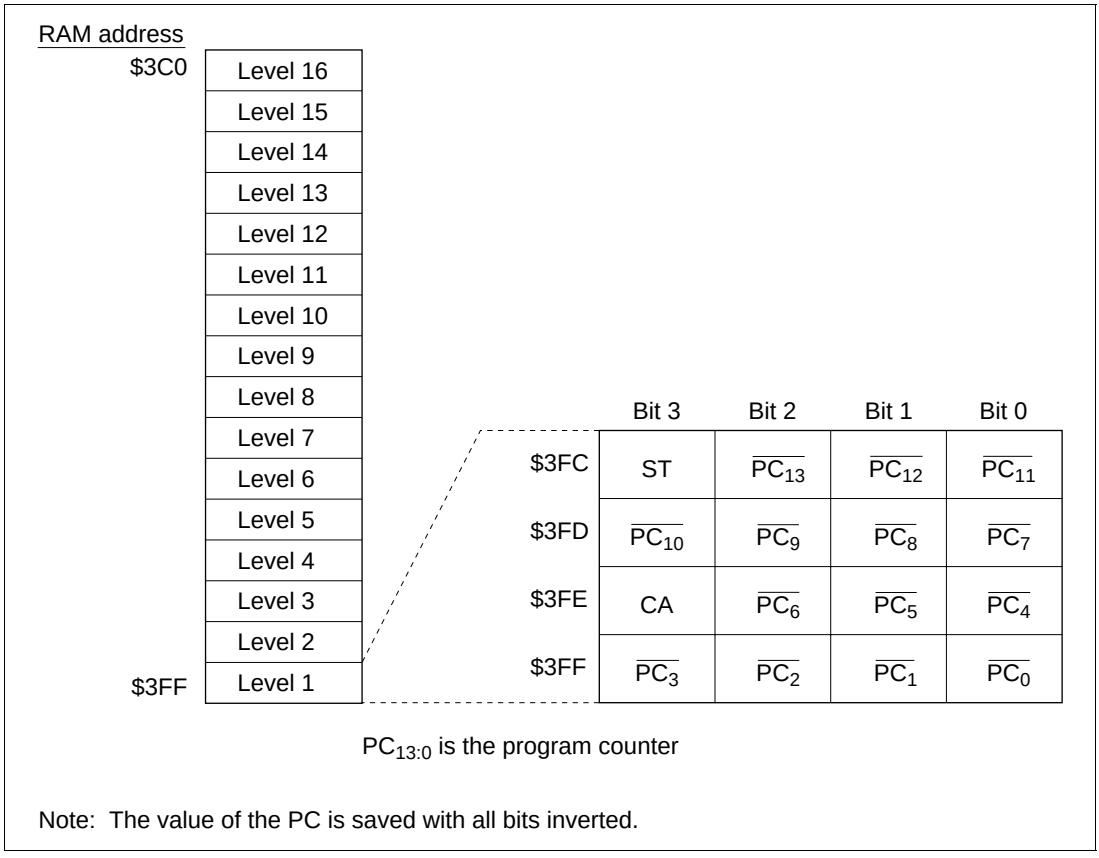
Table 2-4 Data Area Structure

Series	Product	RAM Addresses	Capacity (Digits)
HD404344R	All products	$050 to $0FF	176
HD404394			
HD404318	All products	$050 to $17F	304
HD404358	HD404354/HD40A4354 HD404356/HD40A4356 HD404358/HD40A4358	$050 to $17F	304
	HD407A4359	$050 to $1FF	432
HD404358R	All products	$050 to $1FF	432
HD404339	All products	$050 to $1FF	432
HD404369	All products	$050 to $1FF	432

2.3.4 Stack Area

The stack area is allocated to RAM addresses $3C0 to $3FF. Figure 2-17 shows the structure of the stack area. This area is used to save the program counter (PC), the status (ST), and the carry (CA) on a subroutine call (with the CAL or CALL instruction) or an interrupt. Since four digits are used for each level, up to 16 levels of subroutine calls can be used.

The saved value of the PC is restored by the RTN and RTNI instructions. The ST and CA are only restored by the RTNI instruction. That part of the stack area not used for subroutine calls or interrupts can be used as a data area.



Note: The value of the PC is saved with all bits inverted.

Figure 2-17 Stack Area Structure

Section 3 CPU

3.1 Overview

The HMCS400 CPU supports a concise and efficient instruction set in which all instructions are either one-word or two-word instructions, and all instructions are executed in one or two cycles, except for the return instruction, which requires 3 cycles.

3.1.1 Features

The HMCS400 CPU provides the following features.

- 101 instructions in ten classes
  - — Immediate instructions: 4
  - — Register to register instructions: 8
  - — RAM addressing instructions: 13
  - — RAM/register instructions: 10
  - — Arithmetic instructions: 25
  - — Comparison instructions: 12
  - — RAM bit manipulation instructions: 6
  - — ROM addressing instructions: 8
  - — I/O instructions: 11 (including the P instruction*)
  - — Control instructions: 4
- Three RAM addressing modes and four ROM addressing modes
  - — RAM addressing modes
    - – Register indirect addressing
    - – Direct addressing
    - – Memory register addressing
  - — ROM addressing modes
    - – Direct addressing
    - – Current page addressing
    - – Zero page addressing
    - – Table data addressing*

Note: * The P instruction is a special instruction that transfers the contents of ROM (8 bits) determined by the table data addressing mode to either the accumulator/B register pair or to the R1/R2 port data register pair.

- A 16,384 word ROM address space and a 1,024 digit RAM address space
- Instruction execution time: 1 µs (when f_{OSC} = 4 MHz)
- Low power modes
  The SBY and STOP instructions switch the HMCS400 CPU to a low power mode.

3.1.2 Address Space

The HMCS400 CPU address space consists of two independent address spaces: a ROM address space and a RAM address space. The ROM address space consists of word (10-bit) units with addresses in the range $0000 to $3FFF. The RAM address space consists of digit (4-bit) units with addresses in the range $000 to $3FF. See section 2, “Memory” for detailed information.

3.1.3 Register Organization

Figure 3-1 shows the organization of the HMCS400 CPU internal registers.

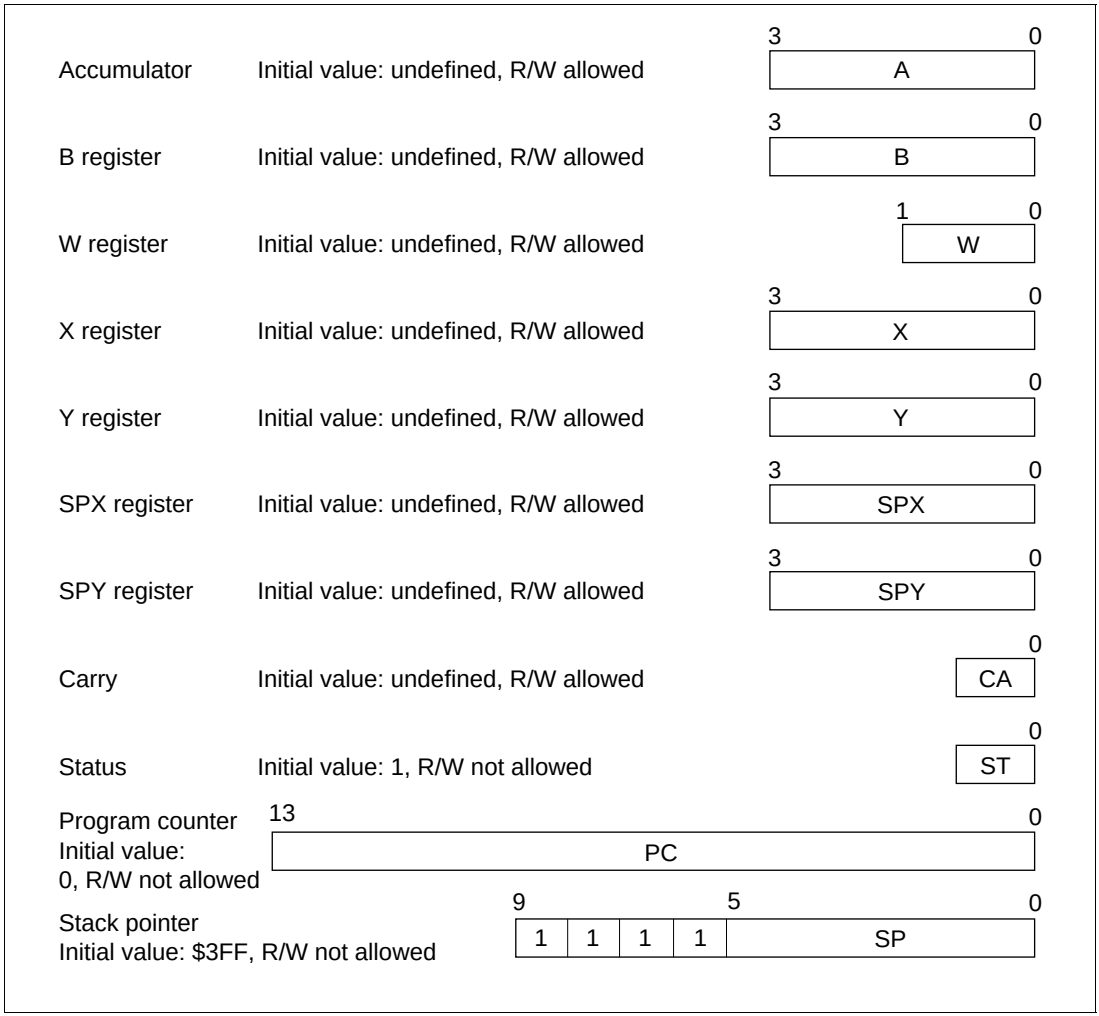


Figure 3-1 HMCS400 CPU Internal Register Organization

3.2 CPU Registers

3.2.1 Accumulator (A) and B Register (B)

The A and B registers are 4-bit registers that hold the results of ALU (arithmetic and logic unit) operations and transfer data with memory, I/O ports, and other registers.

3.2.2 W Register (W), X Register (X), and Y Register (Y)

The W register is a 2-bit register and the X and Y registers are 4-bit registers that are used in the RAM register indirect addressing mode. The Y register is also used for D port addressing.

3.2.3 SPX Register (SPX), SPY Register (SPY)

The SPX and SPY registers are 4-bit registers that are used as auxiliary registers for the X and Y registers.

3.2.4 Carry Flag (CA)

The CA flag is a 1-bit flag that holds the ALU overflow state when an arithmetic instruction is executed. When an overflow occurs CA is set to 1, and when no overflow occurs, it is cleared to 0. The CA flag is influenced by the SEC and REC carry set and reset instructions and by the ROTL and ROTR rotate with carry instructions.

During interrupt handling, the carry state is saved on the stack and restored by the RTNI instruction.

3.2.5 Status Flag (ST)

The ST flag is a 1-bit flag that holds the result of arithmetic instructions, comparison instructions, and bit test instructions. It is used as the condition for the BR, BRL, CAL, and CALL conditional branch instructions. The ST flag retains its value until another arithmetic, comparison, or bit test instruction is executed. The ST flag is set to 1 after a conditional branch instruction is executed, regardless of whether the branch condition holds or not.

During interrupt handling, the ST flag state is saved on the stack and restored by the RTNI instruction.

3.2.6 Program Counter (PC)

The PC is a 14-bit counter that holds the address in ROM of the next instruction that the CPU will execute.

3.2.7 Stack Pointer (SP)

The SP is a 10-bit register that points to the RAM address of the next empty slot in the stack area. The SP is initialized to $3FF by a reset. It is decremented by four each time data is saved when a subroutine is called or an interrupt is handled. It is incremented by four each time a return instruction is executed.

The top four bits of the SP are always 1111. Therefore, 16 levels is the maximum amount of stack that can be used.

In addition to the reset method described above, the stack pointer can also be reset to $3FF by clearing to 0 the reset stack pointer (RSP) bit in the interrupt control bit area with a RAM bit manipulation instruction (REM or REMD).

3.3 Addressing Modes

The HMCS400 CPU supports a total of seven addressing modes; three RAM addressing modes and four ROM addressing modes.

3.3.1 RAM Addressing Modes

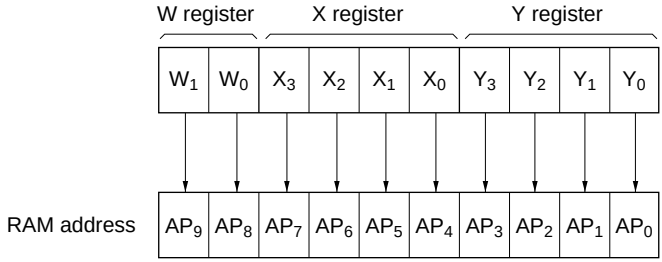
The HMCS400 CPU supports the three RAM addressing modes shown in figure 3-2.

(1) Register Indirect Addressing Mode: Register indirect addressing mode instructions consist of one word, and use the W, X, and Y registers to form a 10-bit RAM address. (See figure 3-2 (1).)

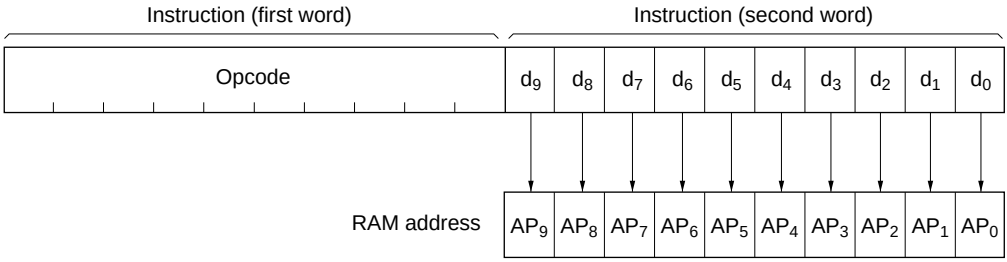
(2) Direct Addressing Mode: Direct addressing mode instructions consist of two words. The first word is the opcode and the second word specifies a 10-bit RAM address. (See figure 3-2 (2).)

(3) Memory Register Addressing Mode: Memory register addressing mode instructions consist of one word, in which the upper 6 bits specify the opcode and the lower 4 bits specify one of the memory registers 0 to 15. (See figure 3-2 (3).)

(1) Register Indirect Addressing



(2) Direct Addressing Mode



(3) Memory Register Addressing Mode

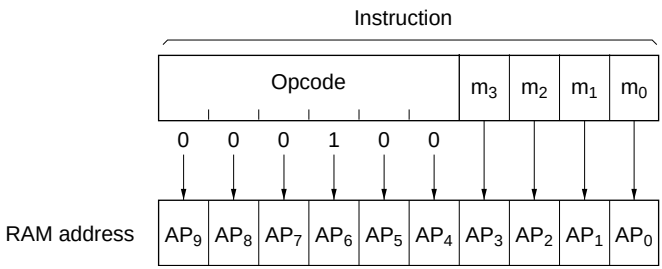


Figure 3-2 RAM Addressing Modes

3.3.2 ROM Addressing Modes and the P Instruction

The HMCS400 CPU supports the four ROM addressing modes shown in figure 3-3. The HMCS400 CPU also supports, as a special case, access to ROM data at addresses determined by table data addressing using the P instruction. (See figure 3-4.)

(1) Direct Addressing Mode: Direct addressing mode instructions consist of two words. The lower 4 bits of the first word and the 10 bits of the second word form a 14-bit ROM address. (See figure 3-3 (1).)

(2) Current Page Addressing Mode: The HMCS400 CPU ROM address space ($0000 to $3FFF) is divided into 256 word units, called pages. Thus the ROM address space is divided into 64 pages numbered page 0 to page 63.

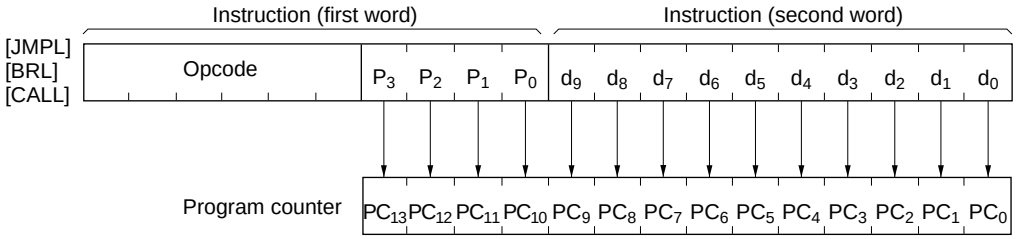
Current page addressing mode instructions consist of one word. The lower 8 bits, which follow the 2-bit opcode, specify a ROM address in the same page as the instruction itself. (See figure 3-3 (2).)

(3) Zero Page Addressing Mode: Zero page addressing mode instructions consist of one word. The lower 6 bits, which follow the 4-bit opcode, specify an address from $0000 to $003F in page zero. (See figure 3-3 (3).)

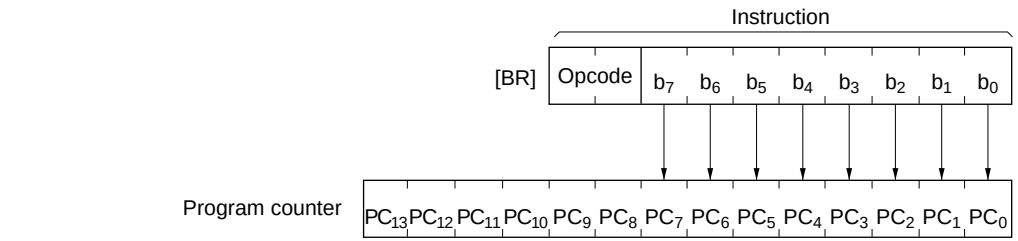
(4) Table Data Addressing Mode: Table data addressing mode instructions consist of one word. The lower 4 bits, which follow the 6-bit opcode, in conjunction with the contents of the accumulator (A) and the B register (B), form a 12-bit ROM address.

(5) P Instruction: The P instruction is used to access ROM data at an address determined by table data addressing. The upper two bits of the referenced ROM data are used to determine where the lower 8 bits will be transferred. If bit 8 is 1, the data is transferred to the A/B pair, if bit 9 is 1 the data is transferred to the R1/R2 port data register (PDR) pair. (See figure 3-4.) If both bits 8 and 9 are 1, the data is transferred to both the A/B pair and the R1/R2 port PDR pair. The PC is not influenced by the execution of a P instruction.

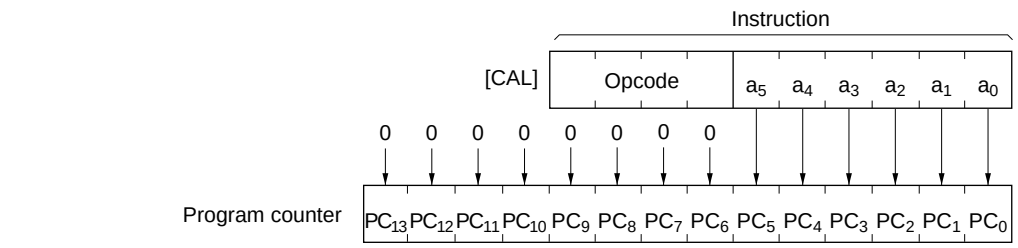
(1) Direct Addressing Mode



(2) Current Page Addressing Mode



(3) Zero page addressing mode



(4) Table Data Addressing Mode

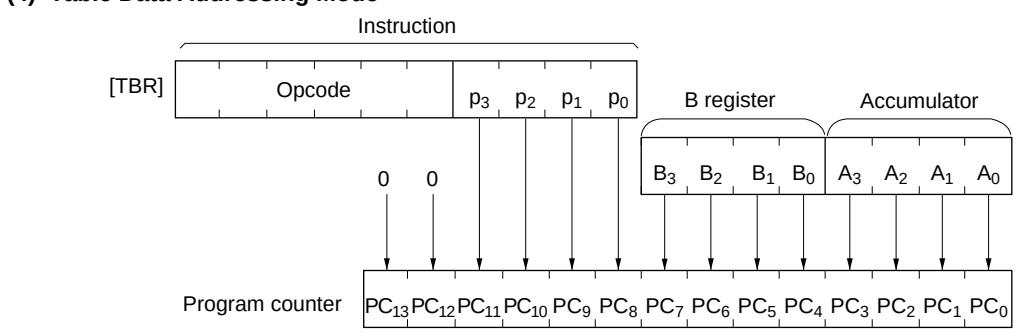
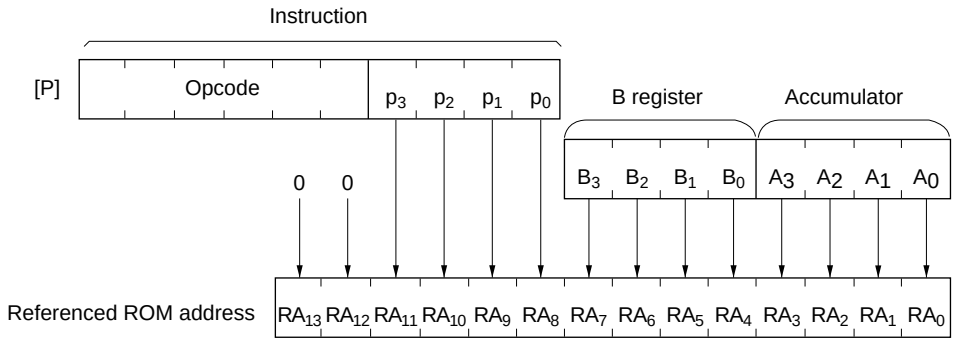


Figure 3-3 ROM Addressing Modes

(1) Address Specification



(2) Pattern Output

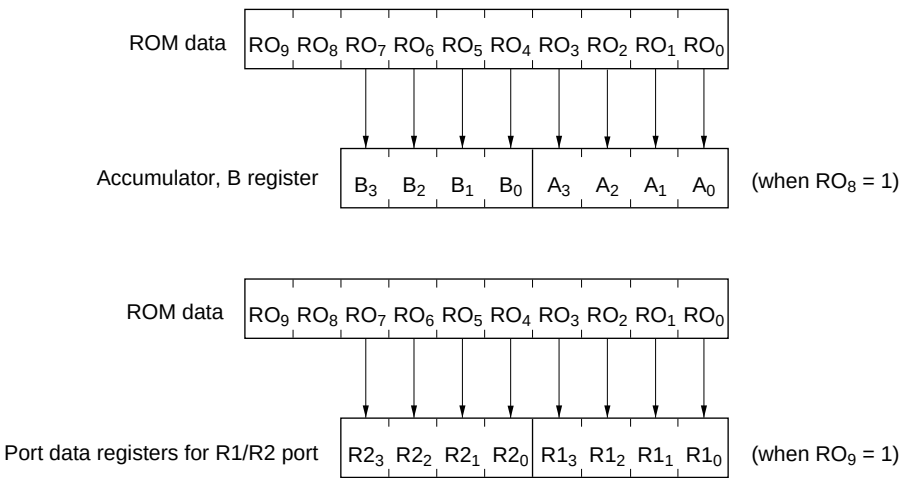


Figure 3-4 ROM Data Reference Using the P Instruction

3.4 Processing States

3.4.1 Overview

The HMCS400 CPU has three processing states: the program execution state, the exception handling state, and the program stopped state. Figure 3-5 shows a classification of the processing states and figure 3-6 shows the state transition diagram for these states.

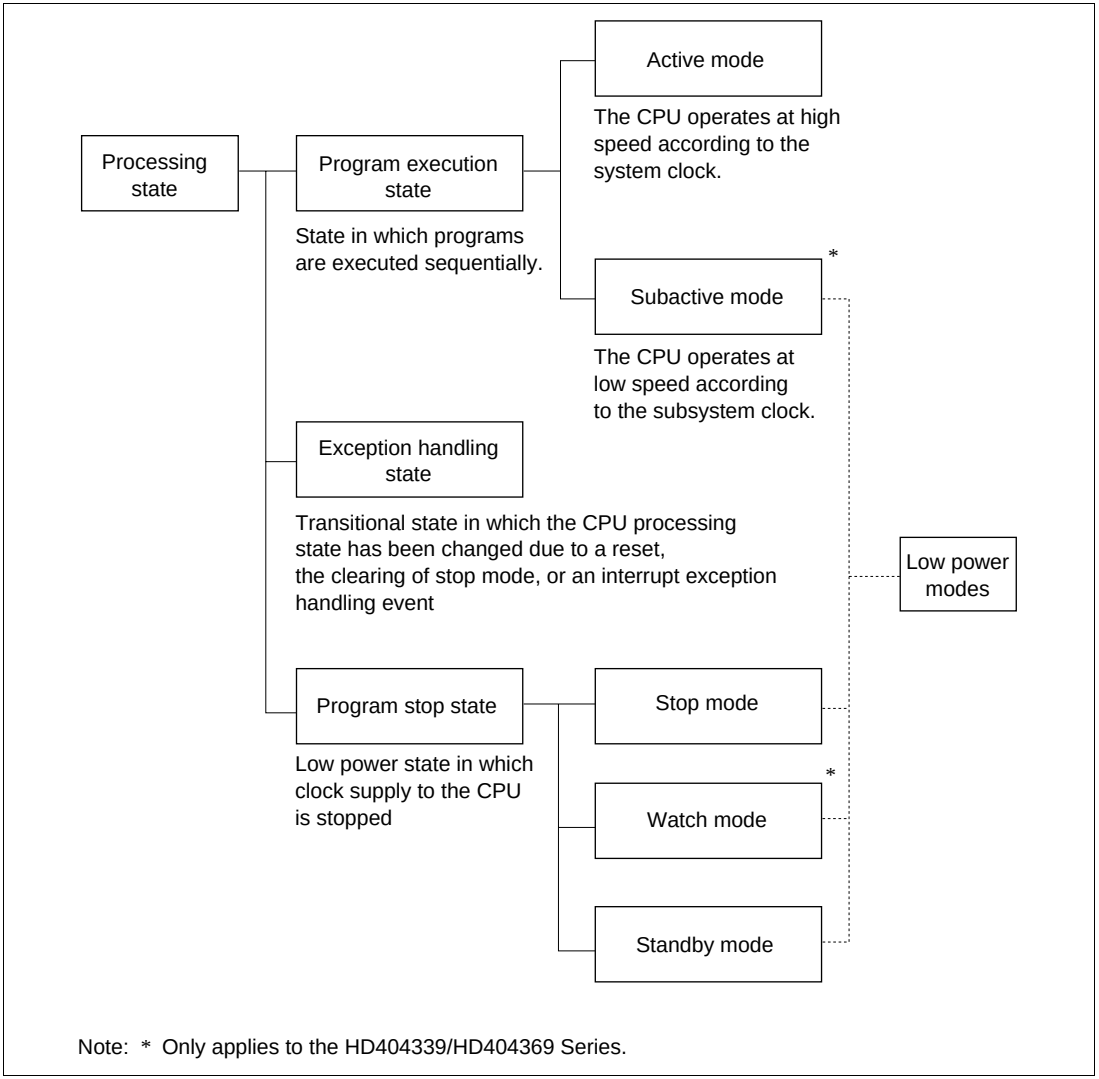


Figure 3-5 Processing State Classification

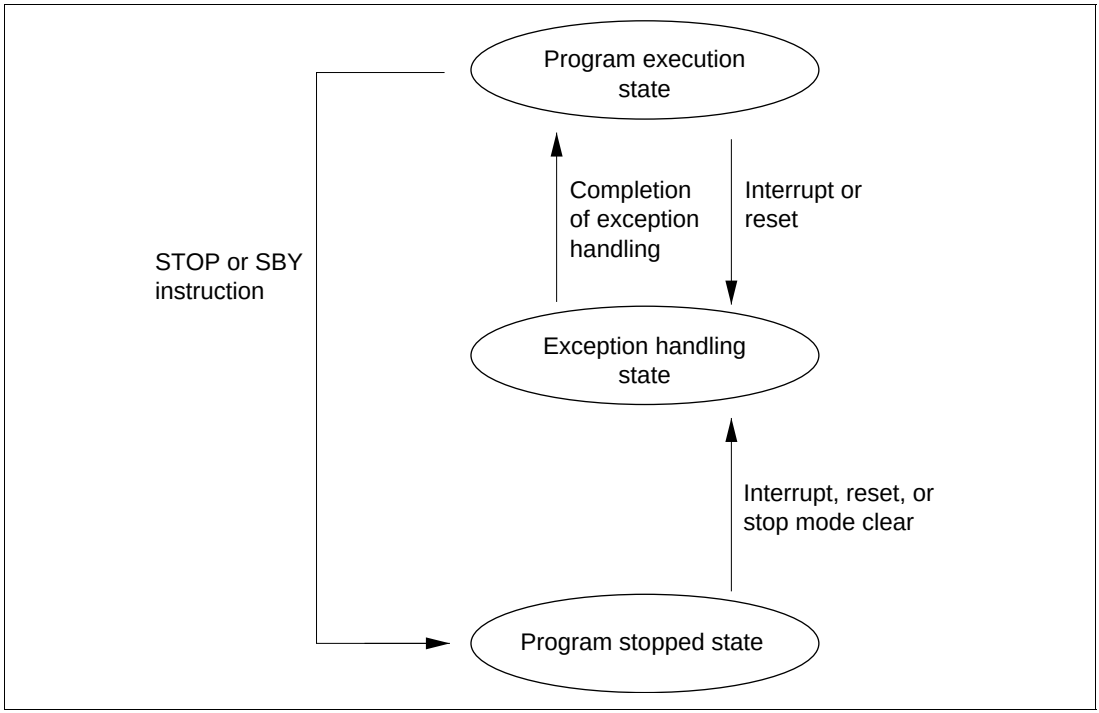


Figure 3-6 State Transition Diagram

3.4.2 Program Execution State

In the program execution state, the HMCS400 CPU executes programs sequentially. The program execution state has two modes: active mode and subactive mode.

(1) Active Mode: In active mode, the HMCS400 CPU operates at high speed on the system clock.

(2) Subactive Mode (HD404339/HD404369 Series Products Only): In subactive mode, the HMCS400 CPU operates at low speed from the subsystem clock. This provides low power operation.

The HMCS400 CPU switches to subactive mode when an $\overline{INT}_0$ or timer A interrupt occurs in watch mode when the LSON bit in the register flag area is 1.

Although the system clock oscillator stops, the CPU, built-in peripheral modules, and the I/O ports operate from the subsystem clock. However, A/D converter operation stops.

Refer to sections 5 and 6, “Low Power Modes”, for details on the low power states.

3.4.3 Exception Handling State

The exception handling state is the transitional state in which the HMCS400 CPU normal processing flow has changed due to a reset, the clearing of stop mode, or an interrupt. In interrupt exception handling, the program counter (PC), carry (CA), and status (ST) are saved on the stack. Refer to section 4, “Exception Handling”, for details on exception handling.

3.4.4 Program Stopped State

The program stopped state has three modes: stop mode, watch mode, and standby modes. These modes realize low power states.

(1) Stop Mode: Stop mode is entered when a STOP instruction is executed in active mode when the TMA3 bit in timer mode register A (TMA) is set to 0.

The system clock oscillator stops and the CPU, peripheral functions, and I/O ports go to the reset state. The contents of RAM will be maintained as long as the stipulated voltage is applied.

The transition to stop mode must be made from active mode.

(2) Watch Mode (HD404339/HD404369 Series Products Only): Watch mode is entered in the following two cases:

- A STOP instruction is executed in active mode with the TMA3 bit in timer mode register A (TMA) set to 1, or
- Either a STOP or SBY instruction is executed in subactive mode with either the LSON flag set to 1 (and the DTON flag either 0 or 1) or both the LSON flag set to 0 and the DTON flag set to 0.

The system clock oscillator stops but the subsystem clock oscillator continues to operate. Although the CPU and the built-in peripheral modules stop, the contents of RAM, the CPU registers, and the peripheral function registers are maintained as long as the stipulated voltage is applied. The I/O port states are also maintained. However, note that of the built-in peripheral modules, timer A continues to operate.

(3) Standby Mode: Standby mode is entered when an SBY instruction is executed. (active mode → standby mode)

Although operating clock supply to the CPU is stopped and the CPU stops, the built-in peripheral functions continue to operate. The contents of the CPU registers and RAM and the I/O port states are maintained.

Section 4 Exception Handling

4.1 Overview

The HMCS400 CPU recognizes three types of exception factors: reset, stop mode clear, and interrupts. Table 4-1 lists the types of exception handling and their priorities.

Table 4-1 Exceptions Their Priorities

Priority	Exception Factor	Exception Handling Initiation Timing
High	Reset	There are two reset exception factors: • $\overline{\text{RESET}}$ pin input When the $\overline{\text{RESET}}$ pin goes low the system enters the reset state and exception handling starts immediately. • Watchdog timer overflow When the watchdog timer overflows the system enters the reset state and exception handling starts immediately.
	Stop mode clear	There are two stop mode clear exception factors: • $\overline{\text{RESET}}$ pin input Stop mode is cleared when the $\overline{\text{RESET}}$ pin goes low. The system enters the reset state and exception handling starts immediately. • $\overline{\text{STOPC}}$ pin input Stop mode is cleared when the $\overline{\text{STOPC}}$ pin goes low. The system enters the reset state and exception handling starts immediately.
Low	Interrupts	When an interrupt request occurs exception handling starts at the completion of the current instruction or at the completion of the current exception handling.

4.2 Reset

4.2.1 Overview

Reset is the highest priority exception. There are two factors that initiate reset exception handling as follows.

(1) $\overline{\text{RESET}}$ Pin Input: When the $\overline{\text{RESET}}$ pin goes low all processing is discontinued and the system goes to the reset state. A reset causes the CPU internal registers and the built-in peripheral module registers to be initialized, and then reset exception handling starts immediately.

(2) Watchdog Timer Overflow: When timer C is used as a watchdog timer, the system enters the reset state when timer C overflows. After performing the same operations as performed in response to a $\overline{\text{RESET}}$ pin input, reset exception handling starts immediately.

4.2.2 Reset Sequence

When a reset exception factor occurs the system enters the reset state.

To reliably reset the system when the system clock oscillator is stopped (including the state immediately following power on), the $\overline{\text{RESET}}$ pin must be held low for at least the duration of the oscillator stabilization period, i.e., tRC. Similarly, when stop mode is cleared by a $\overline{\text{STOPC}}$ pin input, the $\overline{\text{STOPC}}$ pin must be held low for at least tRC.

Also, when resetting during normal operation, the $\overline{\text{RESET}}$ pin must be held low for at least two instruction cycles.

When a reset exception factor occurs, the system operates as follows.

Note: Refer to section 25, “Electrical Characteristics”, for detailed information on tRC.

1. When reset exception handling starts due to either a $\overline{\text{RESET}}$ pin input or a watchdog timer overflow, the RAM enable flag (RAME) in the register flag area is cleared to 0.

2. The CPU internal states and the built-in peripheral module registers are initialized. The interrupt enable flag (IE) is cleared to 0 disabling all interrupts. Refer to section 4.4, “Initial Values of Registers and Flags at Reset and Stop Mode Clear”, for the initial values of the registers.

3. The vector address $0000 is loaded into the PC. Therefore, the CPU will branch to the reset handling routine if a JMPL instruction to that routine is stored in locations $0000 and $0001. The $\overline{\text{RESET}}$ pin input is an asynchronous input; that is, whatever state the system is in, it will always goes to the reset state when the $\overline{\text{RESET}}$ pin goes low.

4.3 Stop Mode Clear

4.3.1 Overview

The exception factors that clear stop mode are input to the $\overline{\text{STOPC}}$ pin and input to the $\overline{\text{RESET}}$ pin when the system is in stop mode. This exception factor causes stop mode to be cleared and the system to be reset.

4.3.2 Stop Mode Clear Sequence ($\overline{\text{RESET}}$ Pin Input)

When the $\overline{\text{RESET}}$ pin goes low with the system in stop mode, stop mode is cleared and the system enters the reset state. To reliably clear stop mode, the $\overline{\text{RESET}}$ pin must be held low for at least tRC.

4.3.3 Stop Mode Clear Sequence ($\overline{\text{STOPC}}$ Pin Input)

When the $\overline{\text{STOPC}}$ pin goes low with the system in stop mode, stop mode is cleared and the system enters the reset state. To reliably clear stop mode, the $\overline{\text{STOPC}}$ pin must be held low for at least tRC.

Except for setting the RAM enable flag to 1 and retaining the values of the PMRB3 bit in port mode register B (PMRB) and the SSR13 bit in system clock selection register 1 (SSR1)*, operation is identical to reset exception handling.

Note: * Applies only to the HD404339 and HD404369 Series.

4.4 Initial Values of Registers and Flags on Reset and Stop Mode Clear

Table 4-2 lists the values of registers and flags on reset and when stop mode is cleared.

Table 4-2 (1) Initial Values of Registers and Flags on Reset and Stop Mode Clear

Item			Initial Value		
			HD404344R and HD404394 Series	HD404318, HD404358 and HD404358R Series	HD404339 and HD404369 Series
Program counter		(PC)	$0000	$0000	$0000
Status		(ST)	1	1	1
Stack pointer		(SP)	$3FF	$3FF	$3FF
Interrupt flags and masks	Interrupt enable flag	(IE)	0	0	0
	Interrupt request flag	(IF)	0	0	0
	Interrupt mask	(IM)	1	1	1
I/O	High voltage pin port data register	(PDR)	All bits 0	All bits 0	All bits 0
	Medium/standard voltage port data register	(PDR)	All bits 1	All bits 1	All bits 1
	Data control register	(DCR)	All bits 0	All bits 0	All bits 0
	Port mode register A	(PMRA)	-000	0000	0000
	Port mode register B	(PMRB)	0--0	0000	0000
	Port mode register C	(RMRC)	--00	0000	0000
Timer and serial interface	Timer mode register A	(TMA)		-000	0000
	Timer mode register B1	(TMB1)	0000	0000	0000
	Timer mode register B2	(TMB2)	--00	-000	-000
	Timer mode register C	(TMC)	0000	0000	0000
	Serial mode register	(SMR)	0000	0000	0000
	Prescaler S	(PSS)	$000	$000	$000
	Prescaler W	(PSW)			$00
	Timer counter A	(TCA)		$00	$00
	Timer counter B	(TCB)	$00	$00	$00
	Timer counter C	(TCC)	$00	$00	$00

Note: "X" indicates undefined bits, and "-" indicates nonexistent bits. Shaded areas indicate that the corresponding register does not exist.

Table 4-2 (1) Initial Values of Registers and Flags on Reset and Stop Mode Clear (cont)

Item			Initial Value		
			HD404344R and HD404394 Series	HD404318, HD404358 and HD404358R Series	HD404339 and HD404369 Series
Timer and serial interface	Timer write register B	(TWBU, L)	$X0	$X0	$X0
	Timer write register C	(TWCU, L)	$X0	$X0	$X0
	Octal counter	(OC)	000	000	000
A/D converter	A/D mode register 1	(AMR1)	0000/000-	0000	0000
	A/D mode register 2	(AMR2)	---0	--00	-000
	A/D channel register	(ACR)	0000	0000	0000
	A/D data register	(ADRU, L)	$80	$80	$80
Bit registers	Low speed on flag	(LSON)			0
	Direct transfer on flag	(DTON)			0
	Watchdog timer on flag	(WDON)	0	0	0
	A/D start flag	(ADSF)	0	0	0
	Input capture status flag	(ICSF)		0	0
	Input capture error flag	(ICEF)		0	0
	IAD off flag	(IAOF)	0	0	0
Others	Miscellaneous register	(MIS)	00--	00--	0000
	System clock selection register 1, bits 2 to 0	(SSR1)			000
	System clock selection register 2	(SSR2)			--00

Note: “X” indicates undefined bits, and “-” indicates nonexistent bits. Shaded areas indicate that the corresponding register does not exist.

Table 4-2 (2) lists the states of the registers and flags not listed in table 4-2 (1).

Table 4-2 (2) Initial Values of Registers and Flags on Reset and Stop Mode Clear

		Stop Mode Cleared by $\overline{\text{STOPC}}$ Pin Input	After Other System Resets
Carry	(CA)	The values directly preceding the system reset are not retained. These must be initialized by the user program.	The values directly preceding the system reset are not retained. These must be initialized by the user program.
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX registers	(X/SPX)		
Y/SPY registers	(Y/SPY)		
Serial data register	(SRU, L)		
RAM		The values immediately prior to the point stop mode was entered are retained.	
Port mode register B, bit 3	(PMRB3)	The values immediately prior to the point stop mode was entered are retained.	
System clock selection register 1, bit 3	(SSR13)		
RAM enable flag	(RAME)	1	0

4.5 Interrupts

4.5.1 Overview

There are two classes of sources that can initiate interrupt handling: external interrupts ($\overline{INT_0}$ and $\overline{INT_1}$) and requests from built-in peripheral modules. Independent vector addresses are allocated to each of these interrupts. Table 4-3 lists the interrupts, their priorities, and their vector addresses. When multiple interrupts occur at the same time, the interrupt with the highest priority is processed.

Table 4-3 Interrupts

Interrupt			
HD404344R and HD404394 Series	**HD404318, HD404358, HD404358R, HD404339, and HD404369 Series**	**Vector Address**	**Priority**
$\overline{INT_0}$	$\overline{INT_0}$	$0002	High
—*	$\overline{INT_1}$	$0004	
—*	Timer A	$0006	
Timer B	Timer B	$0008	
Timer C	Timer C	$000A	
A/D converter	A/D converter	$000C	
Serial interface	Serial interface	$000E	Low

Note: * Vector addresses $0004 to $0007 are not used in the HD404344R and HD404394 Series.

These interrupts have the following features.

- All external and internal interrupts are controlled by the interrupt enable flag (IE). That is, no interrupts are accepted when the IE bit is cleared to 0.
- The $\overline{INT_0}$ and $\overline{INT_1}$ pin input interrupts are falling edge detection external interrupts.

4.5.2 Interrupt Registers and Flags

Table 4-4 lists the registers and flags that control interrupts. Note that the control bits in the interrupt control bit area can only be manipulated with the RAM bit manipulation instructions.

Table 4-4 Interrupt Control Registers

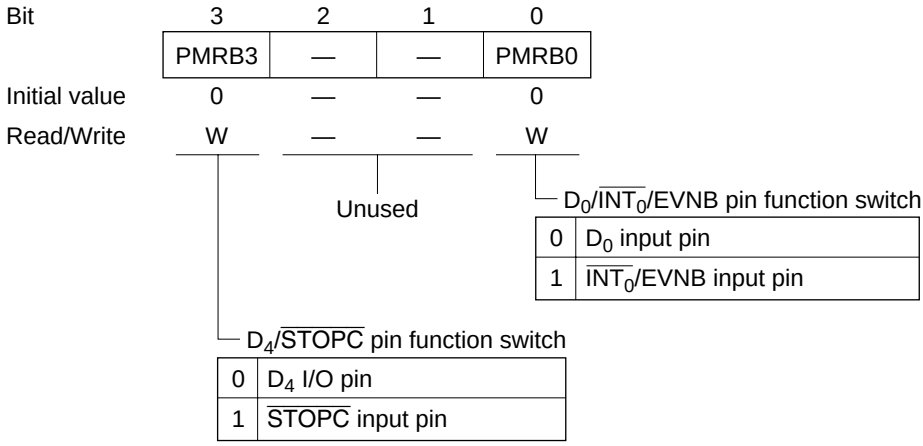
Address	Register		Abbreviation	R/W	Initial Value
$024	Port mode register B		PMRB	W	$0
$000, 0	Interrupt enable flag		IE	R/W	0
$000, 1	Reset SP bit	Interrupt control bit area	RSP	(W)	Undefined
$000, 2	External interrupt 0 request flag		IF0	R/(W)	0
$000, 3	External interrupt mask		IM0	R/W	1
$001, 0	External interrupt 1 request flag*		IF1	R/(W)	0
$001, 1	External interrupt 1 mask*		IM1	R/W	1
$001, 2	Timer A interrupt request flag*		IFTA	R/(W)	0
$001, 3	Timer A interrupt mask*		IMTA	R/W	1
$002, 0	Timer B interrupt request flag		IFTB	R/(W)	0
$002, 1	Timer B interrupt mask		IMTB	R/W	1
$002, 2	Timer C interrupt request flag		IFTC	R/(W)	0
$002, 3	Timer C interrupt mask		IMTC	R/W	1
$003, 0	A/D interrupt request flag		IFAD	R/(W)	0
$003, 1	A/D interrupt mask		IMAD	R/W	1
$003, 2	Serial interrupt request flag		IFS	R/(W)	0
$003, 3	Serial interrupt mask		IMS	R/W	1

"(W)" indicates that only a write of 0 to clear the flag is possible.

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. These flags cannot be used in the HD404344R and HD404394 Series.

(1) Port Mode Register B (PMRB: $024): PMRB is a 4-bit write-only register that switches the D port I/O pin shared functions.

HD404344R and HD404394 Series



Bit 3—D_4/$\overline{\text{STOPC}}$ Pin Function Switch (PMRB3): Selects whether the D_4/$\overline{\text{STOPC}}$ pin is used as the D_4 I/O pin or as the $\overline{\text{STOPC}}$ input pin.

The PMRB3 bit is cleared to 0 on reset. In stop mode, the value of the PMRB3 bit immediately prior to entering stop mode is retained.

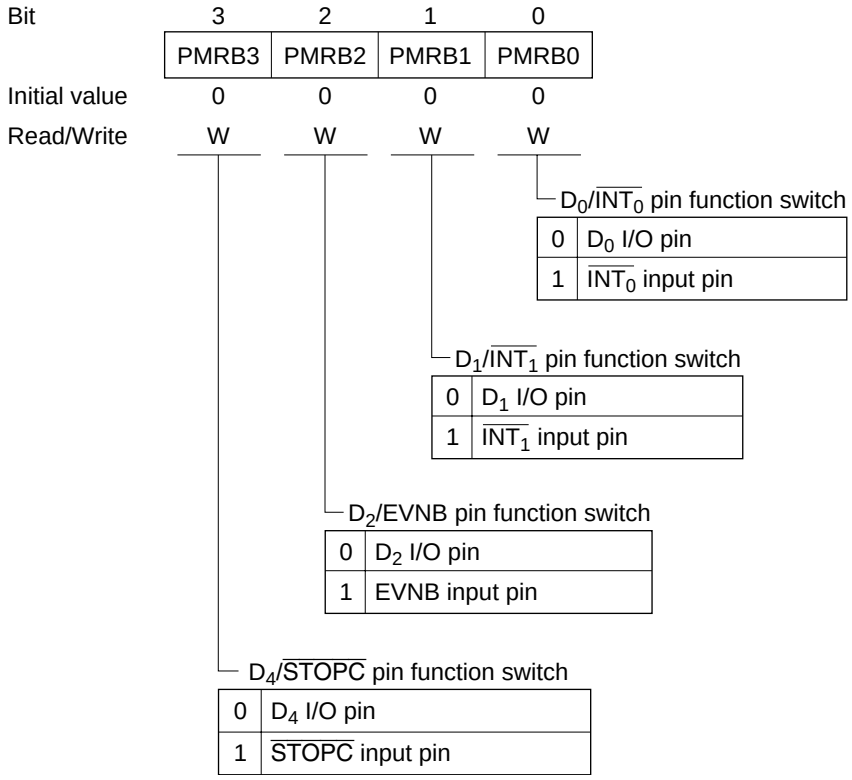
PMRB3	Description	
0	The D_4/$\overline{\text{STOPC}}$ pin functions as the D_4 I/O pin.	(initial value)
1	The D_4/$\overline{\text{STOPC}}$ pin functions as the $\overline{\text{STOPC}}$ input pin.	

Bit 0—D_0/$\overline{\text{INT}_0}$/EVNB Pin Function Switch (PMRB0): Selects whether the D_0 /$\overline{\text{INT}_0}$ /EVNB pin is used as the D_0 I/O pin or as the $\overline{\text{INT}_0}$ /EVNB input pin.

Refer to section 18.2.2, “Timer Mode Register B2 (TMB2)”, for details on switching between the $\overline{\text{INT}_0}$ and EVNB functions.

The PMRB0 bit is cleared to 0 on reset and in stop mode.

PMRB0	Description	
0	The D_0/$\overline{\text{INT}_0}$/EVNB pin functions as the D_0 I/O pin.	(initial value)
1	The D_0/$\overline{\text{INT}_0}$/EVNB pin functions as the $\overline{\text{INT}_0}$/EVNB input pin.	



Bit 3—$D_4/\overline{STOPC}$ Pin Function Switch (PMRB3): Selects whether the $D_4/\overline{STOPC}$ pin is used as the D_4 I/O pin or as the $\overline{STOPC}$ input pin.

The PMRB3 bit is cleared to 0 on reset. In stop mode, the value of the PMRB3 bit immediately prior to entering stop mode is retained.

PMRB3	Description	
0	The $D_4/\overline{STOPC}$ pin functions as the D_4 I/O pin.	(initial value)
1	The $D_4/\overline{STOPC}$ pin functions as the $\overline{STOPC}$ input pin.	

Bit 2—D_2/EVNB Pin Function Switch (PMRB2): Selects whether the D_2/EVNB pin is used as the D_2 I/O pin or as the EVNB input pin.

The PMRB2 bit is cleared to 0 on reset.

PMRB2	Description	
0	The D_2/EVNB pin functions as the D_2 I/O pin.	(initial value)
1	The D_2/EVNB pin functions as the EVNB input pin.	

Bit 1—$D_1/\overline{INT}_1$ Pin Function Switch (PMRB1): Selects whether the $D_1/\overline{INT}_1$ pin is used as the D_1 I/O pin or as the $\overline{INT}_1$ input pin.

The PMRB1 bit is cleared to 0 on reset and in stop mode.

PMRB1	Description	
0	The $D_1/\overline{INT}_1$ pin functions as the D_1 I/O pin.	(initial value)
1	The $D_1/\overline{INT}_1$ pin functions as the $\overline{INT}_1$ input pin.	

Bit 0—$D_0/\overline{INT}_0$ Pin Function Switch (PMRB0): Selects whether the $D_0/\overline{INT}_0$ pin is used as the D_0 I/O pin or as the $\overline{INT}_0$ input pin.

The PMRB0 bit is cleared to 0 on reset and in stop mode.

PMRB0	Description	
0	The $D_0/\overline{INT}_0$ pin functions as the D_0 I/O pin.	(initial value)
1	The $D_0/\overline{INT}_0$ pin functions as the $\overline{INT}_0$ input pin.	

(2) Interrupt Enable Flag (IE: $000, 0): The IE flag controls whether the CPU will accept interrupts for all interrupt request types. The IE flag is cleared to 0 by the hardware when an interrupt is accepted and is set to 1 when an RTNI instruction is executed.

This flag can be read and written by the bit manipulation instructions.

This flag is cleared to 0 on reset and in stop mode.

IE	Description	
0	The CPU disables all interrupts.	(initial value)
1	The CPU accepts interrupts.	

(3) External Interrupt 0 and 1 Request Flags (IF0: $000, 2 , IF1: $001, 0*): IF0 and IF1 are flags that reflect whether an interrupt request is outstanding on the corresponding $\overline{INT}_0$ and $\overline{INT}_1$ external interrupt pin. When the specified input edge is detected on an external interrupt pin, the corresponding external interrupt request flag is set to 1.

Only falling edges are detected on the $\overline{INT}_0$ and $\overline{INT}_1$ pins.

The IF0 and IF1 flags can be read and written only by the bit manipulation instructions. However, note that only a 0 may be written.

IF0 and IF1 are never cleared automatically, even when an interrupt is received. They must be cleared to 0 by the software.

These flags are cleared to 0 on reset and in stop mode.

IF0, IF1*	Description
0	Indicates that no interrupt has been requested on the corresponding $\overline{INT}_0$ or $\overline{INT}_1$. (initial value)
1	Indicates that an interrupt has been requested on the corresponding $\overline{INT}_0$ or $\overline{INT}_1$.

Note: * The external interrupt 1 request flag (IF1) applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. Since there is no $\overline{INT}_1$ pin in HD404344R and HD404394 Series products, the IF1 flag cannot be used in those products.

(4) External Interrupt 0 and 1 Masks (IM0: $000, 3, IM1: $001, 1*): IM0 and IM1 are bits that mask the corresponding IF0 and IF1 flags. The CPU will accept an external interrupt when IF0 or IF1 is set to 1 only if the corresponding IM0 or IM1 is cleared to 0 and IE is 1.

The CPU will not receive an interrupt request from IF0 or IF1 if the corresponding IM0 or IM1 is set to 1. That is, the interrupt will be deferred.

IM0 and IM1 can be read and written only by the bit manipulation instructions.

These masks are set to 1 on reset and in stop mode.

IM0, IM1*	Description
0	IF0 or IF1 is enabled.
1	IF0 or IF1 is masked. The interrupt will be deferred even if either IF0 or IF1 is set to 1. (initial value)

Note: * The external interrupt 1 mask (IM1) applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. Since there is no $\overline{INT}_1$ pin in HD404344R and HD404394 Series products, the IM1 mask cannot be used in those products.

(5) Timer A to C Interrupt Request Flags (IFTA: $001, 2*, IFTB: $002, 0, IFTC: $002, 2): IFTA to IFTC are flags that reflect whether an interrupt request is outstanding from the corresponding timer A to C. When one of timers A to C overflows, the corresponding interrupt request flag (IFTA to IFTC) is set to 1.

IFTA to IFTC can be read and written only by the bit manipulation instructions.

However, note that only a 0 may be written.

IFTA to IFTC are never cleared automatically, even when an interrupt is received. They must be cleared to 0 by the software.

These flags are cleared to 0 on reset and in stop mode.

IFTA* to IFTC	Description
0	Indicates that no interrupt has been requested by the corresponding timer A to C. (initial value)
1	Indicates that an interrupt has been requested by the corresponding timer A to C.

Note: * The timer A interrupt request flag (IFTA) applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. Since there is no timer A in HD404344R and HD404394 Series products, the IFTA flag cannot be used in those products.

(6) Timer A to C Interrupt Masks (IMTA: $001, 3*, IMTB: $002, 1, IMTC: 002, 3): IMTA to IMTC are bits that mask the corresponding IFTA to IFTC flags. The CPU will accept a timer interrupt when one of IFTA to IFTC is set to 1 only if the corresponding IMTA to IMTC is cleared to 0 and IE is 1.

if IMTA to IMTC is set to 1, even if the corresponding IFTA or IFTC is set to 1. That is, the interrupt will be deferred.

IMTA to IMTC can be read and written only by the bit manipulation instructions.

These masks are set to 1 on reset and in stop mode.

IMTA* to IMTC	Description
0	IFTA to IFTC are enabled.
1	IFTA to IFTC are masked. The interrupt will be deferred even if any of IFTA to IFTC are set to 1. (initial value)

Note: * The timer A interrupt mask (IMTA) applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. Since there is no timer A in HD404344R and HD404394 Series products, the IMTA mask cannot be used in those products.

(7) Serial Interrupt Request Flag (IFS: $003, 2): IFS is a bit that reflects whether an interrupt is outstanding from the serial interface. IFS is set to 1 when the serial interface completes a transfer, including forced termination.

The IFS flag can be read and written only by the bit manipulation instructions. However, note that only a 0 may be written.

IFS is never cleared automatically, even when an interrupt is received. It must be cleared to 0 by the software.

This flag is cleared to 0 on reset and in stop mode.

IFS	Description
0	Indicates that no interrupt has been requested by the serial interface. (initial value)
1	Indicates that an interrupt has been requested by the serial interface.

(8) Serial Interrupt Mask (IMS: $003, 3): IMS is a bit that masks the IFS flag. The CPU will accept a serial interrupt when IFS is set to 1 only if IMS is cleared to 0 and IE is 1.

The CPU will not receive an interrupt request from IFS if IMS is set to 1. That is, the interrupt will be deferred.

IMS can be read and written only by the bit manipulation instructions.

This mask is set to 1 on reset and in stop mode.

IMS	Description
0	IFS is enabled.
1	IFS is masked. The interrupt will be deferred even if IFS is set to 1. (initial value)

(9) A/D Interrupt Request Flag (IFAD: $003, 0): IFAD is a bit that reflects whether an A/D interrupt request is outstanding. This bit is set to 1 when the A/D converter completes a conversion.

The IFAD flag can be read and written only by the bit manipulation instructions. However, note that only a 0 may be written.

IFAD is never cleared automatically, even when an interrupt is received. It must be cleared to 0 by the software.

This flag is cleared to 0 on reset and in stop mode.

IFAD	Description
0	Indicates that no interrupt has been requested by the A/D converter. (initial value)
1	Indicates that an interrupt has been requested by the A/D converter.

(10) A/D Interrupt Mask (IMAD: $003, 1): IMAD is a bit that masks the IFAD flag. The CPU will accept an A/D interrupt when IFAD is set to 1 only if IMAD is cleared to 0 and IE is 1.

The CPU will not receive an interrupt request from IFAD if IMAD is set to 1. That is, the interrupt will be deferred.

IMAD can be read and written only by the bit manipulation instructions.

This mask is set to 1 on reset and in stop mode.

IMAD	Description
0	IFAD is enabled.
1	IFAD is masked. The interrupt will be deferred even if IFAD is set to 1. (initial value)

4.5.3 External Interrupts

There is one external interrupt source, the $\overline{INT}_0$ pin, in HD404344R and HD404394 Series products, and there are two external interrupt sources, the $\overline{INT}_0$ and $\overline{INT}_1$ pins, in HD404318, HD404358, HD404358R, HD404339, and HD404369 Series products. These external interrupts are generated by falling edges on the corresponding $\overline{INT}_0$ and $\overline{INT}_1$ pins.

When an external interrupt occurs, the corresponding external interrupt request flag (IF0 or IF1) is set to 1. These interrupts can be masked or enabled independently by the external interrupt masks IM0 and IM1. Note that all interrupts are masked or enabled by the interrupt enable flag IE.

When an external interrupt is accepted, the IE flag is cleared to 0 by the hardware during interrupt handling to disable the acceptance of other interrupts.

The $\overline{INT}_0$ interrupt has higher priority than the $\overline{INT}_1$ interrupt. Refer to table 4-3 for details.

4.5.4 Internal Interrupts

There are four internal interrupt sources from the built-in peripheral modules in the HD404344R and HD404394 Series products: timer B, timer C, the A/D converter, and the serial interface. There are five internal interrupt sources from the built-in peripheral modules in the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series products: timer A, timer B, timer C, the A/D converter, and the serial interface.

When an internal interrupt occurs, the corresponding interrupt request flag (IF) is set to 1. These interrupts can be masked or enabled independently by the interrupt masks (IM). Note that all interrupts are masked or enabled by the interrupt enable flag IE.

When an internal interrupt is accepted, the IE flag is cleared to 0 by the hardware during interrupt handling to disable the acceptance of other interrupts.

Refer to table 4-3 for details on the priority of internal interrupts.

4.5.5 Interrupt Handling Sequence

Interrupts are controlled by the interrupt controller. Figure 4-1 shows the block diagram of the interrupt controller, and tables 4-5 (a) and 4-5 (b) list the activation conditions for interrupt handling. Figures 4-2 and 4-3 show the flowcharts for the sequences up to the point where an interrupt is accepted. The interrupt handling sequence is described below.

1. When an interrupt occurs and the interrupt request flag (IF) is set to 1 in the state where the corresponding interrupt mask (IM) is cleared to 0, an interrupt signal is sent to the priority controller.

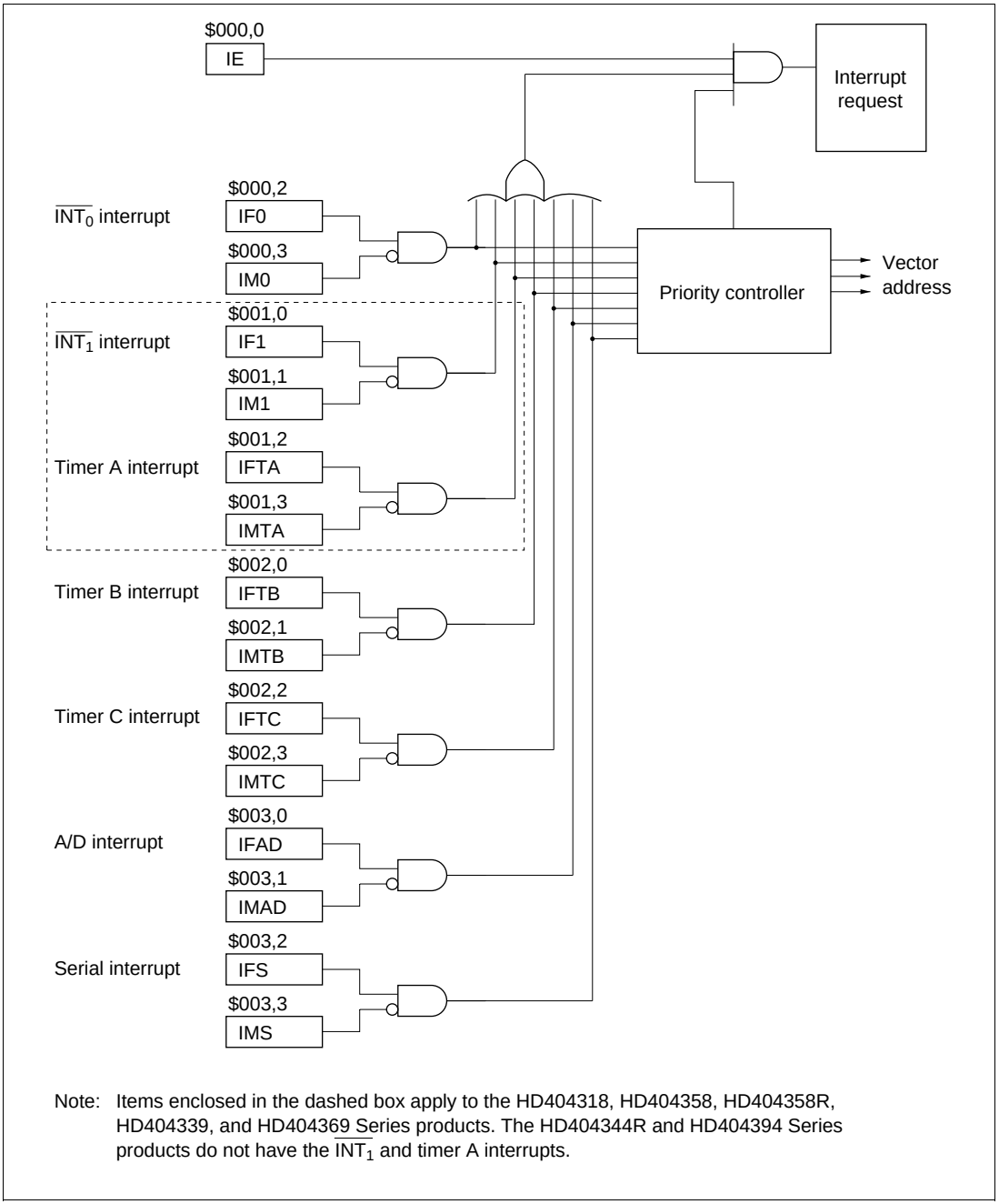
2. The priority controller selects the interrupt with the highest priority and defers the other interrupts.

3. Next the interrupt controller checks the interrupt enable flag (IE). If IE is 1, the highest priority interrupt is accepted, but if IE is 0, all interrupts are deferred.

4. When an interrupt is accepted, the interrupt controller waits for the execution of the current instruction to complete. At that point, the values of the program counter (PC), the carry (CA), and the status (ST) are saved on the stack and the stack pointer is decremented by 4.

5. IE is cleared to 0. This disables all interrupts.

6. The interrupt controller generates the vector address corresponding to the accepted interrupt and loads that value into the PC. Execution of the interrupt handler starts at the branch destination of the JMPL instruction stored at the vector address. (The user must code a JMPL instruction to the start of the corresponding interrupt handler at each vector address.)



Note: Items enclosed in the dashed box apply to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series products. The HD404344R and HD404394 Series products do not have the $\overline{INT_1}$ and timer A interrupts.

Figure 4-1 Interrupt Controller Block Diagram

Table 4-5 (a) Interrupt Handling Activation Conditions (HD404344R and HD404394 Series)

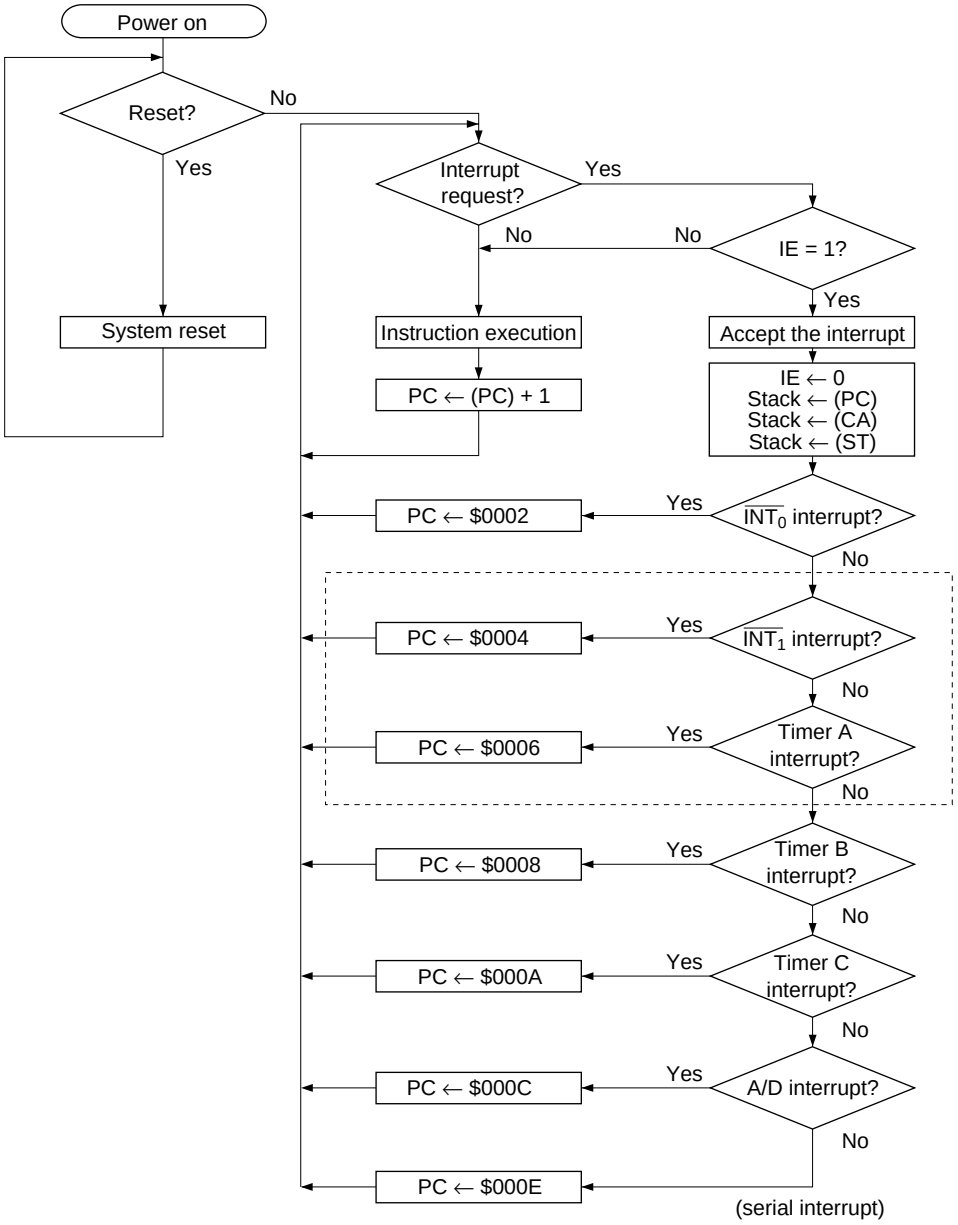
	Interrupt Control Bit				
Interrupt Source	$\overline{\text{INT}_0}$	**Timer B**	**Timer C**	**A/D Converter**	**Serial Interface**
IE	1	1	1	1	1
IF0 · $\overline{\text{IM0}}$	1	0	0	0	0
IFTB · $\overline{\text{IMTB}}$	*	1	0	0	0
IFTC · $\overline{\text{IMTC}}$	*	*	1	0	0
IFAD · $\overline{\text{IMAD}}$	*	*	*	1	0
IFS · $\overline{\text{IMS}}$	*	*	*	*	1

Note: * Operation is not influenced by this value, be it 0 or 1.

Table 4-5 (b) Interrupt Handling Activation Conditions (HD404318, HD404358, HD404358R, HD404339, and HD404369 Series)

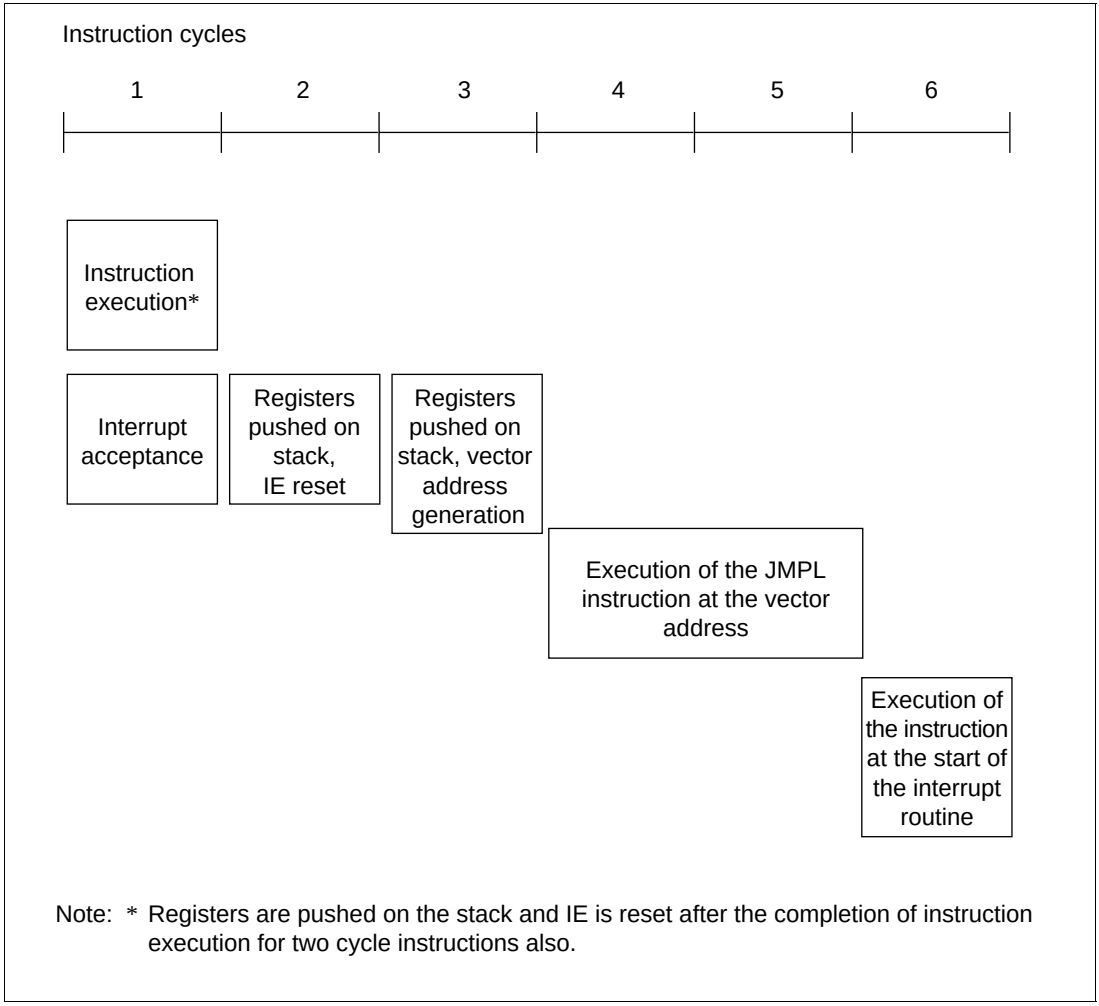
	Interrupt Control Bit						
Interrupt Source	$\overline{\text{INT}_0}$	$\overline{\text{INT}_1}$	**Timer A**	**Timer B**	**Timer B**	**A/D Converter**	**Serial Interface**
IE	1	1	1	1	1	1	1
IF0 · $\overline{\text{IM0}}$	1	0	0	0	0	0	0
IF1 · $\overline{\text{IM1}}$	*	1	0	0	0	0	0
IFTA · $\overline{\text{IMTA}}$	*	*	1	0	0	0	0
IFTB · $\overline{\text{IMTB}}$	*	*	*	1	0	0	0
IFTC · $\overline{\text{IMTC}}$	*	*	*	*	1	0	0
IFAD · $\overline{\text{IMAD}}$	*	*	*	*	*	1	0
IFS · $\overline{\text{IMS}}$	*	*	*	*	*	*	1

Note: * Operation is not influenced by this value, be it 0 or 1.



Note: The section enclosed in the dashed box applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series products. The HD404344R and HD404394 Series products do not have the $\overline{INT_1}$ and timer A interrupts.

Figure 4-2 Interrupt Acceptance Flowchart



Note: * Registers are pushed on the stack and IE is reset after the completion of instruction execution for two cycle instructions also.

Figure 4-3 Interrupt Handling Sequence

Section 5 Low Power Modes (HD404344R/HD404394/HD404318/HD404358 /HD404358R Series)

5.1 Overview

5.1.1 Features

The HD404344R, HD404394, HD404318, HD404358, and HD404358R Series support the following two low power modes.

- Standby mode
- Stop mode

Table 5-1 lists the methods for switching to and clearing these modes and the clock states. Table 5-2 lists the internal states of the CPU and the built-in peripheral modules.

Table 5-1 Operating Modes and Clock States

Mode	Entering Procedure	System Clock Oscillator	Clearing Procedure
Standby mode	SBY instruction	Operating	• $\overline{\text{RESET}}$ pin input
			• Interrupt request
Stop mode	STOP instruction	Stopped	• $\overline{\text{RESET}}$ pin input
			• $\overline{\text{STOPC}}$ pin input in stop mode

Table 5-2 Operation in Low Power Modes

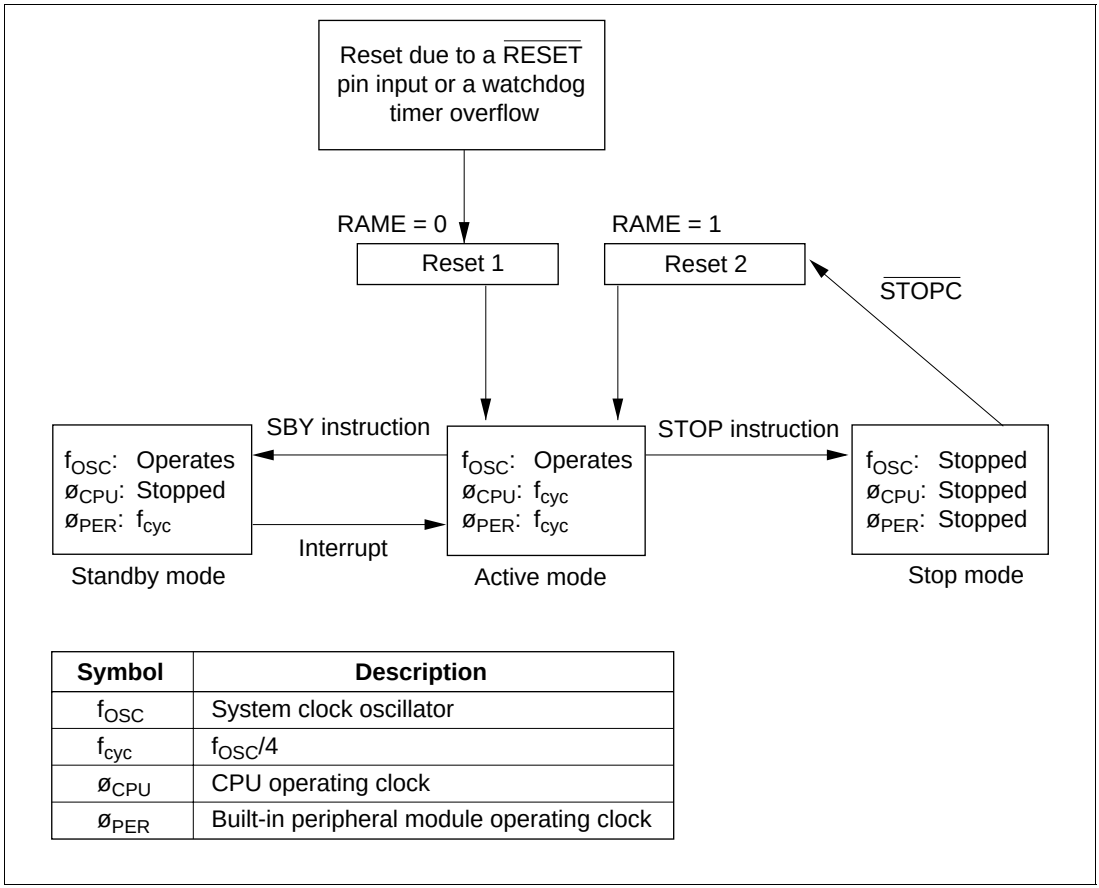
	Mode	
Function	**Stop Mode**	**Standby Mode**
CPU	Reset	Maintained
RAM	Maintained	Maintained
Timer A*	Reset	
Timer B	Reset	
Timer C	Reset	
Serial interface	Reset	
A/D converter	Reset	
I/O ports	Reset (high impedance)	Maintained

Notes: Shaded items operate normally.

* Applies to the HD404318, HD404358 and HD404358R Series.
There is no timer A in the HD404344R and HD404394 Series.

5.1.2 State Transition Diagram

Figure 5-1 shows the state transition diagram for the low power modes.



Symbol	Description
f_{OSC}	System clock oscillator
f_{cyc}	$f_{OSC}/4$
$ø_{CPU}$	CPU operating clock
$ø_{PER}$	Built-in peripheral module operating clock

Figure 5-1 State Transition Diagram

5.1.3 Pin Functions

Table 5-3 lists the functions of the pins used to control the low power operating modes.

Table 5-3 Pin Functions

Pin	Symbol	I/O	Function
Stop mode clear	$\overline{STOPC}$	Input	Stop mode clear

5.1.4 Registers and Flags

Table 5-4 lists the registers and flags that control the low power operating modes.

Table 5-4 Registers and Flags

Address	Item	Abbreviation	R/W	Initial value
$024	Port mode register B	PMRB	W	$0
$021, 3	RAM enable flag	RAME	R/(W)	0

(W): Indicates that only a write of 0 to clear the flag is possible.

Note: The RAME flag is allocated in the register flag area and can only be manipulated with the bit manipulation instructions. Refer to section 2, “Memory”, for details.

5.2 Register and Flag Descriptions

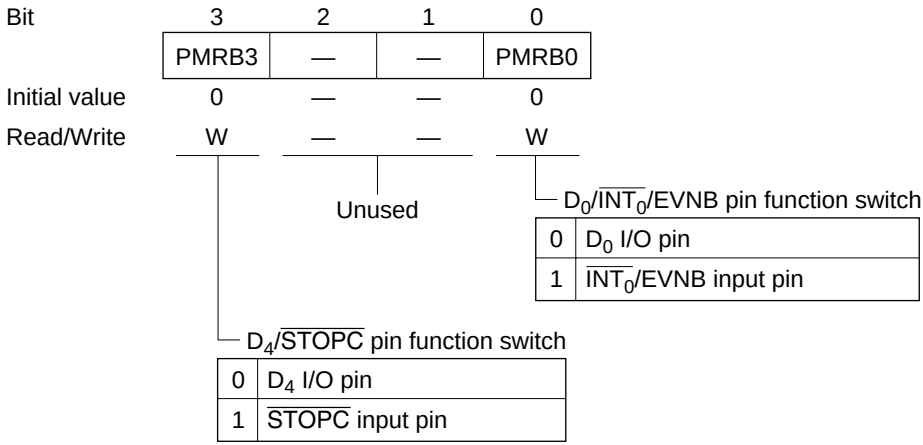
5.2.1 Port Mode Register B (PMRB: $024)

HD404344R and HD404394 Series

PMRB is a 2-bit write-only register that switches the functions of the D port pins.

The PMRB0 bit is cleared to 0 on reset and in stop mode. The PMRB3 bit is cleared to 0 only on reset.

This section describes the PMRB3 bit. Refer to the sections titled “Port Mode Register B” in sections 7 and 8, “I/O Ports”, for details on the PMRB0 bit.



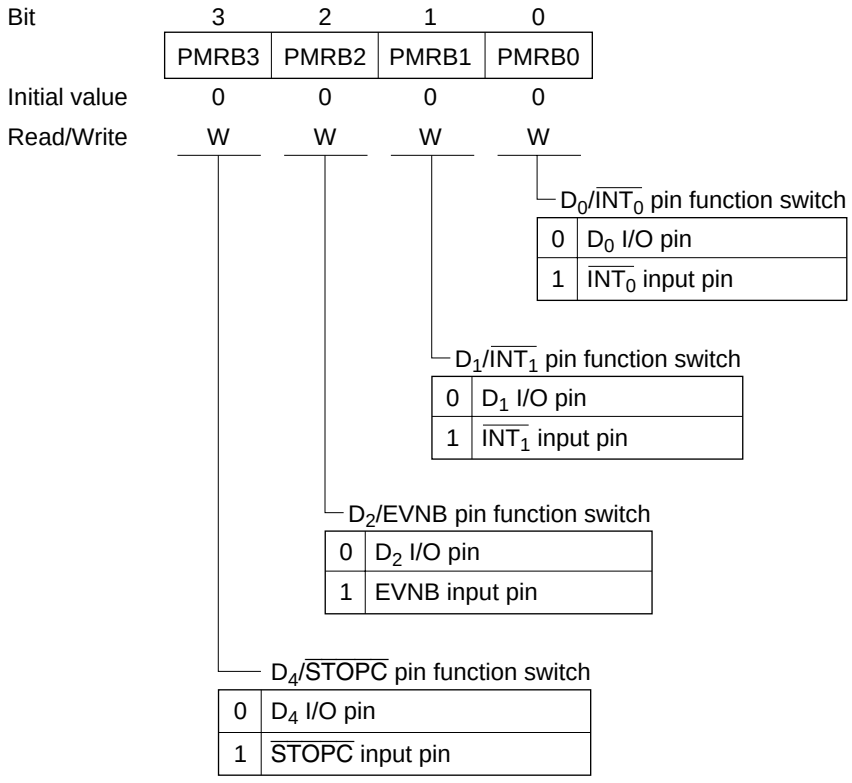
Bit 3—D_4/$\overline{\text{STOPC}}$ Pin Function Switch (PMRB3): Selects whether the D_4/$\overline{\text{STOPC}}$ pin is used as the D_4 I/O pin or as the $\overline{\text{STOPC}}$ input pin.

PMRB3	Description	
0	The D_4/$\overline{\text{STOPC}}$ pin functions as the D_4 I/O pin.	(initial value)
1	The D_4/$\overline{\text{STOPC}}$ pin functions as the $\overline{\text{STOPC}}$ input pin.	

PMRB is a 4-bit write-only register that switches the functions of the D port pins.

The PMRB2 to PMRB0 bits are cleared to 0 on reset and in stop mode. The PMRB3 bit is cleared to 0 only on reset.

This section describes the PMRB3 bit. Refer to the sections titled “Port Mode Register B” in sections 9 and 10, “I/O Ports”, for details on the PMRB0 to PMRB2 bits.



Bit 3—D_4/$\overline{\text{STOPC}}$ Pin Function Switch (PMRB3): Selects whether the D_4/$\overline{\text{STOPC}}$ pin is used as the D_4 I/O pin or as the $\overline{\text{STOPC}}$ input pin. The PMRB3 bit is cleared to 0 only on reset.

PMRB3	Description	
0	The D_4/$\overline{\text{STOPC}}$ pin functions as the D_4 I/O pin.	(initial value)
1	The D_4/$\overline{\text{STOPC}}$ pin functions as the $\overline{\text{STOPC}}$ input pin.	

5.2.2 RAM Enable Flag (RAME: $021, 3)

RAME reflects whether stop mode was cleared by a $\overline{\text{RESET}}$ pin input or by a $\overline{\text{STOPC}}$ pin input.

In stop mode, the contents of RAM directly prior to entering stop mode are maintained, and the contents of RAM are maintained both when stop mode is cleared by a $\overline{\text{STOPC}}$ pin input and when it is cleared by a $\overline{\text{RESET}}$ pin input. However, the contents of RAM are maintained only by resets meant to clear stop mode. Therefore, to use the previous contents of RAM after stop mode is cleared, applications must clear stop mode with a $\overline{\text{STOPC}}$ pin input and test the value of the RAME flag after switching to active mode. If RAME is 1, the contents of RAM are guaranteed to have been maintained.

Although 0 can be written to clear this flag, it cannot be set to 1.

This flag is cleared to 0 on reset.

RAME	Description	
0	Indicates the stop mode was not cleared by a $\overline{\text{STOPC}}$ pin input.	(initial value)
1	Indicates the stop mode was cleared by a $\overline{\text{STOPC}}$ pin input.	

5.3 Standby Mode

5.3.1 Entering Standby Mode

Standby mode is entered by executing an SBY instruction from active mode.

In standby mode, the oscillators continue to operate but the clocks related to instruction execution stop. CPU operation stops and the states of registers, RAM, and D ports and R ports set to output maintain the values they had prior to standby mode. Timers, the serial interface, and other built-in peripheral modules continue to operate.

Power consumption is lower than in active mode due to the CPU being stopped.

5.3.2 Clearing Standby Mode

Standby mode can be cleared either by a $\overline{\text{RESET}}$ pin input or by an interrupt.

(1) Clearing with a $\overline{\text{RESET}}$ Pin Input: When the $\overline{\text{RESET}}$ pin goes low the system enters the reset state and standby mode is cleared.

(2) Clearing with an Interrupt: Standby mode is cleared and the system enters active mode when an interrupt occurs with its corresponding interrupt flag (IF) set to 1 and its interrupt mask (IM) cleared to 0. After the transition the instruction following the SBY instruction is executed. If the interrupt enable flag (IE) is 1, the corresponding interrupt handler will be executed. If IE is 0, the interrupt is deferred and the execution of the immediately preceding instruction sequence continues. Figure 5-2 shows the flowchart for the sequence that occurs when low power modes are cleared.

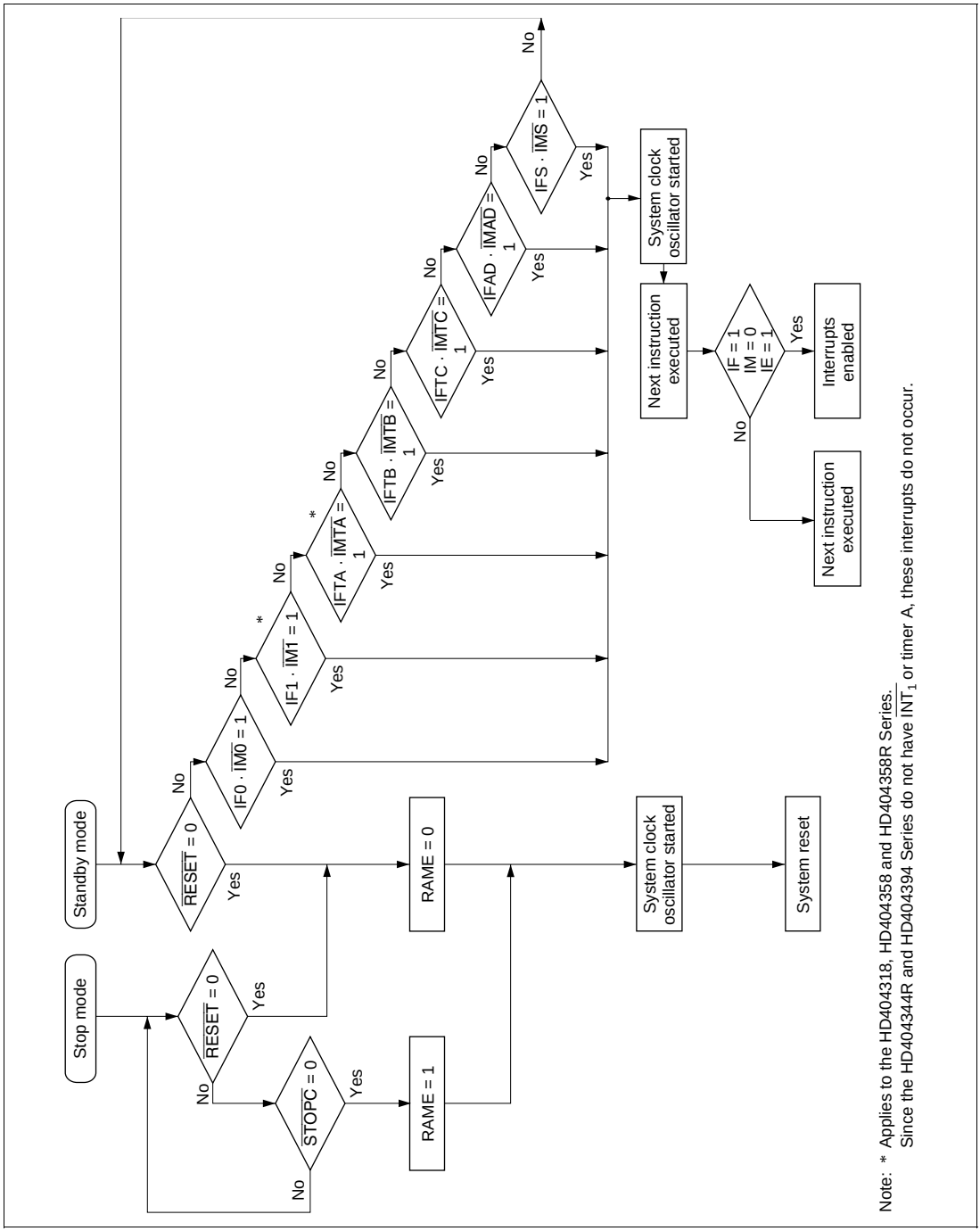


Figure 5-2 Flowchart for Exiting Low Power Modes

5.4 Stop Mode

5.4.1 Entering Stop Mode

The system switches to stop mode when a STOP instruction is executed in active mode. In stop mode, the contents of RAM are maintained and the CPU and all functions of the peripheral modules stop. Accordingly, stop mode is the mode with the lowest power consumption of all operating modes.

Note that the system clock oscillator stops in stop mode.

5.4.2 Clearing Stop Mode

Stop mode is cleared by an input to either the $\overline{\text{RESET}}$ pin or the $\overline{\text{STOPC}}$ pin.

(1) Clearing with a $\overline{\text{RESET}}$ Pin Input: When the $\overline{\text{RESET}}$ pin goes low the system enters the reset state and stop mode is cleared. Although RAME will be cleared during interrupt handling, the contents of RAM are maintained after stop mode is cleared.

(2) Clearing with a $\overline{\text{STOPC}}$ Pin Input: When the $\overline{\text{STOPC}}$ pin goes low the system enters the reset state and stop mode is cleared. Unlike the case for a $\overline{\text{RESET}}$ pin input, RAME is set to 1 during reset exception handling. The contents of RAM are maintained after stop mode is cleared.

After stop mode is cleared by a $\overline{\text{STOPC}}$ pin input and the system has entered active mode, the software can determine that the contents of RAM prior to entering stop mode were maintained by testing the state of the RAME flag.

Although $\overline{\text{RESET}}$ pin input is valid in all operating modes, $\overline{\text{STOPC}}$ pin input is only valid in stop mode and is ignored in other operating modes.

5.4.3 Post-Stop Mode Oscillator Stabilization Period

Figure 5-3 shows the timing chart for clearing stop mode. Be sure to hold the $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ pin low for at least the oscillator stabilization period (t_{RC}). See “AC Characteristics” in section 25, “Electrical Characteristics”, for details.

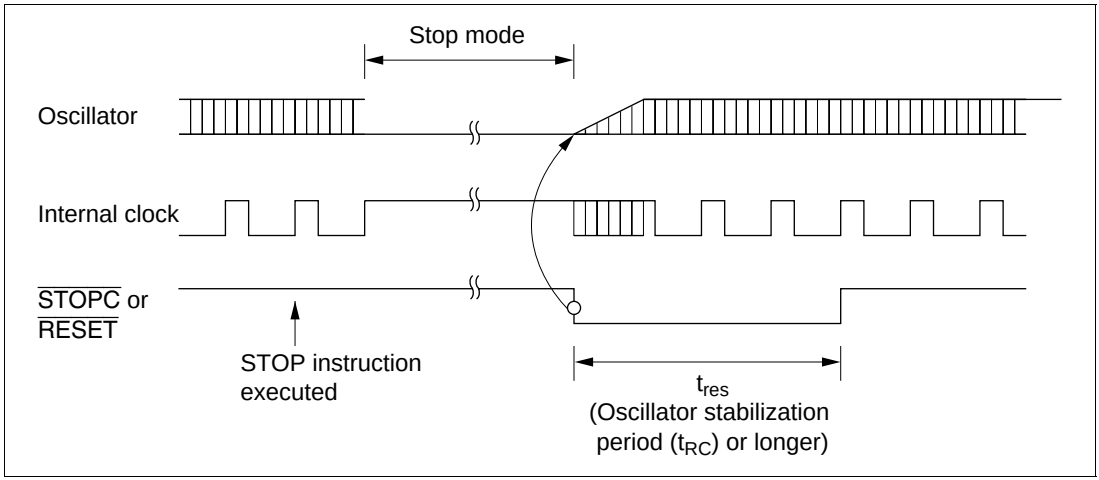
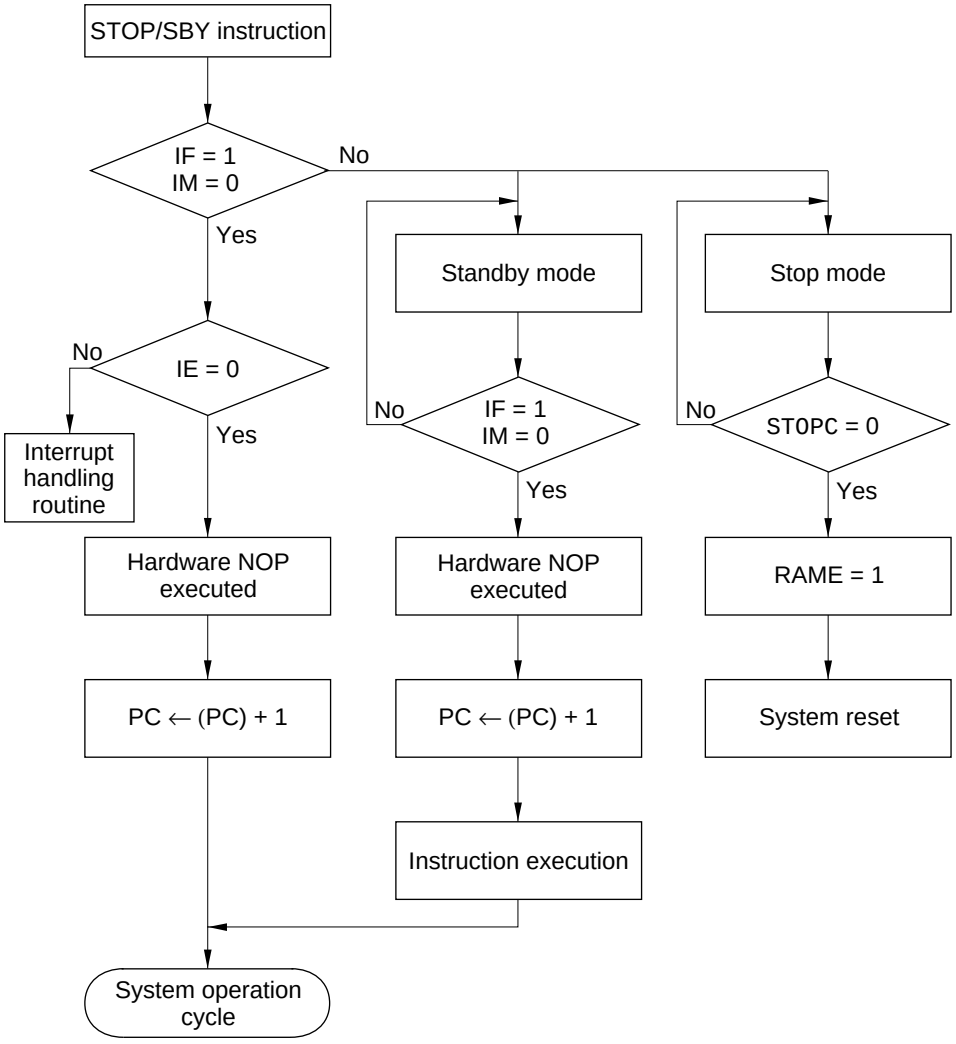


Figure 5-3 Stop Mode Clear Timing

5.5 Low Power Mode Operating Sequence

Figure 5-4 shows the low power mode operating sequence. If a STOP or SBY instruction is executed in the state where the IE flag is cleared, an interrupt flag is set, and the corresponding interrupt mask is cleared, then the STOP or SBY instruction will be cancelled (treated as a NOP) and execution will continue from the next instruction. Therefore, before executing a STOP or SBY instruction, either clear all interrupt flags or mask interrupts.



Note: See figure 5-2, “Flowchart for Exiting Low Power Modes”, for details on IF and IM operation.

Figure 5-4 Low Power Mode Operating Sequence

Section 6 Low Power Modes (HD404339 and HD404369 Series)

6.1 Overview

6.1.1 Features

The HD404339 and HD404369 Series support the following four low power modes.

- Standby mode
- Stop mode
- Watch mode
- Subactive mode

Table 6-1 lists the methods for switching to and clearing these modes and the clock states in these modes. Table 6-2 lists the internal states of the CPU and the built-in peripheral modules.

Table 6-1 Operating Modes and Clock States

		State		
Mode	**Entering Procedure**	**System Clock Oscillator**	**Subsystem Clock Oscillator**	**Clearing Procedure**
Standby mode	SBY instruction from active mode			• $\overline{\text{RESET}}$ pin input • Interrupt request
Stop mode	STOP instruction when TMA3 = 0	Stopped	*	• $\overline{\text{RESET}}$ pin input • $\overline{\text{STOPC}}$ pin input in stop mode
Watch mode	STOP instruction when TMA3 = 1 or SBY instruction from subactive mode (when either LSON is 1 or LSON is 0 and DTON is 0)	Stopped		• $\overline{\text{RESET}}$ pin input • Timer A or $\overline{\text{INT}}_0$ interrupt request
Subactive mode	A timer A or $\overline{\text{INT}}_0$ interrupt request from watch mode when LSON is 1.	Stopped		• $\overline{\text{RESET}}$ pin input • STOP or SBY instruction

Notes: Shaded items indicate normal operation.

* This oscillator either operates or stops in this mode depending on the setting of SSR13 in the system clock selection register 1 (SSR1).

Table 6-2 Operation in Low Power Modes

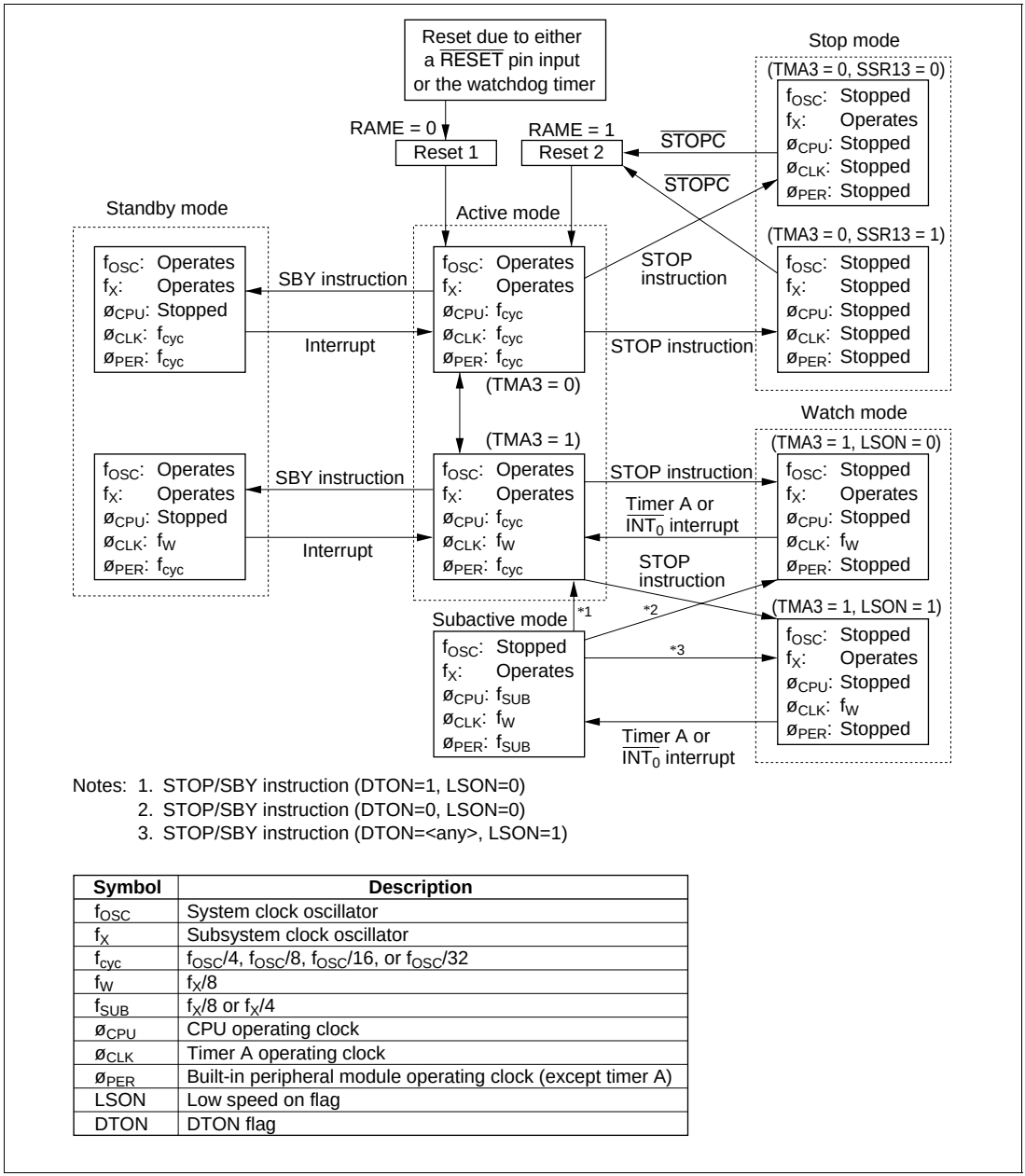
	Mode			
Function	**Stop Mode**	**Watch Mode**	**Standby Mode**	**Subactive Mode**
CPU	Reset	Maintained	Maintained	
RAM	Maintained	Maintained	Maintained	
Timer A	Reset			
Timer B	Reset	Stopped		
Timer C	Reset	Stopped		
Serial interface	Reset	Stopped*		
A/D converter	Reset	Stopped		Stopped
I/O ports	Reset (high impedance)	Maintained	Maintained	

Notes: Shaded items operate normally.

* In external clock mode data transmission and reception are performed if a clock signal is supplied. However, interrupts are stopped.

6.1.2 State Transition Diagram

Figure 6-1 shows the state transition diagram for the low power modes.



Notes: 1. STOP/SBY instruction (DTON=1, LSON=0)
2. STOP/SBY instruction (DTON=0, LSON=0)
3. STOP/SBY instruction (DTON=<any>, LSON=1)

Symbol	Description
f_{OSC}	System clock oscillator
f_X	Subsystem clock oscillator
f_{cyc}	$f_{OSC}/4$, $f_{OSC}/8$, $f_{OSC}/16$, or $f_{OSC}/32$
f_W	$f_X/8$
f_{SUB}	$f_X/8$ or $f_X/4$
$ø_{CPU}$	CPU operating clock
$ø_{CLK}$	Timer A operating clock
$ø_{PER}$	Built-in peripheral module operating clock (except timer A)
LSON	Low speed on flag
DTON	DTON flag

Figure 6-1 State Transition Diagram

6.1.3 Pin Functions

Table 6-3 lists the functions of the pins used to control the low power operating modes.

Table 6-3 Pin Functions

Pin	Symbol	I/O	Function
Stop mode clear	$\overline{\text{STOPC}}$	Input	Stop mode clear

6.1.4 Registers and Flags

Table 6-4 lists the registers and flags that control the low power operating modes.

Table 6-4 Registers and Flags

Address	Item	Abbreviation	R/W	Initial value
$00C	Miscellaneous register	MIS	W	$0
$027	System clock selection register 1	SSR1	W	$0
$008	Timer mode register A	TMA	W	$0
$024	Port mode register B	PMRB	W	$0
$020, 0	Low speed on flag	LSON	R/W	0
$020, 3	DTON flag	DTON	R/W	0
$021, 3	RAM enable flag	RAME	R/(W)	0

(W): Indicates that only a write of 0 to clear the flag is possible.

Note: Control bits in the register flag area can only be manipulated with the bit manipulation instructions. Refer to section 2, “Memory”, for details.

6.2 Register and Flag Descriptions

6.2.1 Miscellaneous Register (MIS: $00C)

MIS is a 4-bit write-only register that turns the port pull-up MOS transistors on or off, turns the R port SO pin output buffer PMOS transistor on or off, and sets both the oscillator stabilization period time when clearing a low power mode as well as the interrupt frame period for watch and subactive modes.

MIS is initialized to $0 on reset and in stop mode.

This section describes the MIS0 and MIS1 bits. The MIS2 and MIS3 bits are described in the “Miscellaneous Register” items in section 11 and 12, “I/O Ports”.

Bit	3	2	1	0
	MIS3	MIS2	MIS1	MIS0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Interrupt frame period and oscillator stabilization period

MIS1	MIS0	Interrupt frame period	Oscillator stabilization period	Oscillator circuit conditions
0	0	0.24414 ms	0.12207 (0.24414) ms*	External clock
	1	15.625 ms	7.8125 ms	Ceramic oscillator
1	0	125 ms	62.5 ms	Crystal oscillator
	1	Unused		—

$R0_2$/SO pin output buffer control

0	PMOS transistor active (CMOS output)
1	PMOS transistor off (NMOS open drain output)

Pull-up MOS transistor control

0	All pull-up MOS transistors off
1	Pull-up MOS transistors active

Note: * Values in parentheses are direct transition time values.

Bits 1, 0—Interrupt Frame Period and Oscillator Stabilization Period (MIS1, MIS0): These bits set the interrupt frame period (in watch mode and subactive mode) and the oscillator stabilization period when clearing low power modes. The oscillator stabilization period set by the MIS1 and MIS0 bits must be longer than the oscillator stabilization period (t_{RC}) for the system clock stipulated in the AC characteristics.

MIS1	MIS0	Interrupt Frame Period (T)*[1]	Oscillator Stabilization Period (tRC)*[1]	Oscillator Circuit Conditions
0	0	0.24414 ms	0.12207 ms (0.24414 ms)*[2]	External clock input
	1	15.625 ms	7.8125 ms	Ceramic oscillator
1	0	125 ms	62.5 ms	Crystal oscillator
	1	Unused	Unused	—

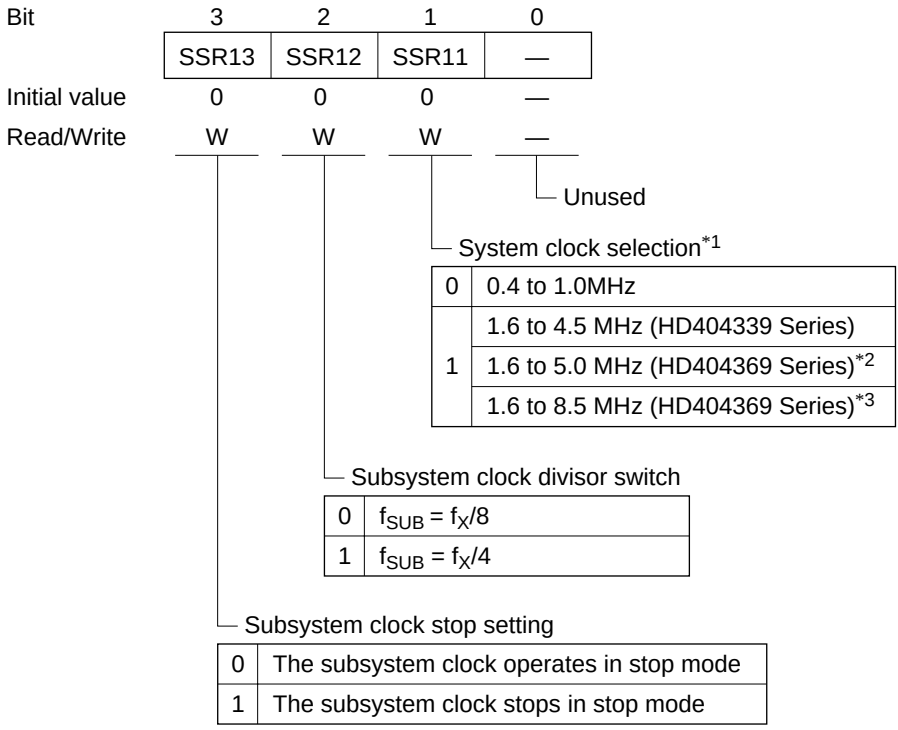
Notes: 1. These values for T and tRC assume a 32.768 kHz crystal oscillator connected to pins X1 and X2.
2. Values in parentheses are for direct transition from subactive mode to active mode.

6.2.2 System Clock Selection Register 1 (SSR1: $027)

SSR1 is a 3-bit write-only register that specifies the system clock oscillator frequency (f_{OSC}) used, sets the divisor for the subsystem clock frequency (f_{SUB}), and sets subsystem clock operation in stop mode.

The SSR12 and SSR11 bits are initialized to 0 on reset and in stop mode. The SSR13 bit is initialized to 0 only on reset.

This section describes SSR13 and SSR12. The SSR11 bit is described in section 14.2.1, “System Clock Selection Register 1 (SSR1)”.



Notes: 1. When the subsystem clock (32.768 kHz crystal oscillator) is used, use the ranges 0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz and 1.6 MHz ≤ f_{OSC} ≤ 4.5 MHz (8.5 MHz: HD404369 Series).
2. Applies to the HD404364, HD404368, HD4043612, and HD404369.
3. Applies to the HD40A4364, HD40A4368, HD40A43612, HD40A4369, and HD407A4369.

Bit 3—Subsystem Clock Stop Setting (SSR13): This bit selects whether the subsystem clock (32.768 kHz oscillator) operates or stops in stop mode.

SSR13	Description	
0	The subsystem clock operates in stop mode	(initial value)
1	The subsystem clock stops in stop mode	

Bit 2—Subsystem Clock Divisor Switch (SSR12): This bit sets the divisor for the subsystem clock supplied to the CPU and the built-in peripheral modules in subactive mode. However, note that the divisor for the subsystem clock supplied to prescaler W (PSW) is fixed at 8, i.e., $f_W = f_X/8$.

SSR12	Description
0	f_{SUB} is 1/8 of the subsystem clock oscillator f_X, i.e., $f_{SUB} = f_X/8$ (initial value) A single CPU instruction cycle takes 244.14 µs (when f_X = 32.768 kHz)
1	f_{SUB} is 1/4 of the subsystem clock oscillator f_X, i.e., $f_{SUB} = f_X/4$ A single CPU instruction cycle takes 122.07 µs (when f_X = 32.768 kHz)

6.2.3 Timer Mode Register A (TMA: $008)

TMA is a 4-bit write-only register that sets the timer counter A operating clock and specifies TCA clearing and prescaler W (PSW) when timer A is used in time base mode.

TMA is initialized to $0 on reset and in stop mode.

This section describes the TMA3 bit. The TMA2 to TMA0 bits are described in section 17.2.1, “Timer Mode Register A”.

Bit	3	2	1	0
	TMA3	TMA2	TMA1	TMA0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Timer A clock selection

TMA3	TMA2	TMA1	TMA0	Prescaler	Input clock period	Mode
0	0	0	0	PSS	2048 t_{cyc}	Free-running timer
			1	PSS	1024 t_{cyc}	
		1	0	PSS	512 t_{cyc}	
			1	PSS	128 t_{cyc}	
	1	0	0	PSS	32 t_{cyc}	
			1	PSS	8 t_{cyc}	
		1	0	PSS	4 t_{cyc}	
			1	PSS	2 t_{cyc}	
1	0	0	0	PSW	32 t_{wcyc}	Clock time base mode
			1	PSW	16 t_{wcyc}	
		1	0	PSW	8 t_{wcyc}	
			1	PSW	2 t_{wcyc}	
	1	0	0	PSW	1/2 t_{wcyc}	
			1	—	Unused	
		1	*	—	PSW, TCA clear	

Note: * Don’t care

Bit 3—Prescaler Selection (TMA3): This bit sets the TCA clock source. When PSW is used as the clock source, timer A operates in time base mode and generates the interrupt frame timing in watch mode and subactive mode.

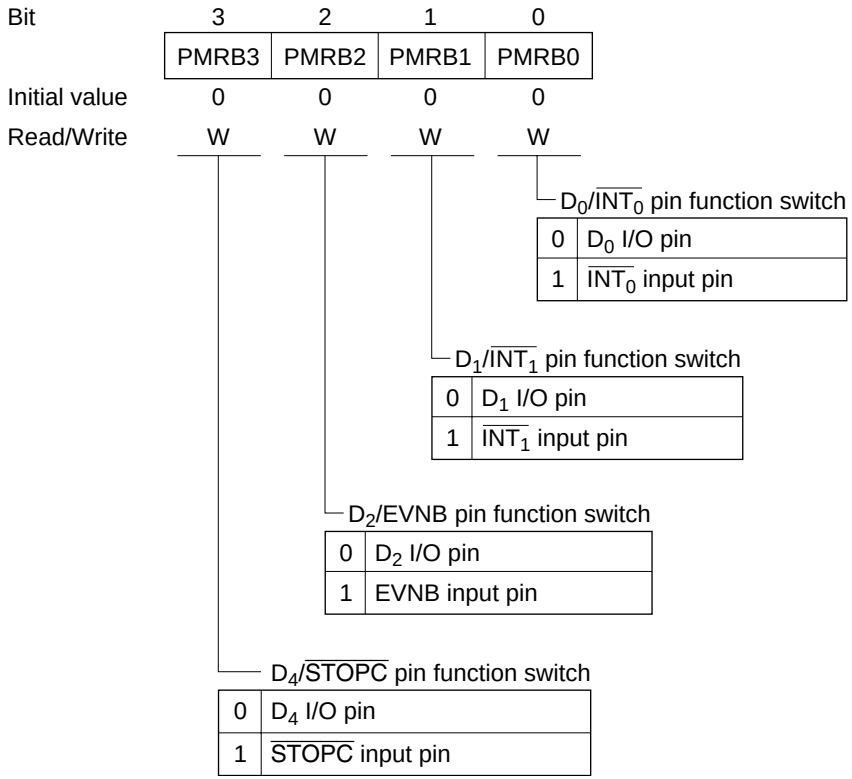
TMA3	Description
0	PSS is used as the TCA clock source. Timer A operates as a free-running timer. (initial value)
1	PSW is used as the TCA clock source. Timer A operates as a clock time base. (See section 17.3.2, “Clock Time Base Operation”.)

6.2.4 Port Mode Register B (PMRB: $024)

PMRB is a 4-bit write-only register that switches the functions of the D port pins.

The PMRB2 to PMRB0 bits are cleared to 0 on reset and in stop mode. The PMRB3 bit is cleared to 0 only on reset.

This section describes the PMRB3 bit. Refer to the sections titled “Port Mode Register B” in sections 11 and 12, “I/O Ports”, for details on the PMRB2 to PMRB0 bits.



Bit 3—$D_4/\overline{STOPC}$ Pin Function Switch (PMRB3): Selects whether the $D_4/\overline{STOPC}$ pin is used as the D_4 I/O pin or as the $\overline{STOPC}$ input pin.

PMRB3	Description	
0	The $D_4/\overline{STOPC}$ pin functions as the D_4 I/O pin.	(initial value)
1	The $D_4/\overline{STOPC}$ pin functions as the $\overline{STOPC}$ input pin.	

6.2.5 Low Speed On Flag (LSON: $020, 0)

LSON selects whether the system clock ($ø_{CPU} = ø_{PER} = f_{CYC}$) or the subsystem clock ($ø_{CPU} = ø_{PER} = f_{SUB}$) is taken as the operating clock for the CPU and the built-in peripheral modules other than timer A at operating mode transitions.

This bit is used for entering and exiting watch mode and subactive mode, and functions in combination with the DTON flag (DTON), the TMA3 bit, the STOP instruction, the SBY instruction, the $\overline{INT_0}$ interrupt during timer A clock time base operation, and the timer A interrupt. This bit has no influence on operations other than at times when a mode transition is caused by an instruction execution or an interrupt.

This flag is cleared to 0 on reset and in stop mode.

LSON	Description
0	The system clock is used as the operating clock for the CPU and peripheral modules other than timer A. (initial value)
1	The subsystem clock is used as the operating clock for the CPU and peripheral modules other than timer A.

Figure 6-2 shows the operating mode transitions that are influenced by LSON and DTON.

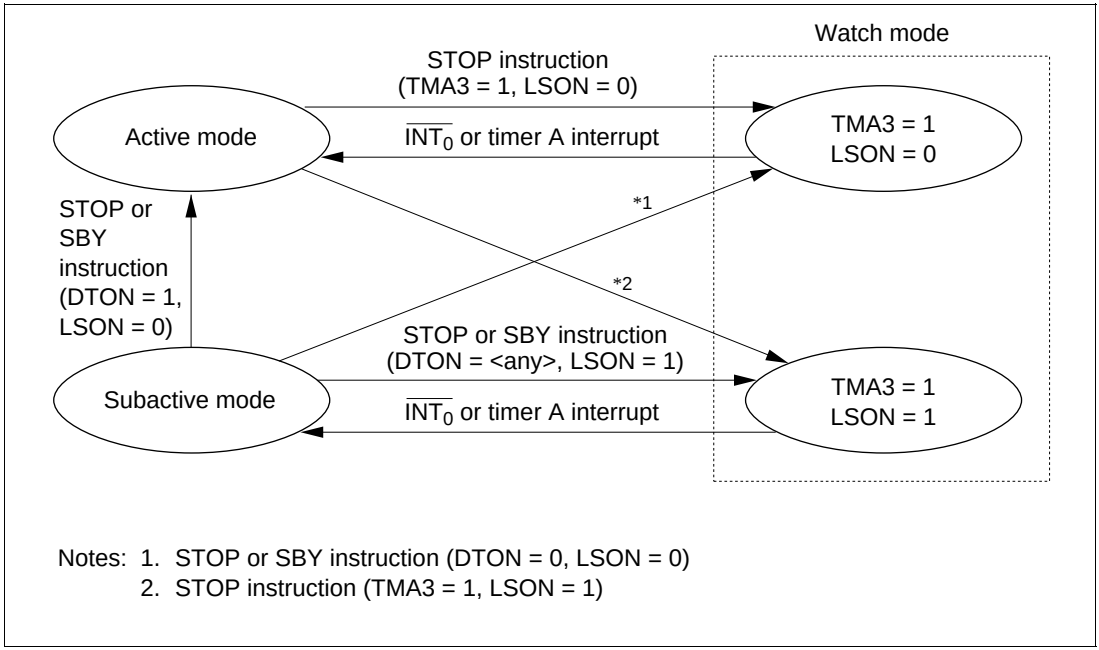
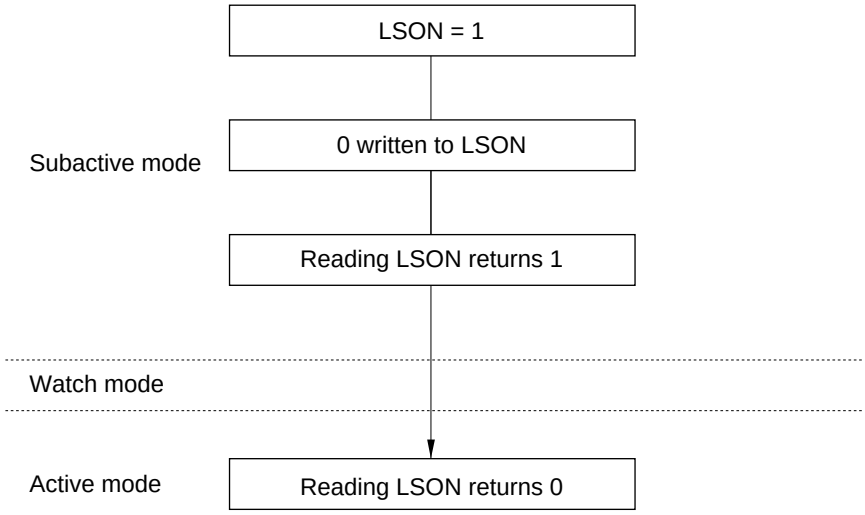


Figure 6-2 Mode Transitions and the LSON and DTON Flags

Although the LSON flag takes effect as soon as it is written, its read value only becomes valid after a state transition. The figure below gives an example.



6.2.6 DTON Flag (DTON: $020, 3)

DTON controls the direct transition from subactive mode to active mode.

This flag can be set to 1 only in subactive mode.

This flag is cleared to 0 on reset, in stop mode, and in active mode.

DTON	Description
0	When a STOP or SBY instruction is executed in subactive mode the system switches to watch mode. (initial value)
1	When a STOP or SBY instruction is executed in subactive mode with LSON set to 0, the system switches to active mode. (If LSON is 1, the system switches to watch mode.)

6.2.7 RAM Enable Flag (RAME: $021, 3)

RAME reflects whether stop mode was cleared by a $\overline{\text{RESET}}$ pin input or by a $\overline{\text{STOPC}}$ pin input.

In stop mode, the contents of RAM directly prior to entering stop mode are maintained, and the contents of RAM are maintained both when stop mode is cleared by a $\overline{\text{STOPC}}$ pin input and when it is cleared by a $\overline{\text{RESET}}$ pin input. However, the contents of RAM are maintained only by resets meant to clear stop mode. Therefore, to use the previous contents of RAM after stop mode is cleared, applications must clear stop mode with a $\overline{\text{STOPC}}$ pin input and test the value of the RAME flag after switching to active mode. If RAME is 1, the contents of RAM are guaranteed to have been maintained.

Although 0 can be written to clear this flag, it cannot be set to 1.

This flag is cleared to 0 on reset.

RAME	Description
0	Indicates the stop mode was not cleared by a $\overline{\text{STOPC}}$ pin input. (initial value)
1	Indicates the stop mode was cleared by a $\overline{\text{STOPC}}$ pin input.

6.3 Standby Mode

6.3.1 Entering Standby Mode

Standby mode is entered by executing an SBY instruction from active mode.

In standby mode, the oscillators continue to operate but the clocks related to instruction execution stop. CPU operation stops and the states of registers, RAM, and D ports and R ports set to output maintain the values they had prior to standby mode. Timers, the serial interface, and other built-in peripheral modules continue to operate.

Power consumption is lower than in active mode due to the CPU being stopped.

6.3.2 Clearing Standby Mode

Standby mode can be cleared either by a $\overline{\text{RESET}}$ pin input or by an interrupt.

(1) Clearing with a $\overline{\text{RESET}}$ Pin Input: When the $\overline{\text{RESET}}$ pin goes low the system enters the reset state and standby mode is cleared.

(2) Clearing with an Interrupt: Standby mode is cleared and the system enters active mode when an interrupt occurs with its corresponding interrupt flag (IF) set to 1 and its interrupt mask (IM) cleared to 0. After the transition the instruction following the SBY instruction is executed. If the interrupt enable flag (IE) is 1, the corresponding interrupt handler will be executed. If IE is 0, the interrupt is deferred and the execution of the immediately preceding instruction sequence continues. Figure 6-3 shows the flowchart for the sequence that occurs when low power modes are cleared.

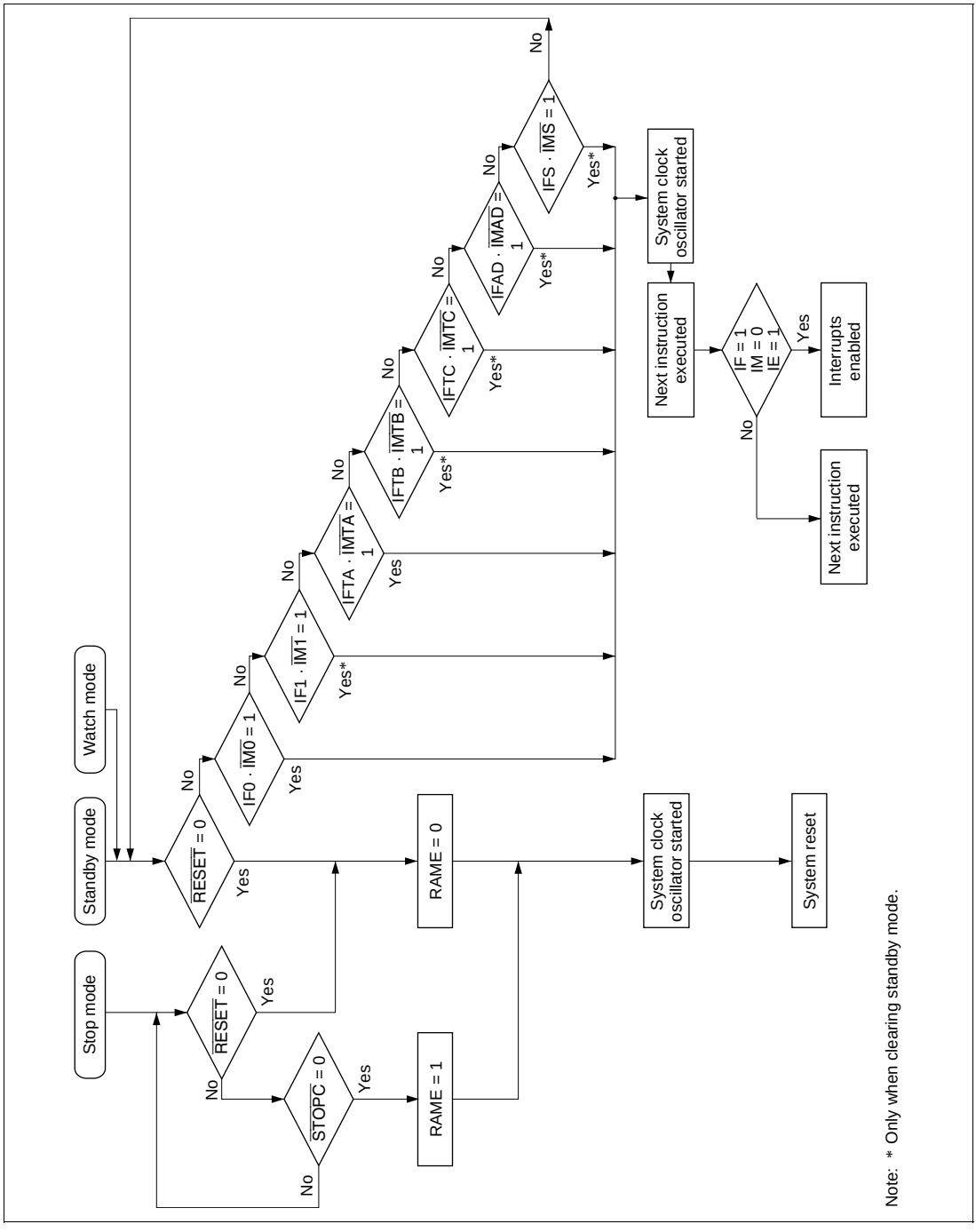


Figure 6-3 Flowchart for Exiting Low Power Modes

6.4 Stop Mode

6.4.1 Entering Stop Mode

The system switches to stop mode when a STOP instruction is executed when the TMA3 bit in TMA is cleared to 0. In stop mode, the contents of RAM are maintained and the CPU and all functions of the peripheral modules stop. Accordingly, stop mode is the mode with the lowest power consumption of all operating modes.

Note that the system clock oscillator stops in stop mode. Also, the SSR13 bit in SSR1 selects whether the subsystem clock operates or stops.

6.4.2 Clearing Stop Mode

Stop mode is cleared by an input to either the $\overline{\text{RESET}}$ pin or the $\overline{\text{STOPC}}$ pin.

(1) Clearing with a $\overline{\text{RESET}}$ Pin Input: When the $\overline{\text{RESET}}$ pin goes low the system enters the reset state and stop mode is cleared. Although RAME will be cleared during reset exception handling the contents of RAM are maintained after stop mode is cleared.

(2) Clearing with a $\overline{\text{STOPC}}$ Pin Input: When the $\overline{\text{STOPC}}$ pin goes low the system enters the reset state and stop mode is cleared. Unlike the case for a $\overline{\text{RESET}}$ pin input, RAME is set to 1 during reset exception handling. The contents of RAM are maintained after stop mode is cleared.

After stop mode is cleared by a $\overline{\text{STOPC}}$ pin input and the system has entered active mode, the software can determine that the contents of RAM prior to entering stop mode were maintained by testing the state of the RAME flag.

Although $\overline{\text{RESET}}$ pin input is valid in all operating modes, $\overline{\text{STOPC}}$ pin input is only valid in stop mode and is ignored in other operating modes.

6.4.3 Post-Stop Mode Oscillator Stabilization Period

Figure 6-4 shows the timing chart for clearing stop mode. Be sure to hold the $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ pin low for at least the oscillator stabilization period (t_{RC}). See “AC Characteristics” in section 25, “Electrical Characteristics”, for details.

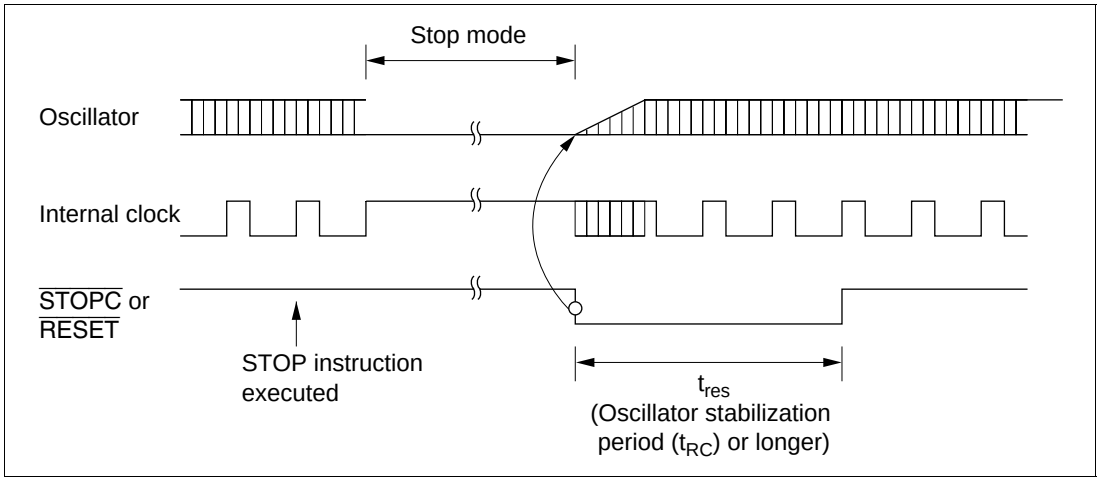


Figure 6-4 Stop Mode Clear Timing

6.5 Watch Mode

6.5.1 Entering Watch Mode

The system switches to watch mode from active when a STOP instruction is executed when the TMA3 bit in TMA is cleared to 1. The system also switches to watch mode from subactive mode when either a STOP or SBY instruction is executed either with LSON set to 1 or with DTON cleared to 0.

In watch mode the system clock stops but the subsystem clock continues to operate, and timer A operates (in clock time base mode) from the subsystem clock. All other built-in peripheral modules stop. RAM and the D and R ports set to output retain their values prior to entering watch mode. Power consumption in watch mode is the second lowest, exceeding only that in stop mode. Watch mode is convenient when only clock operation is required.

6.5.2 Clearing Watch Mode

Watch mode can be cleared either by a $\overline{\text{RESET}}$ pin input or an $\overline{\text{INT}}_0$ or timer A interrupt.

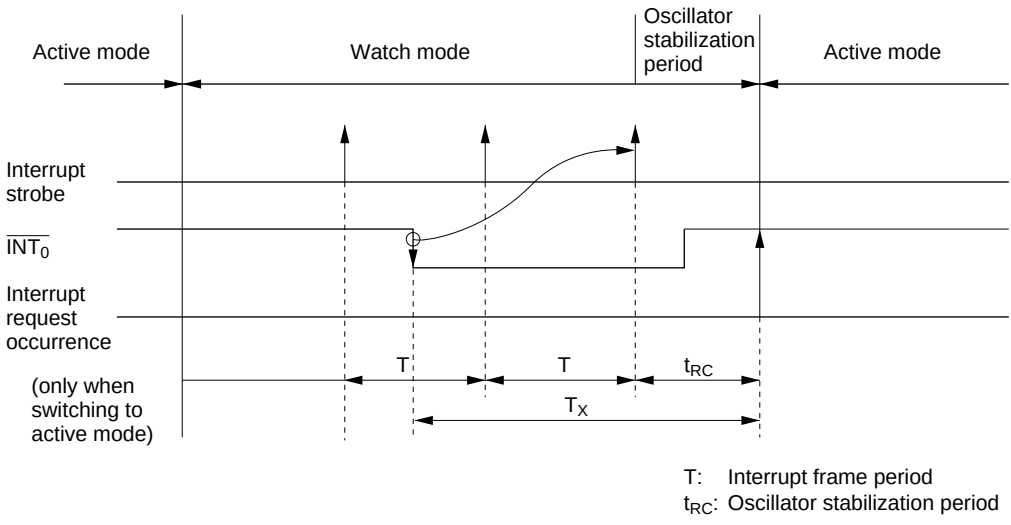
(1) Clearing with a $\overline{\text{RESET}}$ Pin Input: When the $\overline{\text{RESET}}$ pin goes low the system enters the reset state and watch mode is cleared.

(2) Clearing with an $\overline{\text{INT}}_0$ or Timer A Interrupt: Watch mode is cleared when an $\overline{\text{INT}}_0$ or timer A interrupt occurs and the corresponding IF is 1 and IM is 0. If LSON was 0 at that time the system switches to active mode, and if LSON was 1, the system switches to subactive mode.

After the transition the instruction following the STOP or SBY instruction is executed. If the interrupt enable flag (IE) is 1, the corresponding interrupt handler will be executed. If IE is 0, the interrupt is deferred and the execution of the immediately preceding instruction sequence continues. (See figure 6-3.)

6.5.3 Post-Watch Mode Operating Timing

Figure 6-5 shows the operation timing when the system switches to active mode after watch mode is cleared by an $\overline{INT_0}$ or timer A interrupt. The $\overline{INT_0}$ or timer A interrupt is detected in synchronization with the period T set by the MIS register MIS1 and MIS0 bits. Next, interrupt handling for the timer A interrupt starts after the period t_{RC} (also set by the MIS register MIS1 and MIS0 bits) with respect to the interrupt strobe has passed. Interrupt exception handling for the $\overline{INT_0}$ starts after the period $T + t_{RC}$ with respect to the interrupt strobe has passed.



Note: An $\overline{INT_0}$ interrupt is received following the fall of the $\overline{INT_0}$ signal. The time T_X from the fall of $\overline{INT_0}$ to the point active mode is entered will be in the range given by the formula below.

$$T + t_{RC} \leq T_X \leq 2T + t_{RC}$$

Figure 6-5 Watch Mode to Active Mode Transition Timing

6.6 Subactive Mode

6.6.1 Entering Subactive Mode

The system switches to subactive mode when a timer A or $\overline{INT}_0$ interrupt occurs in watch mode with the LSON flag set to 1.

In subactive mode, the system clock stops and the system operates from the subsystem clock.

Although the CPU and the built-in peripheral modules other than the A/D converter operate, since the operating clock is slower, power consumption is lower than all other modes except stop and watch mode.

The CPU instruction cycle time can be selected to be either 244.14 µs ($f_{SUB} = f_X/8$) or 122.07 µs ($f_{SUB} = f_X/4$) by the SSR1 register SSR12 bit. However, note that the SSR12 bit must be set in active mode. System operation is not guaranteed if the SSR12 bit is set in subactive mode.

6.6.2 Clearing Subactive Mode

Subactive mode is cleared by executing either a STOP or SBY instruction. The system will switch to either active mode or watch mode depending on the settings of the LSON and DTON flags as shown in figure 6-2.

6.6.3 System Timing when Switching Directly from Subactive Mode to Active Mode

The system can switch directly from subactive mode to active mode under control of the DTON and LSON flags. The procedure is as follows.

1. In subactive mode, set LSON to 0 and DTON to 1*.
2. Execute either a STOP or an SBY instruction.

This procedure will cause the system to switch directly from subactive mode to active mode after an internal processing time plus the time tRC specified by the MIS register MIS1 and MIS0 bits, as shown in figure 6-6.

Note: * DTON can be set to 1 only in subactive mode. This flag is always cleared to 0 on reset, in stop mode, and in active mode.

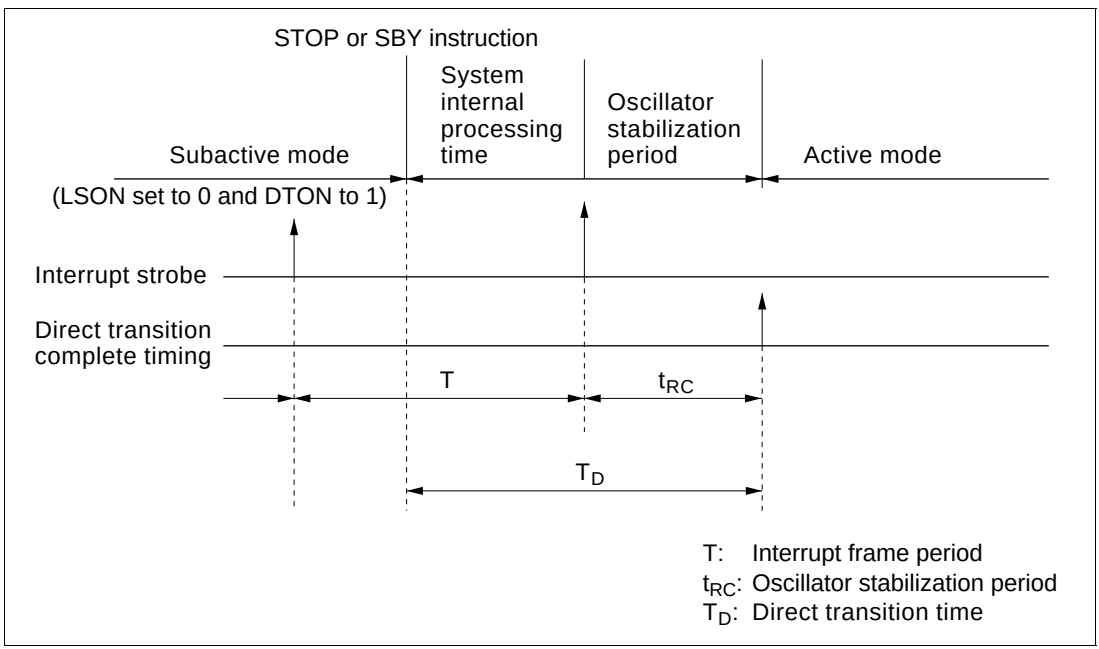


Figure 6-6 Direct Transition Timing

The time TD to switch from subactive mode to active mode is $t_{RC} < TD < T + t_{RC}$, as shown in figure 6-6.

6.7 Interrupt Frame

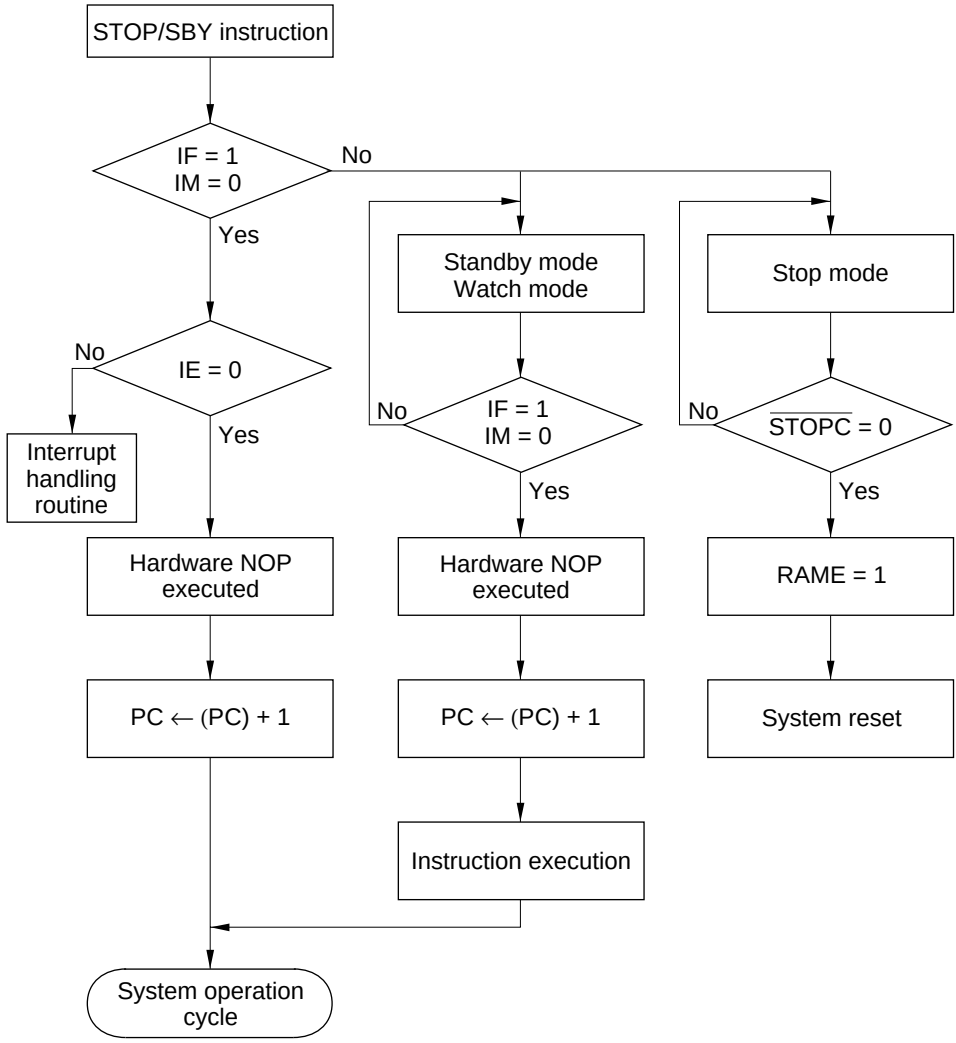
A clock generated by dividing the subsystem clock by 8 is supplied to the timer A and $\overline{INT}_0$ interrupt acceptance circuits in watch and subactive modes. PSW and timer A operate as clock time bases and generate the interrupt frame (T) timing. T can be set to one of three values with the MIS register MIS1 and MIS0 bits.

The $\overline{INT}_0$ and timer A interrupts are generated in synchronization with the interrupt frame in watch and subactive modes. Interrupt exception handling starts on the interrupt strobe in all cases other than the transition to active mode. (See figure 6-5 and 6-6.)

Although the $\overline{INT}_0$ pin input falling edge is input independently of the interrupt frame, it is handled as though it were synchronized with the second following interrupt frame.

6.8 Low Power Mode Operating Sequence

Figure 6-7 shows the low power mode operating sequence. If a STOP or SBY instruction is executed in the state where the IE flag is cleared, an interrupt flag is set, and the corresponding interrupt mask is cleared. The STOP or SBY instruction will then be cancelled (treated as a NOP) and execution will continue from the next instruction. Therefore, before executing a STOP or SBY instruction, either clear all interrupt flags or mask interrupts.



Note: See figure 6-3, “Flowchart for Exiting Low Power Modes”, for details on IF and IM operation.

Figure 6-7 Low Power Mode Operating Sequence

6.9 Usage Notes

Interrupts will not be detected correctly if the high level or low level periods in the $\overline{INT}_0$ signal are shorter than the interrupt frame period in watch and subactive modes.

Figure 6-8 shows the system edge sensing technique. The system samples the $\overline{INT}_0$ signal at fixed periods and determines that a falling edge has occurred when the sampled value changes from high to low on consecutive samples.

Interrupt detection errors can occur since this sampling is performed with the interrupt frame period.

As shown in figure 6-9 (a), if the $\overline{INT}_0$ signal high level period falls between interrupt frames, both points A and B will be low and the falling edge will not be detected. Similarly, as shown in figure 6-9 (b), if the $\overline{INT}_0$ signal low level period falls between interrupt frames, both points A and B will be high and the falling edge will not be detected.

Therefore, the $\overline{INT}_0$ signal high and low level periods must be longer than the interrupt frame period in watch and subactive modes.

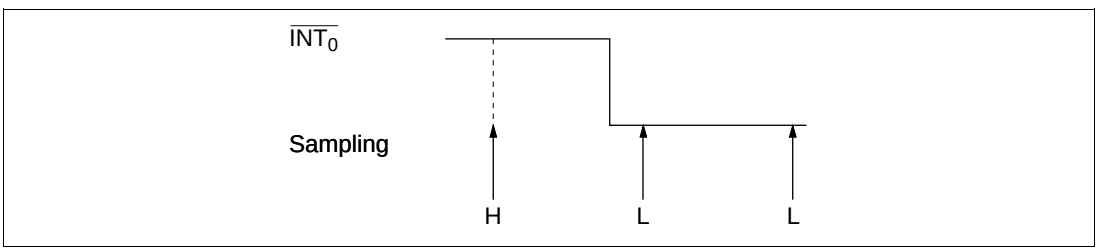


Figure 6-8 Edge Sensing Techniques

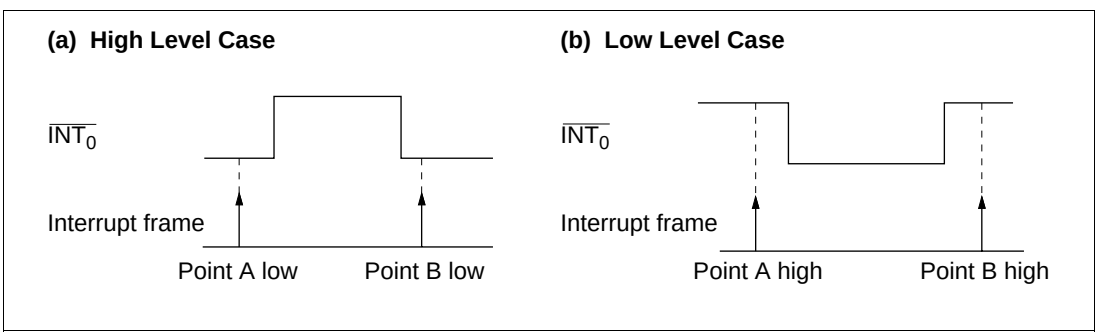


Figure 6-9 Sampling Examples

Section 7 I/O Ports (HD404344R Series)

7.1 Overview

7.1.1 Features

The HD404344R Series I/O ports have the following features.

- The 22 pins in the D and R ports (D_0 to D_5 and the pins in the ports R0 to R3) are all three state CMOS I/O pins. Of these pins, the ten pins D_1, D_2, $R1_0$ to $R1_3$, and $R2_0$ to $R2_3$ are high current I/O pins that can each accept a current influx of up to 15 mA.
- Certain I/O pins (D_0, D_4, and the pins in the ports R_0 and R_3) are shared with the built-in peripheral modules, such as timers and the serial interface. Setting these pins for use with the built-in peripheral modules takes priority over their setting for use as D or R port pins.
- Register settings are used to select input or output for I/O pins and to select the I/O port or peripheral module usage for shared function pins.
- All peripheral module output pins are CMOS outputs. However, the $R0_2$/SO pin can be selected to be an NMOS open drain output by setting a register.
- Since the system is reset in stop mode, the built-in peripheral module selections are cleared and the I/O pins go to the high impedance state.
- The CMOS output pins have built-in programmable pull-up MOS transistors. The on/off state of these transistors can be controlled by register settings on an individual basis. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 7-1 provides an overview of the HD404344R Series port functions.

Table 7-1 Port Functions

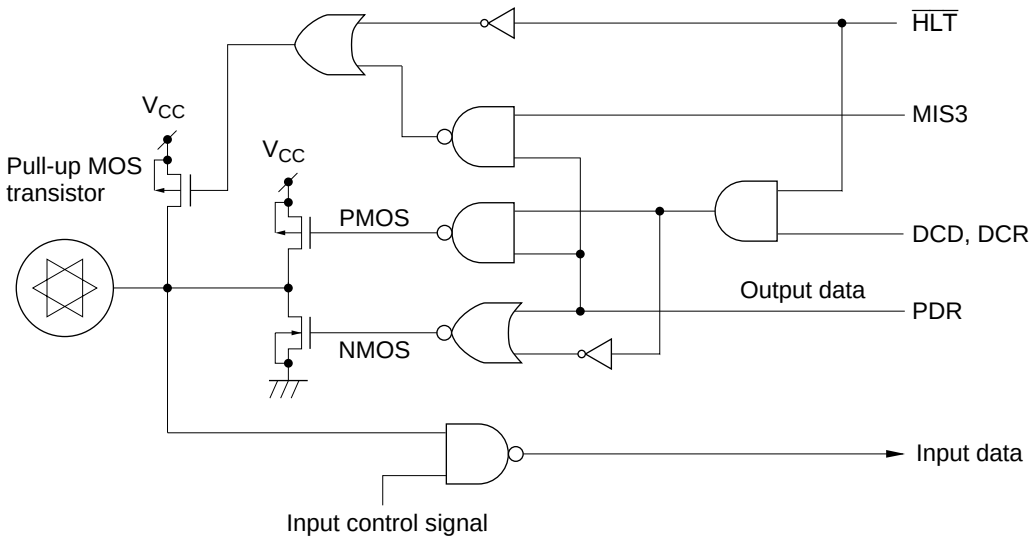
Port	Overview	Pin	Shared Function	Function Switching Register
D_0 to D_5	• I/O port • Accessed in bit units • Accessed with the SED, SEDD, RED, REDD, TD, and TDD instructions. • Programmable pull-up MOS transistors • D_1 and D_2 are high current pins (up to 15 mA)	$D_0/\overline{INT_0}$/EVNB	External interrupt input 0/ timer B event input	PMRB
		D_1	—	—
		D_2		
		D_3		
		$D_4/\overline{STOPC}$	Stop mode clear	PMRB
		D_5	—	—
R0	• I/O ports • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions. • Programmable pull-up MOS transistors • $R1_0$ to $R1_3$ and $R2_0$ to $R2_3$ are high current pins (up to 15 mA).	$R0_0/\overline{SCK}$	Transfer clock I/O	SMR
		$R0_1$/SI	Serial reception data input	PMRA
		$R0_2$/SO	Serial transmission data output	
		$R0_3$/TOC	Timer C output	
R1		$R1_0$	—	—
		$R1_1$		
		$R1_2$		
		$R1_3$		
R2		$R2_0$	—	—
		$R2_1$		
		$R2_2$		
		$R2_3$		
R3		$R3_0/AN_0$	Analog input channel 0	AMR1
		$R3_1/AN_1$	Analog input channel 1	
		$R3_2/AN_2$	Analog input channel 2	
		$R3_3/AN_3$	Analog input channel 3	

7.1.2 I/O Control

All the D port and R port pins are CMOS three state I/O ports.

(1) I/O Pin Circuits: Input and output through the D port and R port pins is controlled by the port data registers (PDR) and the data control registers (DCD, DCR). When a bit in a DCD or DCR register is 1, the corresponding pin will function as an output pin and output the value in its PDR. Similarly, if a DCD or DCR bit is 0, the corresponding pin will function as an input pin.

Figure 7-1 shows the I/O pin circuit structure.



Notes: 1. Since the system is reset in stop mode, the built-in peripheral module selections are cleared. Since the internal $\overline{HLT}$ signal goes to the low (active) level, the I/O pins go to the high impedance state. Also, all the pull-up MOS transistors are turned off.
2. In all low power modes other than stop mode, the internal $\overline{HLT}$ signal goes to the high level.

Figure 7-1 I/O Pin Circuit Structure

(2) Pull-Up MOS Control: Each I/O pin in the D and R ports has a built-in programmable pull-up MOS transistor. When the miscellaneous register (MIS) MIS3 bit is set to 1 the pull-up MOS transistor for pins for which the corresponding PDR is set to 1 will be turned on. Thus the on/off state of each pin can be controlled independently by the PDRs. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 7-2 shows how register settings control the port I/O pins.

Table 7-2 Register Settings for I/O Pin Control

MIS3		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS	PMOS	—		—	On	—		—	On
buffer	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Notes: 1. —: Off

2. The PDR registers are not allocated addresses in RAM. The PDR registers are accessed by special-purpose I/O instructions.

(3) Miscellaneous Register (MIS: $00C): MIS is a 2-bit write-only register that controls the on/off states of the D and R port pin pull-up MOS transistors and the on/off state of the $R0_2$/SO pin output buffer PMOS transistor. MIS is initialized to $0 on reset and in stop mode.

Bit	3	2	1	0
	MIS3	MIS2	—	—
Initial value	0	0	—	—
Read/Write	W	W	—	—

Unused

$R0_2$/SO pin output buffer control

0	PMOS transistor active (CMOS output)
1	PMOS transistor off (NMOS open drain output)

Pull-up MOS transistor control

0	All pull-up MOS transistors off
1	Pull-up MOS transistors active

Bit 3—Pull-Up MOS Transistor Control (MIS3): Controls the on/off states of the pull-up MOS transistors built into the I/O port pins.

MIS3	Description	
0	All pull-up MOS transistors will be turned off.	(initial value)
1	Pull-up MOS transistors for which the corresponding PDR bit is 1 will be turned on.	

Bit 2—$R0_2$/SO Pin Output Buffer Control (MIS2): Controls the on/off state of the $R0_2$/SO pin output buffer PMOS transistor.

MIS2	Description	
0	The $R0_2$/SO pin output will be a CMOS output.	(initial value)
1	The $R0_2$/SO pin output will be an NMOS open drain output.	

7.1.3 I/O Pin Circuit Structures

Table 7-3 shows the port and peripheral module pin circuits.

Table 7-3 Input and Output Pin Circuits

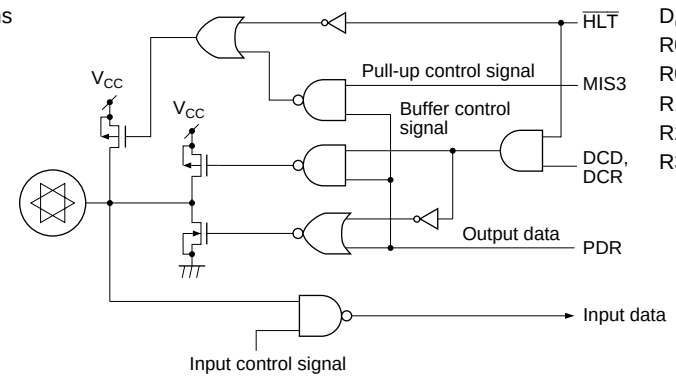
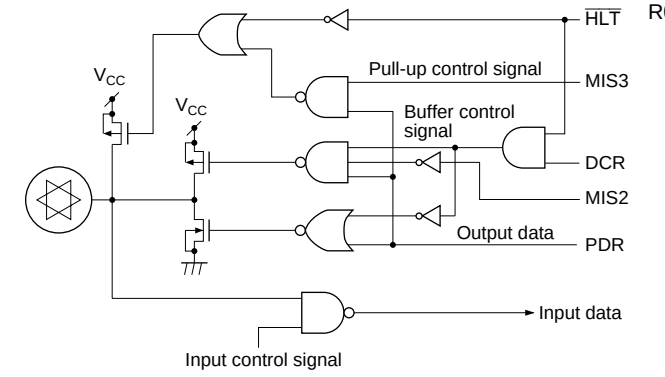
Class		Circuit	Applicable Pins
Standard voltage pins	I/O pins		D_0 to D_5, $R0_0$, $R0_1$, $R0_3$, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$, $R3_0$ to $R3_3$
			$R0_2$

Table 7-3 Input and Output Pin Circuits (cont)

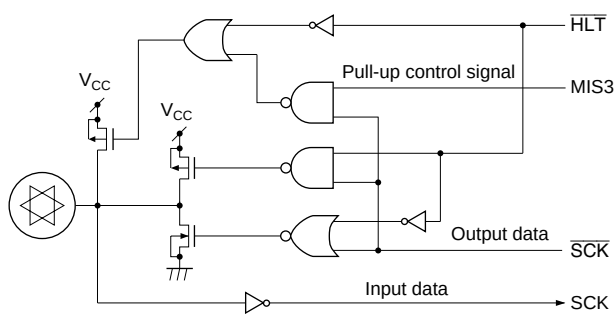
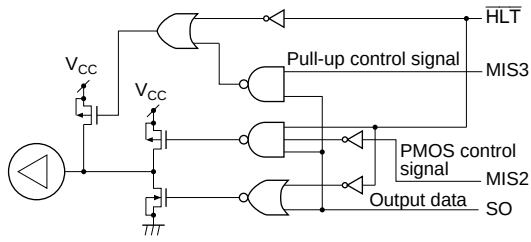
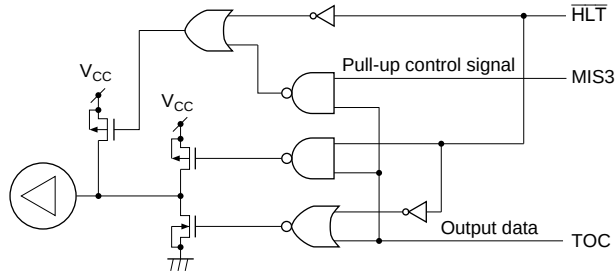
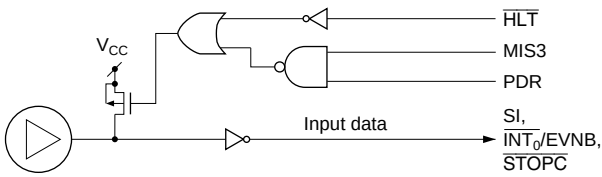
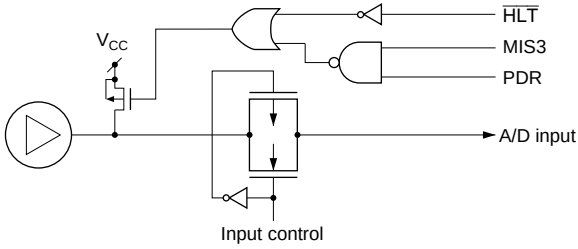
Class			Circuit	Applicable Pins
Standard voltage pins	Built-in peripheral module pins	I/O pins		SCK
		Output pins		SO
				TOC

Table 7-3 Input and Output Pin Circuits (cont)

Class			Circuit	Applicable Pins
Standard voltage pins	Built-in peripheral module pins	Input pins		SI, $\overline{INT_0}$/EVNB, $\overline{STOPC}$
				AN_0 to AN_3

7.1.4 Port States in Low Power Modes

The D_0 and D_4 pins and the R0 and R3 port pins have shared functions as input or output pins for built-in peripheral modules. In standby mode, since the CPU stops, the pins selected as output ports maintain their immediately prior output values. Also, pins selected for use by built-in peripheral modules that operate in standby mode continue to operate. (Output pins used by modules that stop in standby mode maintain their immediately prior output values.) See section 5, “Low Power Modes”, for details on which built-in peripheral modules can operate in each mode.

Table 7-4 lists the port states in the low power modes.

Table 7-4 Port States in Low Power Modes

Low Power Mode	Port States
Standby mode	Pins maintain their values immediately prior to entering standby mode.
Stop mode	Built-in peripheral function selections are cleared, and the port and peripheral function I/O pins go to the high impedance state.

7.1.5 Handling Unused Pins

I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation.

The built-in pull-up MOS transistors can be used to pull up unused pins to VCC. Alternatively, unused pins can be pulled up to V_{CC} with external resistors of about 100 kΩ.

Application programs should maintain the PDR and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

7.2 D Port

7.2.1 Overview

The D port is a 6-pin I/O port (D_0 to D_5, where D_1 and D_2 are high current pins that can each accept a current influx of up to 15 mA) that can be accessed in 1-bit units.

The output levels on the pins D_0 to D_5 can be set to low or high by accessing the port in one-bit units with the SED, SEDD, RED, and REDD output instructions. The output data is stored in the PDR for each pin. The level on each of the pins D0 to D5 can be tested in one-bit units with the TD and TDD input instructions.

The DCD registers are used to turn the D port output buffers on or off. When the DCD bit corresponding to a given pin is 1, the data in the corresponding PDR will be output from that pin. The on/off states of the output buffers can be controlled individually for each D port pin. The DCD registers are allocated in the RAM address space.

The pins D_0 and D_4 have shared functions as built-in peripheral module pins. PMRB is used to switch these functions.

Figure 7-2 shows the structure of the D port.

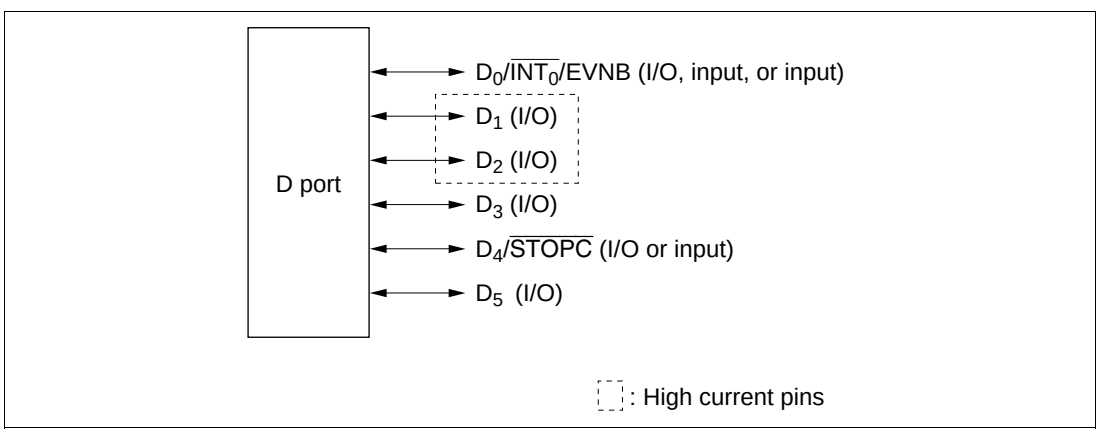


Figure 7-2 D Port Structure

7.2.2 Register Configuration and Descriptions

Table 7-5 shows the configuration of the D port registers.

Table 7-5 D Port Register Configuration

Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	1
$02C	Data control registers	DCD0	W	$0
$02D		DCD1	W	--00
$024	Port mode register B	PMRB	W	0--0

Note: * The SED, SEDD, RED, and REDD instructions can be used to write to the PDRs.

(1) Port Data Registers (PDR): Each of the I/O pins D_0 to D_5 includes a built-in PDR. When a SED or SEDD instruction is executed for one of the pins D_0 to D_5 the corresponding PDR is set to 1, and when a RED or REDD instruction is executed, the corresponding PDR is cleared to 0. When a bit corresponding to a D port pin in DCD0 or DCD1 is 1, the corresponding output buffer is turned on and the value of the corresponding PDR will be output from that pin.

The PDR registers are set to 1 on reset and in stop mode.

(2) Data Control Registers (DCD0, DCD1: $02C, $02D)

	Bit	3	2	1	0
DCD0: $02C		DCD03	DCD02	DCD01	DCD00
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

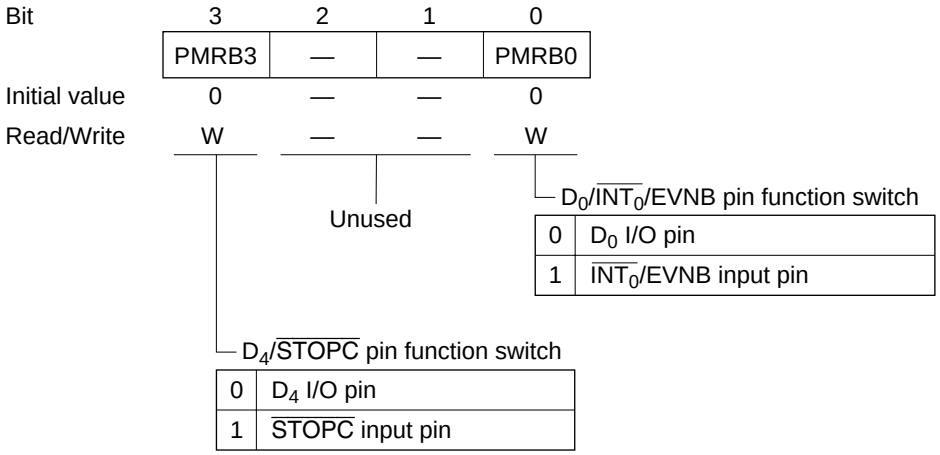
	Bit	3	2	1	0
DCD1: $02D		—	—	DCD11	DCD10
	Initial value	—	—	0	0
	Read/Write	—	—	W	W

Bits in DCD0 and DCD1	Description
0	The CMOS output buffer is turned off and the output goes to the high impedance state. (initial value)
1	The output buffer is turned on and the value in the corresponding PDR is output.

The bits in DCD0 and DCD1 correspond to the D port pins as shown in the table.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCD0	D_3	D_2	D_1	D_0
DCD1	—	—	D_5	D_4

(3) Port Mode Register B (PMRB: $024): PMRB is a 2-bit write-only register that switches the D port I/O pin shared functions.



Bit 3—D_4/$\overline{\text{STOPC}}$ Pin Function Switch (PMRB3): Selects whether the D_4/$\overline{\text{STOPC}}$ pin is used as the D_4 I/O pin or as the stop mode clear pin ($\overline{\text{STOPC}}$).

PMRB3	**Description**	
0	The D_4/$\overline{\text{STOPC}}$ pin functions as the D_4 I/O pin.	(initial value)
1	The D_4/$\overline{\text{STOPC}}$ pin functions as the $\overline{\text{STOPC}}$ input pin.	

Bit 0—D_0/$\overline{\text{INT}_0}$/EVNB Pin Function Switch (PMRB0): Selects whether the D_0/$\overline{\text{INT}_0}$/EVNB pin is used as the D_0 I/O pin or as the $\overline{\text{INT}_0}$/EVNB input pin.

PMRB0	**Description**	
0	The D_0/$\overline{\text{INT}_0}$/EVNB pin functions as the D_0 I/O pin.	(initial value)
1	The D_0/$\overline{\text{INT}_0}$/EVNB pin functions as the $\overline{\text{INT}_0}$/EVNB input pin.	

Refer to section 18.2.2, “Timer Mode Register B2 (TMB2)”, for details on switching between the $\overline{\text{INT}_0}$ and EVNB functions.

7.2.3 Pin Functions

The functions of the pins D_0 to D_5 are switched by register settings as shown in table 7-6.

Table 7-6 D Port Pin Functions

Pin	Pin Functions and Selection Methods
$D_0/\overline{INT_0}$/EVNB	The pin function is switched as shown below by the PMRB PMRB0 bit and the DCD0 DCD00 bit.

PMRB0	0		1
DCD00	0	1	—
Pin function	D_0 input pin	D_0 output pin	$\overline{INT_0}$/EVNB input pin*

Note: * To use this pin as the EVNB pin, mask the $\overline{INT_0}$ interrupt by setting the $\overline{INT_0}$ interrupt mask (IM0: $000,3) to 1.

D_1 — The pin function is switched as shown below by the DCD0 DCD01 bit.

DCD01	0	1
Pin function	D_1 input pin	D_1 output pin

D_2 — The pin function is switched as shown below by the DCD0 DCD02 bit.

DCD02	0	1
Pin function	D_2 input pin	D_2 output pin

D_3 — The pin function is switched as shown below by the DCD0 DCD03 bit.

DCD03	0	1
Pin function	D_3 input pin	D_3 output pin

$D_4/\overline{STOPC}$ — The pin function is switched as shown below by the PMRB PMRB3 bit and the DCD1 DCD10 bit.

PMRB3	0		1
DCD10	0	1	—
Pin function	D_4 input pin	D_4 output pin	$\overline{STOPC}$ input pin

D_5 — The pin function is switched as shown below by the DCD1 DCD11 bit.

DCD11	0	1
Pin function	D_5 input pin	D_5 output pin

7.3 R Ports

7.3.1 Overview

The R port consists of the four 4-bit I/O ports R0 to R3. These ports are accessed in 4-bit units.

The individual ports R0 to R3 are accessed in 4-bit units with the LRA and LRB output instructions to control the output levels (high or low) on each pin. Output data is stored in the PDR built into each pin. Similarly, the LAR and LBR input instructions can be used to access the R ports in 4-bit units to read the input levels on the port pins.

DCR registers are used to control the port R0 to R3 output buffer on/off states. When the DCR bit corresponding to a pin in one of the ports R0 to R3 is set to 1, the data in the corresponding PDR is output from that pin. Thus the output buffer on/off states can be controlled on an individual pin basis for the R port pins. The DCR registers are allocated in the RAM address space.

The pins in ports R1 and R2 are high current pins that can accept current influxes of up to 15 mA.

The R0 and R3 port pins have shared functions as built-in peripheral module pins. Register settings are used to switch these functions. (See table 7-7.)

Figure 7-3 shows the R port pin structure.

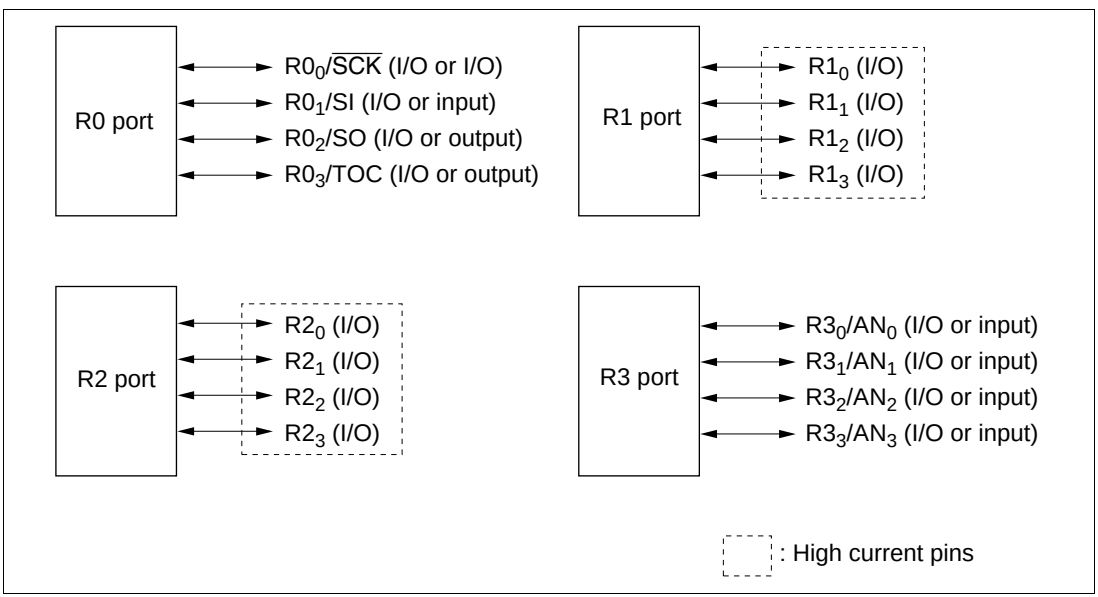


Figure 7-3 R Port Circuit

7.3.2 Register Configuration and Descriptions

Table 7-7 shows the configuration of the R port related registers.

Table 7-7 R Port Register Configuration

Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	1
$030	Data control registers	DCR0	W	$0
$031		DCR1	W	$0
$032		DCR2	W	$0
$033		DCR3	W	$0
$004	Port mode register A	PMRA	W	$0
$005	Serial mode register	SMR	W	$0
$019	A/D mode register 1	AMR1	W	$0

Note: * The LRA and LRB instructions are used to write to the PDR registers.

(1) Port Data Registers (PDR): All the I/O pins in ports R0 to R3 include a PDR that holds the output data. When an LRA or an LRB instruction is executed for one of ports R0 to R3, the contents of the accumulator (A) or the B register (B) are transferred to the specified R port PDRs. When the corresponding bit in DCR0 to DCR3 for the specified port is 1, the output buffers for the corresponding pins will be turned on and the values in the PDRs will be output from the pins.

The PDR registers are set to 1 on reset and in stop mode.

(2) Data Control Registers (DCR0 to DCR3: $030, $031, $032, $033)

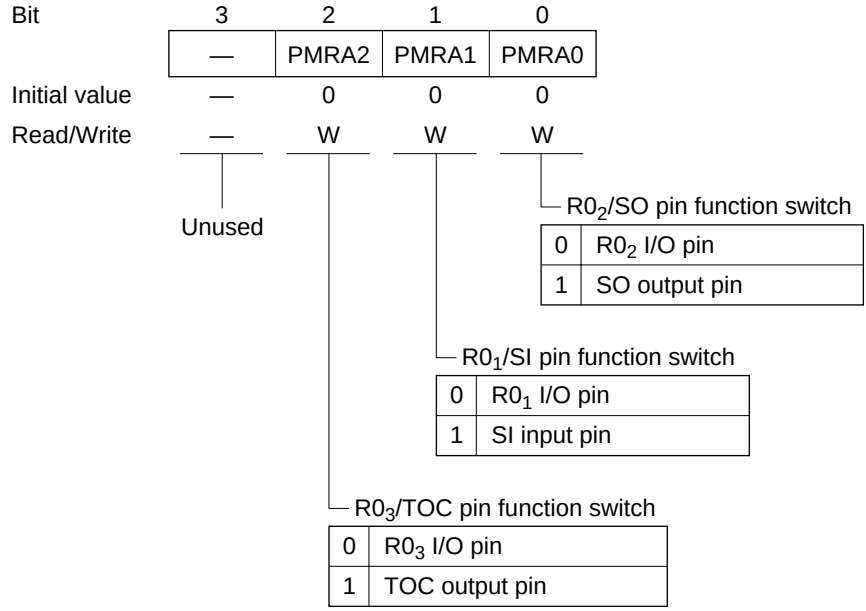
		Bit 3	Bit 2	Bit 1	Bit 0
DCR0: $030		DCR03	DCR02	DCR01	DCR00
	Initial value	0	0	0	0
	Read/Write	W	W	W	W
DCR1: $031		DCR13	DCR12	DCR11	DCR10
	Initial value	0	0	0	0
	Read/Write	W	W	W	W
DCR2: $032		DCR23	DCR22	DCR21	DCR20
	Initial value	0	0	0	0
	Read/Write	W	W	W	W
DCR3: $033		DCR33	DCR32	DCR31	DCR30
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

Bits in DCR0 to DCR3	Description
0	The output buffer (CMOS buffer) is turned off and the output goes to the high impedance state. (initial value)
1	The output buffer is turned on and the corresponding PDR value is output.

The table below lists the correspondence between the bits in DCR0 to DCR3 and the port R0 to R3 pins.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$

(3) Port Mode Register A (PMRA: $004): PMRA is a 3-bit write-only register whose bits PMRA2 to PMRA0 switch the functions of the port R0 shared function pins.



Bit 2—R0$_3$/TOC Pin Function Switch (PMRA2): Selects whether the R0$_3$/TOC pin functions as the R0$_3$ I/O pin or as the timer C output pin (TOC).

PMRA2	Description	
0	The R0$_3$/TOC pin functions as the R0$_3$ I/O pin.	(initial value)
1	The R0$_3$/TOC pin functions as the TOC output pin.	

Bit 1—R0$_1$/SI Pin Function Switch (PMRA1): Selects whether the R0$_1$/SI pin functions as the R0$_1$ I/O pin or as the serial reception data input pin (SI).

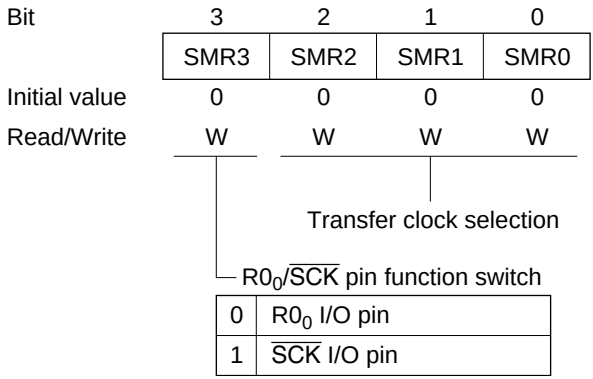
PMRA1	Description	
0	The R0$_1$/SI pin functions as the R0$_1$ I/O pin.	(initial value)
1	The R0$_1$/SI pin functions as the SI input pin.	

Bit 0—R0$_2$/SO Pin Function Switch (PMRA0): Selects whether the R0$_2$/SO pin functions as the R0$_2$ I/O pin or as the serial transmission data output pin (SO).

PMRA0	Description	
0	The R0$_2$/SO pin functions as the R0$_2$ I/O pin.	(initial value)
1	The R0$_2$/SO pin functions as the SO output pin.	

(4) Serial Mode Register (SMR: $005): SMR is a 4-bit write-only register whose SMR3 bit switches the R0$_0$/$\overline{\text{SCK}}$ pin function.

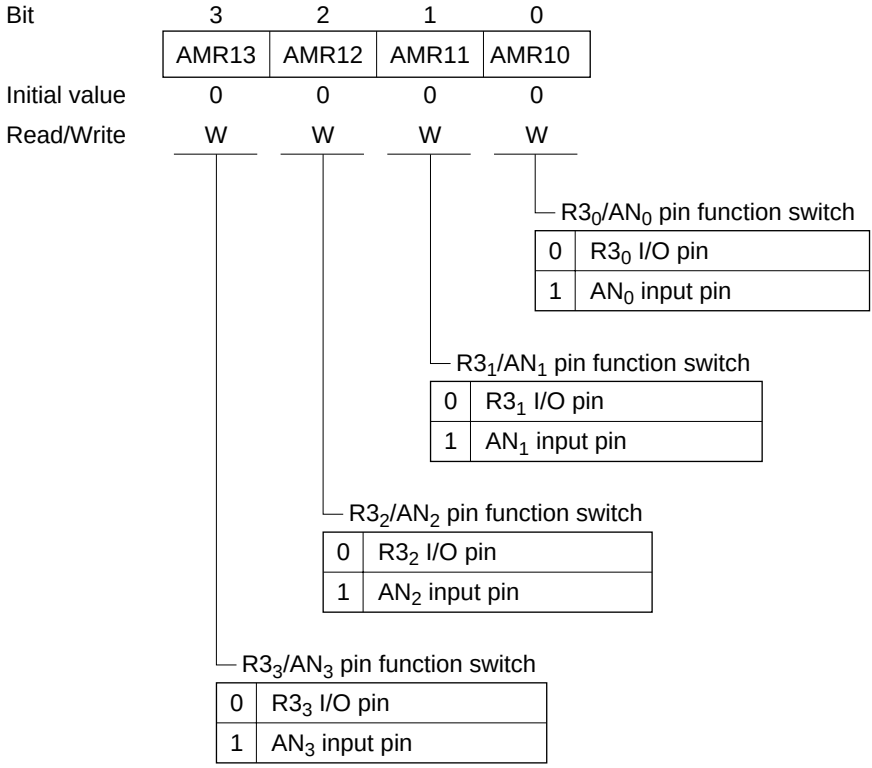
This section only describes the SMR3 bit. See section 20.2.1, “Serial Mode Register (SMR)” for details on bits SMR2 to SMR0.



Bit 3—R0$_0$/$\overline{\text{SCK}}$ Pin Function Switch (SMR3): Selects whether the R0$_0$/$\overline{\text{SCK}}$ pin functions as the R0$_0$ I/O pin or as the serial interface transfer clock I/O pin.

SMR3	Description	
0	The R0$_0$/$\overline{\text{SCK}}$ pin functions as the R0$_0$ I/O pin.	(initial value)
1	The R0$_0$/$\overline{\text{SCK}}$ pin functions as the $\overline{\text{SCK}}$ I/O pin.	

(5) A/D Mode Register 1 (AMR1: $019): AMR1 is a 4-bit write-only register that switches the functions of the R3 port shared function pins.



Bit 3—R3$_3$/AN$_3$ Pin Function Switch (AMR13): Selects whether the R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin or as the A/D converter channel 3 input pin AN$_3$.

AMR13	Description	
0	The R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin.	(initial value)
1	The R3$_3$/AN$_3$ pin functions as the AN$_3$ input pin.	

Bit 2—R3$_2$/AN$_2$ Pin Function Switch (AMR12): Selects whether the R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin or as the A/D converter channel 2 input pin AN$_2$.

AMR12	Description	
0	The R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin.	(initial value)
1	The R3$_2$/AN$_2$ pin functions as the AN$_2$ input pin.	

Bit 1—$R3_1/AN_1$ Pin Function Switch (AMR11): Selects whether the $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin or as the A/D converter channel 1 input pin AN_1.

AMR11	Description	
0	The $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin.	(initial value)
1	The $R3_1/AN_1$ pin functions as the AN_1 input pin.	

Bit 0—$R3_0/AN_0$ Pin Function Switch (AMR10): Selects whether the $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin or as the A/D converter channel 0 input pin AN_0.

AMR10	Description	
0	The $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin.	(initial value)
1	The $R3_0/AN_0$ pin functions as the AN_0 input pin.	

7.3.3 Pin Functions

The pin functions of the R port pins are switched by register settings as shown in table 7-8.

Table 7-8 R Port Pin Functions

Pin	Pin Functions and Selection Methods
$R0_0/\overline{SCK}$	The pin function is switched by the SMR SMR3 bit and the DCR0 DCR00 bit as shown below.

SMR3	0		1
DCR00	0	1	—
Pin function	$R0_0$ input pin	$R0_0$ output pin	$\overline{SCK}$ I/O pin

$R0_1$/SI — The pin function is switched by the PMRA PMRA1 bit and the DCR0 DCR01 bit as shown below.

PMRA1	0		1
DCR01	0	1	—
Pin function	$R0_1$ input pin	$R0_1$ output pin	SI input pin

$R0_2$/SO — The pin function is switched by the PMRA PMRA0 bit and the DCR0 DCR02 bit as shown below.

PMRA0	0		1
DCR02	0	1	—
Pin function	$R0_2$ input pin	$R0_2$ output pin	SO output pin

$R0_3$/TOC — The pin function is switched by the PMRA PMRA2 bit and the DCR0 DCR03 bit as shown below.

PMRA2	0		1
DCR03	0	1	—
Pin function	$R0_3$ input pin	$R0_3$ output pin	TOC output pin

Table 7-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods		
$R1_0$	The pin function is switched by the DCR1 DCR10 bit as shown below.		
	DCR10	0	1
	Pin function	$R1_0$ input pin	$R1_0$ output pin
$R1_1$	The pin function is switched by the DCR1 DCR11 bit as shown below.		
	DCR11	0	1
	Pin function	$R1_1$ input pin	$R1_1$ output pin
$R1_2$	The pin function is switched by the DCR1 DCR12 bit as shown below.		
	DCR12	0	1
	Pin function	$R1_2$ input pin	$R1_2$ output pin
$R1_3$	The pin function is switched by the DCR1 DCR13 bit as shown below.		
	DCR13	0	1
	Pin function	$R1_3$ input pin	$R1_3$ output pin
$R2_0$	The pin function is switched by the DCR2 DCR20 bit as shown below.		
	DCR20	0	1
	Pin function	$R2_0$ input pin	$R2_0$ output pin
$R2_1$	The pin function is switched by the DCR2 DCR21 bit as shown below.		
	DCR21	0	1
	Pin function	$R2_1$ input pin	$R2_1$ output pin
$R2_2$	The pin function is switched by the DCR2 DCR22 bit as shown below.		
	DCR22	0	1
	Pin function	$R2_2$ input pin	$R2_2$ output pin
$R2_3$	The pin function is switched by the DCR2 DCR23 bit as shown below.		
	DCR23	0	1
	Pin function	$R2_3$ input pin	$R2_3$ output pin

Table 7-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R3_0/AN_0$	The pin function is switched by the AMR1 AMR10 bit and the DCR3 DCR30 bit as shown below.

AMR10	0		1
DCR30	0	1	—
Pin function	$R3_0$ input pin	$R3_0$ output pin	AN_0 input pin

$R3_1/AN_1$	The pin function is switched by the AMR1 AMR11 bit and the DCR3 DCR31 bit as shown below.

AMR11	0		1
DCR31	0	1	—
Pin function	$R3_1$ input pin	$R3_1$ output pin	AN_1 input pin

$R3_2/AN_2$	The pin function is switched by the AMR1 AMR12 bit and the DCR3 DCR32 bit as shown below.

AMR12	0		1
DCR32	0	1	—
Pin function	$R3_2$ input pin	$R3_2$ output pin	AN_2 input pin

$R3_3/AN_3$	The pin function is switched by the AMR1 AMR13 bit and the DCR3 DCR33 bit as shown below.

AMR13	0		1
DCR33	0	1	—
Pin function	$R3_3$ input pin	$R3_3$ output pin	AN_3 input pin

7.4 Usage Notes

Keep the following points in mind when using the I/O ports.

- When the MIS MIS2 bit is set to 1, the $R0_2$/SO pin will be an NMOS open drain output regardless of whether it is selected for use as the $R0_2$ pin or as the SO pin by the PMRA PMRA0 bit.

- I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation.

  The built-in pull-up MOS transistors can be used to pull up unused pins to V_{CC}. Alternatively, unused pins can be pulled up to V_{CC} with external resistors of about 100 kΩ.

  Application programs should maintain the PDR and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

- When the MIS MIS3 bit is set to 1 (pull-up MOS transistors active) and the PDR for an R port/analog input shared function pin has the value 1, the MOS transistor for the corresponding pin will not be turned off by selecting the analog input function with the AMR1 register.

  To use an R port/analog input shared function pin as an analog input when the pull-up MOS transistors are active, always clear the PDR for the corresponding pin to 0 first and then turn off the pull-up MOS transistor. (Note that the PDR registers are set to 1 immediately following a reset.)

  Figure 7-4 shows the circuit for the R port/analog input shared function pins.

  AMR1 is used to set the port outputs to high impedance. ACR is used to switch the analog input channel.

  The states of the R port/analog input shared function pins are set, as shown in table 7-9, by the combination of the AMR1 register, the MIS3 bit, the DCR, and the PDR settings.

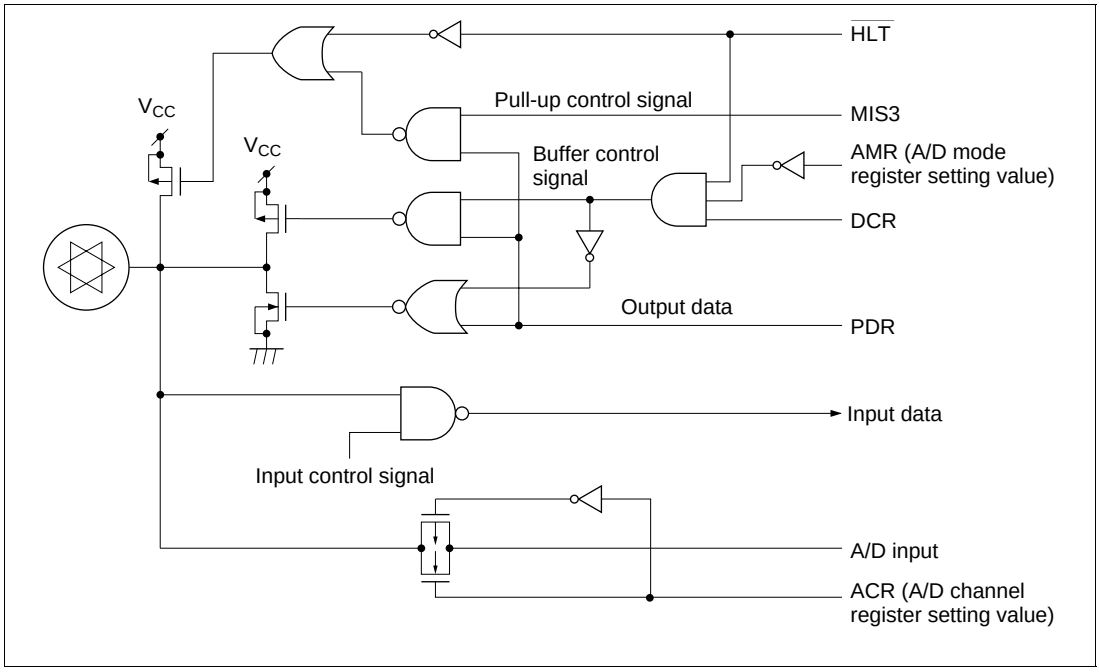


Figure 7-4 R Port/Analog Input Shared Function Pin Circuit Structure

Table 7-9 Program Control of the R Port/Analog Input Shared Function Pins

Corresponding bit in AMR1		0 (R port selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Note: —: off

Corresponding bit in AMR1		1 (analog input selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	—	—		—	—
	NMOS			—	—			—	—
Pull-up MOS transistor		—				—	On	—	On

Note: —: off

Section 8 I/O Ports (HD404394 Series)

8.1 Overview

8.1.1 Features

The HD404394 Series I/O ports have the following features.

- The HD404394 Series microcomputers have a total of 21 I/O pins, of which the three pins $R1_0$ to $R1_2$ are medium voltage NMOS open drain I/O pins. The five pins $R1_3$ and $R2_0$ to $R2_3$ are standard voltage NMOS open drain I/O pins. The remaining 13 pins, D_0 to D_5, $R0_0$ to $R0_3$, and $R3_1$ to $R3_3$, are three state CMOS I/O pins. Of these pins, the pins D_1, D_2, and the R_1 and R_2 port pins are high current I/O pins that can each accept a current influx of up to 15 mA.
- Certain I/O pins (D_0, D_4, and the pins in the ports R0 and R3) are shared with the built-in peripheral modules, such as timers and the serial interface. Setting these pins for use with the built-in peripheral modules takes priority over their setting for use as D or R port pins.
- Register settings are used to select input or output for I/O pins and to select the I/O port or peripheral module usage for shared function pins.
- All peripheral module output pins are CMOS outputs. However, the $R0_2$/SO pin can be selected to be an NMOS open drain output by setting a register.
- Since the system is reset in stop mode, the built-in peripheral module selections are cleared and the I/O pins go to the high impedance state.
- The CMOS output pins have built-in programmable pull-up MOS transistors. The on/off state of these transistors can be controlled by register settings on an individual basis. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 8-1 provides an overview of the HD404394 Series port functions.

Table 8-1 Port Functions

Port	Overview	Pin	Shared Function	Function Switching Register
D_0 to D_5	• I/O port • Accessed in bit units • Accessed with the SED, SEDD, RED, REDD, TD, and TDD instructions. • Programmable pull-up MOS transistors • D_1 and D_2 are high current pins (up to 15 mA)	$D_0/\overline{INT_0}$/EVNB	External interrupt input 0/ timer B event input	PMRB
		D_1	—	—
		D_2		
		D_3		
		$D_4/\overline{STOPC}$	Stop mode clear	PMRB
		D_5	—	—
R0	• I/O ports • Accessed in 4-bit units • Accessed with the LAR, LBR, LRA, and LRB instructions. • The standard I/O pins ($R0_0$ to $R0_3$ and $R3_1$ to $R3_3$) have programmable pull-up MOS transistors. • $R1_0$ to $R1_2$ are medium voltage NMOS open drain I/O pins. • $R1_3$ and $R2_0$ to $R2_3$ are standard voltage NMOS open drain I/O pins. • $R1_0$ to $R1_3$ and $R2_0$ to $R2_3$ are high current pins (up to 15 mA).	$R0_0/\overline{SCK}$	Transfer clock I/O	SMR
		$R0_1$/SI	Serial reception data input	PMRA
		$R0_2$/SO	Serial transmission data output	
		$R0_3$/TOC	Timer C output	
R1		$R1_0$	—	—
		$R1_1$		
		$R1_2$		
		$R1_3$		
R2		$R2_0$	—	—
		$R2_1$		
		$R2_2$		
		$R2_3$		
R3		$R3_1/AN_1$	Analog input channel 1	AMR1
		$R3_2/AN_2$	Analog input channel 2	
		$R3_3/AN_3$	Analog input channel 3	

8.1.2 I/O Control

$R1_0$ to $R1_2$ are medium voltage NMOS open drain I/O ports, $R1_3$ and the R_2 port are standard voltage NMOS open drain I/O ports, and the D port and the R0 and R3 port pins are CMOS three state I/O ports. The different port types have different circuit structures as follows.

(1) Medium Voltage NMOS Open Drain I/O Pin Circuit: $R1_0$ to $R1_2$ are medium voltage NMOS open drain I/O ports. I/O through these ports is controlled by the port data registers (PDR) and the data control registers (DCR). When the DCR bit corresponding to a given pin is 1, that pin functions as an output pin and when the value in the PDR is 0, the NMOS transistor will turn on and the pin will output a low level voltage. When the PDR is 1, the pin will go to the high impedance state.

When a given DCR bit is 0, the corresponding pin will function as an input pin.

(2) Standard Voltage NMOS Open Drain I/O Pin Circuit: $R1_3$ and $R2_0$ to $R2_3$ are standard voltage NMOS open drain I/O ports. I/O through these ports is controlled by the PDR and DCR registers. When the DCR bit corresponding to a given pin is 1, that pin functions as an output pin and when the value in the PDR is 0, the NMOS transistor will turn on and the pin will output a low level voltage. When the PDR is 1, the pin will go to the high impedance state.

When a given DCR bit is 0, the corresponding pin will function as an input pin.

(3) Standard Voltage CMOS Three State I/O Pin Circuit: The D, R0 and R3 ports are standard voltage CMOS three state I/O ports. I/O is controlled by the PDR registers and the data control registers (DCD, DCR). When a bit in a DCD or DCR register is 1, the corresponding pin will function as an output pin and output the value in its PDR. Similarly, if a DCD or DCR bit is 0, the corresponding pin will function as an input pin.

(4) Pull-Up MOS Control: Each I/O pin in the D, R0, and R3 ports has a built-in programmable pull-up MOS transistor. When the miscellaneous register (MIS) MIS3 bit is set to 1 the pull-up MOS transistor for pins for which the corresponding PDR is set to 1 will be turned on. Thus the on/off state of each pin can be controlled independently by the PDRs. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 8-2 shows how register settings control the port I/O pins.

Table 8-2 Register Settings for I/O Pin Control

MIS3		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Notes: 1. —: Off

2. The PDR registers are not allocated addresses in RAM. The PDR registers are accessed by special-purpose I/O instructions.

(5) Miscellaneous Register (MIS: $00C): MIS is a 2-bit write-only register that controls the on/off states of the D, R0, and R3 port pin pull-up MOS transistors and the on/off state of the $R0_2$/SO pin output buffer PMOS transistor. MIS is initialized to $0 on reset and in stop mode.

Bit	3	2	1	0
	MIS3	MIS2	—	—
Initial value	0	0	—	—
Read/Write	W	W	—	—

Unused

$R0_2$/SO pin output buffer control

0	PMOS transistor active (CMOS output)
1	PMOS transistor off (NMOS open drain output)

Pull-up MOS transistor control

0	All pull-up MOS transistors off
1	Pull-up MOS transistors active

Bit 3—Pull-Up MOS Transistor Control (MIS3): Controls the on/off states of the pull-up MOS transistors built into the I/O port pins.

MIS3	Description	
0	All pull-up MOS transistors will be turned off.	(initial value)
1	Pull-up MOS transistors for which the corresponding PDR bit is 1 will be turned on.	

Bit 2—$R0_2$/SO Pin Output Buffer Control (MIS2): Controls the on/off state of the $R0_2$/SO pin output buffer PMOS transistor.

MIS2	Description	
0	The $R0_2$/SO pin output will be a CMOS output.	(initial value)
1	The $R0_2$/SO pin output will be an NMOS open drain output.	

8.1.3 I/O Pin Circuit Structures

Table 8-3 shows the port and peripheral module pin circuits.

Notes: 1. Since the system is reset in stop mode, the built-in peripheral module selections are cleared. Since the internal $\overline{HLT}$ signal goes to the low (active) level, the I/O pins go to the high impedance state. Also, all the pull-up MOS transistors are turned off.

2. In all low power modes other than stop mode, the internal $\overline{HLT}$ signal goes to the high level.

Table 8-3 Input and Output Pin Circuits

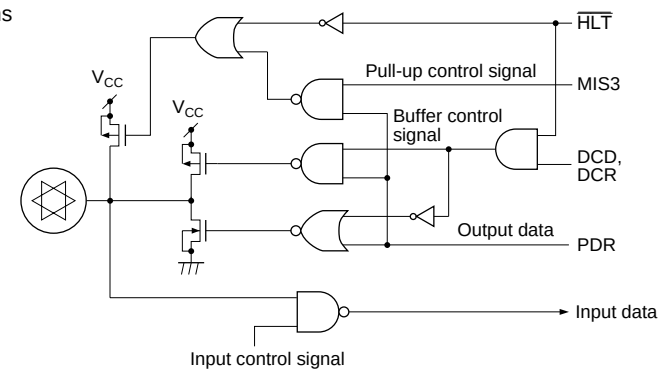
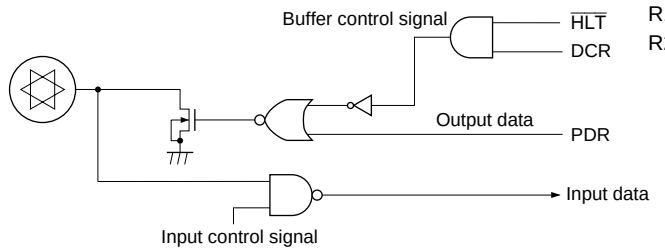
Class		Circuit	Applicable Pins
Standard voltage pins	I/O pins		D_0 to D_5, $R0_0$, $R0_1$, $R0_3$, $R3_1$ to $R3_3$
			$R1_3$, $R2_0$ to $R2_3$

Table 8-3 Input and Output Pin Circuits (cont)

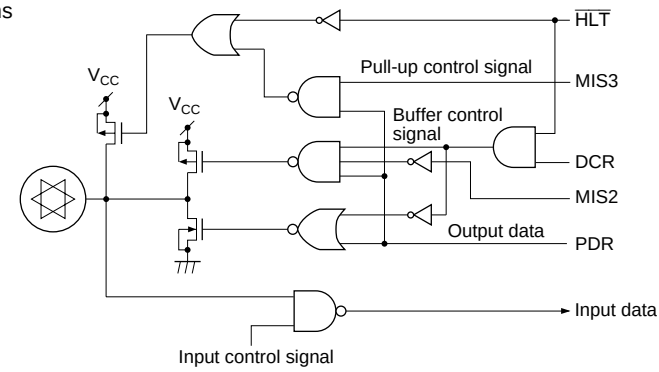
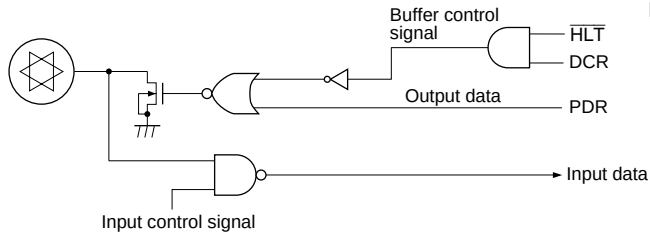
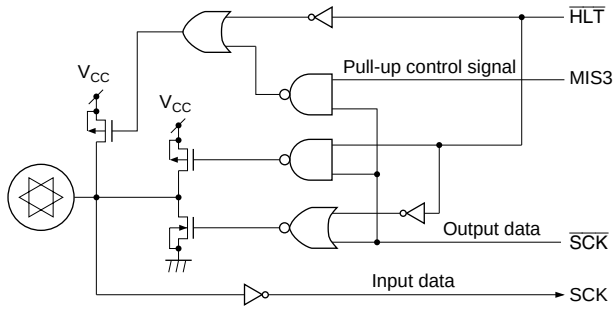
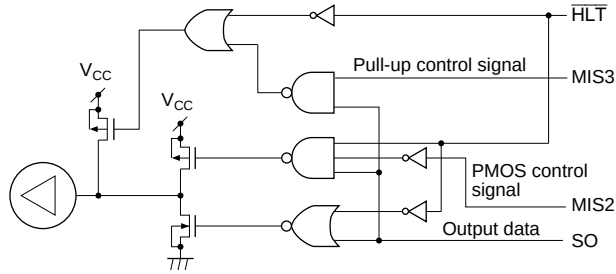
Class	Circuit	Applicable Pins
Standard voltage pins I/O pins		$R0_2$
Medium voltage pins		$R1_0$ to $R1_2$

Table 8-3 Input and Output Pin Circuits (cont)

Class		Circuit	Applicable Pins
Standard voltage pins	Standard peripheral module pins	I/O pins	$\overline{SCK}$
		Output pins	SO
			TOC





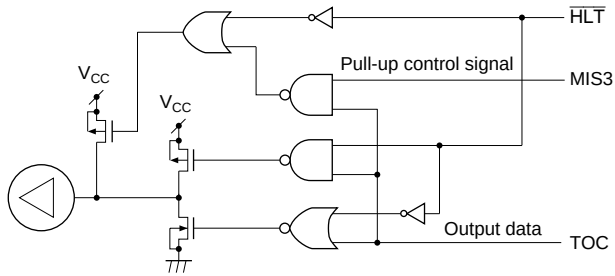
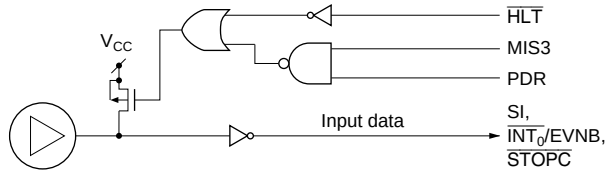
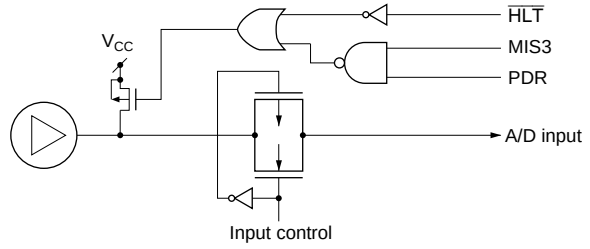


Table 8-3 Input and Output Pin Circuits (cont)

Class			Circuit	Applicable Pins
Standard voltage pins	Built-in peripheral module pins	Input pins		SI, $\overline{INT_0}$/EVNB, $\overline{STOPC}$
				AN_1 to AN_3

8.1.4 Port States in Low Power Modes

The D_0 and D_4 pins and the R0 and R3 port pins have shared functions as input or output pins for built-in peripheral modules. In standby mode, since the CPU stops, the pins selected as output ports maintain their immediately prior output values. Also, pins selected for use by built-in peripheral modules that operate in standby mode continue to operate. (Output pins used by modules that stop in standby mode maintain their immediately prior output values.) See section 5, “Low Power Modes”, for details on which built-in peripheral modules can operate in each mode.

Table 8-4 lists the port states in the low power modes.

Table 8-4 Port States in Low Power Modes

Low Power Mode	Port States
Standby mode	Pins maintain their values immediately prior to entering standby mode.
Stop mode	Built-in peripheral function selections are cleared, and the port and peripheral function I/O pins go to the high impedance state.

8.1.5 Handling Unused Pins

I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation.

The built-in pull-up MOS transistors can be used to pull up unused pins to V_{CC}. Alternatively, unused pins can be pulled up to V_{CC} with external resistors of about 100 kΩ.

Application programs should maintain the PDR, DCD and DCR contents for unused pins at their reset state values. Alternatively, unused pins can be selected for use as peripheral function I/O pins.

8.2 D Port

8.2.1 Overview

The D port is a 6-pin I/O port (D_0 to D_5, where D_1 and D_2 are high current pins that can each accept a current influx of up to 15 mA) that can be accessed in 1-bit units.

The output levels on the pins D_0 to D_5 can be set to low or high by accessing the port in one-bit units with the SED, SEDD, RED, and REDD output instructions. The output data is stored in the PDR for each pin. The level on each of the pins D0 to D5 can be tested in one-bit units with the TD and TDD input instructions.

The DCD registers are used to turn the D port output buffers on or off. When the DCD corresponding to a given pin is 1, the data in the corresponding PDR will be output from that pin. The on/off states of the output buffers can be controlled individually for each D port pin. The DCD registers are allocated in the RAM address space.

The pins D_0 and D_4 have shared functions as built-in peripheral module pins. PMRB is used to switch these functions.

Figure 8-1 shows the structure of the D port.

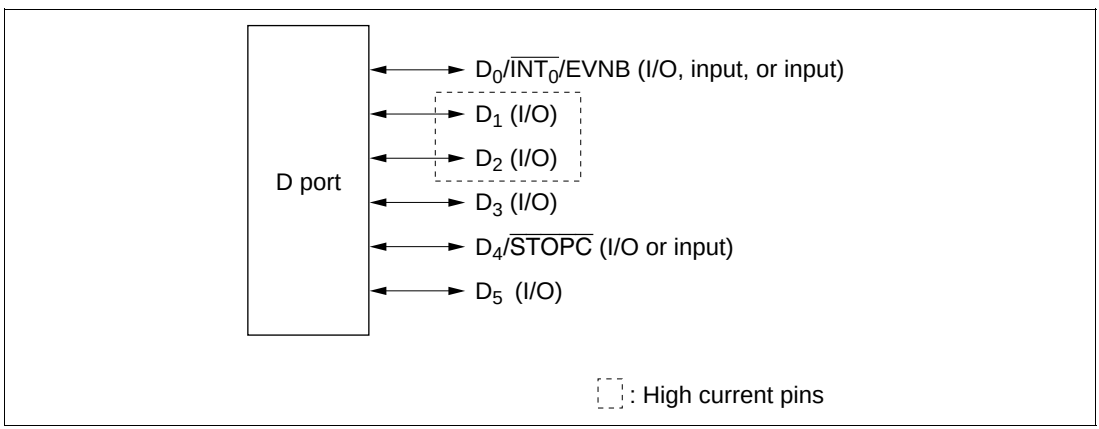


Figure 8-1 D Port Structure

8.2.2 Register Configuration and Descriptions

Table 8-5 shows the configuration of the D port registers.

Table 8-5 D Port Register Configuration

Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	1
$02C	Data control registers	DCD0	W	$0
$02D		DCD1	W	--00
$024	Port mode register B	PMRB	W	0--0

Note: * The SED, SEDD, RED, and REDD instructions can be used to write to the PDRs.

(1) Port Data Registers (PDR): Each of the I/O pins D_0 to D_5 includes a built-in PDR. When a SED or SEDD instruction is executed for one of the pins D_0 to D_5 the corresponding PDR is set to 1, and when a RED or REDD instruction is executed, the corresponding PDR is cleared to 0. When a bit corresponding to a D port pin in DCD0 or DCD1 is 1, the corresponding output buffer is turned on and the value of the corresponding PDR will be output from that pin.

The PDR registers are set to 1 on reset and in stop mode.

(2) Data Control Registers (DCD0, DCD1: $02C, $02D)

	Bit	3	2	1	0
DCD0: $02C		DCD03	DCD02	DCD01	DCD00
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

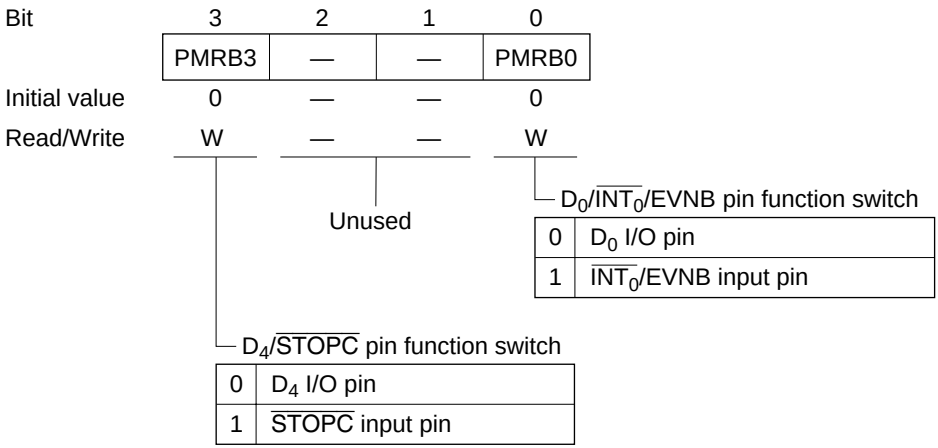
	Bit	3	2	1	0
DCD1: $02D		—	—	DCD11	DCD10
	Initial value	—	—	0	0
	Read/Write	—	—	W	W

Bits in DCD0 and DCD1	Description
0	The CMOS output buffer is turned off and the output goes to the high impedance state. (initial value)
1	The output buffer is turned on and the value in the corresponding PDR is output.

The bits in DCD0 and DCD1 correspond to the D port pins as shown in the table.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCD0	D_3	D_2	D_1	D_0
DCD1	—	—	D_5	D_4

(3) Port Mode Register B (PMRB: $024): PMRB is a 2-bit write-only register that switches the D port I/O pin shared functions.



Bit 3—D_4/$\overline{\text{STOPC}}$ Pin Function Switch (PMRB3): Selects whether the D_4/$\overline{\text{STOPC}}$ pin is used as the D_4 I/O pin or as the stop mode clear pin ($\overline{\text{STOPC}}$).

PMRB3	**Description**	
0	The D_4/$\overline{\text{STOPC}}$ pin functions as the D_4 I/O pin.	(initial value)
1	The D_4/$\overline{\text{STOPC}}$ pin functions as the $\overline{\text{STOPC}}$ input pin.	

Bit 0—D_0/$\overline{\text{INT}_0}$/EVNB Pin Function Switch (PMRB0): Selects whether the D_0/$\overline{\text{INT}_0}$/EVNB pin is used as the D_0 I/O pin or as the $\overline{\text{INT}_0}$/EVNB input pin.

PMRB0	**Description**	
0	The D_0/$\overline{\text{INT}_0}$/EVNB pin functions as the D_0 I/O pin.	(initial value)
1	The D_0/$\overline{\text{INT}_0}$/EVNB pin functions as the $\overline{\text{INT}_0}$/EVNB input pin.	

Refer to section 18.2.2, “Timer Mode Register B2 (TMB2)”, for details on switching between the $\overline{\text{INT}_0}$ and EVNB functions.

8.2.3 Pin Functions

The functions of the pins D0 to D5 are switched by the bits in registers PMRA and PMRB as shown in table 8-6.

Table 8-6 D Port Pin Functions

<table>
<tr><th>Pin</th><th>Pin Functions and Selection Methods</th></tr>
<tr><td>$D_0/\overline{INT_0}$/EVNB</td><td>The pin function is switched as shown below by the PMRB PMRB0 bit and the DCD0 DCD00 bit.
<table>
<tr><td>PMRB0</td><td colspan="2">0</td><td>1</td></tr>
<tr><td>DCD00</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td>Pin function</td><td>D_0 input pin</td><td>D_0 output pin</td><td>$\overline{INT_0}$/EVNB input pin*</td></tr>
</table>
Note: * To use this pin as the EVNB pin, mask the $\overline{INT_0}$ interrupt by setting the $\overline{INT_0}$ interrupt mask (IM0: $000,3) to 1.</td></tr>
<tr><td>D_1</td><td>The pin function is switched as shown below by the DCD0 DCD01 bit.
<table>
<tr><td>DCD01</td><td>0</td><td>1</td></tr>
<tr><td>Pin function</td><td>D_1 input pin</td><td>D_1 output pin</td></tr>
</table></td></tr>
<tr><td>D_2</td><td>The pin function is switched as shown below by the DCD0 DCD02 bit.
<table>
<tr><td>DCD02</td><td>0</td><td>1</td></tr>
<tr><td>Pin function</td><td>D_2 input pin</td><td>D_2 output pin</td></tr>
</table></td></tr>
<tr><td>D_3</td><td>The pin function is switched as shown below by the DCD0 DCD03 bit.
<table>
<tr><td>DCD03</td><td>0</td><td>1</td></tr>
<tr><td>Pin function</td><td>D_3 input pin</td><td>D_3 output pin</td></tr>
</table></td></tr>
<tr><td>$D_4/\overline{STOPC}$</td><td>The pin function is switched as shown below by the PMRB PMRB3 bit and the DCD1 DCD10 bit.
<table>
<tr><td>PMRB3</td><td colspan="2">0</td><td>1</td></tr>
<tr><td>DCD10</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td>Pin function</td><td>D_4 input pin</td><td>D_4 output pin</td><td>$\overline{STOPC}$ input pin</td></tr>
</table></td></tr>
<tr><td>D5</td><td>The pin function is switched as shown below by the DCD1 DCD11 bit.
<table>
<tr><td>DCD11</td><td>0</td><td>1</td></tr>
<tr><td>Pin function</td><td>D_5 input pin</td><td>D_5 output pin</td></tr>
</table></td></tr>
</table>

8.3 R Ports

8.3.1 Overview

The R port consists of the three 4-bit I/O ports and one 3-bit port, ports R0 to R3. These ports are accessed in 4-bit units.

Ports R0 and R3 are standard voltage I/O ports, $R1_0$ to $R1_2$ are medium voltage NMOS open drain I/O ports, and $R1_3$ and R2 are standard voltage NMOS open drain I/O ports.

The individual ports R0 to R3 are accessed in 4-bit units with the LRA and LRB output instructions to control the output levels (high or low) on each pin. Output data is stored in the PDR built into each pin. Similarly, the LAR and LBR input instructions can be used to access the R ports in 4-bit units to read the input levels on the port pins.

DCR registers are used to control the port R0 to R3 output buffer on/off states. When the DCR bit corresponding to a pin in one of the ports R0 to R3 is set to 1, the data in the corresponding PDR is output from that pin. Thus the output buffer on/off states can be controlled on an individual pin basis for the R port pins. The DCR registers are allocated in the RAM address space.

The pins in ports R1 and R2 are high current pins that can accept current influxes of up to 15 mA.

The R0 and R3 port pins have shared functions as built-in peripheral module pins. Register settings are used to switch these functions. (See table 8-7.)

Figure 8-2 shows the R port pin structure.

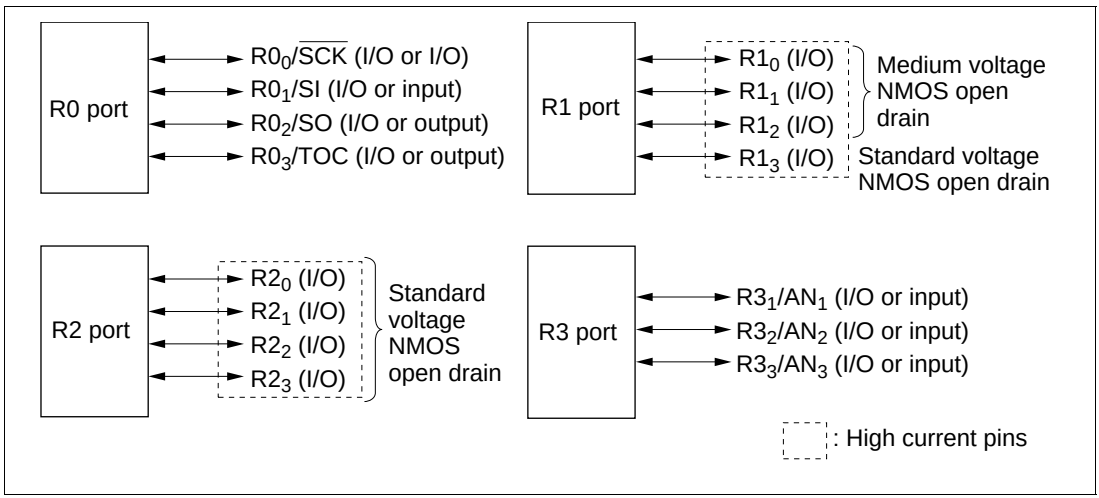


Figure 8-2 R Port Structure

8.3.2 Register Configuration and Descriptions

Table 8-7 shows the configuration of the R port related registers,

Table 8-7 R Port Register Configuration

Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	1
$030	Data control registers	DCR0	W	$0
$031		DCR1	W	$0
$032		DCR2	W	$0
$033		DCR3	W	$0
$004	Port mode register A	PMRA	W	$0
$005	Serial mode register	SMR	W	$0
$019	A/D mode register 1	AMR1	W	$0

Note: * The LRA and LRB instructions are used to write to the PDR registers.

(1) Port Data Registers (PDR): All the I/O pins in ports R0 to R3 include a PDR that holds the output data. When an LRA or an LRB instruction is executed for one of ports R0 to R3, the contents of the accumulator (A) or the B register (B) are transferred to the specified R port PDRs. When the corresponding bit in DCR0 to DCR3 for the specified port is 1, the output buffers for the corresponding pins will be turned on and the values in the PDRs will be output from the pins.

The PDR registers are set to 1 on reset and in stop mode.

(2) Data Control Registers (DCR0 to DCR3: $030, $031, $032, $033)

DCR0: $030	Bit	3	2	1	0
		DCR03	DCR02	DCR01	DCR00
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

DCR1: $031	Bit	3	2	1	0
		DCR13	DCR12	DCR11	DCR10
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

DCR2: $032	Bit	3	2	1	0
		DCR23	DCR22	DCR21	DCR20
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

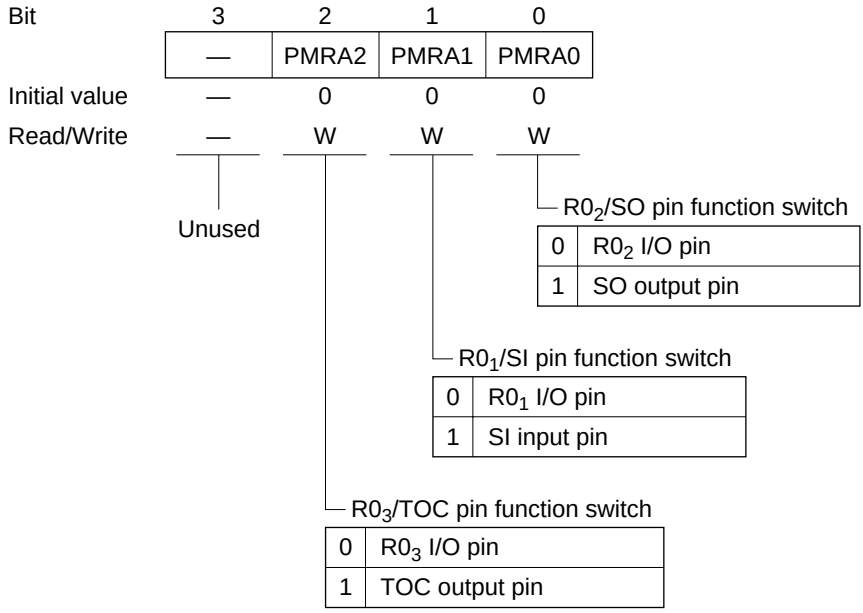
DCR3: $033	Bit	3	2	1	0
		DCR33	DCR32	DCR31	—
	Initial value	0	0	0	—
	Read/Write	W	W	W	—

Bits in DCR0 to DCR3	Description
0	The output buffer (CMOS buffer) is turned off and the output goes to the high impedance state. (initial value)
1	• CMOS three state outputs: the buffer is turned on and the corresponding PDR value is output. • NMOS open drain pins: A low level is output when the PDR is set to 0, and the pin goes to the high impedance state when the PDR is set to 1.

The table below lists the correspondence between the bits in DCR0 to DCR3 and the port R0 to R3 pins.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	—

(3) Port Mode Register A (PMRA: $004): PMRA is a 3-bit write-only register whose bits PMRA2 to PMRA0 switch the functions of the port R0 shared function pins.



Bit 2—$R0_3$/TOC Pin Function Switch (PMRA2): Selects whether the $R0_3$/TOC pin functions as the $R0_3$ input pin or as the timer C output pin (TOC).

PMRA2	Description	
0	The $R0_3$/TOC pin functions as the $R0_3$ I/O pin.	(initial value)
1	The $R0_3$/TOC pin functions as the TOC output pin.	

Bit 1— $R0_1$/SI Pin Function Switch (PMRA1): Selects whether the $R0_1$/SI pin functions as the $R0_1$ I/O pin or as the serial reception data input pin (SI).

PMRA1	Description	
0	The $R0_1$/SI pin functions as the $R0_1$ I/O pin.	(initial value)
1	The $R0_1$/SI pin functions as the SI input pin.	

Bit 0—$R0_2$/SO Pin Function Switch (PMRA0): Selects whether the $R0_2$/SO pin functions as the $R0_2$ I/O pin or as the serial transmission data output pin (SO).

PMRA0	Description	
0	The $R0_2$/SO pin functions as the $R0_2$ I/O pin.	(initial value)
1	The $R0_2$/SO pin functions as the SO output pin.	

(4) Serial Mode Register (SMR: $005): SMR is a 4-bit write-only register whose SMR3 bit switches the $R0_0$/$\overline{SCK}$ pin function.

This section only describes the SMR3 bit. See section 20.2.1, “Serial Mode Register (SMR)” for details on bits SMR2 to SMR0.

Bit	3	2	1	0
	SMR3	SMR2	SMR1	SMR0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Transfer clock selection

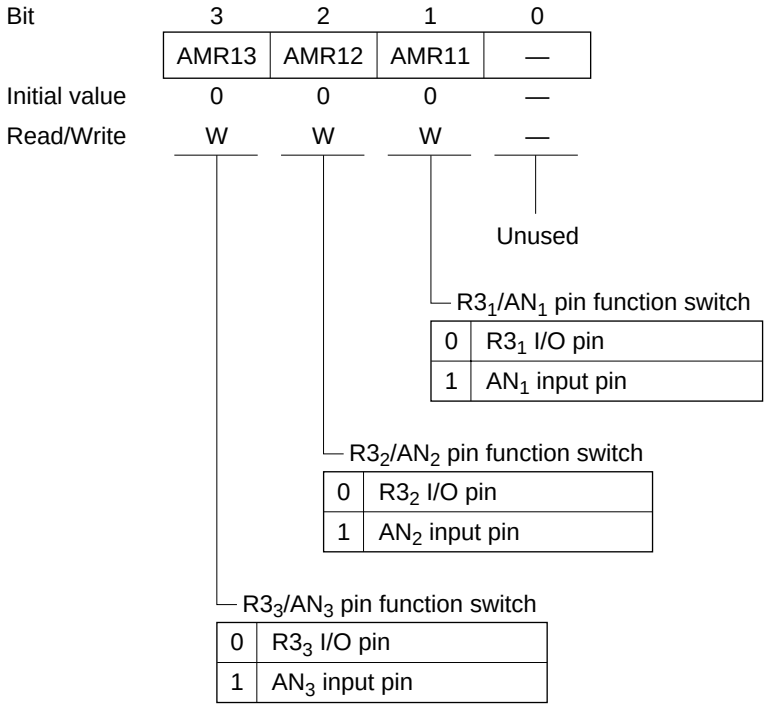
$R0_0$/$\overline{SCK}$ pin function switch

0	$R0_0$ I/O pin
1	$\overline{SCK}$ I/O pin

Bit 3—$R0_0$/$\overline{SCK}$ Pin Function Switch (SMR3): Selects whether the $R0_0$/$\overline{SCK}$ pin functions as the $R0_0$ I/O pin or as the serial interface transfer clock I/O pin.

SMR3	Description	
0	The $R0_0$/$\overline{SCK}$ pin functions as the $R0_0$ I/O pin.	(initial value)
1	The $R0_0$/$\overline{SCK}$ pin functions as the $\overline{SCK}$ I/O pin.	

(5) A/D Mode Register 1 (AMR1: $019): AMR1 is a 3-bit write-only register that switches the functions of the R3 port shared function pins.



Bit 3—R3$_3$/AN$_3$ Pin Function Switch (AMR13): Selects whether the R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin or as the A/D converter channel 3 input pin AN$_3$.

AMR13	Description	
0	The R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin.	(initial value)
1	The R3$_3$/AN$_3$ pin functions as the AN$_3$ input pin.	

Bit 2—$R3_2/AN_2$ Pin Function Switch (AMR12): Selects whether the $R3_2/AN_2$ pin functions as the $R3_2$ I/O pin or as the A/D converter channel 2 input pin AN_2.

AMR12	Description	
0	The $R3_2/AN_2$ pin functions as the $R3_2$ I/O pin.	(initial value)
1	The $R3_2/AN_2$ pin functions as the AN_2 input pin.	

Bit 1— $R3_1/AN_1$ Pin Function Switch (AMR11): Selects whether the $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin or as the A/D converter channel 1 input pin AN_1.

AMR11	Description	
0	The $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin.	(initial value)
1	The $R3_1/AN_1$ pin functions as the AN_1 input pin.	

8.3.3 Pin Functions

The pin functions of the R port pins are switched by register settings as shown in table 8-8.

Table 8-8 R Port Pin Functions

Pin	Pin Functions and Selection Methods
$R0_0/\overline{SCK}$	The pin function is switched by the SMR SMR3 bit and the DCR0 DCR00 bit as shown below.

SMR3	0		1
DCR00	0	1	—
Pin function	$R0_0$ input pin	$R0_0$ output pin	$\overline{SCK}$ I/O pin

$R0_1$/SI	The pin function is switched by the PMRA PMRA1 bit and the DCR0 DCR01 bit as shown below.

PMRA1	0		1
DCR01	0	1	—
Pin function	$R0_1$ input pin	$R0_1$ output pin	SI input pin

$R0_2$/SO	The pin function is switched by the PMRA PMRA0 bit and the DCR0 DCR02 bit as shown below.

PMRA0	0		1
DCR02	0	1	—
Pin function	$R0_2$ input pin	$R0_2$ output pin	SO output pin

$R0_3$/TOC	The pin function is switched by the PMRA PMRA2 bit and the DCR0 DCR03 bit as shown below.

PMRA2	0		1
DCR03	0	1	—
Pin function	$R0_3$ input pin	$R0_3$ output pin	TOC output pin

Table 8-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R1_0$	The pin function is switched by the DCR1 DCR10 bit as shown below.

DCR10	0	1
Pin function	$R1_0$ input pin	$R1_0$ output pin*1

$R1_1$	The pin function is switched by the DCR1 DCR11 bit as shown below.

DCR11	0	1
Pin function	$R1_1$ input pin	$R1_1$ output pin*1

$R1_2$	The pin function is switched by the DCR1 DCR12 bit as shown below.

DCR12	0	1
Pin function	$R1_2$ input pin	$R1_2$ output pin*1

$R1_3$	The pin function is switched by the DCR1 DCR13 bit as shown below.

DCR13	0	1
Pin function	$R1_3$ input pin	$R1_3$ output pin*2

$R2_0$	The pin function is switched by the DCR2 DCR20 bit as shown below.

DCR20	0	1
Pin function	$R2_0$ input pin	$R2_0$ output pin*2

$R2_1$	The pin function is switched by the DCR2 DCR21 bit as shown below.

DCR21	0	1
Pin function	$R2_1$ input pin	$R2_1$ output pin*2

$R2_2$	The pin function is switched by the DCR2 DCR22 bit as shown below.

DCR22	0	1
Pin function	$R2_2$ input pin	$R2_2$ output pin*2

$R2_3$	The pin function is switched by the DCR2 DCR23 bit as shown below.

DCR23	0	1
Pin function	$R2_3$ input pin	$R2_3$ output pin*2

Notes on next page.

Notes: 1. $R1_0$ to $R1_2$ are medium voltage NMOS open drain I/O pins. These pins go to the high impedance state when their PDR is set to 1.

2. $R1_3$ and $R2_0$ to $R2_3$ are standard voltage NMOS open drain I/O pins. These pins go to the high impedance state when their PDR is set to 1.

Table 8-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R3_1/AN_1$	The pin function is switched by the AMR1 AMR11 bit and the DCR3 DCR31 bit as shown below.

AMR11	0		1
DCR31	0	1	—
Pin function	$R3_1$ input pin	$R3_1$ output pin	AN_1 input pin

Pin	Pin Functions and Selection Methods
$R3_2/AN_2$	The pin function is switched by the AMR1 AMR12 bit and the DCR3 DCR32 bit as shown below.

AMR12	0		1
DCR32	0	1	—
Pin function	$R3_2$ input pin	$R3_2$ output pin	AN_2 input pin

Pin	Pin Functions and Selection Methods
$R3_3/AN_3$	The pin function is switched by the AMR1 AMR13 bit and the DCR3 DCR33 bit as shown below.

AMR13	0		1
DCR33	0	1	—
Pin function	$R3_3$ input pin	$R3_3$ output pin	AN_3 input pin

8.4 Usage Notes

Keep the following points in mind when using the I/O ports.

- When the MIS MIS2 bit is set to 1, the $R0_2$/SO pin will be an NMOS open drain output regardless of whether it is selected for use as the $R0_2$ pin or as the SO pin by the PMRA PMRA0 bit.

- I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can cause the LSI to operate incorrectly.

  The built-in pull-up MOS transistors can be used to pull up unused pins to V_{CC}. Alternatively, unused pins can be pulled up to V_{CC} with external resistors of about 100 kΩ.

  Application programs should maintain the PDR and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

- When the MIS MIS3 bit is set to 1 (pull-up MOS transistors active) and the PDR for an R port/analog input shared function pin has the value 1, the MOS transistor for the corresponding pin will not be turned off by selecting the analog input function with the AMR1 register.

  To use an R port/analog input shared function pin as an analog input when the pull-up MOS transistors are active, always clear the PDR for the corresponding pin to 0 first and then turn off the pull-up MOS transistor. (Note that the PDR registers are set to 1 immediately following a reset.)

  Figure 8-3 shows the circuit for the R port/analog input shared function pins.

  AMR1 is used to set the port outputs to high impedance. ACR is used to switch the analog input channel.

  The states of the R port/analog input shared function pins are set, as shown in table 8-9, by the combination of the AMR1 register, the MIS3 bit, the DCR, and the PDR settings.

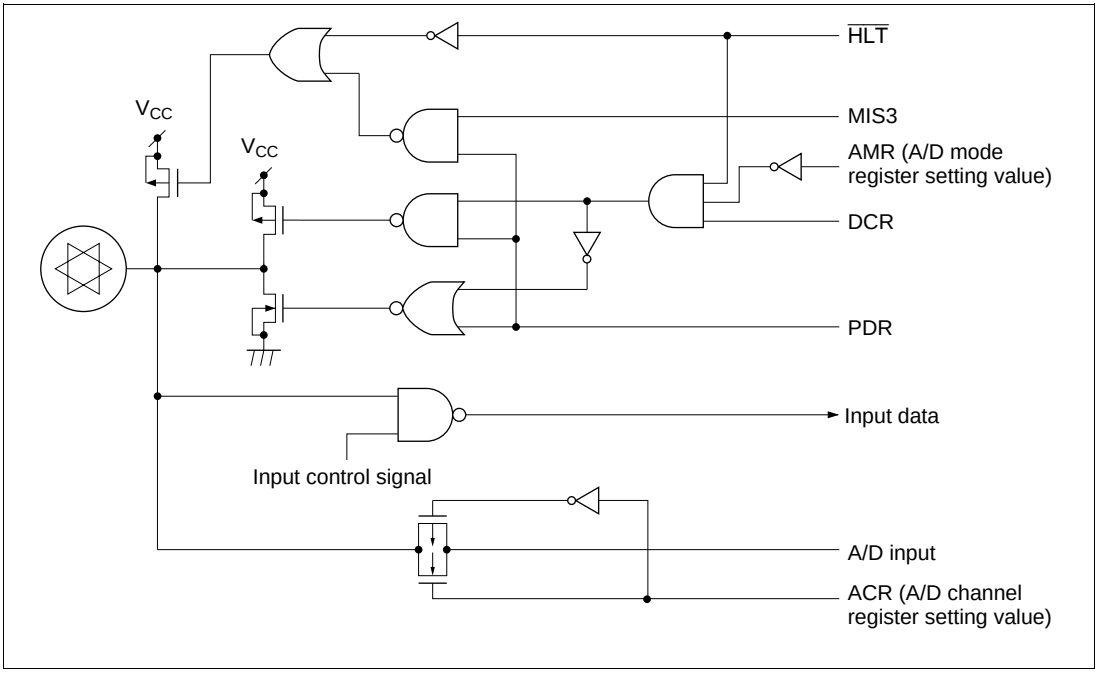


Figure 8-3 R Port/Analog Input Shared Function Pin Circuit

Table 8-9 Program Control of the R Port/Analog Input Shared Function Pins

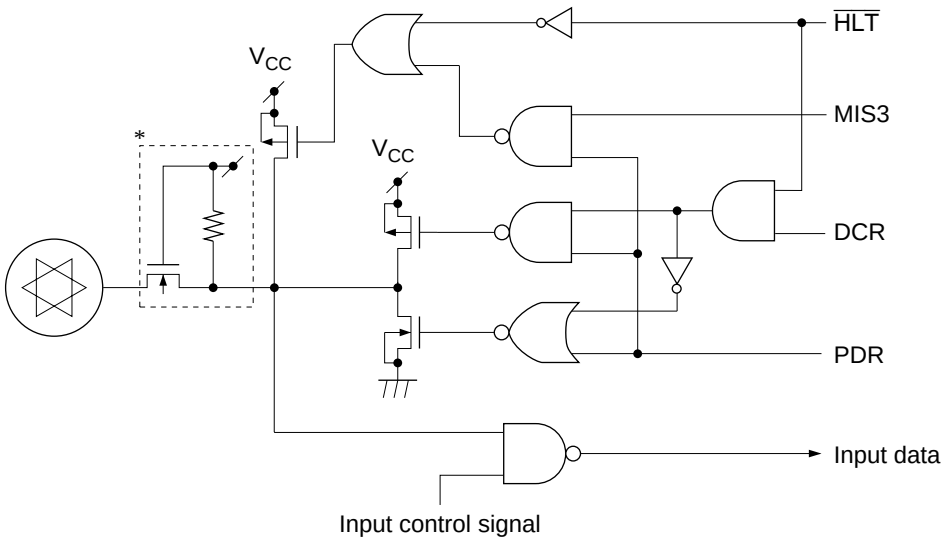
Corresponding bit in AMR1		0 (R port selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Note: —: off

Corresponding bit in AMR1		1 (analog input selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	—	—		—	—
	NMOS			—	—			—	—
Pull-up MOS transistor		—				—	On	—	On

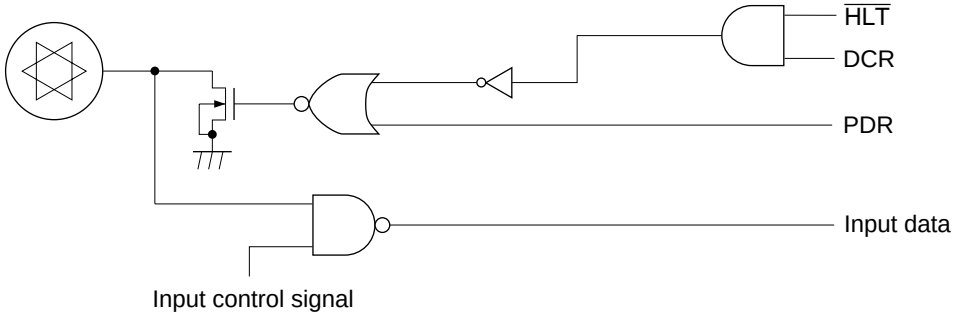
Note: —: off

- In the HD404394 Series evaluation chip set, the circuits for the medium voltage NMOS open drain pins ($R1_0$ to $R1_2$) and the standard voltage NMOS open drain pins ($R1_3$ and $R2_0$ to $R2_3$) differ from the ZTAT™ and the mask ROM microcomputer versions as shown in figure 8-4. Although the outputs in both the ZTAT™ and mask ROM versions can be set to high impedance by the combinations listed in table 8.10, the $R1_0$ to $R1_2$ outputs cannot be set to high impedance in the evaluation chip set. Also note that the $R1_3$ and $R2_0$ to $R2_3$ outputs go to the high level when both the corresponding DCR and PDR are 1. Please keep this in mind when using the evaluation chip set.



Note: * Only included in the $R1_0$ to $R1_2$ pin circuits. Does not appear in the $R1_3$ and $R2_0$ to $R2_3$ pin circuits.

(a) Evaluation Chip Pin Circuit Structure



(b) ZTAT™ and Mask ROM Pin Circuit Structure

Figure 8-4 Medium Voltage NMOS Open Drain Pin Circuits

Table 8-10 ZTAT™ and Mask ROM Microcomputer NMOS Open Drain Pin High Impedance Control

DCR	PDR	Description	
0	*	High impedance output	(initial value)
1	0	NMOS buffer on. Low level output	
	1	High impedance output	

Note: * Don’t care

Section 9 I/O Ports (HD404318 Series)

9.1 Overview

9.1.1 Features

The HD404318 Series I/O ports have the following features.

- The nine pins D_0 to D_8 as well as the R1, R2, and R8 ports are high voltage I/O pins. Also, RA_1 is a high voltage input pin. R0, R3, and R4 are standard voltage I/O pins that, in output mode, are CMOS three state outputs.
- Certain I/O pins (D_0 to D_4, and the pins in the R0, R3, and R4 ports) are shared with the built-in peripheral modules, such as timers and the serial interface. Setting these pins for use with the built-in peripheral modules takes priority over their setting for use as D or R port pins.
- Register settings are used to select input or output for I/O pins and to select the I/O port or peripheral module usage for shared function pins.
- Of the built-in peripheral module pins, the D_3/BUZZ pin is a PMOS open drain output. All other output pins are CMOS outputs. However, the $R0_2$/SO pin can be selected to be an NMOS open drain output by setting a register.
- Since the system is reset in stop mode, the built-in peripheral module selections are cleared and the I/O pins go to the high impedance state.
- The CMOS output pins have built-in programmable pull-up MOS transistors. The on/off state of these transistors can be controlled by register settings on an individual basis. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 9-1 provides an overview of the HD404318 Series port functions.

Table 9-1 Port Functions

Port	Overview	Pin	Shared Function	Function Switching Register
D_0 to D_8	• High voltage I/O port • Accessed in bit units • Accessed with the SED, SEDD, RED, REDD, TD, and TDD instructions. • Pull-down resistors available as a mask option.	$D_0/\overline{INT}_0$	External interrupt input 0	PMRB
		$D_1/\overline{INT}_1$	External interrupt input 1	
		D_2/EVNB	Timer B event input	
		D_3/BUZZ	Alarm output	PMRA
		$D_4/\overline{STOPC}$	Stop mode clear	PMRB
		D_5 to D_8	—	—
R0	• Standard voltage I/O ports • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions. • Programmable pull-up MOS transistors	$R0_0/\overline{SCK}$	Transfer clock I/O	SMR
		$R0_1$/SI	Serial reception data input	PMRA
		$R0_2$/SO	Serial transmission data output	
		$R0_3$/TOC	Timer C output	
R3		$R3_0/AN_0$	Analog input channel 0	AMR1
		$R3_1/AN_1$	Analog input channel 1	
		$R3_2/AN_2$	Analog input channel 2	
		$R3_3/AN_3$	Analog input channel 3	
R4		$R4_0/AN_4$	Analog input channel 4	AMR2
		$R4_1/AN_5$	Analog input channel 5	
		$R4_2/AN_6$	Analog input channel 6	
		$R4_3/AN_7$	Analog input channel 7	

Table 9-1 Port Functions (cont)

Port	Overview	Pin	Shared Function	Function Switching Register
R1	• High voltage I/O ports • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions. • Pull-down resistors available as a mask option.	$R1_0$	—	—
		$R1_1$		
		$R1_2$		
		$R1_3$		
R2		$R2_0$	—	—
		$R2_1$		
		$R2_2$		
		$R2_3$		
R8		$R8_0$	—	—
		$R8_1$		
		$R8_2$		
		$R8_3$		
RA	• High voltage input port (1 bit) • Accessed with the LAR and LBR instructions.	RA_1/V_{disp}	High voltage pin output power supply	Mask option

9.1.2 I/O Control

The D, R1, R2, and R8 ports are high voltage I/O ports, RA_1 is a 1-bit high voltage input port, and R0, R3, and R4 are standard voltage I/O ports. The different port types have different circuit structures as follows.

(1) High Voltage I/O Pin Circuit: The D, R1, R2, and R8 port pins are high voltage I/O pins that have no I/O switching function. When a port data register is set to 1, the PMOS transistor turns on and a high level voltage is output from the pin. When the PDR is set to 0, the pin goes to the open state. If the built-in pull-down resistor mask option was selected, the V_{disp} voltage is output. When external signals are applied, applications must set the PDR value to 0 so that the external (input) and internal (output) signals do not collide at the pin.

Note that there are no pull-down resistors on the high voltage I/O pins in the ZTAT™ versions of these microcomputers.

(2) Standard Voltage CMOS Three State I/O Pin Circuit: The pins in the R0, R3, and R4 ports are standard voltage CMOS three state I/O ports. I/O through these ports is controlled by the PDRs and the data control registers (DCR). When the DCR bit corresponding to a given pin is 1, that pin functions as an output pin and outputs the value in the PDR. When a given DCR bit is 0, the corresponding pin functions as an input pin.

(3) Pull-Up MOS Control: Each I/O pin in the R0, R3, and R4 ports has a built-in programmable pull-up MOS transistor. When the miscellaneous register (MIS) MIS3 bit is set to 1 the pull-up MOS transistor for pins for which the corresponding PDR is set to 1 will be turned on. Thus the on/off state of each pin can be controlled independently by the PDRs. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 9-2 shows how register settings control the port I/O pins.

Table 9-2 Register Settings for I/O Pin Control

MIS3		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Notes: 1. —: Off
2. The PDR registers are not allocated addresses in RAM. The PDR registers are accessed by special-purpose I/O instructions.

(4) Miscellaneous Register (MIS: $00C): MIS is a 2-bit write-only register that controls the on/off states of the R0, R3, and R4 port pin pull-up MOS transistors and the on/off state of the $R0_2$/SO pin output buffer PMOS transistor. MIS is initialized to $0 on reset and in stop mode.

Bit	3	2	1	0
	MIS3	MIS2	—	—
Initial value	0	0	—	—
Read/Write	W	W	—	—

Unused

$R0_2$/SO pin output buffer control

0	PMOS transistor active (CMOS output)
1	PMOS transistor off (NMOS open drain output)

Pull-up MOS transistor control

0	All pull-up MOS transistors off
1	Pull-up MOS transistors active

Bit 3—Pull-Up MOS Transistor Control (MIS3): Controls the on/off states of the pull-up MOS transistors built into the I/O port pins.

MIS3	Description	
0	All pull-up MOS transistors will be turned off.	(initial value)
1	Pull-up MOS transistors for which the corresponding PDR bit is 1 will be turned on.	

Bit 2—$R0_2$/SO Pin Output Buffer Control (MIS2): Controls the on/off state of the $R0_2$/SO pin output buffer PMOS transistor.

MIS2	Description	
0	The $R0_2$/SO pin output will be a CMOS output.	(initial value)
1	The $R0_2$/SO pin output will be an NMOS open drain output.	

9.1.3 I/O Pin Circuit Structures

Table 9-3 shows the port and peripheral module pin circuits.

Notes: 1. Since the system is reset in stop mode, the built-in peripheral module selections are cleared. Since the internal $\overline{HLT}$ signal goes to the low (active) level, the I/O pins go to the high impedance state. Also, all the pull-up MOS transistors are turned off.

2. In all low power modes other than stop mode, the internal $\overline{HLT}$ signal goes to the high level.

Table 9-3 Input and Output Pin Circuits

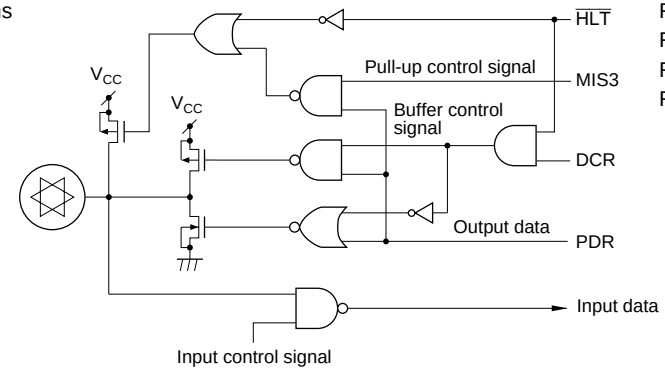
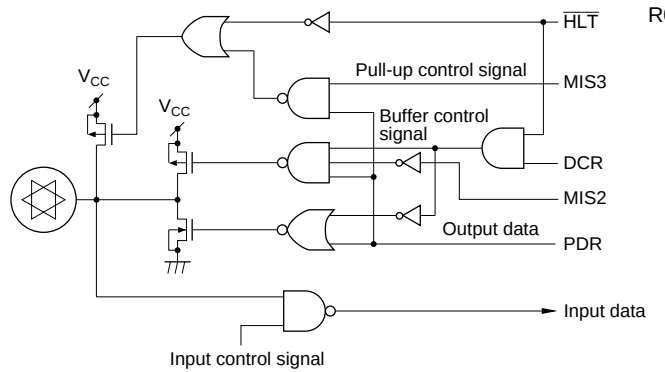
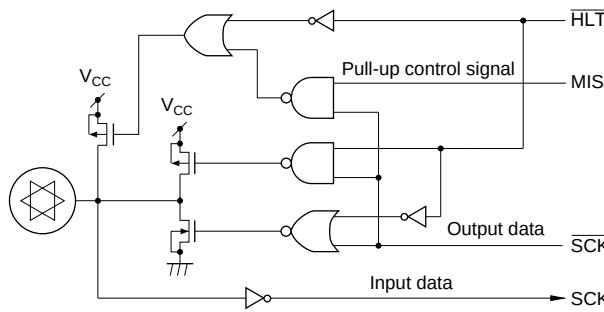
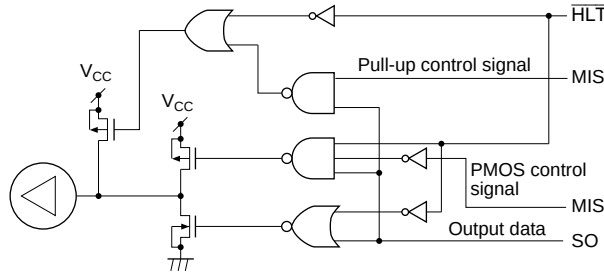
Class	Circuit	Applicable Pins
Standard voltage pins I/O pins		$R0_0$, $R0_1$, $R0_3$, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$
		$R0_2$

Table 9-3 Input and Output Pin Circuits (cont)

Class		Circuit	Applicable Pins
Standard voltage pins	Standard peripheral module pins	I/O pins	$\overline{SCK}$
		Output pins	SO
			TOC





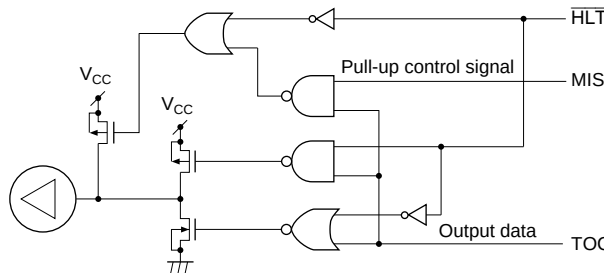


Table 9-3 Input and Output Pin Circuits (cont)

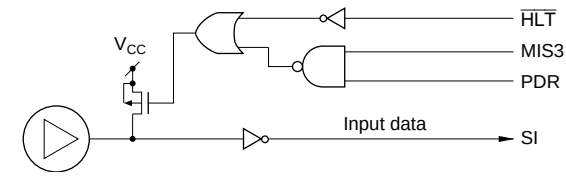
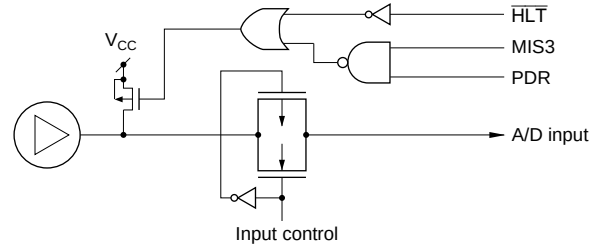
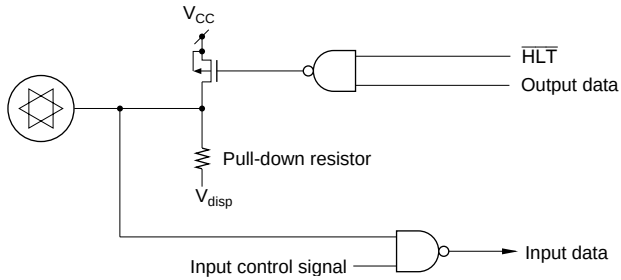
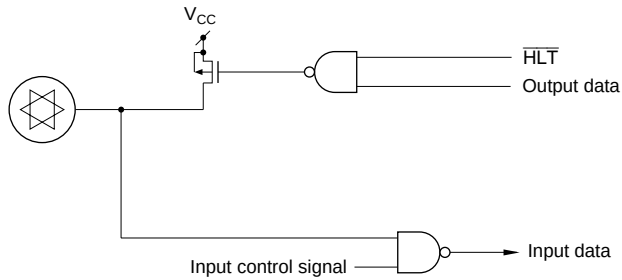
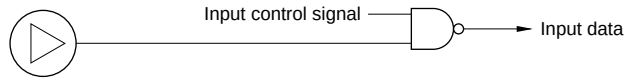
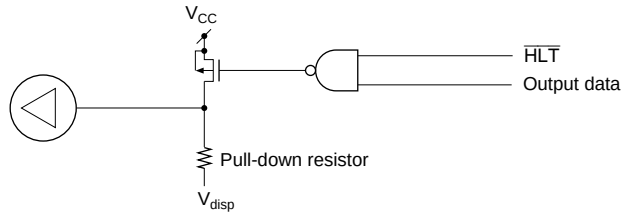
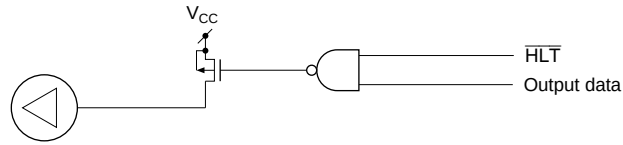
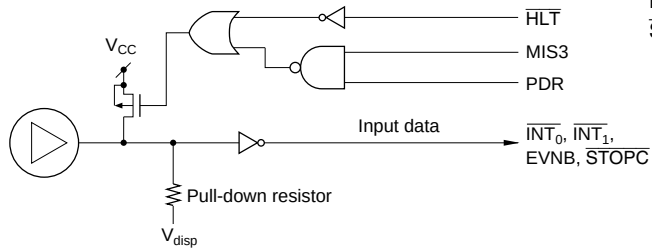
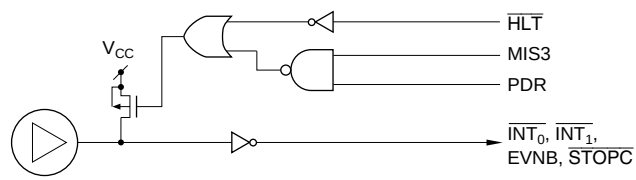
Class			Circuit	Applicable Pins
Standard voltage pins	Built-in peripheral module pins	Input pins		SI
				AN_0 to AN_7

Table 9-3 Input and Output Pin Circuits (cont)

Class	Circuit	Applicable Pins
High voltage pins	I/O pins Pins with pull-down resistors	D_0 to D_8, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$, $R8_0$ to $R8_3$
		
	Pins without pull-down resistors*	
		
	Input pin	RA_1
		

Note: * The ZTAT™ versions of these microcomputers only support pins without pull-down resistors.

Table 9-3 Input and Output Pin Circuits (cont)

Class			Circuit	Applicable Pins
High voltage pins	Built-in peripheral module pins	Output pins	Pins with pull-down resistors	BUZZ
				
			Pins without pull-down resistors*	
				
		Input pins	Pins with pull-down resistors	$\overline{INT}_0$, $\overline{INT}_1$, EVNB, $\overline{STOPC}$
				
			Pins without pull-down resistors*	
				

Note: * The ZTAT™ versions of these microcomputers only support pins without pull-down resistors.

9.1.4 Port States in Low Power Modes

The D_0 to D_4 pins and the R0, R3, and R4 port pins have shared functions as input or output pins for built-in peripheral modules. In standby mode, since the CPU stops, the pins selected as output ports maintain their immediately prior output values. Also, pins selected for use by built-in peripheral modules that operate in standby mode continue to operate. (Output pins used by modules that stop in standby mode maintain their immediately prior output values.) See section 5, “Low Power Modes”, for details on which built-in peripheral modules can operate in each mode.

Table 9-4 lists the port states in the low power modes.

Table 9-4 Port States in Low Power Modes

Low Power Mode	Port States
Standby mode	Pins maintain their values immediately prior to entering standby mode.
Stop mode	Built-in peripheral function selections are cleared, and the port and peripheral function I/O pins go to the high impedance state.

9.1.5 Handling Unused Pins

I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation. The following are examples of techniques that can prevent noise problems.

High voltage pin: Select “no pull-down MOS transistor (PMOS open drain)” as the mask option and connect the pin to V_{CC} on the user system printed circuit board.

Standard voltage pin: Either use the built-in pull-up MOS transistor to pull the pin up to V_{CC}, or pull up the pin to V_{CC} externally with a pull-up resistor of about 100 kΩ.

Application programs should maintain the PDR and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

9.2 D Port

9.2.1 Overview

The D port is a 9-pin high voltage I/O port (D_0 to D_8) that can be accessed in 1-bit units.

The output levels on the pins D_0 to D_8 can be set to low or high by accessing the port in one-bit units with the SED, SEDD, RED, and REDD output instructions. The output data is stored in the PDR for each pin. The level on each of the pins D_0 to D_8 can be tested in one-bit units with the TD and TDD input instructions.

The pins D_0 to D_4 have shared functions as built-in peripheral module pins. PMRA and PMRB are used to switch these functions.

Figure 9-1 shows the structure of the D port.

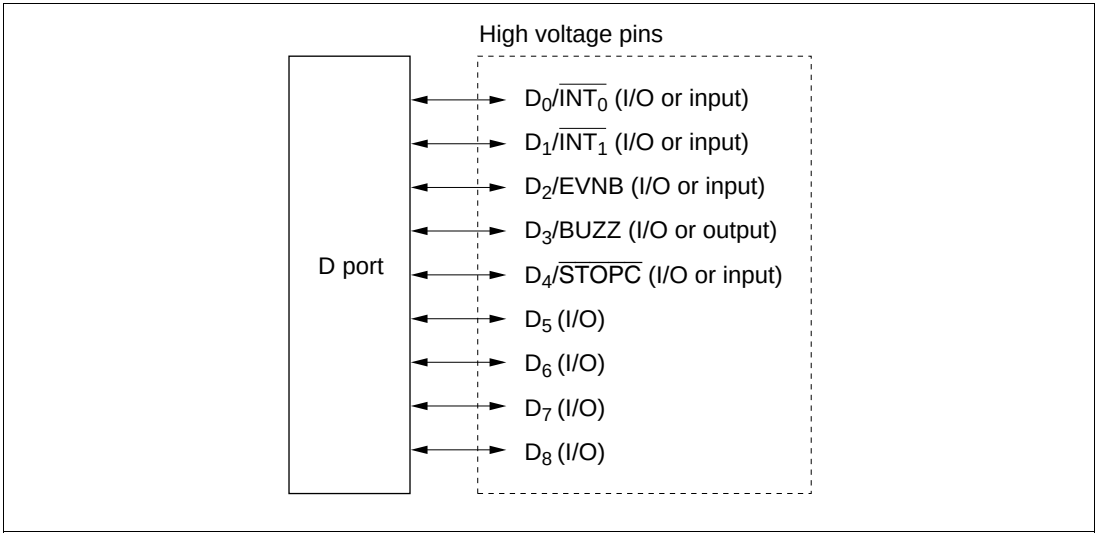


Figure 9-1 D Port Structure

9.2.2 Register Configuration and Descriptions

Table 9-5 shows the configuration of the D port registers.

Table 9-5 D Port Register Configuration

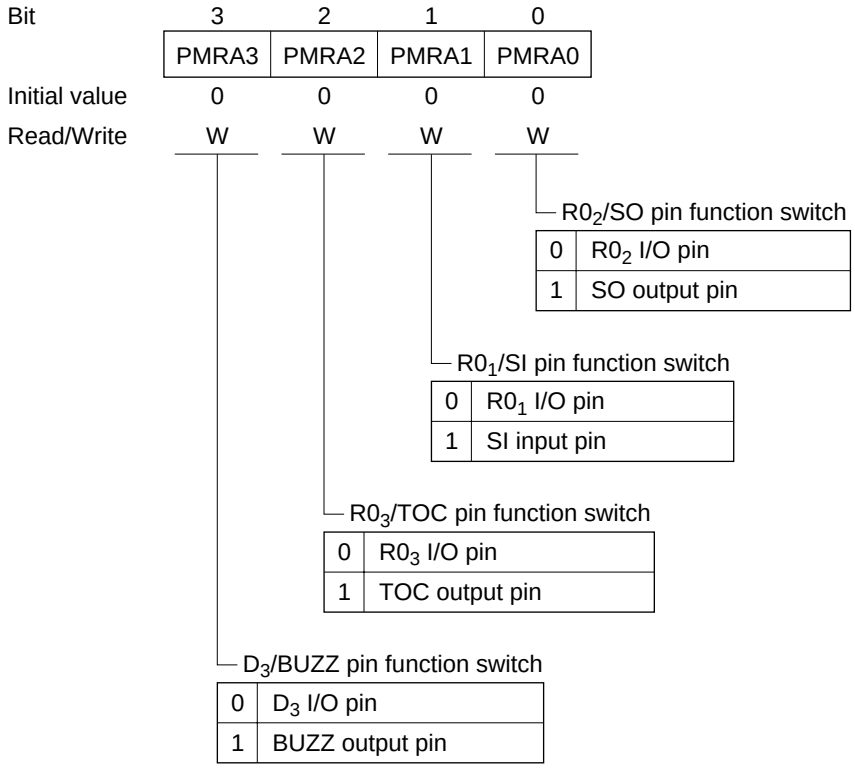
Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	0
$004	Port mode register A	PMRA	W	$0
$024	Port mode register B	PMRB	W	$0

Note: * The SED, SEDD, RED, and REDD instructions can be used to write to the PDRs.

(1) Port Data Registers (PDR): Each of the I/O pins D_0 to D_8 includes a built-in PDR that stores the output data. When a SED or SEDD instruction is executed for one of the pins D_0 to D_8 the corresponding PDR is set to 1, and when a RED or REDD instruction is executed, the corresponding PDR is cleared to 0.

The PDRs are cleared to 0 on reset and in stop mode.

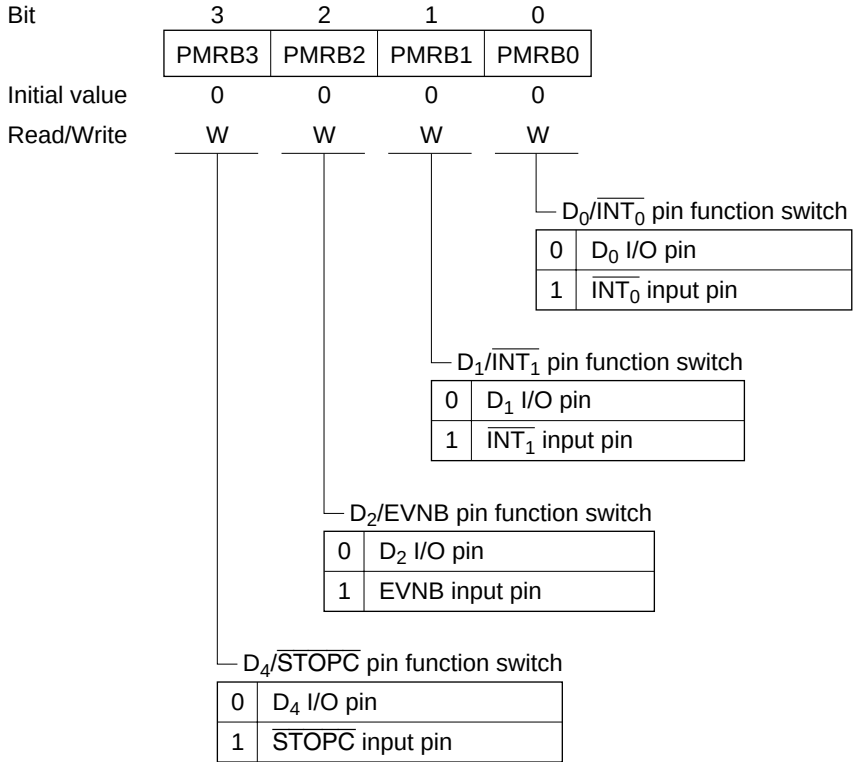
(2) Port Mode Register A (PMRA: $004): PMRA is a 4-bit write-only register whose PMRA3 bit switches the function of the D_3/BUZZ pin. This section describes the function of the PMRA3 bit. See section 9.3.2 (3), “Port Mode Register A (PMRA)”, for details on the PMRA2 to PMRA0 bits.



Bit 3—D_3/BUZZ Pin Function Switch (PMRA3): Selects whether the D_3/BUZZ pin functions as the D_3 input pin or as the alarm output pin (BUZZ).

PMRA3	Description	
0	D_3/BUZZ pin functions as the D_3 I/O pin.	(initial value)
1	D_3/BUZZ pin functions as the BUZZ output pin.	

(3) Port Mode Register B (PMRB: $024): PMRB is a 4-bit write-only register that switches the D port I/O pin shared functions.



Bit 3—D_4/$\overline{\text{STOPC}}$ Pin Function Switch (PMRB3): Selects whether the D_4/$\overline{\text{STOPC}}$ pin is used as the D_4 I/O pin or as the stop mode clear pin ($\overline{\text{STOPC}}$).

PMRB3	Description	
0	The D_4/$\overline{\text{STOPC}}$ pin functions as the D_4 I/O pin.	(initial value)
1	The D_4/$\overline{\text{STOPC}}$ pin functions as the $\overline{\text{STOPC}}$ input pin.	

Bit 2—D_2/EVNB Pin Function Switch (PMRB2): Selects whether the D_2/EVNB pin is used as the D_2 I/O pin or as the timer B event count input pin (EVNB).

PMRB2	Description	
0	The D_2/EVNB pin functions as the D_2 I/O pin.	(initial value)
1	The D_2/EVNB pin functions as the EVNB input pin.	

Bit 1—$D_1/\overline{INT}_1$ Pin Function Switch (PMRB1): Selects whether the $D_1/\overline{INT}_1$ pin is used as the D_1 I/O pin or as external interrupt 1 input pin ($\overline{INT}_1$).

PMRB1	Description	
0	The $D_1/\overline{INT}_1$ pin functions as the D_1 I/O pin.	(initial value)
1	The $D_1/\overline{INT}_1$ pin functions as the $\overline{INT}_1$ input pin.	

Bit 0—$D_0/\overline{INT}_0$ Pin Function Switch (PMRB0): Selects whether the $D_0/\overline{INT}_0$ pin is used as the D_0 I/O pin or as external interrupt 0 input pin ($\overline{INT}_0$).

PMRB0	Description	
0	The $D_0/\overline{INT}_0$ pin functions as the D_0 I/O pin.	(initial value)
1	The $D_0/\overline{INT}_0$ pin functions as the $\overline{INT}_0$ input pin.	

9.2.3 Pin Functions

The functions of the pins D_0 to D_4 are switched by register PMRA and PMRB settings as shown in table 9-6.

Table 9-6 D_0 to D_4 Port Pin Functions

Pin	Pin Functions and Selection Methods		
$D_0/\overline{INT_0}$	The pin function is switched as shown below by the PMRB PMRB0 bit.		
	PMRB0	0	1
	Pin function	D_0 I/O pin	$\overline{INT_0}$ input pin
$D_1/\overline{INT_1}$	The pin function is switched as shown below by the PMRB PMRB1 bit.		
	PMRB1	0	1
	Pin function	D_1 I/O pin	$\overline{INT_1}$ input pin
D_2/EVNB	The pin function is switched as shown below by the PMRB PMRB2 bit.		
	PMRB2	0	1
	Pin function	D_2 I/O pin	EVNB input pin
D_3/BUZZ	The pin function is switched as shown below by the PMRA PMRA3 bit.		
	PMRA3	0	1
	Pin function	D_3 I/O pin	BUZZ output pin
$D_4/\overline{STOPC}$	The pin function is switched as shown below by the PMRB PMRB3 bit.		
	PMRB3	0	1
	Pin function	D_4 I/O pin	$\overline{STOPC}$ input pin

9.3 R Ports

9.3.1 Overview

The R port consists of the six 4-bit I/O ports R0 to R4 and R8 and the 1-bit input port RA_1. These ports are accessed in 4-bit units.

R0, R3, and R4 are standard voltage I/O ports. RA is a high voltage input port and R1, R2 and R8 are high voltage I/O ports that can directly drive fluorescent display tubes.

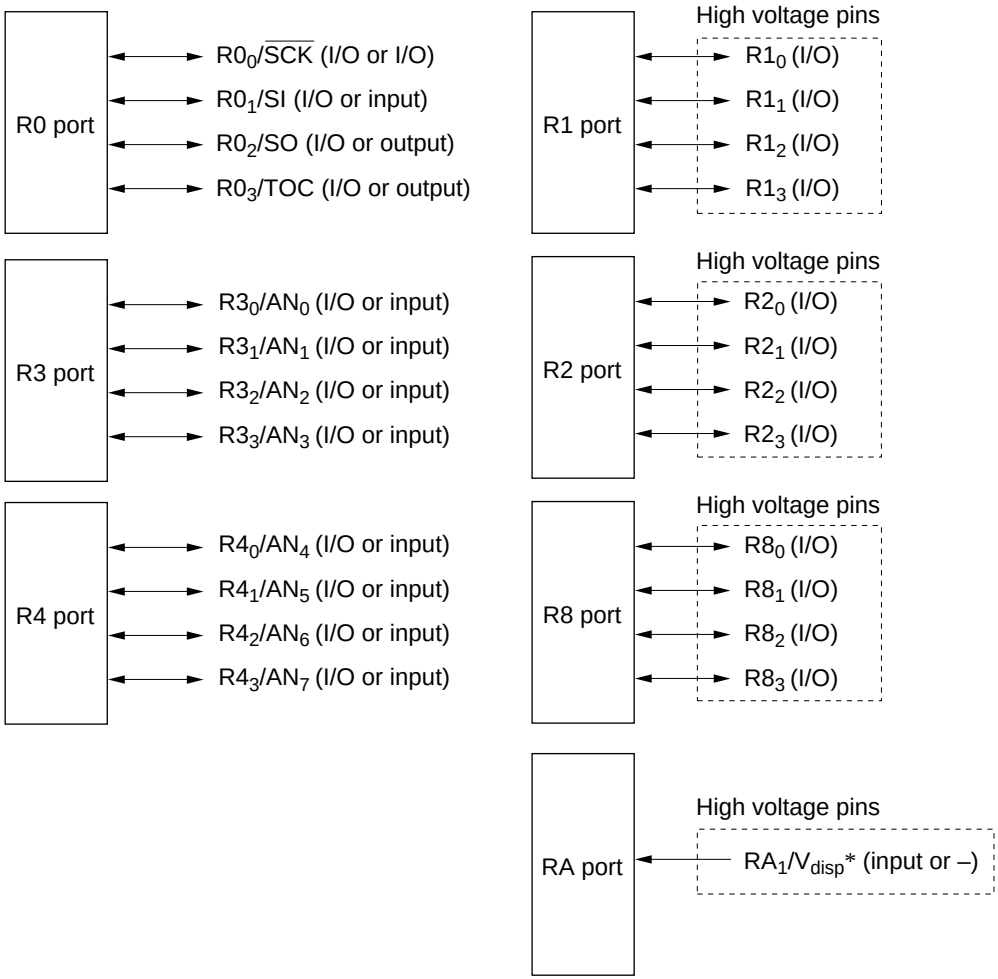
The individual ports R0 to R4 and R8 are accessed in 4-bit units with the LRA and LRB output instructions to control the output levels (high or low) on each pin. Output data is stored in the PDR built into each pin. Similarly, the LAR and LBR input instructions can be used to access the R ports in 4-bit units to read the input levels on the port pins.

The RA_1 input-only port consists of a single bit. The values of bits 3, 2, and 0 are undefined when this port is accessed by the input instructions.

DCR registers are used to control on/off states of the R0, R3, and R4 output buffers. When the DCR bit corresponding to a pin in an R0, R3, or R4 port is set to 1, the contents of the PDR corresponding to that pin is output from the pin. Thus the output buffer on/off states can be controlled on an individual pin basis for the R port pins. The DCR registers are allocated in the RAM address space.

The R0, R3, and R4 port pins have shared functions as built-in peripheral module pins. Register settings are used to switch these functions. (See table 9-7.)

Figure 9-2 shows the R port pin structure.



Note: * In products with on-chip mask resistors, the use of this pin as the V_{disp} pin (display power supply pin) can be selected as a mask option.
High voltage pins for which a pull-down MOS transistor is selected are pulled down to the V_{disp} potential.

Figure 9-2 R Port Structure

9.3.2 Register Configuration and Descriptions

Table 9-7 shows the configuration of the R port related registers.

Table 9-7 R Port Register Configuration

Address	Register		Symbol	R/W	Initial Value
—	Port data registers	Standard voltage pins	PDR	W*	1
		High voltage pins			0
$030	Data control registers		DCR0	W	$0
$033			DCR3	W	$0
$034			DCR4	W	$0
$004	Port mode register A		PMRA	W	$0
$005	Serial mode register		SMR	W	$0
$019	A/D mode register 1		AMR1	W	$0
$01A	A/D mode register 2		AMR2	W	--00

Note: * The LRA and LRB instructions are used to write to the PDR registers.

(1) Port Data Registers (PDR): All the I/O pins in ports R0 to R4 and R8 include a PDR that holds the output data. When an LRA or an LRB instruction is executed for one of ports R0 to R4 or R8, the contents of the accumulator (A) or the B register (B) are transferred to the specified R port PDRs. When bits in DCR0, DCR3, or DCR4 are set to 1, the output buffers for the corresponding pins in port R0, R3 or R4 will be turned on and the values in the PDRs will be output from those pins.

The PDR registers for standard voltage pins are set to 1 on reset and in stop mode, and the PDRs for high voltage pins are cleared to 0.

(2) Data Control Registers (DCR0, DCR3, DCR4: $030, $033, $034)

	Bit	3	2	1	0
DCR0: $030		DCR03	DCR02	DCR01	DCR00
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

	Bit	3	2	1	0
DCR3: $033		DCR33	DCR32	DCR31	DCR30
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

	Bit	3	2	1	0
DCR4: $034		DCR43	DCR42	DCR41	DCR40
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

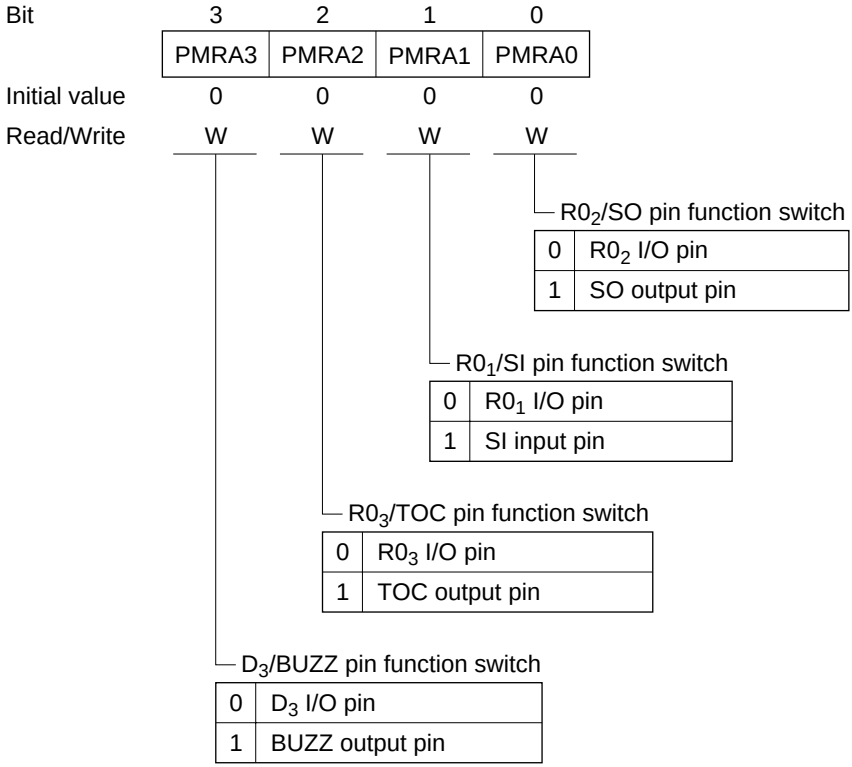
Bits in DCR0, DCR3, and DCR4	Description
0	The output buffer (CMOS buffer) is turned off and the output goes to the high impedance state. (initial value)
1	The output buffer is turned on and the corresponding PDR value is output.

The table below lists the correspondence between the bits in DCR0, DCR3, and DCR4 and the port R0, R3, and R4 pins.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$

(3) Port Mode Register A (PMRA: $004): PMRA is a 4-bit write-only register whose bits PMRA2 to PMRA0 switch the functions of the port R0 shared function pins.

This section describes the bits PMRA2 to PMRA0. See section 9.2.2 (2), “Port Mode Register A (PMRA)”, for details on the PMRA3 bit.



Bit 2—R0$_3$/TOC Pin Function Switch (PMRA2): Selects whether the R0$_3$/TOC pin functions as the R0$_3$ I/O pin or as the timer C output pin (TOC).

PMRA2	Description	
0	The R0$_3$/TOC pin functions as the R0$_3$ I/O pin.	(initial value)
1	The R0$_3$/TOC pin functions as the TOC output pin.	

Bit 1—$R0_1$/SI Pin Function Switch (PMRA1): Selects whether the $R0_1$/SI pin functions as the $R0_1$ I/O pin or as the serial reception data input pin (SI).

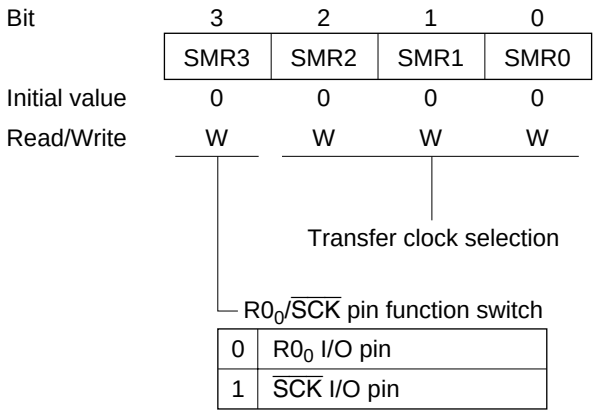
PMRA1	Description	
0	The $R0_1$/SI pin functions as the $R0_1$ I/O pin.	(initial value)
1	The $R0_1$/SI pin functions as the SI input pin.	

Bit 0—$R0_2$/SO Pin Function Switch (PMRA0): Selects whether the $R0_2$/SO pin functions as the $R0_2$ I/O pin or as the serial transmission data output pin (SO).

PMRA0	Description	
0	The $R0_2$/SO pin functions as the $R0_2$ I/O pin.	(initial value)
1	The $R0_2$/SO pin functions as the SO output pin.	

(4) Serial Mode Register (SMR: $005): SMR is a 4-bit write-only register whose SMR3 bit switches the $R0_0$/$\overline{SCK}$ pin function.

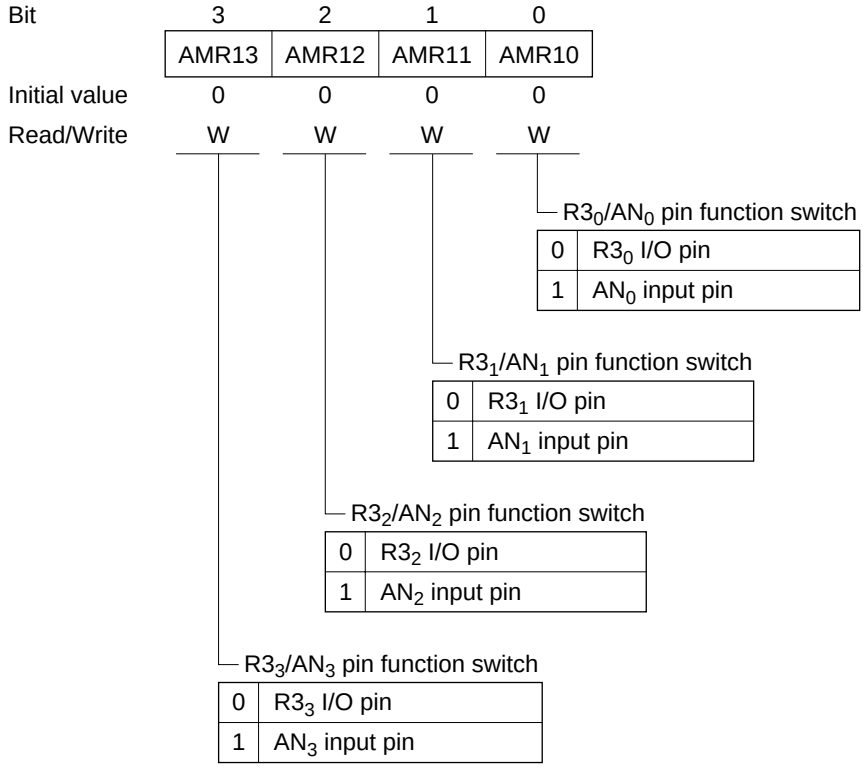
This section only describes the SMR3 bit. See section 20.2.1, “Serial Mode Register (SMR)” for details on bits SMR2 to SMR0.



Bit 3—$R0_0$/$\overline{SCK}$ Pin Function Switch (SMR3): Selects whether the $R0_0$/$\overline{SCK}$ pin functions as the $R0_0$ I/O pin or as the serial interface transfer clock I/O pin ($\overline{SCK}$).

SMR3	Description	
0	The $R0_0$/$\overline{SCK}$ pin functions as the $R0_0$ I/O pin.	(initial value)
1	The $R0_0$/$\overline{SCK}$ pin functions as the $\overline{SCK}$ I/O pin.	

(5) A/D Mode Register 1 (AMR1: $019): AMR1 is a 4-bit write-only register that switches the functions of the R3 port shared function pins.



Bit 3—R3$_3$/AN$_3$ Pin Function Switch (AMR13): Selects whether the R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin or as the A/D converter channel 3 input pin AN$_3$.

AMR13	Description	
0	The R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin.	(initial value)
1	The R3$_3$/AN$_3$ pin functions as the AN$_3$ input pin.	

Bit 2—R3$_2$/AN$_2$ Pin Function Switch (AMR12): Selects whether the R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin or as the A/D converter channel 2 input pin AN$_2$.

AMR12	Description	
0	The R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin.	(initial value)
1	The R3$_2$/AN$_2$ pin functions as the AN$_2$ input pin.	

Bit 1—$R3_1/AN_1$ Pin Function Switch (AMR11): Selects whether the $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin or as the A/D converter channel 1 input pin AN_1.

AMR11	Description	
0	The $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin.	(initial value)
1	The $R3_1/AN_1$ pin functions as the AN_1 input pin.	

Bit 0—$R3_0/AN_0$ Pin Function Switch (AMR10): Selects whether the $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin or as the A/D converter channel 0 input pin AN_0.

AMR10	Description	
0	The $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin.	(initial value)
1	The $R3_0/AN_0$ pin functions as the AN_0 input pin.	

(6) A/D Mode Register 2 (AMR2: $01A): AMR2 is a 2-bit write-only register whose AMR21 bit switches the functions of all four bits of the R4 port ($R4_0$ to $R4_3$) to be A/D converter input channels (AN_4 to AN_7). This section describes the AMR21 bit. See section 15.2.2, “A/D Mode Register 2 (AMR2)”, for details on the AMR20 bit.

Bit	3	2	1	0
	—	—	AMR21	AMR20
Initial value	—	—	0	0
Read/Write	—	—	W	W

Unused

A/D conversion time

0	34 t_{cyc}
1	67 t_{cyc}

$R4_0/AN_4$ to $R4_3/AN_7$ pin function switch

0	$R4_0$ to $R4_3$ I/O pins
1	AN_4 to AN_7 input pins

Bit 1—$R4_0/AN_4$ to $R4_3/AN_7$ Pin Function Switch (AMR21): Selects whether the $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins or as the A/D converter channel 4 to 7 input pins (AN_4 to AN_7).

AMR21	Description	
0	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins.	(initial value)
1	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the AN_4 to AN_7 input pins.	

9.3.3 Pin Functions

The pin functions of the R port pins are switched by register settings as shown in table 9-8.

Table 9-8 R Port Pin Functions

Pin	Pin Functions and Selection Methods
$R_0/\overline{SCK}$	The pin function is switched by the SMR SMR3 bit and the DCR0 DCR00 bit as shown below.

SMR3	0		1
DCR00	0	1	—
Pin function	$R0_0$ input pin	$R0_0$ output pin	$\overline{SCK}$ I/O pin

$R0_1$/SI — The pin function is switched by the PMRA PMRA1 bit and the DCR0 DCR01 bit as shown below.

PMRA1	0		1
DCR01	0	1	—
Pin function	$R0_1$ input pin	$R0_1$ output pin	SI input pin

$R0_2$/SO — The pin function is switched by the PMRA PMRA0 bit and the DCR0 DCR02 bit as shown below.

PMRA0	0		1
DCR02	0	1	—
Pin function	$R0_2$ input pin	$R0_2$ output pin	SO output pin

$R0_3$/TOC — The pin function is switched by the PMRA PMRA2 bit and the DCR0 DCR03 bit as shown below.

PMRA2	0		1
DCR03	0	1	—
Pin function	$R0_3$ input pin	$R0_3$ output pin	TOC output pin

Table 9-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R3_0/AN_0$	The pin function is switched by the AMR1 AMR10 bit and the DCR3 DCR30 bit as shown below.

AMR10	0		1
DCR30	0	1	—
Pin function	$R3_0$ input pin	$R3_0$ output pin	AN_0 input pin

$R3_1/AN_1$	The pin function is switched by the AMR1 AMR11 bit and the DCR3 DCR31 bit as shown below.

AMR11	0		1
DCR31	0	1	—
Pin function	$R3_1$ input pin	$R3_1$ output pin	AN_1 input pin

$R3_2/AN_2$	The pin function is switched by the AMR1 AMR12 bit and the DCR3 DCR32 bit as shown below.

AMR12	0		1
DCR32	0	1	—
Pin function	$R3_2$ input pin	$R3_2$ output pin	AN_2 input pin

$R3_3/AN_3$	The pin function is switched by the AMR1 AMR13 bit and the DCR3 DCR33 bit as shown below.

AMR13	0		1
DCR33	0	1	—
Pin function	$R3_3$ input pin	$R3_3$ output pin	AN_3 input pin

$R4_0/AN_4$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR40 bit as shown below.

AMR21	0		1
DCR40	0	1	—
Pin function	$R4_0$ input pin	$R4_0$ output pin	AN_4 input pin

Table 9-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R4_1/AN_5$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR41 bit as shown below.

AMR21	0		1
DCR41	0	1	—
Pin function	$R4_1$ input pin	$R4_1$ output pin	AN_5 input pin

$R4_2/AN_6$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR42 bit as shown below.

AMR21	0		1
DCR42	0	1	—
Pin function	$R4_2$ input pin	$R4_2$ output pin	AN_6 input pin

$R4_3/AN_7$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR43 bit as shown below.

AMR21	0		1
DCR43	0	1	—
Pin function	$R4_3$ input pin	$R4_3$ output pin	AN_7 input pin

9.4 Usage Notes

Keep the following points in mind when using the I/O ports.

- When the MIS MIS2 bit is set to 1, the $R0_2$/SO pin will be an NMOS open drain output regardless of whether it is selected for use as the $R0_2$ pin or as the SO pin by the PMRA PMRA0 bit.

- I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation. The following are examples of techniques that can prevent noise problems.

  High voltage pin: Select “no pull-down MOS transistor (PMOS open drain)” as the mask option and connect the pin to V_{CC} on the user system printed circuit board.

  Standard voltage pin: Either use the built-in pull-up MOS transistor to pull the pin up to V_{CC}, or pull up the pin to V_{CC} externally with a pull-up resistor of about 100 kΩ.

  Application programs should maintain the PDR and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

- When the MIS MIS3 bit is set to 1 (pull-up MOS transistors active) and the PDR for an R port/analog input shared function pin has the value 1, the pull-up MOS transistor for the corresponding pin will not be turned off by selecting the analog input function with the AMR1 and AMR2 register.

  To use an R port/analog input shared function pin as an analog input when the pull-up MOS transistors are active, always clear the PDR for the corresponding pin to 0 first and then turn off the pull-up MOS transistor. (Note that the PDR registers are set to 1 immediately following a reset.)

  Figure 9-3 shows the circuit for the R port/analog input shared function pins. AMR1 and AMR2 are used to set the port outputs to high impedance. ACR is used to switch the analog input channel.

  The states of the R port/analog input shared function pins are set, as shown in table 9-9, by the combination of the AMR1 (or AMR2) register, the MIS3 bit, the DCR, and the PDR settings.

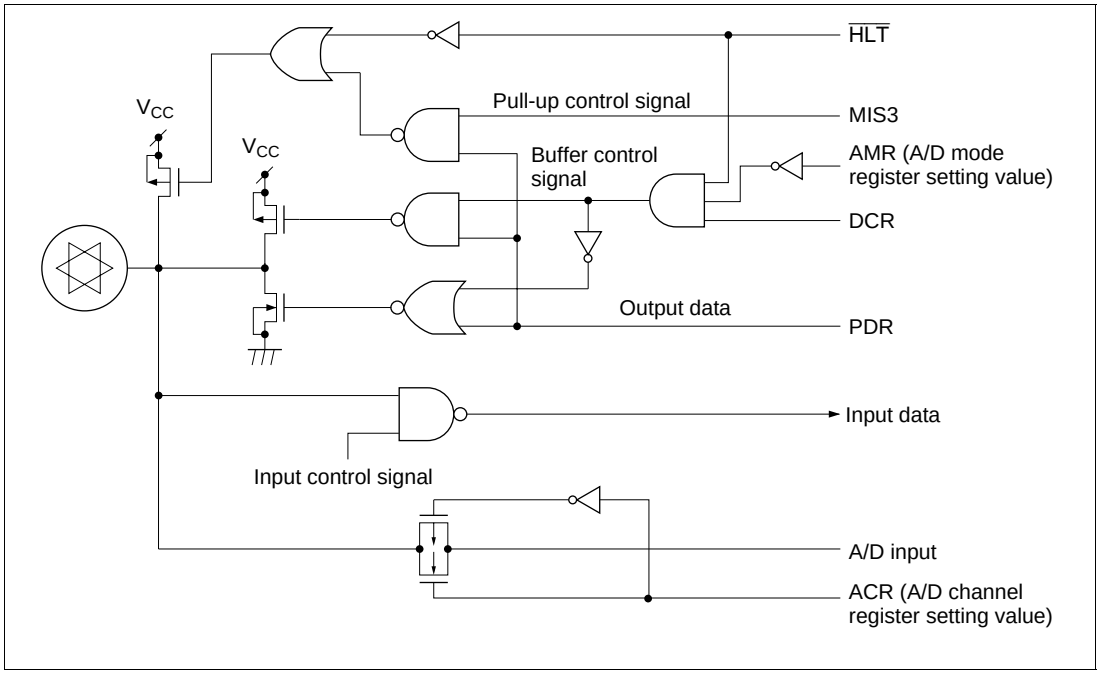


Figure 9-3 R Port/Analog Input Shared Function Pin Circuit Structure

Table 9-9 Program Control of the R Port/Analog Input Shared Use Pins

Corresponding bit in AMR1 or AMR2		0 (R port selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Note: —: off

Corresponding bit in AMR1 or AMR2		1 (analog input selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	—	—		—	—
	NMOS			—	—			—	—
Pull-up MOS transistor		—				—	On	—	On

Note: —: off

Section 10 I/O Ports (HD404358 and HD404358R Series)

10.1 Overview

10.1.1 Features

The HD404358 and HD404358R Series I/O ports have the following features.

- HD404358 Series: The four pins $R2_0$ to $R2_3$ are medium voltage NMOS open drain I/O pins. RA_1 is an input-only pin. The D, R0, R1, R3, R4, and R8 port pins are standard voltage I/O pins that, in output mode, are CMOS three state outputs.

  HD404358R Series: Pins D_0 to D_8, R0, R1, R2, R3, R4, and R8 are CMOS three state standard voltage I/O pins. Of these, 20 pins (D_5 to D_8, R0, R1, R2, and R8) can handle current levels of up to 15 mA. Also, RA_1 is an input-only pin.

- Certain I/O pins (D_0 to D_4, and the pins in the R0, R3, and R4 ports) are shared with the built-in peripheral modules, such as timers and the serial interface. Setting these pins for use with the built-in peripheral modules takes priority over their setting for use as D or R port pins.

- Register settings are used to select input or output for I/O pins and to select the I/O port or peripheral module usage for shared function pins.

- All peripheral module output pins are CMOS outputs. However, the $R0_2$/SO pin can be selected to be an NMOS open drain output by setting a register.

- Since the system is reset in stop mode, the built-in peripheral module selections are cleared and the I/O pins go to the high impedance state.

- The CMOS output pins have built-in programmable pull-up MOS transistors. The on/off state of these transistors can be controlled by register settings on an individual basis. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 10-1 provides an overview of the HD404358 Series port functions.

Table 10-1 Port Functions

Port	Overview	Pin	Shared Function	Function Switching Register
D_0 to D_8	HD404358 Series: • Standard voltage I/O port • Accessed in bit units • Accessed with the SED, SEDD, RED, REDD, TD, and TDD instructions. • Programmable pull-up MOS transistors HD404358R Series: • Standard voltage I/O port. • D_5 to D_8 is high current pins (max. 15 mA) • Accessed in bit units • Accessed with the SED, SEDD, RED, REDD, TD, and TDD instructions. • Programmable pull-up MOS transistors	$D_0/\overline{INT}_0$	External interrupt input 0	PMRB
		$D_1/\overline{INT}_1$	External interrupt input 1	
		D_2/EVNB	Timer B event input	
		D_3/BUZZ	Alarm output	PMRA
		$D_4/\overline{STOPC}$	Stop mode clear	PMRB
		D_5 to D_8	—	—

Table 10-1 Port Functions (cont)

Port	Overview	Pin	Shared Function	Function Switching Register
R0	HD404358 Series: • Standard voltage I/O port • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions.	$R0_0/\overline{SCK}$	Transfer clock I/O	SMR
		$R0_1$/SI	Serial reception data input	PMRA
		$R0_2$/SO	Serial transmission data output	
		$R0_3$/TOC	Timer C output	
R3	• Programmable pull-up MOS transistors HD404358R Series: • Standard voltage I/O port. • R0, R1, R8 is high current pins (max. 15 mA)	$R3_0/AN_0$	Analog input channel 0	AMR1
		$R3_1/AN_1$	Analog input channel 1	
		$R3_2/AN_2$	Analog input channel 2	
		$R3_3/AN_3$	Analog input channel 3	
R4		$R4_0/AN_4$	Analog input channel 4	AMR2
		$R4_1/AN_5$	Analog input channel 5	
		$R4_2/AN_6$	Analog input channel 6	
		$R4_3/AN_7$	Analog input channel 7	
R1	• Programmable pull-up MOS transistors • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions.	$R1_0$	—	—
		$R1_1$		
		$R1_2$		
		$R1_3$		
R8		$R8_0$	—	—
		$R8_1$		
		$R8_2$		
		$R8_3$		

Table 10-1 Port Functions (cont)

Port	Overview	Pin	Shared Function	Function Switching Register
R2	HD404358 Series: • Medium voltage NMOS open drain I/O port • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions. HD404358R Series: • Standard voltage I/O port. • High current pins (max. 15 mA) • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions. • Programmable pull-up MOS transistors	$R2_0$ $R2_1$ $R2_2$ $R2_3$	—	—
RA	• Standard voltage input port (1 bit) • Accessed with the LAR and LBR instructions.	RA_1	—	—

10.1.2 I/O Control

HD404358 Series: R2 is a medium voltage NMOS open drain I/O port and the D_0 to D_8, R0, R1, R3, R4 and R8 ports are standard voltage I/O ports. The different port types have different circuit structures as follows.

HD404358R Series: The D_0 to D_8, R0, R1, R2, R3, R4 and R8 are standard voltage I/O ports.

(1) Medium Voltage NMOS Open Drain I/O Pin Circuit (HD404358 Series): R2 is a medium voltage NMOS open drain I/O port and I/O through this port is controlled by the port data registers (PDR) and the data control registers (DCR). When the DCR bit corresponding to a given pin is 1, that pin functions as an output pin and when the value in the PDR is 0, the pin's NMOS transistor turns on and the pin outputs a low level voltage. When the value in the PDR is 1 the pin goes to the high impedance state. When a given DCR bit is 0, the corresponding pin functions as an input pin.

(2) Standard Voltage CMOS Three State I/O Pin Circuit: The pins in the D_0 to D_8, R0, R1, R3, R4, and R8 ports (HD404358 Series) or D_0 to D_8, R0, R1, R2, R3, R4 and R8 ports (HD404358R) are standard voltage CMOS three state I/O ports. I/O through these ports is controlled by the PDRs and the data control registers (DCD or DCR). When the DCD or DCR bit corresponding to a given pin is 1, that pin functions as an output pin and outputs the value in the PDR. When a given DCD or DCR bit is 0, the corresponding pin functions as an input pin.

(3) Pull-Up MOS Control: The I/O pins in ports D_0 to D_8 and ports R0, R1, R3, R4, and R8 (HD404358 series) have built-in programmable pull-up MOS transistors. This also applies to I/O pins in ports D_0 to D_8 and ports R0, R1, R2, R3, R4, and R8 (HD404358R series). When the miscellaneous register (MIS) MIS3 bit is set to 1 the pull-up MOS transistor for pins for which the corresponding PDR is set to 1 will be turned on. Thus the on/off state of each pin can be controlled independently by the PDRs. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

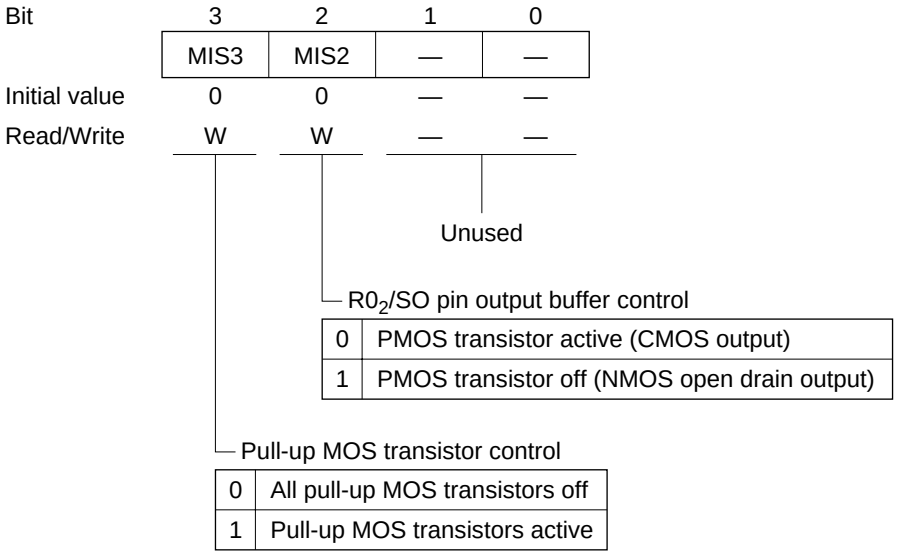
Table 10-2 shows how register settings control the port I/O pins.

Table 10-2 Register Settings for I/O Pin Control

MIS3		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Notes: 1. —: Off
2. The PDR registers are not allocated addresses in RAM. The PDR registers are accessed by special-purpose I/O instructions.

(4) Miscellaneous Register (MIS: $00C): MIS is a 2-bit write-only register that controls the on/off states of the D, R0, and R3 port pin pull-up MOS transistors and the on/off state of the $R0_2$/SO pin output buffer PMOS transistor. MIS is initialized to $0 on reset and in stop mode.



Bit 3—Pull-Up MOS Transistor Control (MIS3): Controls the on/off states of the pull-up MOS transistors built into the I/O port pins.

MIS3	Description	
0	All pull-up MOS transistors will be turned off.	(initial value)
1	Pull-up MOS transistors for which the corresponding PDR bit is 1 will be turned on.	

Bit 2—$R0_2$/SO Pin Output Buffer Control (MIS2): Controls the on/off state of the $R0_2$/SO pin output buffer PMOS transistor.

MIS2	Description	
0	The $R0_2$/SO pin output will be a CMOS output.	(initial value)
1	The $R0_2$/SO pin output will be an NMOS open drain output.	

10.1.3 I/O Pin Circuit Structures

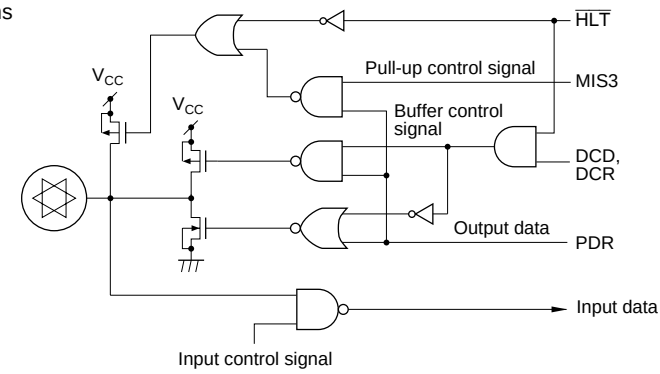
Table 10-3 shows the port and peripheral module pin circuits for the HD404358 series, and table 10-4 shows the port and peripheral module pin circuits for the HD404358R series.

Notes: 1. Since the system is reset in stop mode, the built-in peripheral module selections are cleared. Since the internal $\overline{HLT}$ signal goes to the low (active) level, the I/O pins go to the high impedance state. Also, all the pull-up MOS transistors are turned off.

2. In all low power modes other than stop mode, the internal $\overline{HLT}$ signal goes to the high level.

Table 10-3 Input and Output Pin Circuits

Class	Circuit	Applicable Pins
Standard voltage pins	I/O pins	D_0 to D_8, $R0_0$, $R0_1$, $R0_3$, $R1_0$ to $R1_3$, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$, $R8_0$ to $R8_3$
		$R0_2$



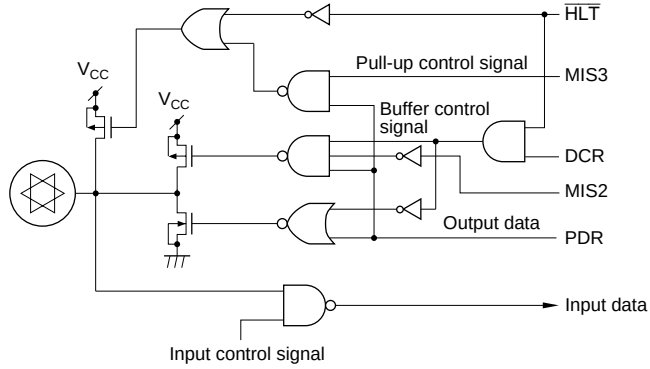


Table 10-3 Input and Output Pin Circuits (cont)

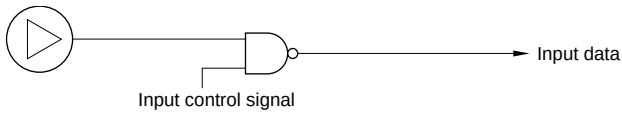
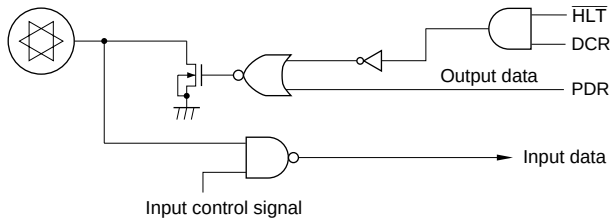
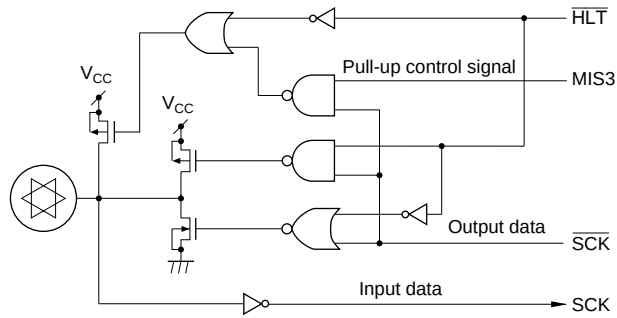
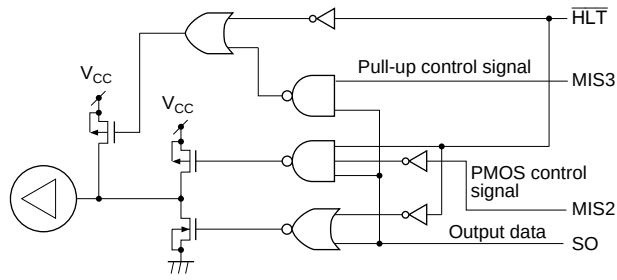
Class	Circuit	Applicable Pins
Standard voltage pins	Input pins 	RA_1
Medium voltage pins	I/O pins 	$R2_0$ to $R2_3$

Table 10-3 Input and Output Pin Circuits (cont)

Class		Circuit	Applicable Pins
Standard voltage pins	Standard peripheral module pins	I/O pins	$\overline{SCK}$
		Output pins	SO
			TOC, BUZZ





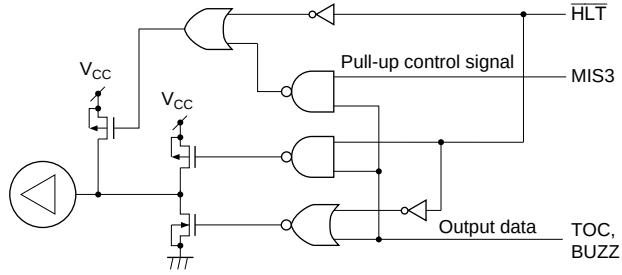


Table 10-3 Input and Output Pin Circuits (cont)

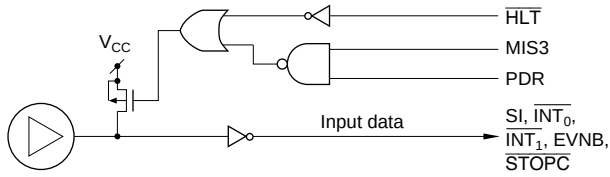
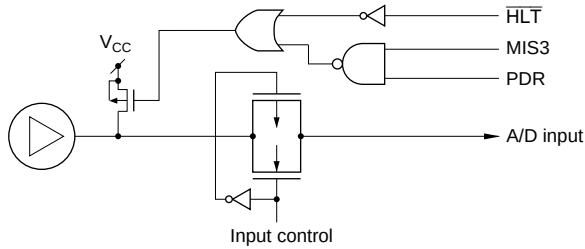
Class			Circuit	Applicable Pins
Standard voltage pins	Built-in peripheral module pins	Input pins		SI, $\overline{INT_0}$, $\overline{INT_1}$, EVNB, $\overline{STOPC}$
				AN_0 to AN_7

Table 10-4 Input and Output Pin Circuits

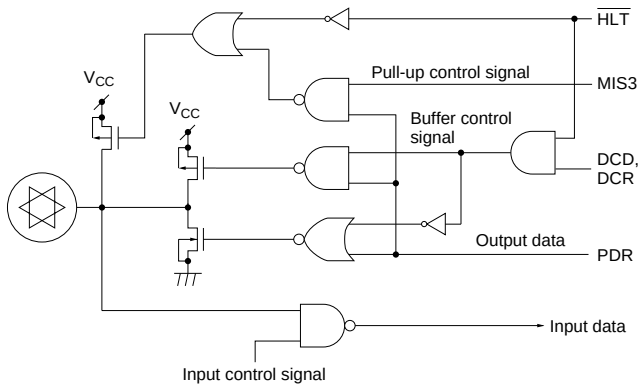
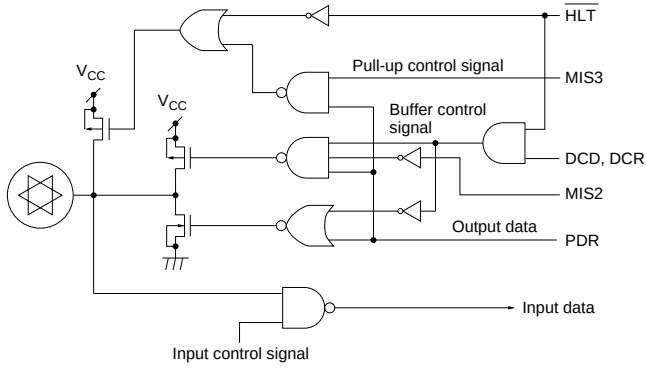
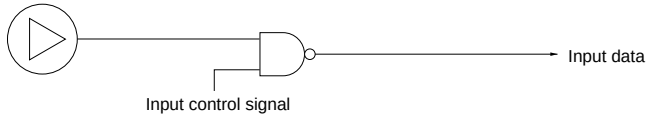
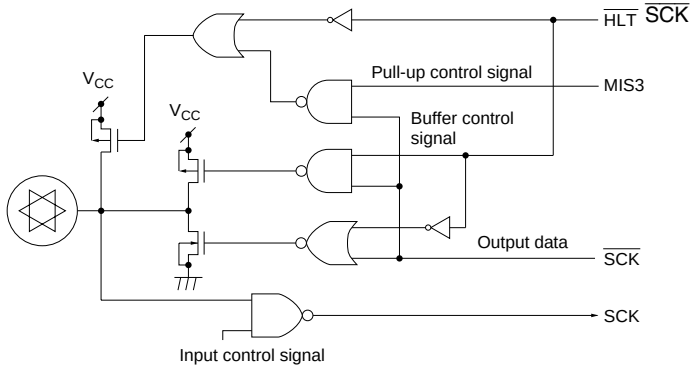
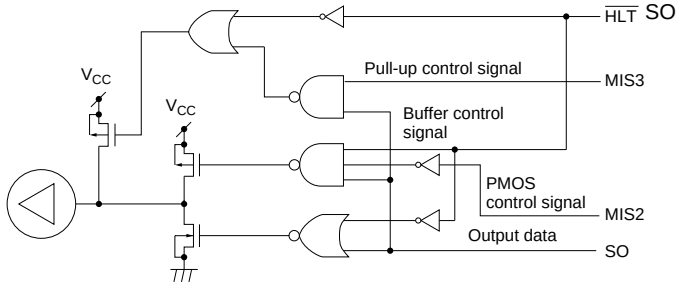
Class	Circuit	Applicable Pins
Standard voltage pins	I/O pins 	D_0 to D_8, $R0_0$, $R0_1$, $R0_3$, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$, $R8_0$ to $R8_3$
		$R0_2$
	Input pins 	RA_1

Table 10-4 Input and Output Pin Circuits (cont)

Class		Circuit	Applicable Pins
Standard voltage pins	Standard peripheral module pins	I/O pins	



Output pins



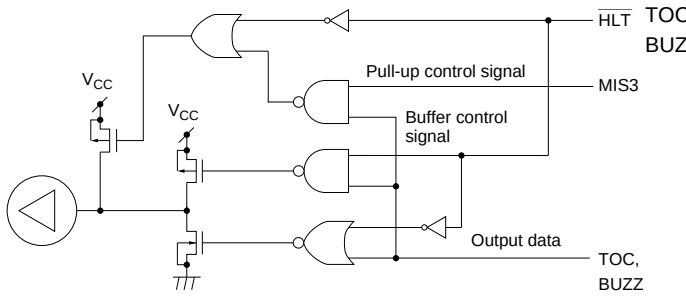
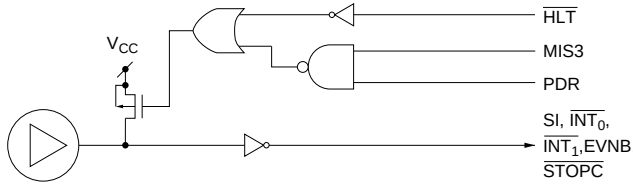
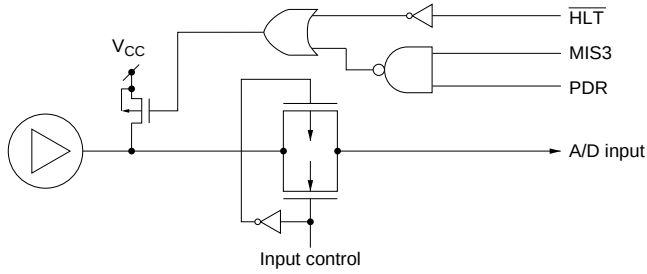


Table 10-4 Input and Output Pin Circuits (cont)

Class			Circuit	Applicable Pins
Standard voltage pins	Standard peripheral module pins	Input pins		SI, $\overline{INT_0}$, $\overline{INT_1}$, EVNB, $\overline{STOPC}$
				AN_0 to AN_7

10.1.4 Port States in Low Power Modes

The D_0 to D_4 pins and the R0, R3, and R4 port pins have shared functions as input or output pins for built-in peripheral modules. In standby mode, since the CPU stops, the pins selected as output ports maintain their immediately prior output values. Also, pins selected for use by built-in peripheral modules that operate in standby mode continue to operate. (Output pins used by modules that stop in standby mode maintain their immediately prior output values.) See section 5, “Low Power Modes”, for details on which built-in peripheral modules can operate in each mode.

Table 10-5 lists the port states in the low power modes.

Table 10-5 Port States in Low Power Modes

Low Power Mode	Port States
Standby mode	Pins maintain their values immediately prior to entering standby mode.
Stop mode	Built-in peripheral function selections are cleared, and the port and peripheral function I/O pins go to the high impedance state.

10.1.5 Handling Unused Pins

I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation.

The built-in pull-up MOS transistors can be used to pull up unused pins to V_{CC}. Alternatively, unused pins can be pulled up to V_{CC} with external resistors of about 100 k.

Application programs should maintain the PDR, DCD and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

10.2 D Port

10.2.1 Overview

The D port of the HD404358 series consists of nine I/O ports (D_0 to D_8) that can be accessed in 1-bit units.

The D port of the HD404358R series consists of nine I/O ports (D_0 to D_8; of which D_5 to D_8 are capable of handling high current levels of up to 15 mA) that can be accessed in 1-bit units.

The output levels on the pins D_0 to D_8 can be set to low or high by accessing the port in one-bit units with the SED, SEDD, RED, and REDD output instructions. The output data is stored in the PDR for each pin. The level on each of the pins D_0 to D_8 can be tested in one-bit units with the TD and TDD input instructions.

The DCD registers are used to turn the D port output buffers on or off. When the DCD bit corresponding to a given pin is 1, the data in the corresponding PDR will be output from that pin. The on/off states of the output buffers can be controlled individually for each D port pin. The DCD registers are allocated in the RAM address space.

The pins D_0 to D_4 have shared functions as built-in peripheral module pins. PMRB is used to switch these functions.

Figure 10-1 shows the structure of the D port.

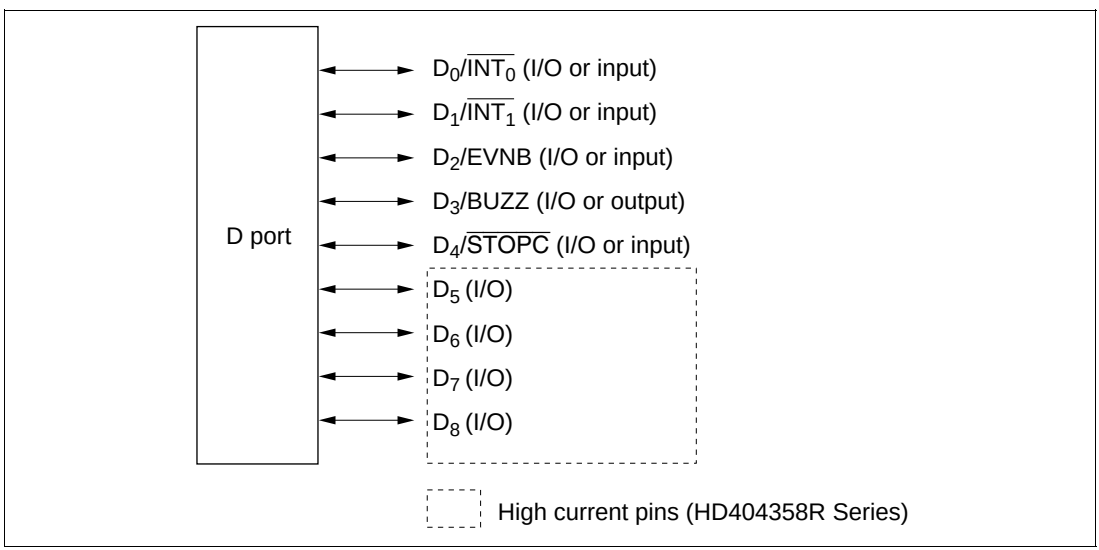


Figure 10-1 D Port Structure

10.2.2 Register Configuration and Descriptions

Table 10-6 shows the configuration of the D port registers.

Table 10-6 D Port Register Configuration

Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	1
$02C	Data control registers	DCD0	W	$0
$02D		DCD1	W	$0
$02E		DCD2	W	---0
$004	Port mode register A	PMRA	W	$0
$024	Port mode register B	PMRB	W	$0

Note: * The SED, SEDD, RED, and REDD instructions can be used to write to the PDRs.

(1) Port Data Registers (PDR): Each of the I/O pins D_0 to D_8 includes a built-in PDR. When a SED or SEDD instruction is executed for one of the pins D_0 to D_8 the corresponding PDR is set to 1, and when a RED or REDD instruction is executed, the corresponding PDR is cleared to 0. When bits in DCD0 to DCD2 are set to 1, the output buffers for the corresponding pins will be turned on and the values in the PDRs will be output from those pins.

The PDRs are cleared to 1 on reset and in stop mode.

(2) Data Control Registers (DCD0 to DCD2: $02C, $02D, $02E)

DCD0: $02C	Bit	3	2	1	0
		DCD03	DCD02	DCD01	DCD00
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

DCD1: $02D	Bit	3	2	1	0
		DCD13	DCD12	DCD11	DCD10
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

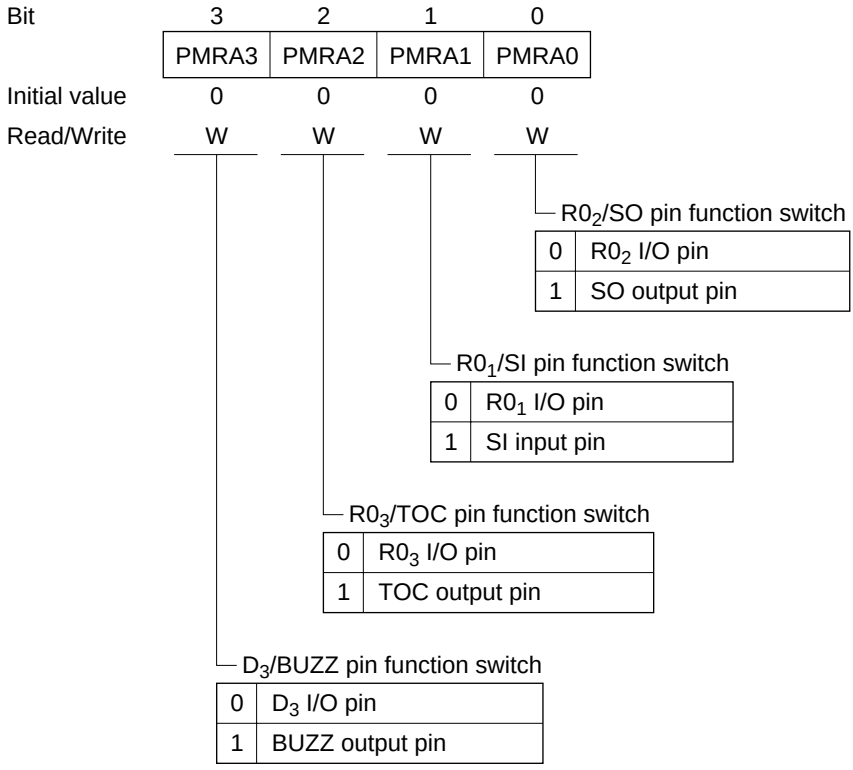
DCD2: $02E	Bit	3	2	1	0
		—	—	—	DCD20
	Initial value	—	—	—	0
	Read/Write	—	—	—	W

Bits in DCD0 to DCD2	Description
0	The output buffer (CMOS buffer) is turned off and the output goes to the high impedance state. (initial value)
1	The output buffer is turned on and the corresponding PDR value is output.

The table below lists the correspondence between the bits in DCD0 to DCD2 and the D port pins.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCD0	D_3	D_2	D_1	D_0
DCD1	D_7	D_6	D_5	D_4
DCD2	—	—	—	D_8

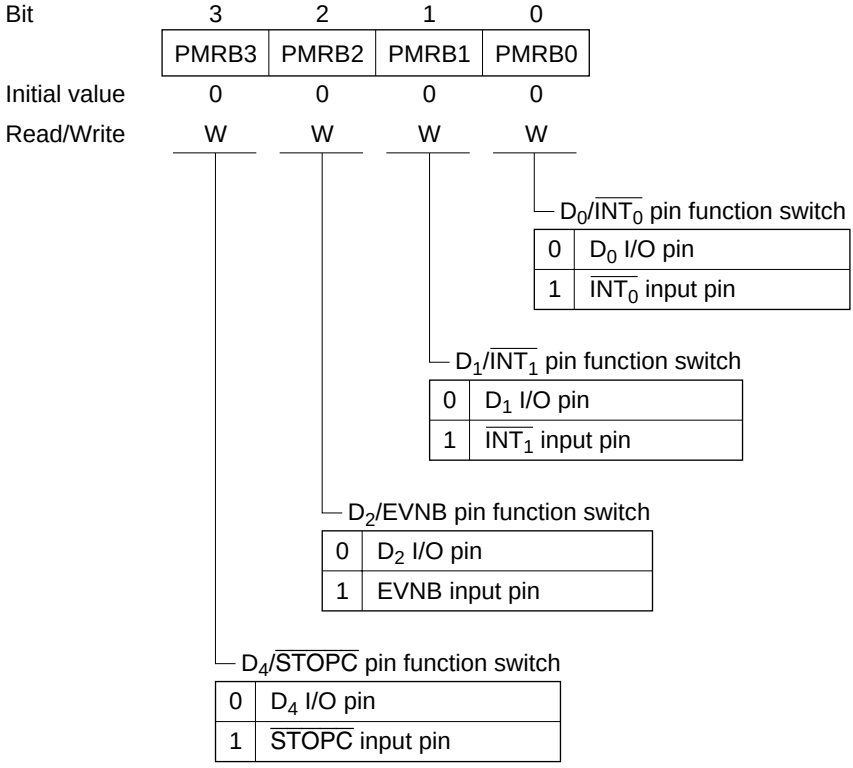
(3) Port Mode Register A (PMRA: $004): PMRA is a 4-bit write-only register whose PMRA3 bit switches the function of the D_3/BUZZ pin. This section describes the function of the PMRA3 bit. See section 10.3.2 (3), “Port Mode Register A (PMRA)”, for details on the PMRA2 to PMRA0 bits.



Bit 3—D_3/BUZZ Pin Function Switch (PMRA3): Selects whether the D_3/BUZZ pin functions as the D_3 I/O pin or as the alarm output pin (BUZZ).

PMRA3	Description	
0	The D_3/BUZZ pin functions as the D_3 I/O pin.	(initial value)
1	The D_3/BUZZ pin functions as the BUZZ output pin.	

(4) Port Mode Register B (PMRB: $024): PMRB is a 4-bit write-only register that switches the D port I/O pin shared functions.



Bit 3—D_4/$\overline{\text{STOPC}}$ Pin Function Switch (PMRB3): Selects whether the D_4/$\overline{\text{STOPC}}$ pin is used as the D_4 I/O pin or as the stop mode clear pin ($\overline{\text{STOPC}}$).

PMRB3	Description	
0	The D_4/$\overline{\text{STOPC}}$ pin functions as the D_4 I/O pin.	(initial value)
1	The D_4/$\overline{\text{STOPC}}$ pin functions as the $\overline{\text{STOPC}}$ input pin.	

Bit 2—D_2/EVNB Pin Function Switch (PMRB2): Selects whether the D_2/EVNB pin is used as the D_2 I/O pin or as the timer B event count input pin (EVNB).

PMRB2	Description	
0	The D_2/EVNB pin functions as the D_2 I/O pin.	(initial value)
1	The D_2/EVNB pin functions as the EVNB input pin.	

Bit 1—$D_1/\overline{INT}_1$ Pin Function Switch (PMRB1): Selects whether the $D_1/\overline{INT}_1$ pin is used as the D_1 I/O pin or as external interrupt 1 input pin ($\overline{INT}_1$).

PMRB1	Description	
0	The $D_1/\overline{INT}_1$ pin functions as the D_1 I/O pin.	(initial value)
1	The $D_1/\overline{INT}_1$ pin functions as the $\overline{INT}_1$ input pin.	

Bit 0—$D_0/\overline{INT}_0$ Pin Function Switch (PMRB0): Selects whether the $D_0/\overline{INT}_0$ pin is used as the D_0 I/O pin or as external interrupt 0 input pin ($\overline{INT}_0$).

PMRB0	Description	
0	The $D_0/\overline{INT}_0$ pin functions as the D_0 I/O pin.	(initial value)
1	The $D_0/\overline{INT}_0$ pin functions as the $\overline{INT}_0$ input pin.	

10.2.3 Pin Functions

The functions of the pins D_0 to D_8 are switched by register settings as shown in table 10-7.

Table 10-7 D_0 to D_8 Port Pin Functions

Pin	Pin Functions and Selection Methods
$D_0/\overline{INT_0}$	The pin function is switched as shown below by the PMRB PMRB0 bit and the DCD0 DCD00 bit.

PMRB	0		1
DCD00	0	1	—
Pin function	D_0 input pin	D_0 output pin	$\overline{INT_0}$ input pin

$D_1/\overline{INT_1}$	The pin function is switched as shown below by the PMRB PMRB1 bit and the DCD0 DCD01 bit.

PMRB1	0		1
DCD01	0	1	—
Pin function	D_1 input pin	D_1 output pin	$\overline{INT_1}$ input pin

D_2/EVNB	The pin function is switched as shown below by the PMRB PMRB2 bit and the DCD0 DCD02 bit.

PMRB2	0		1
DCD02	0	1	—
Pin function	D_2 input pin	D_2 output pin	EVNB input pin

D_3/BUZZ	The pin function is switched as shown below by the PMRA PMRA3 bit and the DCD0 DCD03 bit.

PMRA3	0		1
DCD03	0	1	—
Pin function	D_3 input pin	D_3 output pin	BUZZ output pin

$D_4/\overline{STOPC}$	The pin function is switched as shown below by the PMRB PMRB3 bit and the DCD1 DCD10 bit.

PMRB3	0		1
DCD10	0	1	—
Pin function	D_4 input pin	D_4 output pin	$\overline{STOPC}$ input pin

Table 10-7 D_0 to D_8 Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
D_5	The pin function is switched as shown below by the DCD1 DCD11 bit.

DCD11	0	1
Pin function	D_5 input pin	D_5 output pin

D_6	The pin function is switched as shown below by the DCD1 DCD12 bit.

DCD12	0	1
Pin function	D_6 input pin	D_6 output pin

D_7	The pin function is switched as shown below by the DCD1 DCD13 bit.

DCD13	0	1
Pin function	D_7 input pin	D_7 output pin

D_8	The pin function is switched as shown below by the DCD2 DCD20 bit.

DCD20	0	1
Pin function	D_8 input pin	D_8 output pin

10.3 R Ports

10.3.1 Overview

The R port consists of the six 4-bit I/O ports R0 to R4 and R8 and the 1-bit input port RA_1. These ports are accessed in 4-bit units.

R0, R1, R3, R4, and R8 are standard voltage CMOS three state I/O ports and R2 is a medium voltage NMOS open drain I/O port of HD404358 Series.

On the HD404358R series pins R0, R1, R2, R3, R4, and R8 are CMOS three state standard voltage I/O pins. Of these, R0, R1, R2, and R8 can handle high current levels of up to 15 mA.

The individual ports R0 to R4 and R8 are accessed in 4-bit units with the LRA and LRB output instructions to control the output levels (high or low) on each pin. Output data is stored in the PDR built into each pin. Similarly, the LAR and LBR input instructions can be used to access the R ports in 4-bit units to read the input levels on the port pins.

The RA1 input-only port consists of a single bit. The values of bits 3, 2, and 0 are undefined when this port is accessed by the input instructions.

DCR registers are used to control on/off states of the R port output buffers. When the DCR bit corresponding to a pin in an R port is set to 1, the contents of the PDR corresponding to that pin is output from the pin. Thus the output buffer on/off states can be controlled on an individual pin basis for the R port pins. The DCR registers are allocated in the RAM address space.

The R0, R3, and R4 port pins have shared functions as built-in peripheral module pins. Register settings are used to switch these functions. (See table 10-8.)

Figure 10-2 shows the R port pin structure.

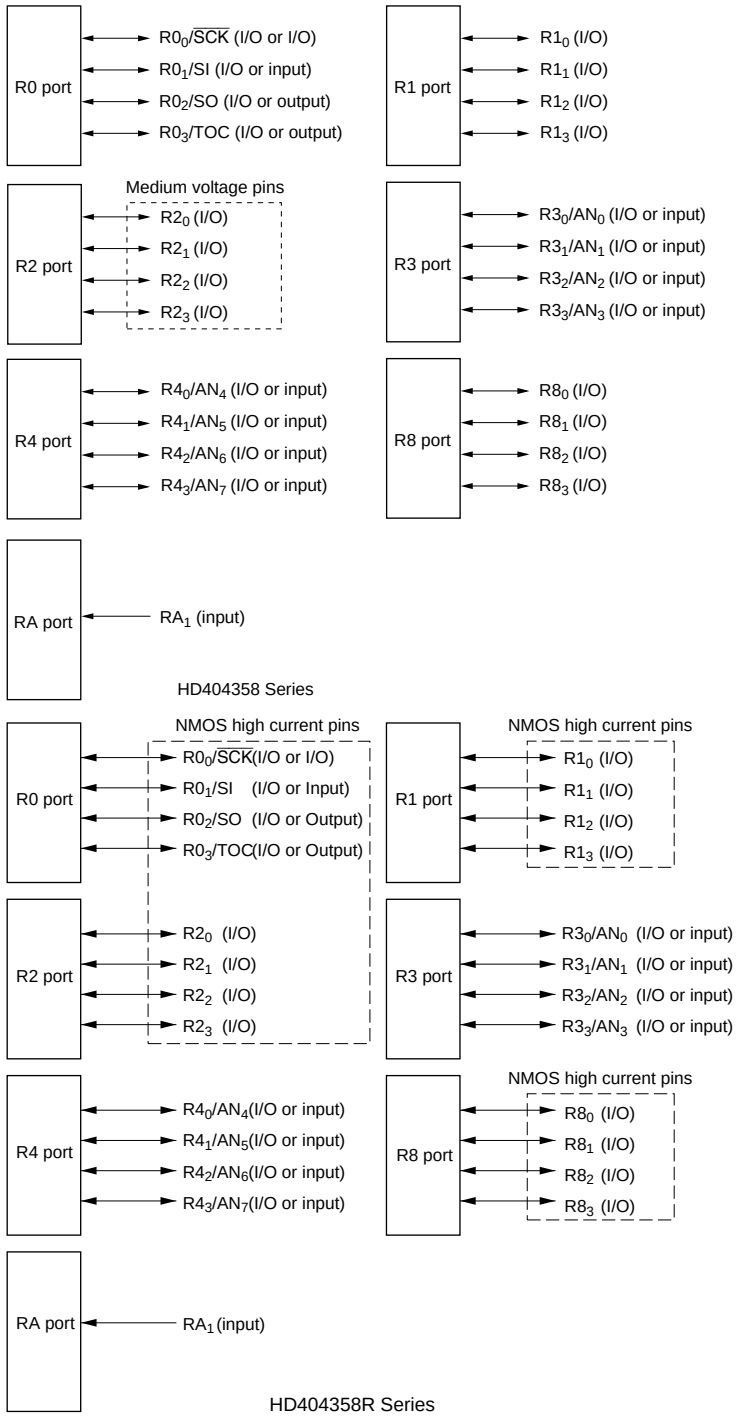


Figure 10-2 R Port Structure

10.3.2 Register Configuration and Descriptions

Table 10-8 shows the configuration of the R port related registers.

Table 10-8 R Port Register Configuration

Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	1
$030	Data control registers	DCR0	W	$0
$031		DCR1	W	$0
$032		DCR2	W	$0
$033		DCR3	W	$0
$034		DCR4	W	$0
$038		DCR8	W	$0
$004	Port mode register A	PMRA	W	$0
$005	Serial mode register	SMR	W	$0
$019	A/D mode register 1	AMR1	W	$0
$01A	A/D mode register 2	AMR2	W	--00

Note: * The LRA and LRB instructions are used to write to the PDR registers.

(1) Port Data Registers (PDR): All the I/O pins in ports R0 to R4 and R8 include a PDR that holds the output data. When an LRA or an LRB instruction is executed for one of ports R0 to R4 or R8, the contents of the accumulator (A) or the B register (B) are transferred to the specified R port PDRs. When bits in DCR0 to DCR4, or DCR8 are set to 1, the output buffers for the corresponding pins in port R0 to R4 or R8 will be turned on and the values in the PDRs will be output from those pins.

The PDR registers are set to 1 on reset and in stop mode.

(2) Data Control Registers (DCR0 to DCR4, DCR8: $030, $031, $032, $033, $034, $038)

DCR0: $030

Bit	3	2	1	0
	DCR03	DCR02	DCR01	DCR00
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR1: $031

Bit	3	2	1	0
	DCR13	DCR12	DCR11	DCR10
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR2: $032

Bit	3	2	1	0
	DCR23	DCR22	DCR21	DCR20
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR3: $033

Bit	3	2	1	0
	DCR33	DCR32	DCR31	DCR30
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR4: $034

Bit	3	2	1	0
	DCR43	DCR42	DCR41	DCR40
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR8: $038

Bit	3	2	1	0
	DCR83	DCR82	DCR81	DCR80
Initial value	0	0	0	0
Read/Write	W	W	W	W

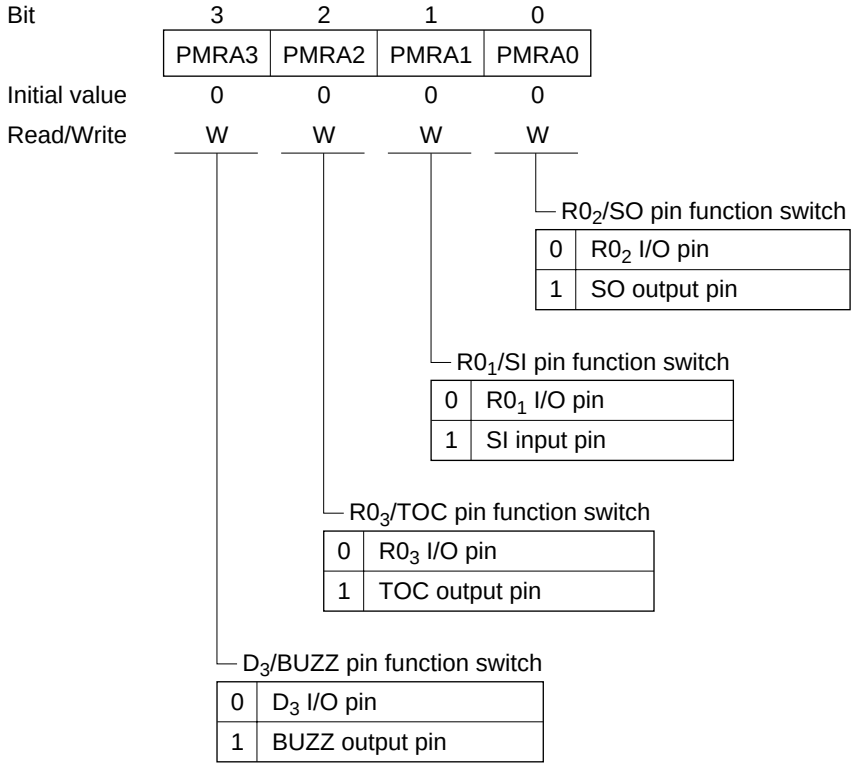
Bits in DCR0 to DCR4, and DCR8	Description
0	The output buffer (CMOS buffer) is turned off and the output goes to the high impedance state. (initial value)
1	• The CMOS three state output buffer is turned on and the corresponding PDR value is output. • For medium voltage NMOS open drain pins (R2) of HD404358 Series, when the PDR is 0 a low level is output. When the PDR is 1, the pin goes to the high impedance state.

The table below lists the correspondence between the bits in DCR0 to DCR4 and DCR8 and the port R0 to R4 and R8 pins.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR8	$R8_3$	$R8_2$	$R8_1$	$R8_0$

(3) Port Mode Register A(PMRA: $004): PMRA is a 4-bit write-only register whose bits PMRA2 to PMRA0 switch the functions of the port R0 shared function pins.

This section describes the bits PMRA2 to PMRA0. See section 10.2.2 (3), “Port Mode Register A (PMRA)”, for details on the PMRA3 bit.



Bit 2—R0$_3$/TOC Pin Function Switch (PMRA2): Selects whether the R0$_3$/TOC pin functions as the R0$_3$ I/O pin or as the timer C output pin (TOC).

PMRA2	Description	
0	The R0$_3$/TOC pin functions as the R0$_3$ I/O pin.	(initial value)
1	The R0$_3$/TOC pin functions as the TOC output pin.	

Bit 1—$R0_1$/SI Pin Function Switch (PMRA1): Selects whether the $R0_1$/SI pin functions as the $R0_1$ I/O pin or as the serial reception data input pin (SI).

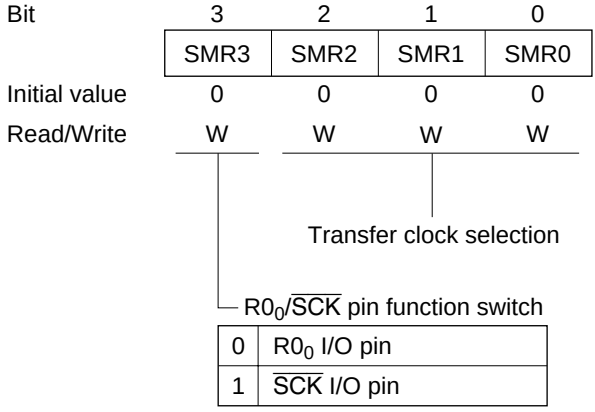
PMRA1	Description	
0	The $R0_1$/SI pin functions as the R01 I/O pin.	(initial value)
1	The $R0_1$/SI pin functions as the SI input pin.	

Bit 0—$R0_2$/SO Pin Function Switch (PMRA0): Selects whether the $R0_2$/SO pin functions as the $R0_2$ I/O pin or as the serial transmission data output pin (SO).

PMRA0	Description	
0	The $R0_2$/SO pin functions as the $R0_2$ I/O pin.	(initial value)
1	The $R0_2$/SO pin functions as the SO output pin.	

(4) Serial Mode Register (SMR: $005): SMR is a 4-bit write-only register whose SMR3 bit switches the $R0_0/\overline{SCK}$ pin function.

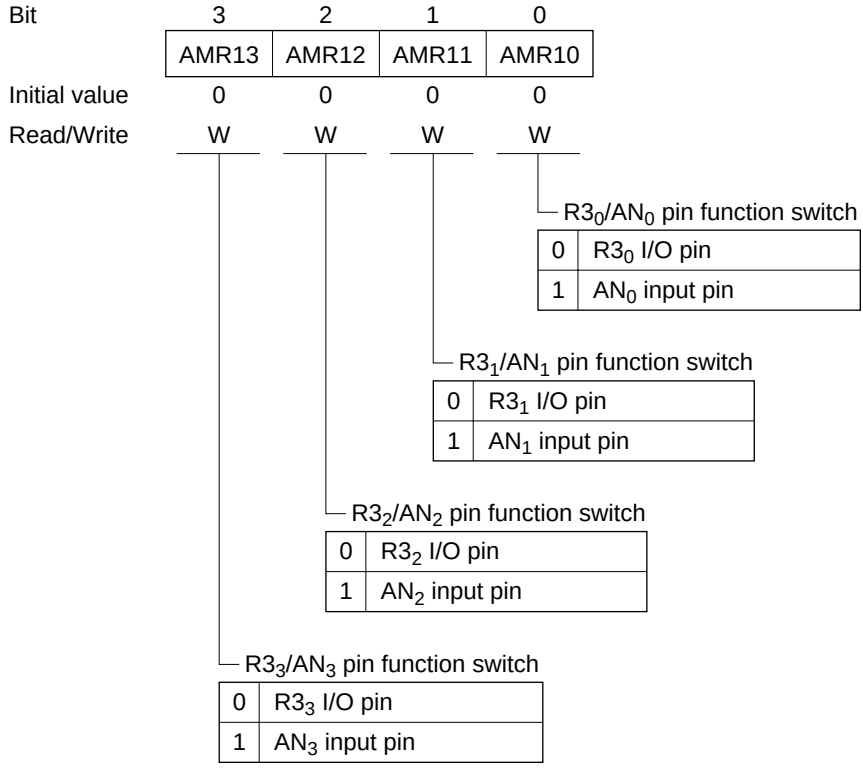
This section only describes the SMR3 bit. See section 20.2.1, “Serial Mode Register (SMR)” for details on bits SMR2 to SMR0.



Bit 3—$R0_0/\overline{SCK}$ Pin Function Switch (SMR3): Selects whether the $R0_0/\overline{SCK}$ pin functions as the $R0_0$ I/O pin or as the serial interface transfer clock I/O pin.

SMR3	Description	
0	The $R0_0/\overline{SCK}$ pin functions as the $R0_0$ I/O pin.	(initial value)
1	The $R0_0/\overline{SCK}$ pin functions as the $\overline{SCK}$ I/O pin.	

(5) A/D Mode Register 1 (AMR1: $019): AMR1 is a 4-bit write-only register that switches the functions of the R3 port shared function pins.



Bit 3—R3$_3$/AN$_3$ Pin Function Switch (AMR13): Selects whether the R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin or as the A/D converter channel 3 input pin AN$_3$.

AMR13	Description	
0	The R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin.	(initial value)
1	The R3$_3$/AN$_3$ pin functions as the AN$_3$ input pin.	

Bit 2—R3$_2$/AN$_2$ Pin Function Switch (AMR12): Selects whether the R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin or as the A/D converter channel 2 input pin AN$_2$.

AMR12	Description	
0	The R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin.	(initial value)
1	The R3$_2$/AN$_2$ pin functions as the AN$_2$ input pin.	

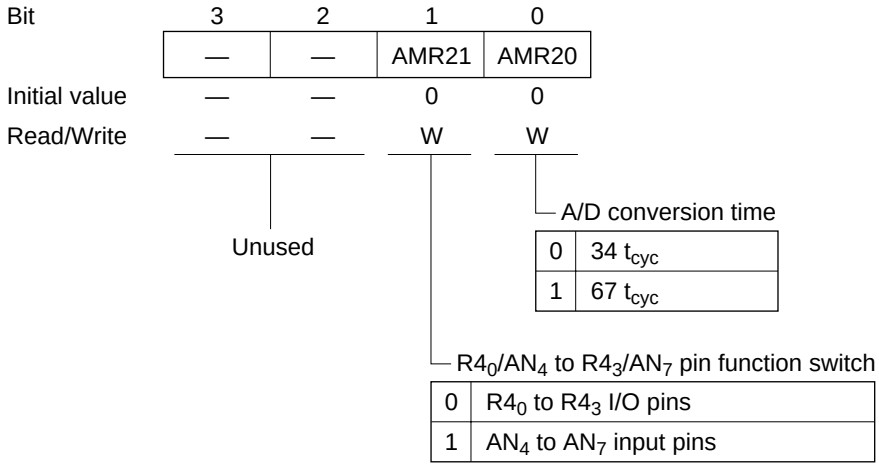
Bit 1—$R3_1/AN_1$ Pin Function Switch (AMR11): Selects whether the $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin or as the A/D converter channel 1 input pin AN_1.

AMR11	Description	
0	The $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin.	(initial value)
1	The $R3_1/AN_1$ pin functions as the AN_1 input pin.	

Bit 0—$R3_0/AN_0$ Pin Function Switch (AMR10): Selects whether the $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin or as the A/D converter channel 0 input pin AN_0.

AMR10	Description	
0	The $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin.	(initial value)
1	The $R3_0/AN_0$ pin functions as the AN_0 input pin.	

(6) A/D Mode Register 2 (AMR2: $1A): AMR2 is a 2-bit write-only register whose AMR21 bit switches the functions of all four bits of the R4 port ($R4_0$ to $R4_3$) to be A/D converter input channels (AN_4 to AN_7). This section describes the AMR21 bit. See section 15.2.2, “A/D Mode Register 2 (AMR2)”, for details on the AMD20 bit.



Bit 1—$R4_0/AN_4$ to $R4_3/AN_7$ Pin Function Switch (AMR21): Selects whether the $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins or as the A/D converter channel 4 to 7 input pins (AN_4 to AN_7).

AMR21	Description	
0	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins.	(initial value)
1	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the AN_4 to AN_7 input pins.	

10.3.3 Pin Functions

The pin functions of the R port pins are switched by register settings as shown in table 10-9.

Table 10-9 R Port Pin Functions

Pin	Pin Functions and Selection Methods
$R0_0/\overline{SCK}$	The pin function is switched by the SMR SMR3 bit and the DCR0 DCR00 bit as shown below.

SMR3	0		1
DCR00	0	1	—
Pin function	$R0_0$ input pin	$R0_0$ output pin	$\overline{SCK}$ I/O pin

$R0_1$/SI	The pin function is switched by the PMRA PMRA1 bit and the DCR0 DCR01 bit as shown below.

PMRA1	0		1
DCR01	0	1	—
Pin function	$R0_1$ input pin	$R0_1$ output pin	SI input pin

$R0_2$/SO	The pin function is switched by the PMRA PMRA0 bit and the DCR0 DCR02 bit as shown below.

PMRA0	0		1
DCR02	0	1	—
Pin function	$R0_2$ input pin	$R0_2$ output pin	SO output pin

$R0_3$/TOC	The pin function is switched by the PMRA PMRA2 bit and the DCR0 DCR03 bit as shown below.

PMRA2	0		1
DCR03	0	1	—
Pin function	$R0_3$ input pin	$R0_3$ output pin	TOC output pin

Table 10-9 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods		
$R1_0$	The pin function is switched by the DCR1 DCR10 bit as shown below.		
	DCR10	0	1
	Pin function	$R1_0$ input pin	$R1_0$ output pin
$R1_1$	The pin function is switched by the DCR1 DCR11 bit as shown below.		
	DCR11	0	1
	Pin function	$R1_1$ input pin	$R1_1$ output pin
$R1_2$	The pin function is switched by the DCR1 DCR12 bit as shown below.		
	DCR12	0	1
	Pin function	$R1_2$ input pin	$R1_2$ output pin
$R1_3$	The pin function is switched by the DCR1 DCR13 bit as shown below.		
	DCR13	0	1
	Pin function	$R1_3$ input pin	$R1_3$ output pin
$R2_0$	The pin function is switched by the DCR2 DCR20 bit as shown below.		
	DCR20	0	1
	Pin function	$R2_0$ input pin	$R2_0$ output pin*
$R2_1$	The pin function is switched by the DCR2 DCR21 bit as shown below.		
	DCR21	0	1
	Pin function	$R2_1$ input pin	$R2_1$ output pin*
$R2_2$	The pin function is switched by the DCR2 DCR22 bit as shown below.		
	DCR22	0	1
	Pin function	$R2_2$ input pin	$R2_2$ output pin*

Note: * $R2_0$ to $R2_3$ are medium voltage NMOS open drain I/O pins of HD404358 Series. These pins go to the high impedance state when their PDR is set to 1.

Table 10-9 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R2_3$	The pin function is switched by the DCR2 DCR23 bit as shown below.

DCR23	0	1
Pin function	$R2_3$ input pin	$R2_3$ output pin*

$R3_0/AN_0$	The pin function is switched by the AMR1 AMR10 bit and the DCR3 DCR30 bit as shown below.		
AMR10	0		1
DCR30	0	1	—
Pin function	$R3_0$ input pin	$R3_0$ output pin	AN_0 input pin

$R3_1/AN_1$	The pin function is switched by the AMR1 AMR11 bit and the DCR3 DCR31 bit as shown below.		
AMR11	0		1
DCR31	0	1	—
Pin function	$R3_1$ input pin	$R3_1$ output pin	AN_1 input pin

$R3_2/AN_2$	The pin function is switched by the AMR1 AMR12 bit and the DCR3 DCR32 bit as shown below.		
AMR12	0		1
DCR32	0	1	—
Pin function	$R3_2$ input pin	$R3_2$ output pin	AN_2 input pin

$R3_3/AN_3$	The pin function is switched by the AMR1 AMR13 bit and the DCR3 DCR33 bit as shown below.		
AMR13	0		1
DCR33	0	1	—
Pin function	$R3_3$ input pin	$R3_3$ output pin	AN_3 input pin

Note: * $R2_0$ to $R2_3$ are medium voltage NMOS open drain I/O pins of HD404358 Series. These pins go to the high impedance state when their PDR is set to 1.

Table 10-9 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R4_0/AN_4$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR40 bit as shown below.

AMR21	0		1
DCR40	0	1	—
Pin function	$R4_0$ input pin	$R4_0$ output pin	AN_4 input pin

$R4_1/AN_5$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR41 bit as shown below.

AMR21	0		1
DCR41	0	1	—
Pin function	$R4_1$ input pin	$R4_1$ output pin	AN_5 input pin

$R4_2/AN_6$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR42 bit as shown below.

AMR21	0		1
DCR42	0	1	—
Pin function	$R4_2$ input pin	$R4_2$ output pin	AN_6 input pin

$R4_3/AN_7$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR43 bit as shown below.

AMR21	0		1
DCR43	0	1	—
Pin function	$R4_3$ input pin	$R4_3$ output pin	AN_7 input pin

Table 10-9 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R8_0$	The pin function is switched by the DCR8 DCR80 bit as shown below.

DCR80	0	1
Pin function	$R8_0$ input pin	$R8_0$ output pin

$R8_1$	The pin function is switched by the DCR8 DCR81 bit as shown below.

DCR81	0	1
Pin function	$R8_1$ input pin	$R8_1$ output pin

$R8_2$	The pin function is switched by the DCR8 DCR82 bit as shown below.

DCR82	0	1
Pin function	$R8_2$ input pin	$R8_2$ output pin

$R8_3$	The pin function is switched by the DCR8 DCR83 bit as shown below.

DCR83	0	1
Pin function	$R8_3$ input pin	$R8_3$ output pin

10.4 Usage Notes

Keep the following points in mind when using the I/O ports.

- When the MIS MIS2 bit is set to 1, the $R0_2$/SO pin will be an NMOS open drain output regardless of whether it is selected for use as the $R0_2$ pin or as the SO pin by the PMRA PMRA0 bit.

- I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation.

  The built-in pull-up MOS transistors can be used to pull up unused pins to V_{CC}. Alternatively, unused pins can be pulled up to V_{CC} with external resistors of about 100 k.

  Application programs should maintain the PDR, DCD and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

- When the MIS MIS3 bit is set to 1 (pull-up MOS transistors active) and the PDR for an R port/analog input shared function pin has the value 1, the MOS transistor for the corresponding pin will not be turned off by selecting the analog input function with the AMR1 or AMR2 register.

  To use an R port/analog input shared function pin as an analog input when the pull-up MOS transistors are active, always clear the PDR for the corresponding pin to 0 first and then turn off the pull-up MOS transistor. (Note that the PDR registers are set to 1 immediately following a reset.)

  Figure 10-3 shows the circuit for the R port/analog input shared function pins. AMR1 and AMR2 are used to set the port outputs to high impedance. ACR is used to switch the analog input channel.

  The states of the R port/analog input shared function pins are set, as shown in table 10-10, by the combination of the AMR1 or AMR2 register, the MIS3 bit, the DCR, and the PDR settings.

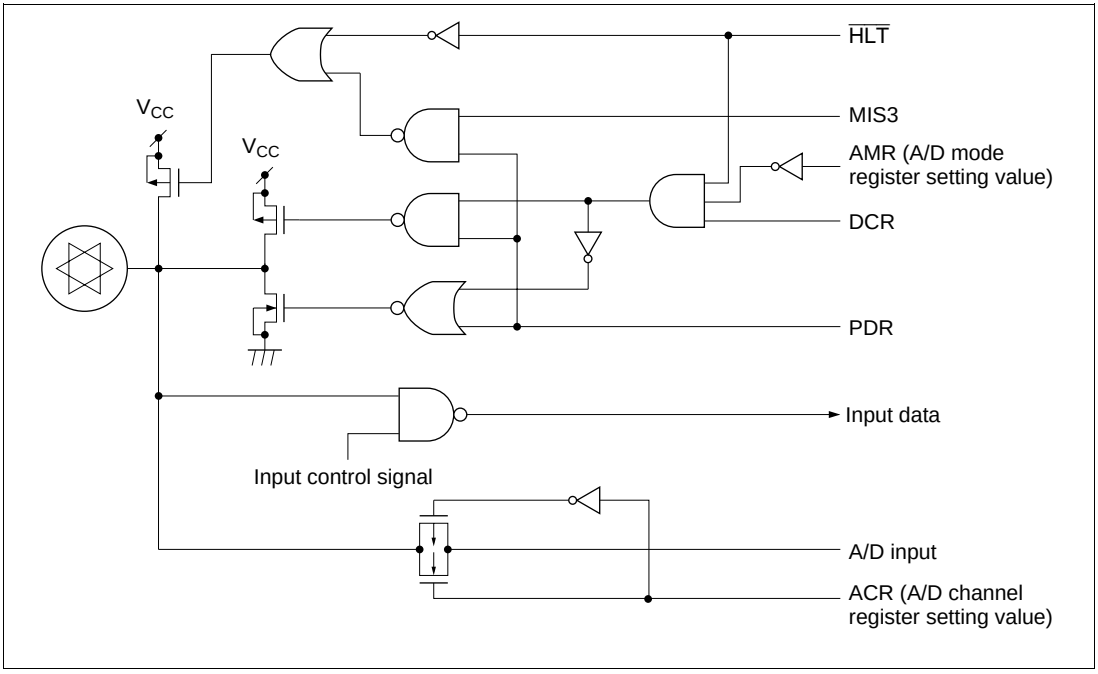


Figure 10-3 R Port/Analog Input Shared Function Pin Circuit

Table 10-10 Program Control of the R Port/Analog Input Shared Function Pins

Corresponding bit in AMR1 or AMR2		0 (R port selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

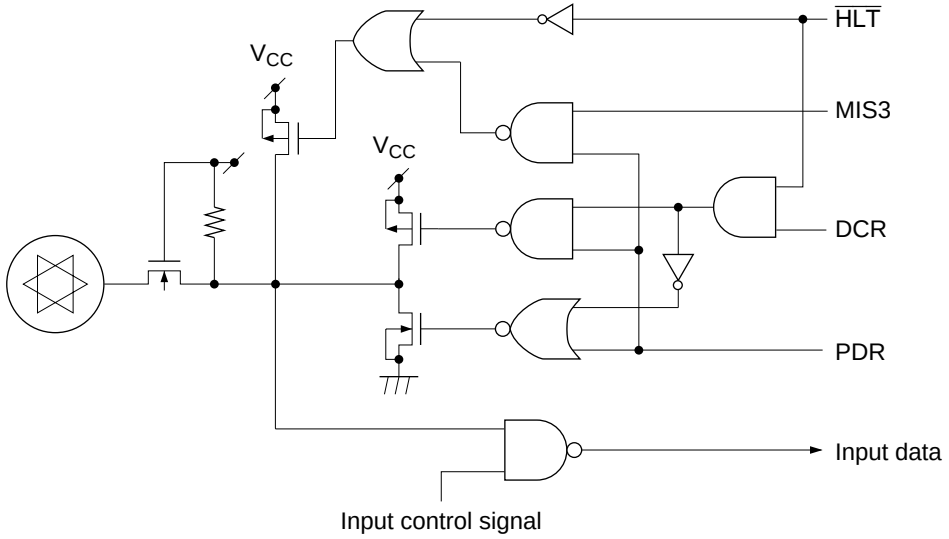
Note: —: off

Corresponding bit in AMR1 or AMR2		1 (analog input selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	—	—		—	—
	NMOS			—	—			—	—
Pull-up MOS transistor		—				—	On	—	On

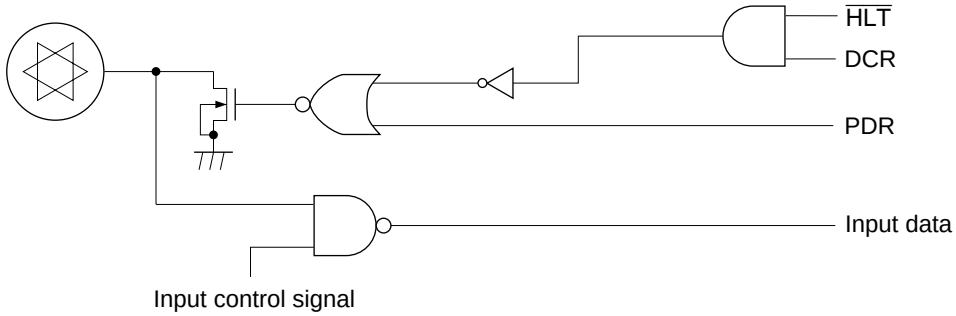
Note: —: off

- In the HD404358 Series evaluation chip set, the circuits for the medium voltage NMOS open drain pins (the R2 port pins) differ from the ZTAT™ and the mask ROM microcomputer versions as shown in figure 10-4. Although the outputs in both the ZTAT™ and mask ROM versions can be set to high impedance by the combinations listed in table 10-11, these outputs cannot be set to high impedance in the evaluation chip set. Please keep this in mind when using the evaluation chip set.

  Figure 10-4 shows the circuit for the medium voltage NMOS open drain pins.



(a) Evaluation Chip Pin Circuit Structure



(b) ZTAT™ and Mask ROM Pin Circuit Structure

Figure 10-4 Medium Voltage NMOS Open Drain Pin Circuits

Table 10-11 ZTAT™ and Mask ROM Microcomputer Medium Voltage Pin High Impedance Control

DCR	PDR	Description	
0	*	High impedance output	(initial value)
1	0	NMOS buffer on. Low level output	
	1	High impedance output	

Note: * Don't care

Section 11 I/O Ports (HD404339 Series)

11.1 Overview

11.1.1 Features

The HD404339 Series I/O ports have the following features.

- The 14 pins D_0 to D_{13} as well as the R1, R2, R8, and R9 ports are high voltage I/O pins. Also, RA_1 is a high voltage input pin.
- R0, R3, and R4 are standard voltage I/O pins that, in output mode, are CMOS three state outputs.
- Certain I/O pins (D_0 to D_4, and the pins in the R0 and R3 to R5 ports) are shared with the built-in peripheral modules, such as timers and the serial interface. Setting these pins for use with the built-in peripheral modules takes priority over their setting for use as D or R port pins.
- Register settings are used to select input or output for I/O pins and to select the I/O port or peripheral module usage for shared function pins.
- Of the built-in peripheral module pins, the D_3/BUZZ pin is a PMOS open drain output. All other output pins are CMOS three state outputs. However, the $R0_2$/SO pin can be selected to be an NMOS open drain output by setting a register.
- Since the system is reset in stop mode, the built-in peripheral module selections are cleared and the I/O pins go to the high impedance state.
- The CMOS output pins have built-in programmable pull-up MOS transistors. The on/off state of these transistors can be controlled by register settings on an individual basis. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 11-1 provides an overview of the HD404339 Series port functions.

Table 11-1 Port Functions

Port	Overview	Pin	Shared Function	Function Switching Register
D_0 to D_{13}	• High voltage I/O port • Accessed in bit units • Accessed with the SED, SEDD, RED, REDD, TD, and TDD instructions. • Pull-down resistors available as a mask option.	$D_0/\overline{INT}_0$	External interrupt input 0	PMRB
		$D_1/\overline{INT}_1$	External interrupt input 1	
		D_2/EVNB	Timer B event input	
		D_3/BUZZ	Alarm output	PMRA
		$D_4/\overline{STOPC}$	Stop mode clear	PMRB
		D_5 to D_{13}	—	—
R0	• Standard voltage I/O ports • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions. • Programmable pull-up MOS transistors	$R0_0/\overline{SCK}$	Transfer clock I/O	SMR
		$R0_1$/SI	Serial reception data input	PMRA
		$R0_2$/SO	Serial transmission data output	
		$R0_3$/TOC	Timer C output	
R3		$R3_0/AN_0$	Analog input channel 0	AMR1
		$R3_1/AN_1$	Analog input channel 1	
		$R3_2/AN_2$	Analog input channel 2	
		$R3_3/AN_3$	Analog input channel 3	
R4		$R4_0/AN_4$	Analog input channel 4	AMR2
		$R4_1/AN_5$	Analog input channel 5	
		$R4_2/AN_6$	Analog input channel 6	
		$R4_3/AN_7$	Analog input channel 7	
R5		$R5_0/AN_8$	Analog input channel 8	AMR2
		$R5_1/AN_9$	Analog input channel 9	
		$R5_2/AN_{10}$	Analog input channel 10	
		$R5_3/AN_{11}$	Analog input channel 11	
R6, R7		$R6_0$ to $R6_3$ $R7_0$ to $R7_2$	—	—

Table 11-1 Port Functions (cont)

Port	Overview	Pin	Shared Function	Function Switching Register
R1, R2, R8, R9	• High voltage I/O ports • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions. • Pull-down resistors available as a mask option.	$R1_0$ to $R1_3$ $R2_0$ to $R2_3$ $R8_0$ to $R8_3$ $R9_0$ to $R9_3$	—	—
RA	• High voltage input port (1 bit) • Accessed with the LAR and LBR instructions.	RA_1/V_{disp}	High voltage pin output power supply	Mask option

11.1.2 I/O Control

The D, R1, R2, R8, and R9 ports are high voltage I/O ports, RA_1 is a 1-bit high voltage input port, and R0 and R3 to R7 are standard voltage I/O ports. The different port types have different circuit structures as follows.

(1) High Voltage I/O Pin Circuit: The D, R1, R2, R8, and R9 port pins are high voltage I/O pins that have no I/O switching function. When a port data register is set to 1, the PMOS transistor turns on and a high level voltage is output from the pin. When the PDR is set to 0, the pin goes to the open state. If the built-in pull-down resistor mask option was selected, the V_{disp} voltage is output. When external signals are applied, applications must set the PDR value to 0 so that the external (input) and internal (output) signals do not collide at the pin.

Note that there are no pull-down resistors on the high voltage I/O pins in the ZTAT™ versions of these microcomputers.

(2) Standard Voltage CMOS Three State I/O Pin Circuit: The pins in the R0 and R3 to R7 ports are standard voltage CMOS three state I/O ports. I/O through these ports is controlled by the PDRs and the data control registers (DCR). When the DCR bit corresponding to a given pin is 1, that pin functions as an output pin and outputs the value in the PDR. When a given DCR bit is 0, the corresponding pin functions as an input pin.

(3) Pull-Up MOS Control: Each I/O pin in the R0 and R3 to R7 ports has a built-in programmable pull-up MOS transistor. When the miscellaneous register (MIS) MIS3 bit is set to 1 the pull-up MOS transistor for pins for which the corresponding PDR is set to 1 will be turned on. Thus the on/off state of each pin can be controlled independently by the PDRs. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 11-2 shows how register settings control the port I/O pins.

Table 11-2 Register Settings for I/O Pin Control

MIS3		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Notes: 1. —: Off

2. The PDR registers are not allocated addresses in RAM. The PDR registers are accessed by special-purpose I/O instructions.

(4) Miscellaneous Register (MIS: $00C): MIS is a 4-bit write-only register that controls the on/off states of the R0 and R3 to R7 port pin pull-up MOS transistors, the on/off state of the $R0_2$/SO pin output buffer PMOS transistor, the interrupt frame period in watch and subactive modes, and the oscillator stabilization period when a low power mode is cleared.

MIS is initialized to $0 on reset and in stop mode.

This section describes the MIS2 and MIS3 bits. Refer to section 6.2.1, “Miscellaneous Register (MIS)”, for details on the MIS0 and MIS1 bits.

Bit	3	2	1	0
	MIS3	MIS2	MIS1	MIS0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Interrupt frame period and oscillator stabilization time settings

$R0_2$/SO pin output buffer control

0	PMOS transistor active (CMOS output)
1	PMOS transistor off (NMOS open drain output)

Pull-up MOS transistor control

0	All pull-up MOS transistors off
1	Pull-up MOS transistors active

Bit 3—Pull-Up MOS Transistor Control (MIS3): Controls the on/off states of the pull-up MOS transistors built into the I/O port pins.

MIS3	Description	
0	All pull-up MOS transistors will be turned off.	(initial value)
1	Pull-up MOS transistors for which the corresponding PDR bit is 1 will be turned on.	

Bit 2—$R0_2$/SO Pin Output Buffer Control (MIS2): Controls the on/off state of the $R0_2$/SO pin output buffer PMOS transistor.

MIS2	Description	
0	The $R0_2$/SO pin output will be a CMOS output.	(initial value)
1	The $R0_2$/SO pin output will be an NMOS open drain output.	

11.1.3 I/O Pin Circuit Structures

Table 11-3 shows the port and peripheral module pin circuits.

Notes: 1. Since the system is reset in stop mode, the built-in peripheral module selections are cleared. Since the internal $\overline{HLT}$ signal goes to the low (active) level, the I/O pins go to the high impedance state. Also, all the pull-up MOS transistors are turned off.

2. In all low power modes other than stop mode, the internal $\overline{HLT}$ signal goes to the high level.

Table 11-3 Input and Output Pin Circuits

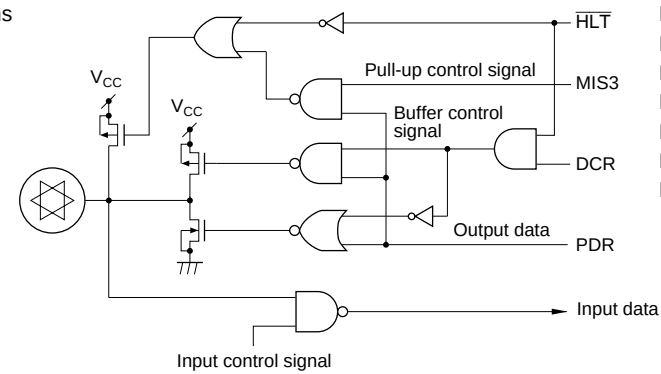
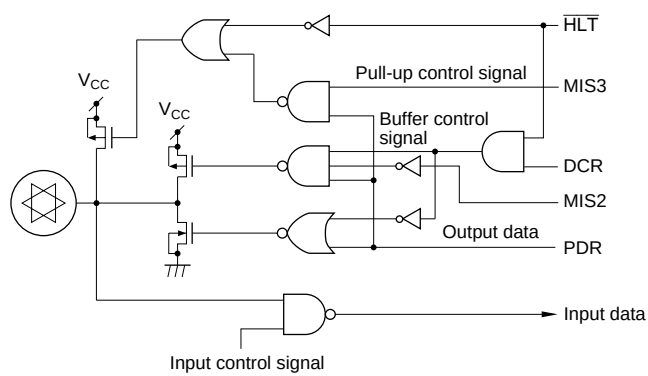
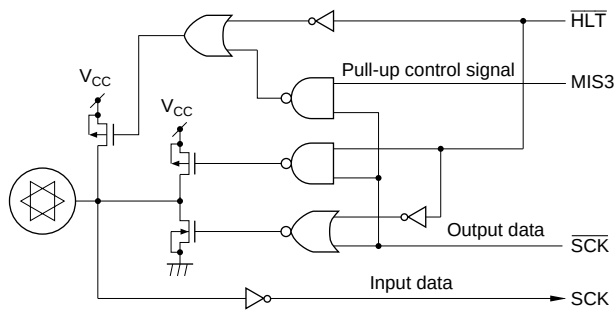
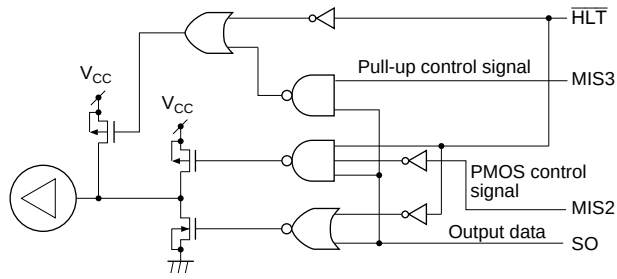
Class	Circuit	Applicable Pins
Standard voltage pins	I/O pins 	$R0_0$, $R0_1$, $R0_3$, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$, $R5_0$ to $R5_3$, $R6_0$ to $R6_3$, $R7_0$ to $R7_2$
		$R0_2$

Table 11-3 Input and Output Pin Circuits (cont)

Class		Circuit	Applicable Pins
Standard voltage pins	Standard peripheral module pins	I/O pins	$\overline{SCK}$
		Output pins	SO
			TOC





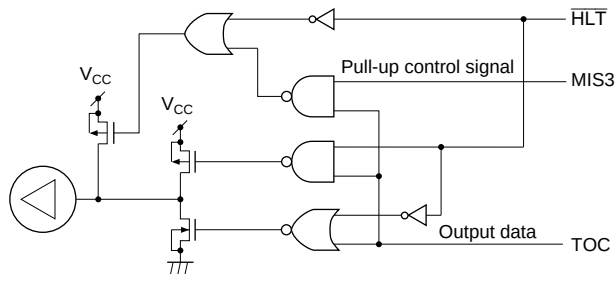


Table 11-3 Input and Output Pin Circuits (cont)

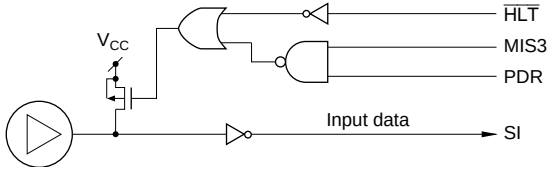
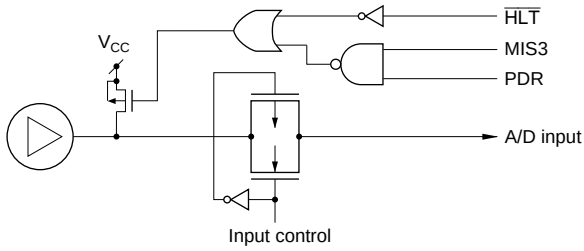
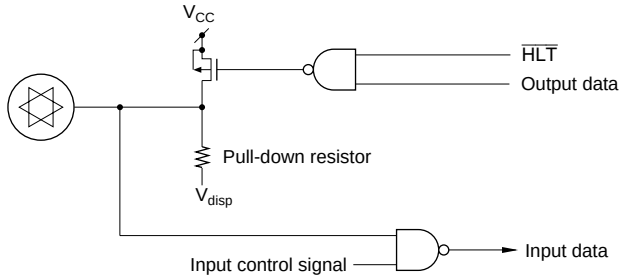
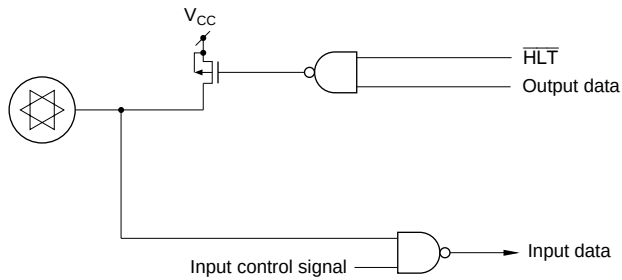
Class			Circuit	Applicable Pins
Standard voltage pins	Built-in peripheral module pins	Input pins		SI
				AN_0 to AN_{11}

Table 11-3 Input and Output Pin Circuits (cont)

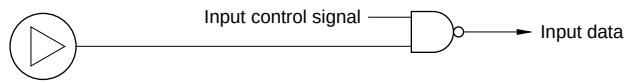
Class	Circuit	Applicable Pins
High voltage pins	I/O pins Pins with pull-down resistors	D_0 to D_{13}, $R1_0$ to $R1_3$, $R2_0$ to $R2_3$, $R8_0$ to $R8_3$, $R9_0$ to $R9_3$



Pins without pull-down resistors*

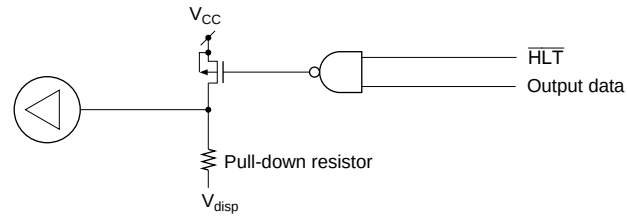
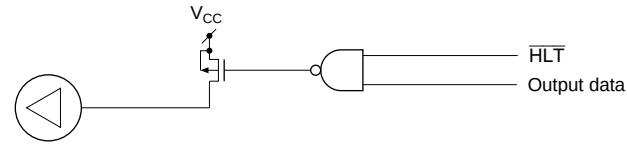
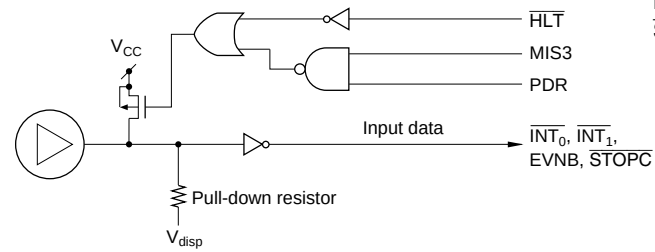
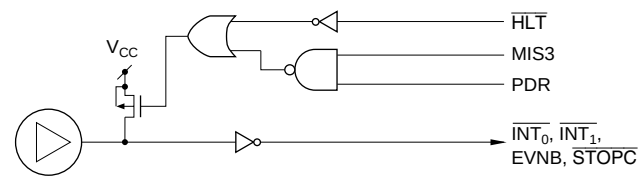


	Input pins	RA_1



Note: * The ZTAT™ versions of these microcomputers only support pins without pull-down resistors.

Table 11-3 Input and Output Pin Circuits (cont)

Class			Circuit	Applicable Pins
High voltage pins	Built-in peripheral module pins	Output pins	Pins with pull-down resistors 	BUZZ
			Pins without pull-down resistors* 	
		Input pins	Pins with pull-down resistors 	$\overline{INT_0}$, $\overline{INT_1}$, EVNB, $\overline{STOPC}$
			Pins without pull-down resistors* 	

Note: * The ZTAT™ versions of these microcomputers only support pins without pull-down resistors.

11.1.4 Port States in Low Power Modes

The D_0 to D_4 pins and the R0 and R3 to R5 port pins have shared functions as input or output pins for built-in peripheral modules. Since the CPU stops in standby and watch modes, the pins selected as output ports maintain their immediately prior output values. Also, pins selected for use by built-in peripheral modules that operate in standby or watch mode continue to operate. (Output pins used by modules that stop in these modes maintain their immediately prior output values.) See section 6, “Low Power Modes”, for details on which built-in peripheral modules can operate in each mode.

Table 11-4 lists the port states in the low power modes.

Table 11-4 Port States in Low Power Modes

Low Power Mode	Port States
Standby mode, watch mode	Pins maintain their values immediately prior to entering standby or watch mode.
Stop mode	Built-in peripheral function selections are cleared, and the port and peripheral function I/O pins go to the high impedance state.

11.1.5 Handling Unused Pins

I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation. The following are examples of techniques that can prevent noise problems.

High voltage pin: Select “no pull-down MOS transistor (PMOS open drain)” as the mask option and connect the pin to V_{CC} on the user system printed circuit board.

Standard voltage pin: Either use the built-in pull-up MOS transistor to pull the pin up to V_{CC}, or pull up the pin to V_{CC} externally with a pull-up resistor of about 100 kΩ.

Application programs should maintain the PDR and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

11.2 D Port

11.2.1 Overview

The D port is a 14-pin high voltage I/O port (D_0 to D_{13}) that can be accessed in 1-bit units.

The output levels on the pins D_0 to D_{13} can be set to low or high by accessing the port in one-bit units with the SED, SEDD, RED, and REDD output instructions. The output data is stored in the PDR for each pin. The level on each of the pins D_0 to D_{13} can be tested in one-bit units with the TD and TDD input instructions.

The pins D_0 to D_4 have shared functions as built-in peripheral module pins. PMRA and PMRB are used to switch these functions.

Figure 11-1 shows the structure of the D port.

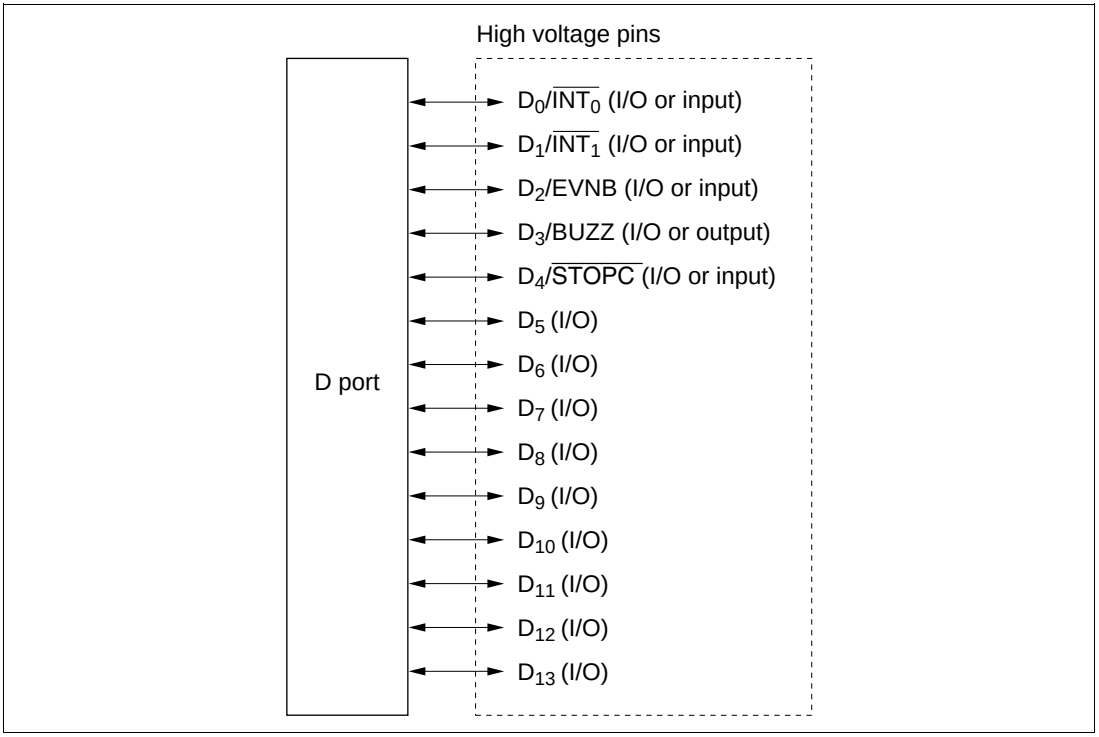


Figure 11-1 D Port Structure

11.2.2 Register Configuration and Descriptions

Table 11-5 shows the configuration of the D port registers.

Table 11-5 D Port Register Configuration

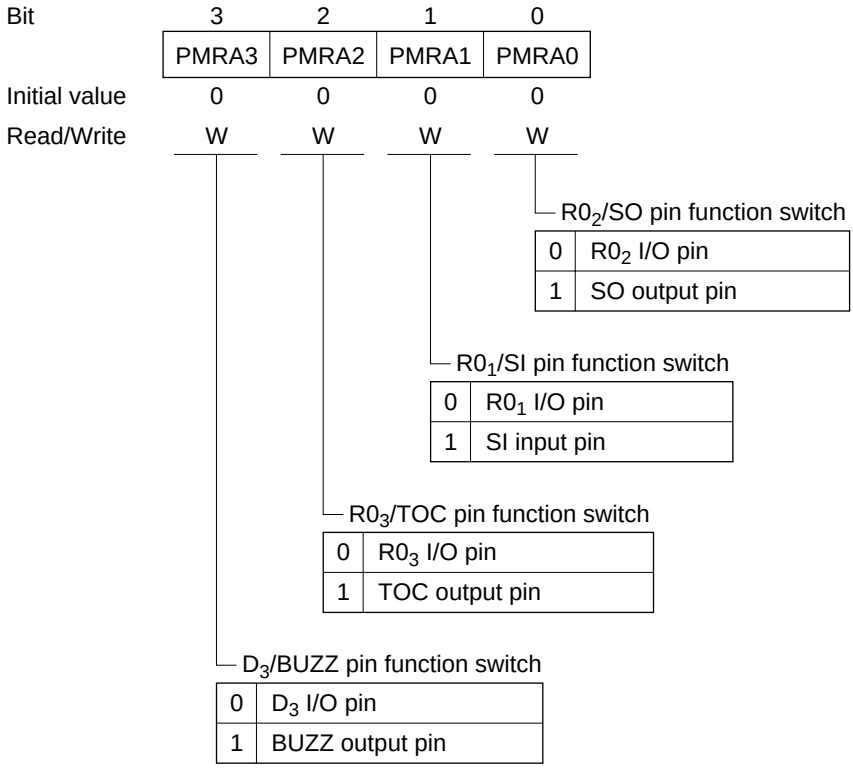
Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	0
$004	Port mode register A	PMRA	W	$0
$024	Port mode register B	PMRB	W	$0

Note: * The SED, SEDD, RED, and REDD instructions can be used to write to the PDRs.

(1) Port Data Registers (PDR): Each of the I/O pins D_0 to D_{13} includes a built-in PDR. When a SED or SEDD instruction is executed for one of the pins D_0 to D_{13} the corresponding PDR is set to 1, and when a RED or REDD instruction is executed, the corresponding PDR is cleared to 0.

The PDRs are cleared to 0 on reset and in stop mode.

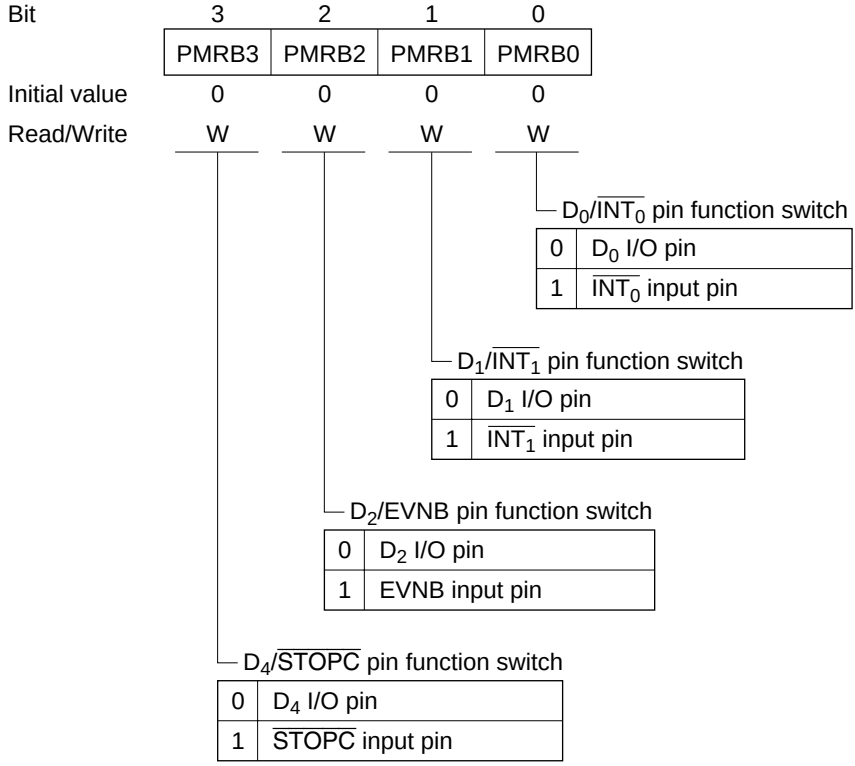
(2) Port Mode Register A (PMRA: $004): PMRA is a 4-bit write-only register whose PMRA3 bit switches the function of the D_3/BUZZ pin. This section describes the function of the PMRA3 bit. See section 11.3.2 (3), “Port Mode Register A (PMRA)”, for details on the PMRA2 to PMRA0 bits.



Bit 3—D_3/BUZZ Pin Function Switch (PMRA3): Selects whether the D_3/BUZZ pin functions as the D_3 I/O pin or as the alarm output pin (BUZZ).

PMRA3	Description	
0	D_3/BUZZ pin functions as the D_3 I/O pin.	(initial value)
1	D_3/BUZZ pin functions as the BUZZ output pin.	

(3) Port Mode Register B (PMRB: $024): PMRB is a 4-bit write-only register that switches the D port I/O pin shared functions.



Bit 3—D_4/$\overline{\text{STOPC}}$ Pin Function Switch (PMRB3): Selects whether the D_4/$\overline{\text{STOPC}}$ pin is used as the D_4 I/O pin or as the stop mode clear pin ($\overline{\text{STOPC}}$).

PMRB3	Description	
0	The D_4/$\overline{\text{STOPC}}$ pin functions as the D_4 I/O pin.	(initial value)
1	The D_4/$\overline{\text{STOPC}}$ pin functions as the $\overline{\text{STOPC}}$ input pin.	

Bit 2—D_2/EVNB Pin Function Switch (PMRB2): Selects whether the D_2/EVNB pin is used as the D_2 I/O pin or as the timer B event count input pin (EVNB).

PMRB2	Description	
0	The D_2/EVNB pin functions as the D_2 I/O pin.	(initial value)
1	The D_2/EVNB pin functions as the EVNB input pin.	

Bit 1—$D_1/\overline{INT}_1$ Pin Function Switch (PMRB1): Selects whether the $D_1/\overline{INT}_1$ pin is used as the D_1 I/O pin or as the external interrupt 1 input pin ($\overline{INT}_1$).

PMRB1	Description	
0	The $D_1/\overline{INT}_1$ pin functions as the D_1 I/O pin.	(initial value)
1	The $D_1/\overline{INT}_1$ pin functions as the $\overline{INT}_1$ input pin.	

Bit 0—$D_0/\overline{INT}_0$ Pin Function Switch (PMRB0): Selects whether the $D_0/\overline{INT}_0$ pin is used as the D_0 I/O pin or as the external interrupt 0 input pin ($\overline{INT}_0$).

PMRB0	Description	
0	The $D_0/\overline{INT}_0$ pin functions as the D_0 I/O pin.	(initial value)
1	The $D_0/\overline{INT}_0$ pin functions as the $\overline{INT}_0$ input pin.	

11.2.3 Pin Functions

The pin functions of the pins D_0 to D_4 are switched by register settings as shown in table 11-6.

Table 11-6 D_0 to D_4 Port Pin Functions

Pin	Pin Functions and Selection Methods		
$D_0/\overline{INT}_0$	The pin function is switched as shown below by the PMRB PMRB0 bit.		
	PMRB0	0	1
	Pin function	D0 I/O pin	INT0 input pin
$D_1/\overline{INT}_1$	The pin function is switched as shown below by the PMRB PMRB1 bit.		
	PMRB1	0	1
	Pin function	D_1 I/O pin	$\overline{INT}_1$ input pin
D_2/EVNB	The pin function is switched as shown below by the PMRB PMRB2 bit.		
	PMRB2	0	1
	Pin function	D_2 I/O pin	EVNB input pin
D_3/BUZZ	The pin function is switched as shown below by the PMRA PMRA3 bit.		
	PMRA3	0	1
	Pin function	D_3 I/O pin	BUZZ output pin
$D_4/\overline{STOPC}$	The pin function is switched as shown below by the PMRB PMRB3 bit.		
	PMRB3	0	1
	Pin function	D_4 I/O pin	$\overline{STOPC}$ input pin

11.3 R Ports

11.3.1 Overview

The R port consists of the nine 4-bit I/O ports R0 to R6, R8, and R9, the 3-bit I/O port R7, and the 1-bit input port RA_1. These ports are accessed in 4-bit units.

R0 and R3 to R7 are standard voltage I/O ports. RA is a high voltage input port and R1, R2, R8 and R9 are high voltage I/O ports that can directly drive fluorescent display tubes.

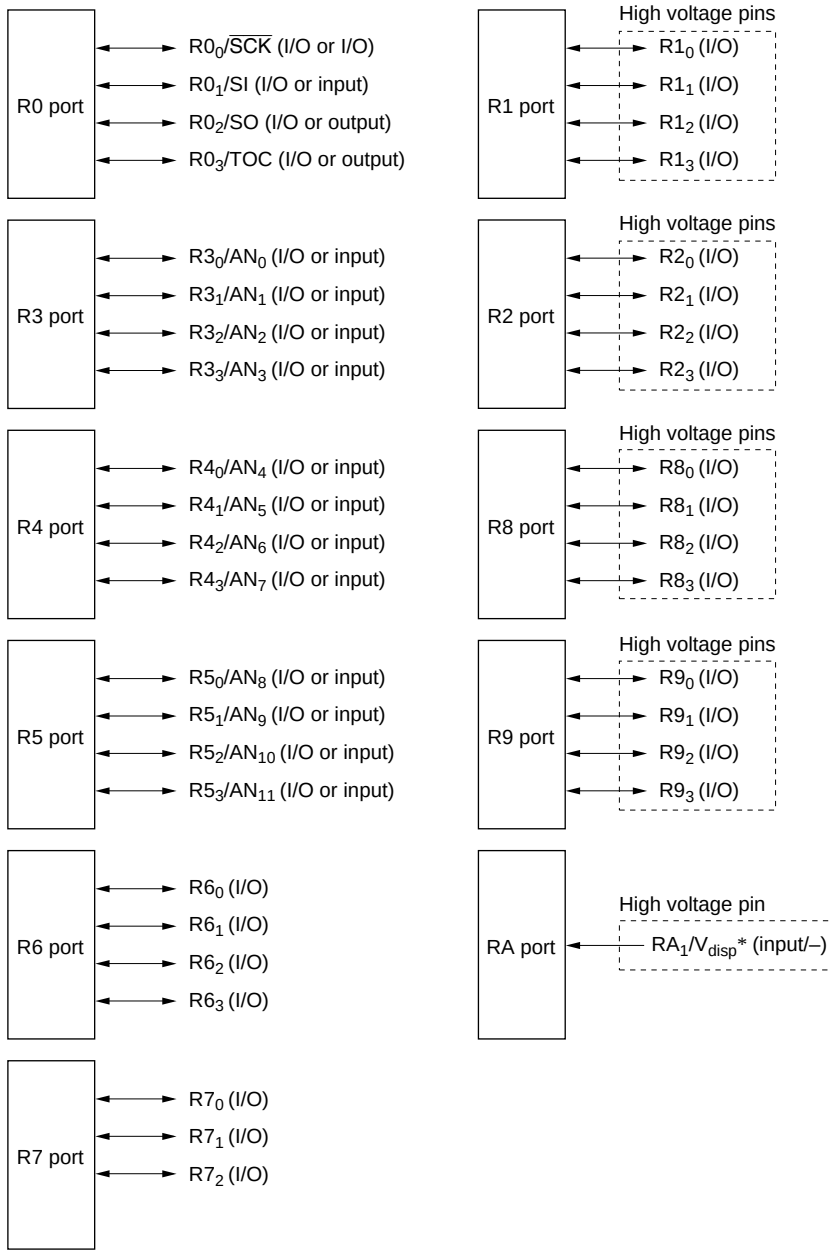
The individual R ports are accessed in 4-bit units with the LRA and LRB output instructions to control the output levels (high or low) on each pin. Output data is stored in the PDR built into each pin. Similarly, the LAR and LBR input instructions can be used to access the R ports in 4-bit units to read the input levels on the port pins.

The RA_1 input-only port consists of a single bit. The values of bits 3, 2, and 0 are undefined when this port is accessed by the input instructions.

DCR registers are used to control on/off states of the R0 and R3 to R7 output buffers. When the DCR bit corresponding to a pin in an R0 or R3 to R7 port is set to 1, the contents of the PDR corresponding to that pin is output from the pin. Thus the output buffer on/off states can be controlled on an individual pin basis for the R port pins. The DCR registers are allocated in the RAM address space.

The R0 and R3 to R5 port pins have shared functions as built-in peripheral module pins. Register settings are used to switch these functions. (See table 11-7.)

Figure 11-2 shows the R port pin structure.



Note: * In products with on-chip mask resistors, the use of this pin as the V_{disp} pin (display power supply pin) can be selected as a mask option.
High voltage pins for which a pull-down MOS transistor is selected are pulled down to the V_{disp} potential.

Figure 11-2 R Port Structure

11.3.2 Register Configuration and Descriptions

Table 11-7 shows the configuration of the R port related registers,

Table 11-7 R Port Register Configuration

Address	Register		Symbol	R/W	Initial Value
—	Port data registers	Standard voltage pins	PDR	W*	1
		High voltage pins			0
$030	Data control registers		DCR0	W	$0
$033			DCR3	W	$0
$034			DCR4	W	$0
$035			DCR5	W	$0
$036			DCR6	W	$0
$037			DCR7	W	-000
$004	Port mode register A		PMRA	W	$0
$005	Serial mode register		SMR	W	$0
$019	A/D mode register 1		AMR1	W	$0
$01A	A/D mode register 2		AMR2	W	-000

Note: * The LRA and LRB instructions are used to write to the PDR registers.

(1) Port Data Registers: All the I/O pins in ports R0 to R9 include a PDR that holds the output data. When an LRA or an LRB instruction is executed for one of ports R0 to R9, the contents of the accumulator (A) or the B register (B) are transferred to the specified R port PDRs. When bits in DCR0 and DCR3 to DCR7 are set to 1, the output buffers for the corresponding pins in ports R0 and R3 to R7 will be turned on and the values in the PDRs will be output from those pins.

The PDR registers for standard voltage pins are set to 1 on reset and in stop mode, and the PDRs for high voltage pins are cleared to 0.

(2) Data Control Registers (DCR0, DCR3 to DCR7: $030, $033 to $037)

DCR0: $030

Bit	3	2	1	0
	DCR03	DCR02	DCR01	DCR00
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR3: $033

Bit	3	2	1	0
	DCR33	DCR32	DCR31	DCR30
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR4: $034

Bit	3	2	1	0
	DCR43	DCR42	DCR41	DCR40
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR5: $035

Bit	3	2	1	0
	DCR53	DCR52	DCR51	DCR50
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR6: $036

Bit	3	2	1	0
	DCR63	DCR62	DCR61	DCR60
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR7: $037

Bit	3	2	1	0
	—	DCR72	DCR71	DCR70
Initial value	—	0	0	0
Read/Write	—	W	W	W

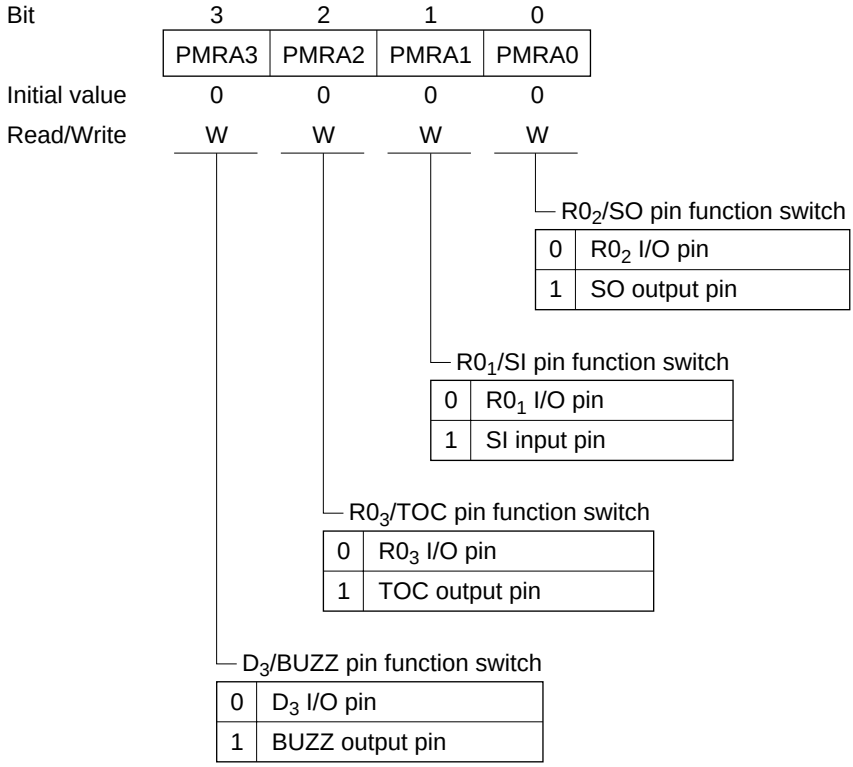
Bits in DCR0 and DCR3 to DCR7	Description
0	The output buffer (CMOS buffer) is turned off and the output goes to the high impedance state. (initial value)
1	The output buffer is turned on and the corresponding PDR value is output.

The table below lists the correspondence between the bits in DCR0 and DCR3 to DCR7 and the port R0 and R3 to R7 pins.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCR6	$R6_3$	$R6_2$	$R6_1$	$R6_0$
DCR7	—	$R7_2$	$R7_1$	$R7_0$

(3) Port Mode Register A (PMRA: $004): PMRA is a 4-bit write-only register whose bits PMRA2 to PMRA0 switch the functions of the port R0 shared function pins.

This section describes the bits PMRA2 to PMRA0. See section 11.2.2 (2), “Port Mode Register A (PMRA)”, for details on the PMRA3 bit.



Bit 2—R0$_3$/TOC Pin Function Switch (PMRA2): Selects whether the R0$_3$/TOC pin functions as the R0$_3$ I/O pin or as the timer C output pin (TOC).

PMRA2	Description	
0	The R0$_3$/TOC pin functions as the R0$_3$ I/O pin.	(initial value)
1	The R0$_3$/TOC pin functions as the TOC output pin.	

Bit 1—$R0_1$/SI Pin Function Switch (PMRA1): Selects whether the $R0_1$/SI pin functions as the $R0_1$ I/O pin or as the serial reception data input pin (SI).

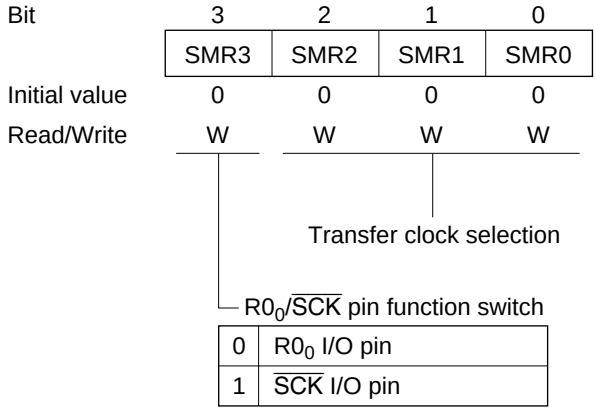
PMRA1	Description	
0	The $R0_1$/SI pin functions as the $R0_1$ I/O pin.	(initial value)
1	The $R0_1$/SI pin functions as the SI input pin.	

Bit 0—$R0_2$/SO Pin Function Switch (PMRA0): Selects whether the $R0_2$/SO pin functions as the $R0_2$ I/O pin or as the serial transmission data output pin (SO).

PMRA0	Description	
0	The $R0_2$/SO pin functions as the $R0_2$ I/O pin.	(initial value)
1	The $R0_2$/SO pin functions as the SO output pin.	

(4) Serial Mode Register (SMR: $005): SMR is a 4-bit write-only register whose SMR3 bit switches the $R0_0/\overline{SCK}$ pin function.

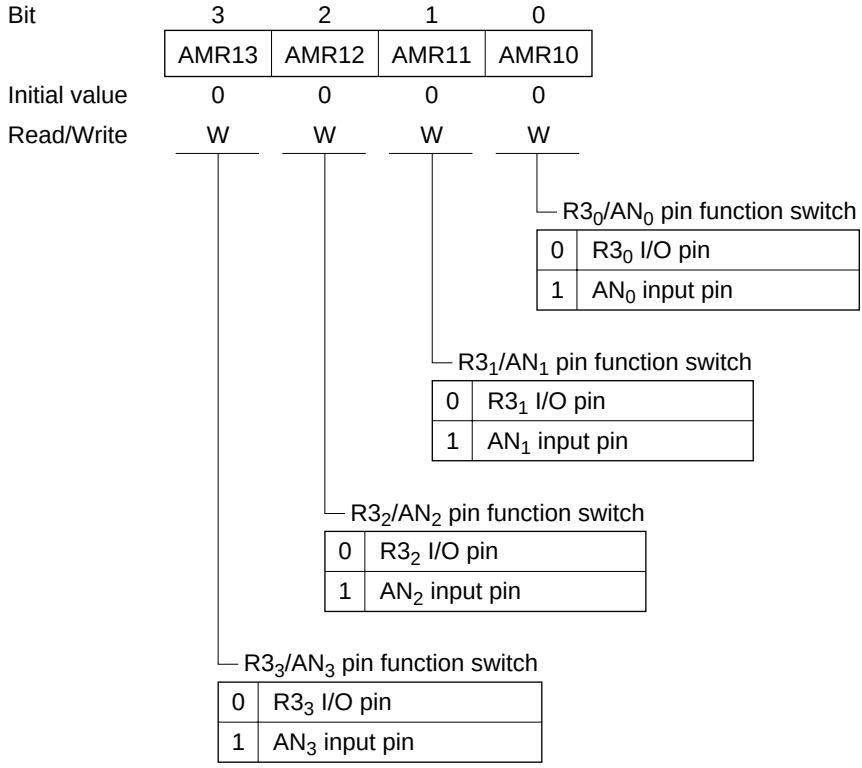
This section only describes the SMR3 bit. See section 20.2.1, “Serial Mode Register (SMR)” for details on bits SMR2 to SMR0.



Bit 3—$R0_0/\overline{SCK}$ Pin Function Switch (SMR3): Selects whether the $R0_0/\overline{SCK}$ pin functions as the $R0_0$ I/O pin or as the serial interface transfer clock I/O pin ($\overline{SCK}$).

SMR3	Description	
0	The $R0_0/\overline{SCK}$ pin functions as the $R0_0$ I/O pin.	(initial value)
1	The $R0_0/\overline{SCK}$ pin functions as the $\overline{SCK}$ I/O pin.	

(5) A/D Mode Register 1 (AMR1: $019): AMR1 is a 4-bit write-only register that switches the functions of the R3 port shared function pins.



Bit 3—R3$_3$/AN$_3$ Pin Function Switch (AMR13): Selects whether the R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin or as the A/D converter channel 3 input pin AN$_3$.

AMR13	Description	
0	The R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin.	(initial value)
1	The R3$_3$/AN$_3$ pin functions as the AN$_3$ input pin.	

Bit 2—R3$_2$/AN$_2$ Pin Function Switch (AMR12): Selects whether the R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin or as the A/D converter channel 2 input pin AN$_2$.

AMR12	Description	
0	The R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin.	(initial value)
1	The R3$_2$/AN$_2$ pin functions as the AN$_2$ input pin.	

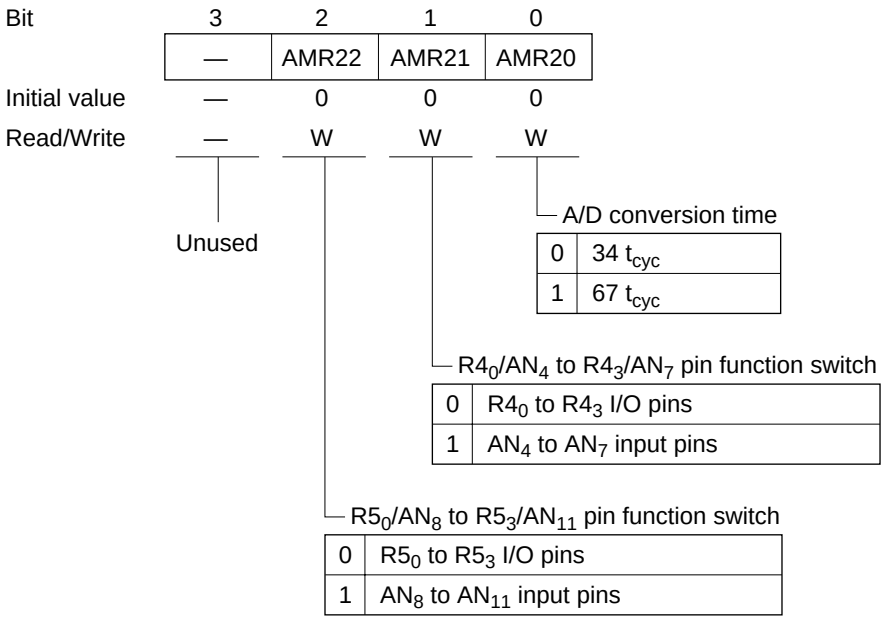
Bit 1—$R3_1/AN_1$ Pin Function Switch (AMR11): Selects whether the $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin or as the A/D converter channel 1 input pin AN_1.

AMR11	Description	
0	The $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin.	(initial value)
1	The $R3_1/AN_1$ pin functions as the AN_1 input pin.	

Bit 0—$R3_0/AN_0$ Pin Function Switch (AMR10): Selects whether the $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin or as the A/D converter channel 0 input pin AN_0.

AMR10	Description	
0	The $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin.	(initial value)
1	The $R3_0/AN_0$ pin functions as the AN_0 input pin.	

(6) A/D Mode Register 2 (AMR2: $01A): AMR2 is a 3-bit write-only register whose AMR21 bit switches the functions of all four bits of the R4 port ($R4_0$ to $R4_3$) to be A/D converter input channels (AN_4 to AN_7), and whose AMR22 bit switches the R5 port to be the AN_8 to AN_{11} input channels. This section describes the AMR21 and AMR22 bits. See section 15.2.2, “A/D Mode Register 2 (AMR2)”, for details on the AMR20 bit.



Bit 2—$R5_0/AN_8$ to $R5_3/AN_{11}$ Pin Function Switch (AMR22): Selects whether the $R5_0/AN_8$ to $R5_3/AN_{11}$ pins function as the $R5_0$ to $R5_3$ I/O pins or as the A/D converter channel 8 to 11 input pins (AN_8 to AN_{11}).

AMR22	Description	
0	The $R5_0/AN_8$ to $R5_3/AN_{11}$ pins function as the $R5_0$ to $R5_3$ I/O pins.	(initial value)
1	The $R5_0/AN_8$ to $R5_3/AN_{11}$ pins function as the AN_8 to AN_{11} input pins.	

Bit 1—$R4_0/AN_4$ to $R4_3/AN_7$ Pin Function Switch (AMR21): Selects whether the $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins or as the A/D converter channel 4 to 7 input pins (AN_4 to AN_7).

AMR21	Description	
0	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins.	(initial value)
1	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the AN_4 to AN_7 input pins.	

11.3.3 Pin Functions

The pin functions of the R port pins are switched by register settings as shown in table 11-8.

Table 11-8 R Port Pin Functions

Pin	Pin Functions and Selection Methods
$R0_0$/$\overline{SCK}$	The pin function is switched by the SMR SMR3 bit and the DCR0 DCR00 bit as shown below.

SMR3	0		1
DCR00	0	1	—
Pin function	$R0_0$ input pin	$R0_0$ output pin	$\overline{SCK}$ I/O pin

$R0_1$/SI	The pin function is switched by the PMRA PMRA1 bit and the DCR0 DCR01 bit as shown below.

PMRA1	0		1
DCR01	0	1	—
Pin function	$R0_1$ input pin	$R0_1$ output pin	SI input pin

$R0_2$/SO	The pin function is switched by the PMRA PMRA0 bit and the DCR0 DCR02 bit as shown below.

PMRA0	0		1
DCR02	0	1	—
Pin function	$R0_2$ input pin	$R0_2$ output pin	SO output pin

$R0_3$/TOC	The pin function is switched by the PMRA PMRA2 bit and the DCR0 DCR03 bit as shown below.

PMRA2	0		1
DCR03	0	1	—
Pin function	$R0_3$ input pin	$R0_3$ output pin	TOC output pin

Table 11-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R3_0/AN_0$	The pin function is switched by the AMR1 AMR10 bit and the DCR3 DCR30 bit as shown below.

AMR10	0		1
DCR30	0	1	—
Pin function	$R3_0$ input pin	$R3_0$ output pin	AN_0 input pin

$R3_1/AN_1$	The pin function is switched by the AMR1 AMR11 bit and the DCR3 DCR31 bit as shown below.

AMR11	0		1
DCR31	0	1	—
Pin function	$R3_1$ input pin	$R3_1$ output pin	AN_1 input pin

$R3_2/AN_2$	The pin function is switched by the AMR1 AMR12 bit and the DCR3 DCR32 bit as shown below.

AMR12	0		1
DCR32	0	1	—
Pin function	$R3_2$ input pin	$R3_2$ output pin	AN_2 input pin

$R3_3/AN_3$	The pin function is switched by the AMR1 AMR13 bit and the DCR3 DCR33 bit as shown below.

AMR13	0		1
DCR33	0	1	—
Pin function	$R3_3$ input pin	$R3_3$ output pin	AN_3 input pin

$R4_0/AN_4$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR40 bit as shown below.

AMR21	0		1
DCR40	0	1	—
Pin function	$R4_0$ input pin	$R4_0$ output pin	AN_4 input pin

Table 11-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R4_1/AN_5$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR41 bit as shown below.

AMR21	0		1
DCR41	0	1	—
Pin function	$R4_1$ input pin	$R4_1$ output pin	AN_5 input pin

$R4_2/AN_6$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR42 bit as shown below.

AMR21	0		1
DCR42	0	1	—
Pin function	$R4_2$ input pin	$R4_2$ output pin	AN_6 input pin

$R4_3/AN_7$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR43 bit as shown below.

AMR21	0		1
DCR43	0	1	—
Pin function	$R4_3$ input pin	$R4_3$ output pin	AN_7 input pin

$R5_0/AN_8$	The pin function is switched by the AMR2 AMR22 bit and the DCR5 DCR50 bit as shown below.

AMR22	0		1
DCR50	0	1	—
Pin function	$R5_0$ input pin	$R5_0$ output pin	AN_8 input pin

$R5_1/AN_9$	The pin function is switched by the AMR2 AMR22 bit and the DCR5 DCR51 bit as shown below.

AMR22	0		1
DCR51	0	1	—
Pin function	$R5_1$ input pin	$R5_1$ output pin	AN_9 input pin

Table 11-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R5_2/AN_{10}$	The pin function is switched by the AMR2 AMR22 bit and the DCR5 DCR52 bit as shown below.

AMR22	0		1
DCR52	0	1	—
Pin function	$R5_2$ input pin	$R5_2$ output pin	AN_{10} input pin

Pin	Pin Functions and Selection Methods
$R5_3/AN_{11}$	The pin function is switched by the AMR2 AMR22 bit and the DCR5 DCR53 bit as shown below.

AMR22	0		1
DCR53	0	1	—
Pin function	$R5_3$ input pin	$R5_3$ output pin	AN_{11} input pin

11.4 Usage Notes

Keep the following points in mind when using the I/O ports.

- When the MIS MIS2 bit is set to 1, the $R0_2$/SO pin will be an NMOS open drain output regardless of whether it is selected for use as the $R0_2$ pin or as the SO pin by the PMRA PMRA0 bit.

- I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation. The following are examples of techniques that can prevent noise problems.

  High voltage pin: Select “no pull-down MOS transistor (PMOS open drain)” as the mask option and connect the pin to V_{CC} on the user system printed circuit board.

  Standard voltage pin: Either use the built-in pull-up MOS transistor to pull the pin up to V_{CC}, or pull up the pin to V_{CC} externally with a pull-up resistor of about 100 kΩ.

  Application programs should maintain the PDR and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

- When the MIS MIS3 bit is set to 1 (pull-up MOS transistors active) and the PDR for an R port/analog input shared function pin has the value 1, the MOS transistor for the corresponding pin will not be turned off by selecting the analog input function with the AMR1 or AMR2 register.

  To use an R port/analog input shared function pin as an analog input when the pull-up MOS transistors are active, always clear the PDR for the corresponding pin to 0 first and then turn off the pull-up MOS transistor. (Note that the PDR registers are set to 1 immediately following a reset.)

  Figure 11-3 shows the circuit for the R port/analog input shared function pins. AMR1 and AMR2 are used to set the port outputs to high impedance. ACR is used to switch the analog input channel.

  The states of the R port/analog input shared function pins are set, as shown in table 11-9, by the combination of the AMR1 (or AMR2) register, the MIS3 bit, the DCR, and the PDR settings.

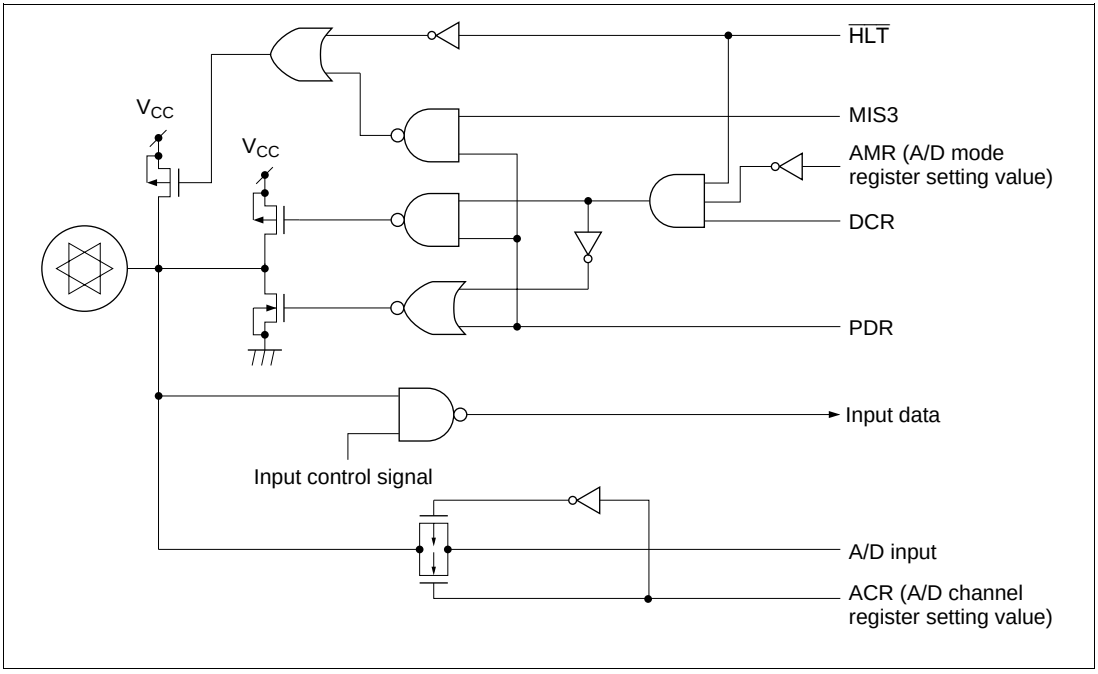


Figure 11-3 R Port/Analog Input Shared Function Pin Circuit Structure

Table 11-9 Program Control of the R Port/Analog Input Shared Function Pins

Corresponding bit in AMR1 or AMR2		0 (R port selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Note: —: off

Corresponding bit in AMR1 or AMR2		1 (analog input selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	—	—		—	—
	NMOS			—	—			—	—
Pull-up MOS transistor		—				—	On	—	On

Note: —: off

Section 12 I/O Ports (HD404369 Series)

12.1 Overview

12.1.1 Features

The HD404369 Series I/O ports have the following features.

- The eight pins $R1_0$ to $R1_3$ and $R2_0$ to $R2_3$ are medium voltage NMOS open drain I/O pins. RA_1 is an input-only pin. The D, R0, R1, and R3 to R9 port pins are standard voltage I/O pins that, in output mode, are CMOS three state outputs.
- Certain I/O pins (D_0 to D_4, and the pins in the R0 and R3 to R5 ports) are shared with the built-in peripheral modules, such as timers and the serial interface. Setting these pins for use with the built-in peripheral modules takes priority over their setting for use as D or R port pins.
- Register settings are used to select input or output for I/O pins and to select the I/O port or peripheral module usage for shared function pins.
- All peripheral module output pins are CMOS outputs. However, the $R0_2$/SO pin can be selected to be an NMOS open drain output by setting a register.
- Since the system is reset in stop mode, the built-in peripheral module selections are cleared and the I/O pins go to the high impedance state.
- The CMOS output pins have built-in programmable pull-up MOS transistors. The on/off state of these transistors can be controlled by register settings on an individual basis. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 12-1 provides an overview of the HD404369 Series port functions.

Table 12-1 Port Functions

Port	Overview	Pin	Shared Function	Function Switching Register
D_0 to D_{13}	• Standard voltage I/O port • Accessed in bit units • Accessed with the SED, SEDD, RED, REDD, TD, and TDD instructions. • Programmable pull-up MOS transistors	$D_0/\overline{INT}_0$	External interrupt input 0	PMRB
		$D_1/\overline{INT}_1$	External interrupt input 1	
		D_2/EVNB	Timer B event input	
		D_3/BUZZ	Alarm output	PMRA
		$D_4/\overline{STOPC}$	Stop mode clear	PMRB
		D_5 to D_{13}	—	—
R0	• Standard voltage I/O port • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions. • Programmable pull-up MOS transistors	$R0_0/\overline{SCK}$	Transfer clock I/O	SMR
		$R0_1$/SI	Serial reception data input	PMRA
		$R0_2$/SO	Serial transmission data output	
		$R0_3$/TOC	Timer C output	
R3		$R3_0/AN_0$	Analog input channel 0	AMR1
		$R3_1/AN_1$	Analog input channel 1	
		$R3_2/AN_2$	Analog input channel 2	
		$R3_3/AN_3$	Analog input channel 3	
R4		$R4_0/AN_4$	Analog input channel 4	AMR2
		$R4_1/AN_5$	Analog input channel 5	
		$R4_2/AN_6$	Analog input channel 6	
		$R4_3/AN_7$	Analog input channel 7	
R5		$R5_0/AN_8$	Analog input channel 8	AMR2
		$R5_1/AN_9$	Analog input channel 9	
		$R5_2/AN_{10}$	Analog input channel 10	
		$R5_3/AN_{11}$	Analog input channel 11	
R6 to R9		$R6_0$ to $R6_3$	—	—
		$R7_0$ to $R7_2$		
		$R8_0$ to $R8_3$		
		$R9_0$ to $R9_3$		

Table 12-1 Port Functions (cont)

Port	Overview	Pin	Shared Function	Function Switching Register
R1, R2	• Medium voltage NMOS open drain I/O port • Accessed in 4-bit units. • Accessed with the LAR, LBR, LRA, and LRB instructions.	$R1_0$ to $R1_3$ $R2_0$ to $R2_3$	—	—
RA	• Standard voltage input port (1 bit) • Accessed with the LAR and LBR instructions.	RA_1	—	—

12.1.2 I/O Control

R1 and R2 are medium voltage NMOS open drain I/O ports and the D, R0, and R3 to R9 ports are standard voltage I/O ports. The different port types have different circuit structures as follows.

(1) Medium Voltage NMOS Open Drain I/O Pin Circuit: R1 and R2 are medium voltage NMOS open drain I/O ports and I/O through these ports is controlled by the port data registers (PDR) and the data control registers (DCR). When the DCR bit corresponding to a given pin is 1, that pin functions as an output pin and when the value in the PDR is 0, the pin's NMOS transistor turns on and the pin outputs a low level voltage. When the value in the PDR is 1 the pin goes to the high impedance state. When a given DCR bit is 0, the corresponding pin functions as an input pin.

(2) Standard Voltage CMOS Three State I/O Pin Circuit: The pins in the D, R0, and R3 to R9 ports are standard voltage CMOS three state I/O ports. I/O through these ports is controlled by the PDRs and the data control registers (DCD or DCR). When the DCD or DCR bit corresponding to a given pin is 1, that pin functions as an output pin and outputs the value in the PDR. When a given DCD or DCR bit is 0, the corresponding pin functions as an input pin.

(3) Pull-Up MOS Control: Each I/O pin in the D, R0 and R3 to R9 ports has a built-in programmable pull-up MOS transistor. When the miscellaneous register (MIS) MIS3 bit is set to 1 the pull-up MOS transistor for pins for which the corresponding PDR is set to 1 will be turned on. Thus the on/off state of each pin can be controlled independently by the PDRs. Note that the pull-up MOS transistor on/off settings are independent of the pin settings for use as built-in peripheral module pins.

Table 12-2 shows how register settings control the port I/O pins.

Table 12-2 Register Settings for I/O Pin Control

MIS3		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

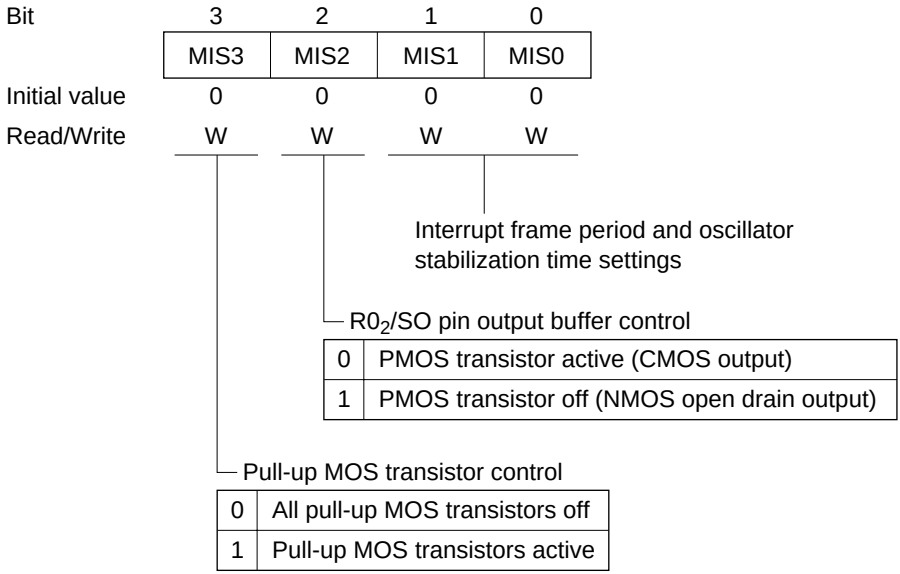
Notes: 1. —: Off

2. The PDR registers are not allocated addresses in RAM. The PDR registers are accessed by special-purpose I/O instructions.

(4) Miscellaneous Register (MIS: $00C): MIS is a 4-bit write-only register that controls the on/off states of the D, R0, and R3 to R9 port pin pull-up MOS transistors and the on/off state of the $R0_2$/SO pin output buffer PMOS transistor.

MIS is initialized to $0 on reset and in stop mode.

This section describes the MIS2 and MIS3 bits. Refer to section 6.2.1, “Miscellaneous Register (MIS)”, for details on the MIS0 and MIS1 bits.



Bit 3—Pull-Up MOS Transistor Control (MIS3): Controls the on/off states of the pull-up MOS transistors built into the I/O port pins.

MIS3	Description	
0	All pull-up MOS transistors will be turned off.	(initial value)
1	Pull-up MOS transistors for which the corresponding PDR bit is 1 will be turned on.	

Bit 2—$R0_2$/SO Pin Output Buffer Control (MIS2): Controls the on/off state of the $R0_2$/SO pin output buffer PMOS transistor.

MIS2	Description	
0	The $R0_2$/SO pin output will be a CMOS output.	(initial value)
1	The $R0_2$/SO pin output will be an NMOS open drain output.	

12.1.3 I/O Pin Circuit Structures

Table 12-3 shows the port and peripheral module pin circuits.

Notes: 1. Since the system is reset in stop mode, the built-in peripheral module selections are cleared. Since the internal $\overline{HLT}$ signal goes to the low (active) level, the I/O pins go to the high impedance state. Also, all the pull-up MOS transistors are turned off.

2. In all low power modes other than stop mode, the internal $\overline{HLT}$ signal goes to the high level.

Table 12-3 Input and Output Pin Circuits

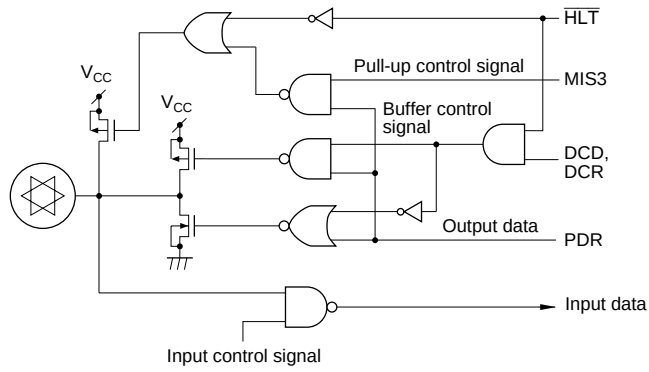
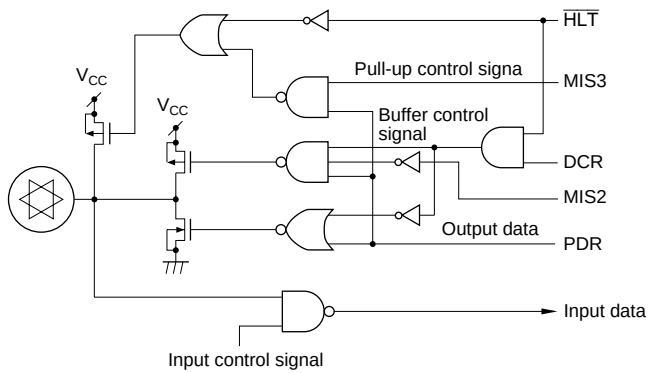
Class	Circuit	Applicable Pins
Standard voltage pins	I/O pins	D_0 to D_{13}, $R0_0$, $R0_1$, $R0_3$, $R3_0$ to $R3_3$, $R4_0$ to $R4_3$, $R5_0$ to $R5_3$, $R6_0$ to $R6_3$, $R7_0$ to $R7_2$, $R8_0$ to $R8_3$, $R9_0$ to $R9_3$
		
		$R0_2$

Table 12-3 Input and Output Pin Circuits (cont)

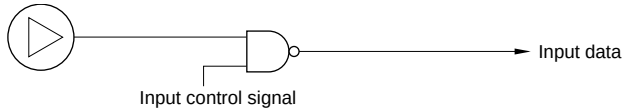
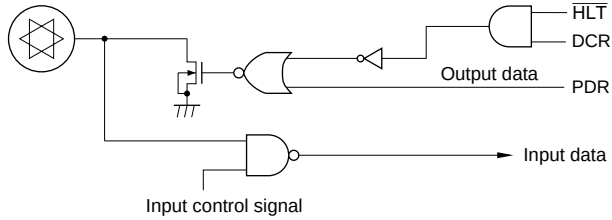
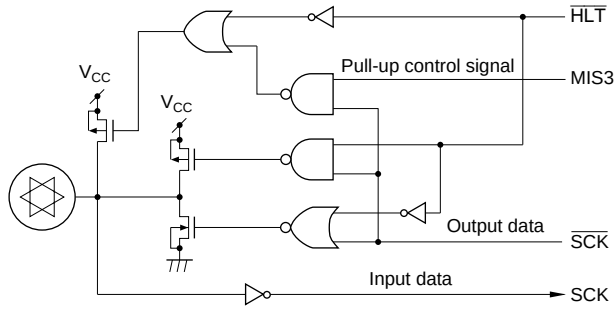
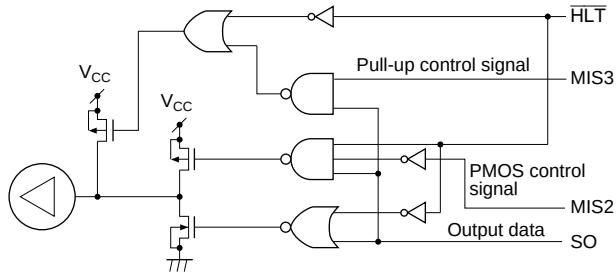
Class		Circuit	Applicable Pins
Standard voltage pins	Input pins		RA_1
Medium voltage pins	I/O pins		$R1_0$ to $R1_3$, $R2_0$ to $R2_3$

Table 12-3 Input and Output Pin Circuits (cont)

Class		Circuit	Applicable Pins
Standard voltage pins	Standard peripheral module pins	I/O pins	$\overline{SCK}$
		Output pins	SO
			TOC, BUZZ





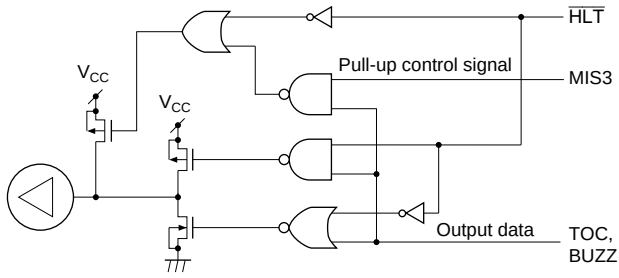
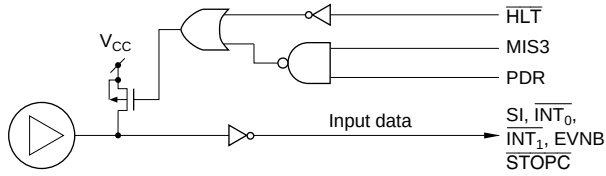
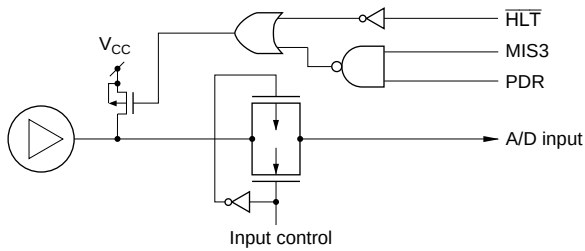


Table 12-3 Input and Output Pin Circuits (cont)

Class			Circuit	Applicable Pins
Standard voltage pins	Built-in peripheral module pins	Input pins		SI, $\overline{INT_0}$, $\overline{INT_1}$, EVNB, $\overline{STOPC}$
				AN_0 to AN_{11}

12.1.4 Port States in Low Power Modes

The D_0 to D_4 pins and the R0 and R3 to R5 port pins have shared functions as input or output pins for built-in peripheral modules. Since the CPU stops in standby and watch mode, the pins selected as output ports maintain their immediately prior output values. Also, pins selected for use by built-in peripheral modules that operate in standby or watch mode continue to operate. (Output pins used by modules that stop in standby or watch mode maintain their immediately prior output values.) See section 6, “Low Power Modes”, for details on which built-in peripheral modules can operate in each mode.

Table 12-4 lists the port states in the low power modes.

Table 12-4 Port States in Low Power Modes

Low Power Mode	Port States
Standby mode, watch mode	Pins maintain their values immediately prior to entering standby mode.
Stop mode	Built-in peripheral function selections are cleared, and the port and peripheral function I/O pins go to the high impedance state.

12.1.5 Handling Unused Pins

I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation.

The built-in pull-up MOS transistors can be used to pull up unused pins to V_{CC}. Alternatively, unused pins can be pulled up to V_{CC} with external resistors of about 100 kΩ.

Application programs should maintain the PDR and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

12.2 D Port

12.2.1 Overview

The D port is a 14-pin I/O port (D_0 to D_{13}) that can be accessed in 1-bit units.

The output levels on the pins D_0 to D_{13} can be set to low or high by accessing the port in one-bit units with the SED, SEDD, RED, and REDD output instructions. The output data is stored in the PDR for each pin. The level on each of the pins D_0 to D_{13} can be tested in one-bit units with the TD and TDD input instructions.

The DCD registers are used to turn the D port output buffers on or off. When the DCD bit corresponding to a given pin is 1, the data in the corresponding PDR will be output from that pin. The on/off states of the output buffers can be controlled individually for each D port pin. The DCD registers are allocated in the RAM address space.

The pins D_0 to D_4 have shared functions as built-in peripheral module pins. PMRB is used to switch these functions.

Figure 12-1 shows the structure of the D port.

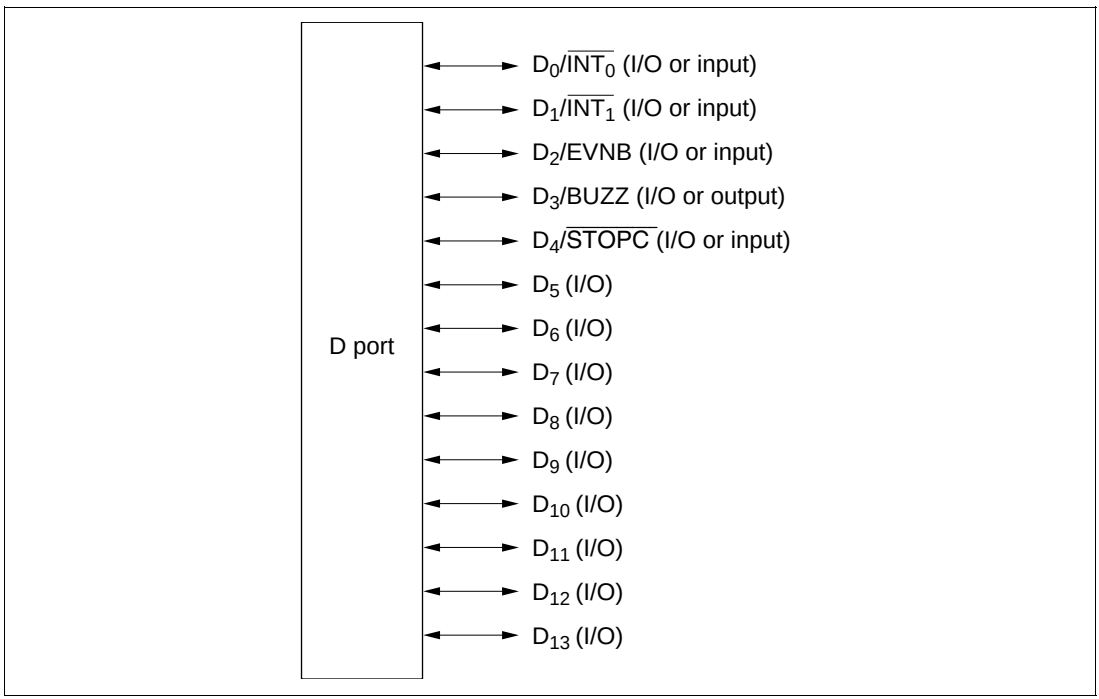


Figure 12-1 D Port Structure

12.2.2 Register Configuration and Descriptions

Table 12-5 shows the configuration of the D port registers.

Table 12-5 D Port Register Configuration

Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	1
$02C	Data control registers	DCD0	W	$0
$02D		DCD1	W	$0
$02E		DCD2	W	$0
$02F		DCD3	W	--00
$024	Port mode register B	PMRB	W	$0

Note: * The SED, SEDD, RED, and REDD instructions can be used to write to the PDRs.

(1) Port Data Registers (PDR): Each of the I/O pins D_0 to D_{13} includes a built-in PDR. When a SED or SEDD instruction is executed for one of the pins D_0 to D_{13} the corresponding PDR is set to 1, and when a RED or REDD instruction is executed, the corresponding PDR is cleared to 0. When bits in DCD0 to DCD3 are set to 1, the output buffers for the corresponding pins will be turned on and the values in the PDRs will be output from those pins.

The PDRs are cleared to 1 on reset and in stop mode.

(2) Data Control Registers (DCD0 to DCD3: $02C, $02D, $02E, $02F)

DCD0: $02C	Bit	3	2	1	0
		DCD03	DCD02	DCD01	DCD00
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

DCD1: $02D	Bit	3	2	1	0
		DCD13	DCD12	DCD11	DCD10
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

DCD2: $02E	Bit	3	2	1	0
		DCD23	DCD22	DCD21	DCD20
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

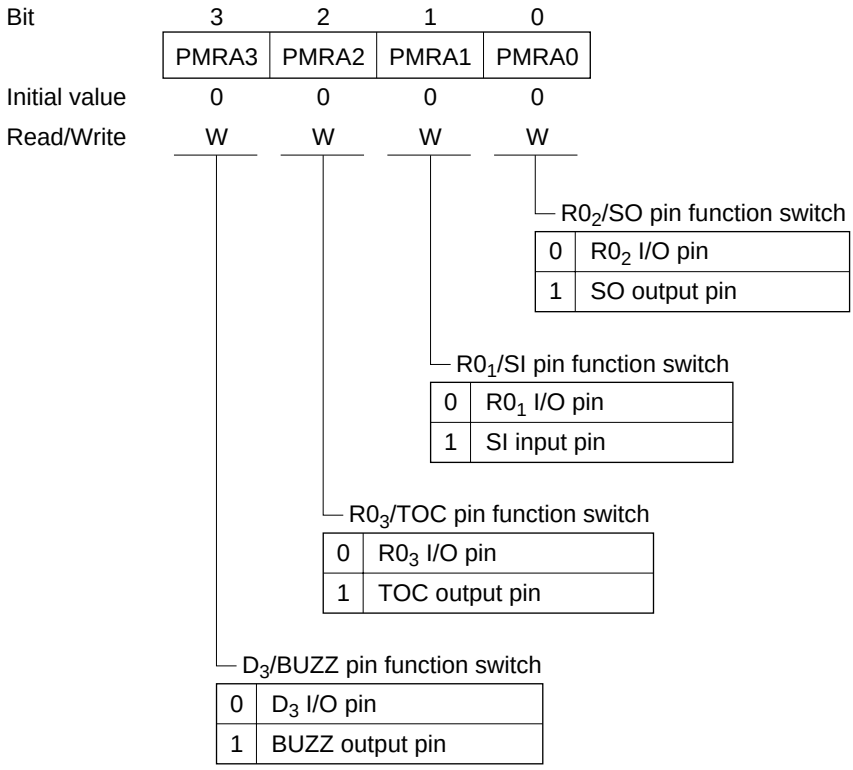
DCD3: $02F	Bit	3	2	1	0
		—	—	DCD31	DCD30
	Initial value	—	—	0	0
	Read/Write	—	—	W	W

Bits in DCD0 to DCD3	Description
0	The output buffer (CMOS buffer) is turned off and the output goes to the high impedance state. (initial value)
1	The output buffer is turned on and the corresponding PDR value is output.

The table below lists the correspondence between the bits in DCD0 to DCD2 and the D port pins.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCD0	D_3	D_2	D_1	D_0
DCD1	D_7	D_6	D_5	D_4
DCD2	D_{11}	D_{10}	D_9	D_8
DCD3	—	—	D_{13}	D_{12}

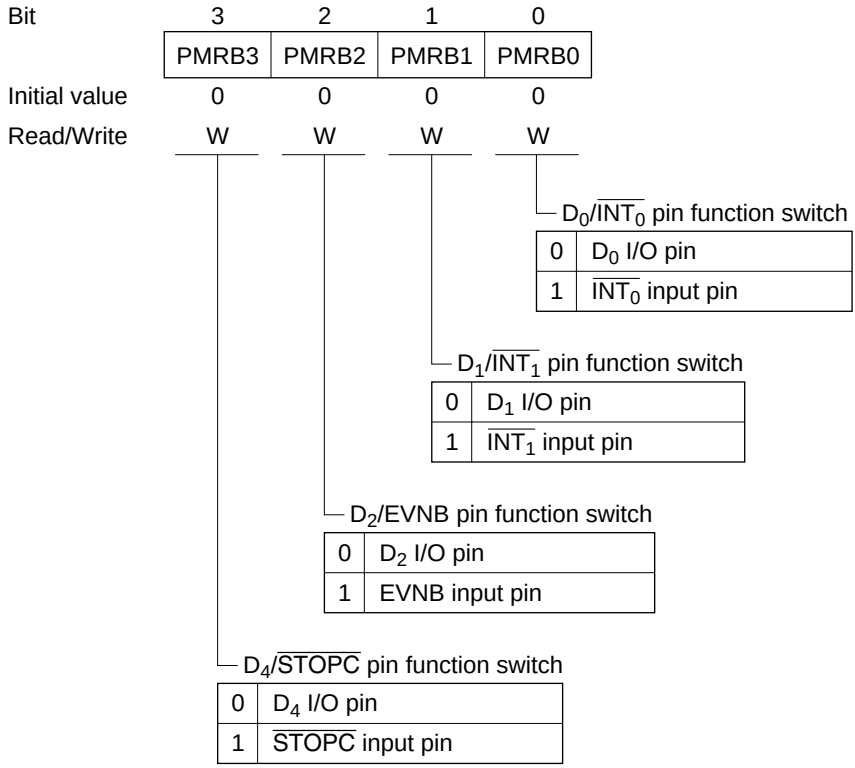
(3) Port Mode Register A (PMRA: $004): PMRA is a 4-bit write-only register whose PMRA3 bit switches the function of the D_3/BUZZ pin. This section describes the function of the PMRA3 bit. See section 12.3.2 (3), “Port Mode Register A (PMRA)”, for details on the PMRA2 to PMRA0 bits.



Bit 3—D_3/BUZZ Pin Function Switch (PMRA3): Selects whether the D_3/BUZZ pin functions as the D_3 I/O pin or as the alarm output pin (BUZZ).

PMRA3	Description	
0	D_3/BUZZ pin functions as the D_3 I/O pin.	(initial value)
1	D_3/BUZZ pin functions as the BUZZ output pin.	

(4) Port Mode Register B (PMRB: $024): PMRB is a 4-bit write-only register that switches the D port I/O pin shared functions.



Bit 3—D_4/$\overline{\text{STOPC}}$ Pin Function Switch (PMRB3): Selects whether the D_4/$\overline{\text{STOPC}}$ pin is used as the D_4 I/O pin or as the stop mode clear pin ($\overline{\text{STOPC}}$).

PMRB3	Description	
0	The D_4/$\overline{\text{STOPC}}$ pin functions as the D_4 I/O pin.	(initial value)
1	The D_4/$\overline{\text{STOPC}}$ pin functions as the $\overline{\text{STOPC}}$ input pin.	

Bit 2—D_2/EVNB Pin Function Switch (PMRB2): Selects whether the D_2/EVNB pin is used as the D_2 I/O pin or as the timer B event count input pin (EVNB).

PMRB2	Description	
0	The D_2/EVNB pin functions as the D_2 I/O pin.	(initial value)
1	The D_2/EVNB pin functions as the EVNB input pin.	

Bit 1—$D_1/\overline{INT}_1$ Pin Function Switch (PMRB1): Selects whether the $D_1/\overline{INT}_1$ pin is used as the D_1 I/O pin or as the external interrupt 1 input pin ($\overline{INT}_1$).

PMRB1	Description	
0	The $D_1/\overline{INT}_1$ pin functions as the D_1 I/O pin.	(initial value)
1	The D1/$\overline{INT}_1$ pin functions as the $\overline{INT}_1$ input pin.	

Bit 0—$D_0/\overline{INT}_0$ Pin Function Switch (PMRB0): Selects whether the $D_0/\overline{INT}_0$ pin is used as the D_0 I/O pin or as the external interrupt 0 input pin ($\overline{INT}_0$).

PMRB0	Description	
0	The $D_0/\overline{INT}_0$ pin functions as the D_0 I/O pin.	(initial value)
1	The $D_0/\overline{INT}_0$ pin functions as the $\overline{INT}_0$ input pin.	

12.2.3 Pin Functions

The functions of the pins D_0 to D_{13} are switched by register settings as shown in table 12-6.

Table 12-6 D_0 to D_{13} Port Pin Functions

Pin	Pin Functions and Selection Methods
$D_0/\overline{INT}_0$	The pin function is switched as shown below by the PMRB PMRB0 bit and the DCD0 DCD00 bit.

PMRB	0		1
DCD00	0	1	—
Pin function	D_0 input pin	D_0 output pin	$\overline{INT}_0$ input pin

$D_1/\overline{INT}_1$	The pin function is switched as shown below by the PMRB PMRB1 bit and the DCD0 DCD01 bit.

PMRB1	0		1
DCD01	0	1	—
Pin function	D_1 input pin	D_1 output pin	$\overline{INT}_1$ input pin

D_2/EVNB	The pin function is switched as shown below by the PMRB PMRB2 bit and the DCD0 DCD02 bit.

PMRB2	0		1
DCD02	0	1	—
Pin function	D_2 input pin	D_2 output pin	EVNB input pin

D_3/BUZZ	The pin function is switched as shown below by the PMRA PMRA3 bit and the DCD0 DCD03 bit.

PMRA3	0		1
DCD03	0	1	—
Pin function	D_3 input pin	D_3 output pin	BUZZ output pin

$D_4/\overline{STOPC}$	The pin function is switched as shown below by the PMRB PMRB3 bit and the DCD1 DCD10 bit.

PMRB3	0		1
DCD10	0	1	—
Pin function	D_4 input pin	D_4 output pin	$\overline{STOPC}$ input pin

Table 12-6 D_0 to D_{13} Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
D_5	The pin function is switched as shown below by the DCD1 DCD11 bit.

DCD11	0	1
Pin function	D_5 input pin	D_5 output pin

D_6	The pin function is switched as shown below by the DCD1 DCD12 bit.

DCD12	0	1
Pin function	D_6 input pin	D_6 output pin

D_7	The pin function is switched as shown below by the DCD1 DCD13 bit.

DCD13	0	1
Pin function	D_7 input pin	D_7 output pin

D_8	The pin function is switched as shown below by the DCD2 DCD20 bit.

DCD20	0	1
Pin function	D_8 input pin	D_8 output pin

D_9	The pin function is switched as shown below by the DCD2 DCD21 bit.

DCD21	0	1
Pin function	D_9 input pin	D_9 output pin

D_{10}	The pin function is switched as shown below by the DCD2 DCD22 bit.

DCD22	0	1
Pin function	D_{10} input pin	D_{10} output pin

D_{11}	The pin function is switched as shown below by the DCD2 DCD23 bit.

DCD23	0	1
Pin function	D_{11} input pin	D_{11} output pin

D_{12}	The pin function is switched as shown below by the DCD3 DCD30 bit.

DCD30	0	1
Pin function	D_{12} input pin	D_{12} output pin

Table 12-6 D_0 to D_{13} Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
D_{13}	The pin function is switched as shown below by the DCD3 DCD31 bit.

DCD31	0	1
Pin function	D_{13} input pin	D_{13} output pin

12.3 R Ports

12.3.1 Overview

The R port consists of the nine 4-bit I/O ports R0 to R6, R8, and R9, the 3-bit I/O port R7, and the 1-bit input port RA_1.

R0 and R3 to R9 are standard voltage CMOS three state I/O ports and R1 and R2 are medium voltage NMOS open drain I/O ports.

The individual ports R0 to R9 are accessed in 4-bit units with the LRA and LRB output instructions to control the output levels (high or low) on each pin. Output data is stored in the PDR built into each pin. Similarly, the LAR and LBR input instructions can be used to access the R ports in 4-bit units to read the input levels on the port pins.

The RA_1 input-only port consists of a single bit. The values of bits 3, 2, and 0 are undefined when this port is accessed by the input instructions.

DCR registers are used to control on/off states of the R port output buffers. When the DCR bit corresponding to a pin in an R port is set to 1, the contents of the PDR corresponding to that pin is output from the pin. Thus the output buffer on/off states can be controlled on an individual pin basis for the R port pins. The DCR registers are allocated in the RAM address space.

The R0 and R3 to R5 port pins have shared functions as built-in peripheral module pins. Register settings are used to switch these functions. (See table 12-7.)

Figure 12-2 shows the R port pin structure.

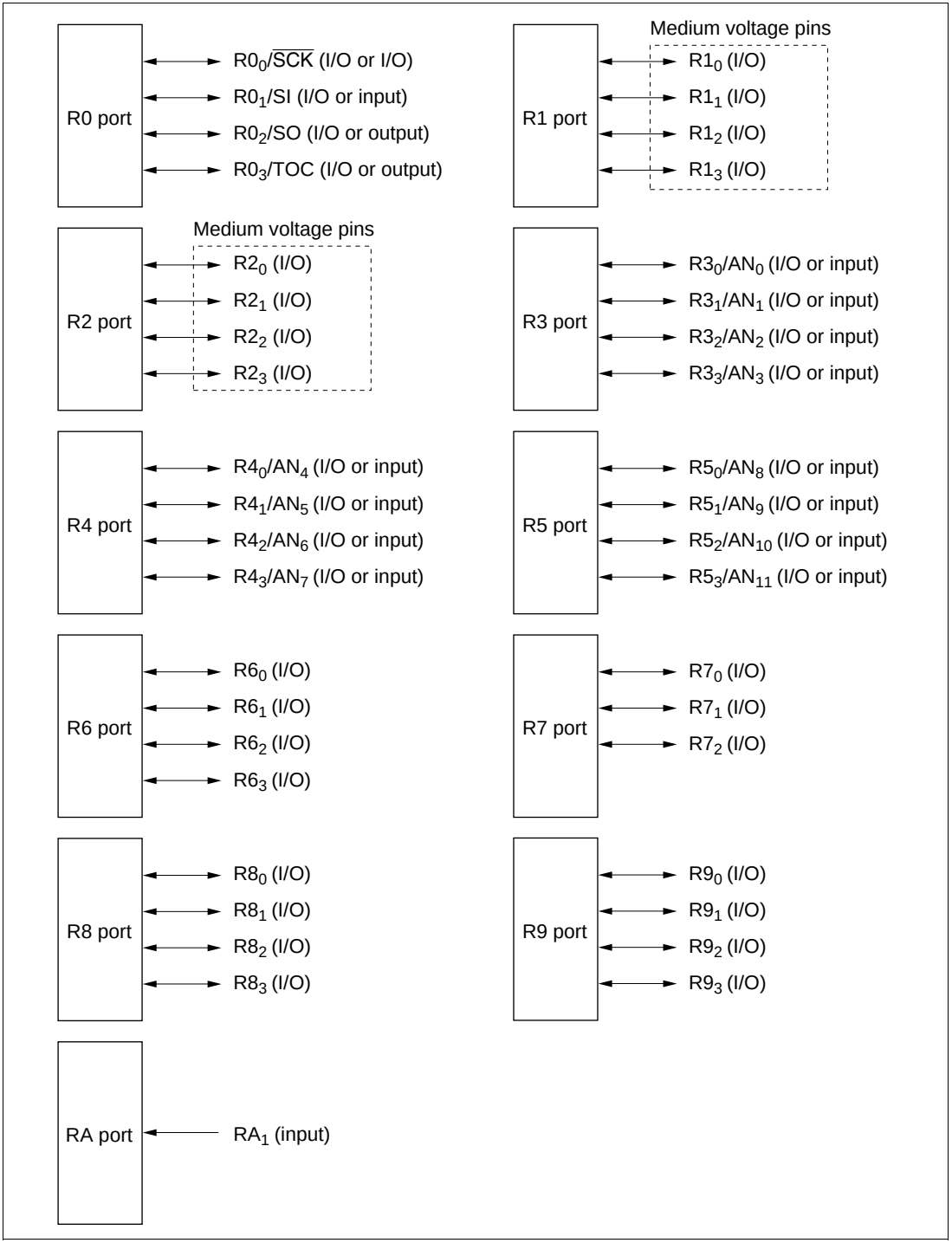


Figure 12-2 R Port Structure

12.3.2 Register Configuration and Descriptions

Table 12-7 shows the configuration of the R port related registers.

Table 12-7 R Port Register Configuration

Address	Register	Symbol	R/W	Initial Value
—	Port data registers	PDR	W*	1
$030	Data control registers	DCR0	W	$0
$031		DCR1	W	$0
$032		DCR2	W	$0
$033		DCR3	W	$0
$034		DCR4	W	$0
$035		DCR5	W	$0
$036		DCR6	W	$0
$037		DCR7	W	-000
$038		DCR8	W	$0
$039		DCR9	W	$0
$004	Port mode register A	PMRA	W	$0
$005	Serial mode register	SMR	W	$0
$019	A/D mode register 1	AMR1	W	$0
$01A	A/D mode register 2	AMR2	W	-000

Note: * The LRA and LRB instructions are used to write to the PDR registers.

(1) Port Data Registers (PDR): All the I/O pins in ports R0 to R9 include a PDR that holds the output data. When an LRA or an LRB instruction is executed for one of ports R0 to R9, the contents of the accumulator (A) or the B register (B) are transferred to the specified R port PDRs. When bits in DCR0 to DCR9 are set to 1, the output buffers for the corresponding pins in ports R0 to R9 will be turned on and the values in the PDRs will be output from those pins.

The PDR registers are set to 1 on reset and in stop mode.

(2) Data Control Registers (DCR0 to DCR9: $030 to $039)

DCR0: $030

Bit	3	2	1	0
	DCR03	DCR02	DCR01	DCR00
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR1: $031

Bit	3	2	1	0
	DCR13	DCR12	DCR11	DCR10
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR2: $032

Bit	3	2	1	0
	DCR23	DCR22	DCR21	DCR20
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR3: $033

Bit	3	2	1	0
	DCR33	DCR32	DCR31	DCR30
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR4: $034

Bit	3	2	1	0
	DCR43	DCR42	DCR41	DCR40
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR5: $035

Bit	3	2	1	0
	DCR53	DCR52	DCR51	DCR50
Initial value	0	0	0	0
Read/Write	W	W	W	W

DCR6: $036

Bit	3	2	1	0
	DCR63	DCR62	DCR61	DCR60
Initial value	0	0	0	0
Read/Write	W	W	W	W

	Bit	3	2	1	0
DCR7: $037		—	DCR72	DCR71	DCR70
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

	Bit	3	2	1	0
DCR8: $038		DCR83	DCR82	DCR81	DCR80
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

	Bit	3	2	1	0
DCR9: $039		DCR93	DCR92	DCR91	DCR90
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

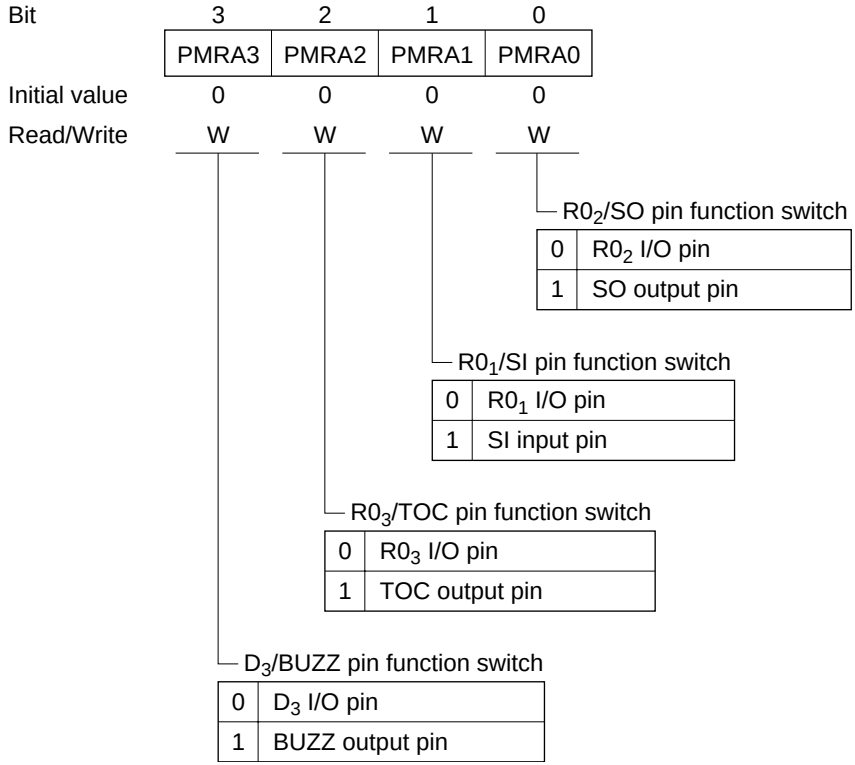
Bits in DCR0 to DCR9	Description
0	The output buffer (CMOS buffer) is turned off and the output goes to the high impedance state. (initial value)
1	• The CMOS three state output buffer is turned on and the corresponding PDR value is output. • For medium voltage NMOS open drain pins (R1 and R2), when the PDR is 0 a low level is output. When the PDR is 1, the pin goes to the high impedance state.

The table below lists the correspondence between the bits in DCR0 to DCR9 and the port R0 to R9 pins.

	Bit			
Register	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$
DCR5	$R5_3$	$R5_2$	$R5_1$	$R5_0$
DCR6	$R6_3$	$R6_2$	$R6_1$	$R6_0$
DCR7	—	$R7_2$	$R7_1$	$R7_0$
DCR8	$R8_3$	$R8_2$	$R8_1$	$R8_0$
DCR9	$R9_3$	$R9_2$	$R9_1$	$R9_0$

(3) Port Mode Register A (PMRA: $004): PMRA is a 4-bit write-only register whose bits PMRA2 to PMRA0 switch the functions of the port R0 shared function pins.

This section describes the bits PMRA2 to PMRA0. See section 12.2.2 (3), “Port Mode Register A (PMRA)”, for details on the PMRA3 bit.



Bit 2—R0$_3$/TOC Pin Function Switch (PMRA2): Selects whether the R0$_3$/TOC pin functions as the R0$_3$ I/O pin or as the timer C output pin (TOC).

PMRA2	Description	
0	The R0$_3$/TOC pin functions as the R0$_3$ I/O pin.	(initial value)
1	The R0$_3$/TOC pin functions as the TOC output pin.	

Bit 1—$R0_1$/SI Pin Function Switch (PMRA1): Selects whether the $R0_1$/SI pin functions as the $R0_1$ I/O pin or as the serial reception data input pin (SI).

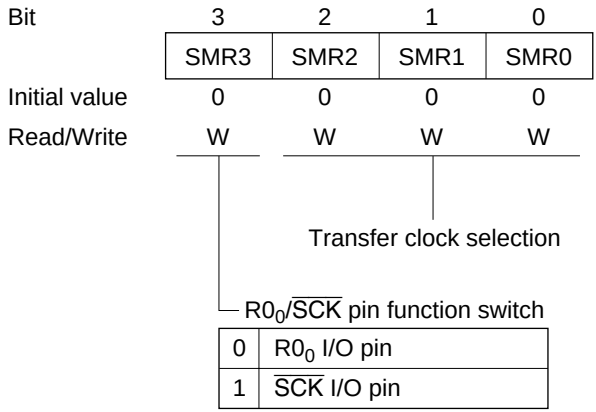
PMRA1	Description	
0	The $R0_1$/SI pin functions as the $R0_1$ I/O pin.	(initial value)
1	The $R0_1$/SI pin functions as the SI input pin.	

Bit 0—$R0_2$/SO Pin Function Switch (PMRA0): Selects whether the $R0_2$/SO pin functions as the $R0_2$ I/O pin or as the serial transmission data output pin (SO).

PMRA0	Description	
0	The $R0_2$/SO pin functions as the $R0_2$ I/O pin.	(initial value)
1	The $R0_2$/SO pin functions as the SO output pin.	

(4) Serial Mode Register (SMR: $005): SMR is a 4-bit write-only register whose SMR3 bit switches the $R0_0$/$\overline{SCK}$ pin function.

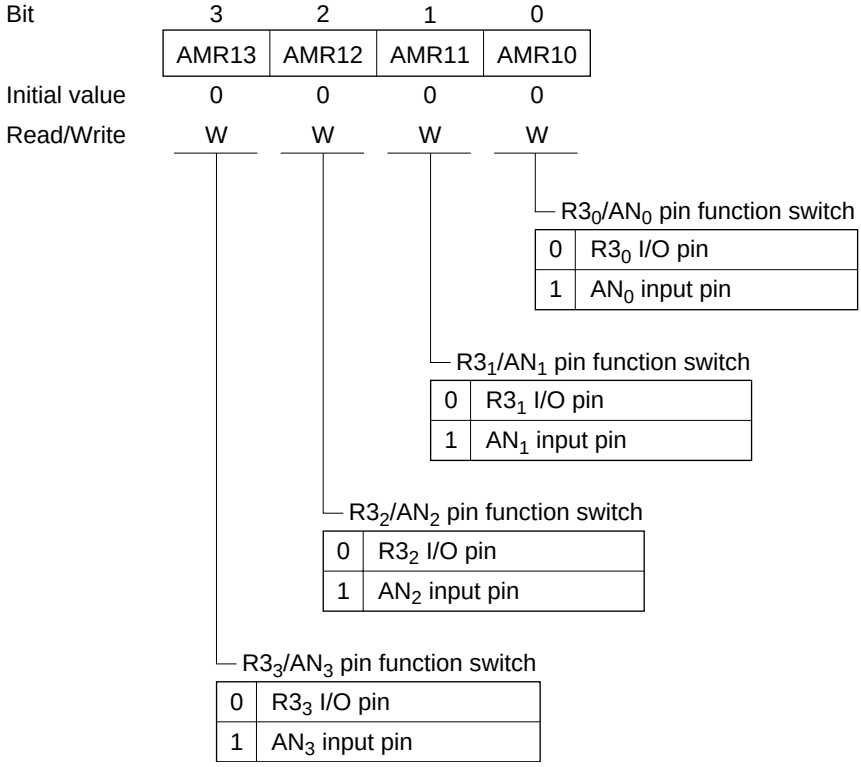
This section only describes the SMR3 bit. See section 20.2.1, “Serial Mode Register (SMR)” for details on bits SMR2 to SMR0.



Bit 3—$R0_0$/$\overline{SCK}$ Pin Function Switch (SMR3): Selects whether the $R0_0$/$\overline{SCK}$ pin functions as the $R0_0$ I/O pin or as the serial interface transfer clock I/O pin ($\overline{SCK}$).

SMR3	Description	
0	The $R0_0$/$\overline{SCK}$ pin functions as the $R0_0$ I/O pin.	(initial value)
1	The $R0_0$/$\overline{SCK}$ pin functions as the $\overline{SCK}$ I/O pin.	

(5) A/D Mode Register 1 (AMR1: $019): AMR1 is a 4-bit write-only register that switches the functions of the R3 port shared function pins.



Bit 3—R3$_3$/AN$_3$ Pin Function Switch (AMR13): Selects whether the R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin or as the A/D converter channel 3 input pin AN$_3$.

AMR13	Description	
0	The R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin.	(initial value)
1	The R3$_3$/AN$_3$ pin functions as the AN$_3$ input pin.	

Bit 2—R3$_2$/AN$_2$ Pin Function Switch (AMR12): Selects whether the R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin or as the A/D converter channel 2 input pin AN$_2$.

AMR12	Description	
0	The R3$_2$/AN$_2$ pin functions as the R3$_2$ I/O pin.	(initial value)
1	The R3$_2$/AN$_2$ pin functions as the AN$_2$ input pin.	

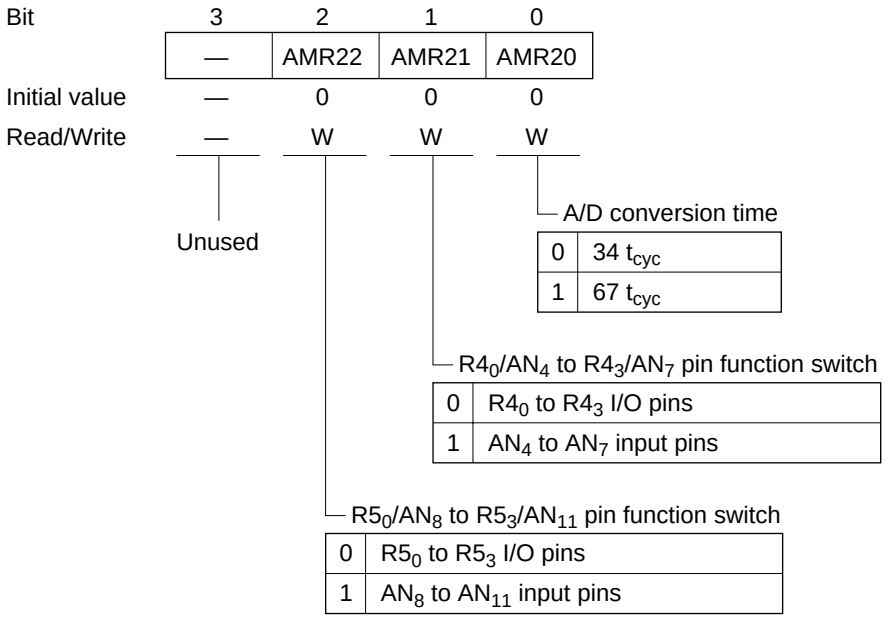
Bit 1—$R3_1/AN_1$ Pin Function Switch (AMR11): Selects whether the $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin or as the A/D converter channel 1 input pin AN_1.

AMR11	Description	
0	The $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin.	(initial value)
1	The $R3_1/AN_1$ pin functions as the AN_1 input pin.	

Bit 0—$R3_0/AN_0$ Pin Function Switch (AMR10): Selects whether the $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin or as the A/D converter channel 0 input pin AN_0.

AMR10	Description	
0	The $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin.	(initial value)
1	The $R3_0/AN_0$ pin functions as the AN_0 input pin.	

(6) A/D Mode Register 2 (AMR2: $01A): AMR2 is a 3-bit write-only register whose AMR21 bit switches the functions of all four bits of the R4 port to be A/D converter input channels (AN_4 to AN_7), and whose AMR22 bit switches the functions of all four bits of the R5 port to be A/D converter input channels (AN_8 to AN_{11}). This section describes the AMR22 and AMR21 bits. See section 15.2.2, “A/D Mode Register 2 (AMR2)”, for details on the AMR20 bit.



Bit 2—$R5_0/AN_8$ to $R5_3/AN_{11}$ Pin Function Switch (AMR22): Selects whether the $R5_0/AN_8$ to $R5_3/AN_{11}$ pins function as the $R5_0$ to $R5_3$ I/O pins or as the A/D converter channel 8 to 11 input pins (AN_8 to AN_{11}).

AMR22	Description	
0	The $R5_0/AN_8$ to $R5_3/AN_{11}$ pins function as the $R5_0$ to $R5_3$ I/O pins.	(initial value)
1	The $R5_0/AN_8$ to $R5_3/AN_{11}$ pins function as the AN_8 to AN_{11} input pins.	

Bit 1—$R4_0/AN_4$ to $R4_3/AN_7$ Pin Function Switch (AMR21): Selects whether the $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins or as the A/D converter channel 4 to 7 input pins (AN_4 to AN_7).

AMR21	Description	
0	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins.	(initial value)
1	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the AN_4 to AN_7 input pins.	

12.3.3 Pin Functions

The pin functions of the R port pins are switched by register settings as shown in table 12-8.

Table 12-8 R Port Pin Functions

Pin	Pin Functions and Selection Methods
$R0_0/\overline{SCK}$	The pin function is switched by the SMR SMR3 bit and the DCR0 DCR00 bit as shown below.

SMR3	0		1
DCR00	0	1	—
Pin function	$R0_0$ input pin	$R0_0$ output pin	$\overline{SCK}$ I/O pin

$R0_1$/SI	The pin function is switched by the PMRA PMRA1 bit and the DCR0 DCR01 bit as shown below.

PMRA1	0		1
DCR01	0	1	—
Pin function	R01 input pin	R01 output pin	SI input pin

$R0_2$/SO	The pin function is switched by the PMRA PMRA0 bit and the DCR0 DCR02 bit as shown below.

PMRA0	0		1
DCR02	0	1	—
Pin function	$R0_2$ input pin	$R0_2$ output pin	SO output pin

$R0_3$/TOC	The pin function is switched by the PMRA PMRA2 bit and the DCR0 DCR03 bit as shown below.

PMRA2	0		1
DCR03	0	1	—
Pin function	$R0_3$ input pin	$R0_3$ output pin	TOC output pin

Table 12-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods		
$R1_0$	The pin function is switched by the DCR1 DCR10 bit as shown below.		
	DCR10	0	1
	Pin function	$R1_0$ input pin	$R1_0$ output pin*
$R1_1$	The pin function is switched by the DCR1 DCR11 bit as shown below.		
	DCR11	0	1
	Pin function	$R1_1$ input pin	$R1_1$ output pin*
$R1_2$	The pin function is switched by the DCR1 DCR12 bit as shown below.		
	DCR12	0	1
	Pin function	$R1_2$ input pin	$R1_2$ output pin*
$R1_3$	The pin function is switched by the DCR1 DCR13 bit as shown below.		
	DCR13	0	1
	Pin function	$R1_3$ input pin	$R1_3$ output pin*
$R2_0$	The pin function is switched by the DCR2 DCR20 bit as shown below.		
	DCR20	0	1
	Pin function	$R2_0$ input pin	$R2_0$ output pin*
$R2_1$	The pin function is switched by the DCR2 DCR21 bit as shown below.		
	DCR21	0	1
	Pin function	$R2_1$ input pin	$R2_1$ output pin*
$R2_2$	The pin function is switched by the DCR2 DCR22 bit as shown below.		
	DCR22	0	1
	Pin function	$R2_2$ input pin	$R2_2$ output pin*

Note: * $R1_0$ to $R1_3$ and $R2_0$ to $R2_3$ are medium voltage NMOS open drain I/O pins. These pins go to the high impedance state when their PDR is set to 1.

Table 12-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R2_3$	The pin function is switched by the DCR2 DCR23 bit as shown below.

DCR23	0	1
Pin function	$R2_3$ input pin	$R2_3$ output pin*

$R3_0/AN_0$	The pin function is switched by the AMR1 AMR10 bit and the DCR3 DCR30 bit as shown below.		
AMR10	0		1
DCR30	0	1	—
Pin function	$R3_0$ input pin	$R3_0$ output pin	AN_0 input pin

$R3_1/AN_1$	The pin function is switched by the AMR1 AMR11 bit and the DCR3 DCR31 bit as shown below.		
AMR11	0		1
DCR31	0	1	—
Pin function	$R3_1$ input pin	$R3_1$ output pin	AN_1 input pin

$R3_2/AN_2$	The pin function is switched by the AMR1 AMR12 bit and the DCR3 DCR32 bit as shown below.		
AMR12	0		1
DCR32	0	1	—
Pin function	$R3_2$ input pin	$R3_2$ output pin	AN_2 input pin

$R3_3/AN_3$	The pin function is switched by the AMR1 AMR13 bit and the DCR3 DCR33 bit as shown below.		
AMR13	0		1
DCR33	0	1	—
Pin function	$R3_3$ input pin	$R3_3$ output pin	AN_3 input pin

Note: * $R1_0$ to $R1_3$ and $R2_0$ to $R2_3$ are medium voltage NMOS open drain I/O pins. These pins go to the high impedance state when their PDR is set to 1.

Table 12-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R4_0/AN_4$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR40 bit as shown below.

AMR21	0		1
DCR40	0	1	—
Pin function	$R4_0$ input pin	$R4_0$ output pin	AN_4 input pin

$R4_1/AN_5$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR41 bit as shown below.

AMR21	0		1
DCR41	0	1	—
Pin function	$R4_1$ input pin	$R4_1$ output pin	AN_5 input pin

$R4_2/AN_6$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR42 bit as shown below.

AMR21	0		1
DCR42	0	1	—
Pin function	$R4_2$ input pin	$R4_2$ output pin	AN_6 input pin

$R4_3/AN_7$	The pin function is switched by the AMR2 AMR21 bit and the DCR4 DCR43 bit as shown below.

AMR21	0		1
DCR43	0	1	—
Pin function	$R4_3$ input pin	$R4_3$ output pin	AN_7 input pin

Table 12-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods
$R5_0/AN_8$	The pin function is switched by the AMR2 AMR22 bit and the DCR5 DCR50 bit as shown below.

AMR22	0		1
DCR50	0	1	—
Pin function	$R5_0$ input pin	$R5_0$ output pin	AN_8 input pin

$R5_1/AN_9$	The pin function is switched by the AMR2 AMR22 bit and the DCR5 DCR51 bit as shown below.

AMR22	0		1
DCR51	0	1	—
Pin function	$R5_1$ input pin	$R5_1$ output pin	AN_9 input pin

$R5_2/AN_0$	The pin function is switched by the AMR2 AMR22 bit and the DCR5 DCR52 bit as shown below.

AMR22	0		1
DCR52	0	1	—
Pin function	$R5_2$ input pin	$R5_2$ output pin	AN_{10} input pin

$R5_3/AN_{11}$	The pin function is switched by the AMR2 AMR22 bit and the DCR5 DCR53 bit as shown below.

AMR22	0		1
DCR53	0	1	—
Pin function	$R5_3$ input pin	$R5_3$ output pin	AN_{11} input pin

Table 12-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods		
$R6_0$	The pin function is switched by the DCR6 DCR60 bit as shown below.		
	DCR60	0	1
	Pin function	$R6_0$ input pin	$R6_0$ output pin
$R6_1$	The pin function is switched by the DCR6 DCR61 bit as shown below.		
	DCR61	0	1
	Pin function	$R6_1$ input pin	$R6_1$ output pin
$R6_2$	The pin function is switched by the DCR6 DCR62 bit as shown below.		
	DCR62	0	1
	Pin function	$R6_2$ input pin	$R6_2$ output pin
$R6_3$	The pin function is switched by the DCR6 DCR63 bit as shown below.		
	DCR63	0	1
	Pin function	$R6_3$ input pin	$R6_3$ output pin
$R7_0$	The pin function is switched by the DCR7 DCR70 bit as shown below.		
	DCR70	0	1
	Pin function	$R7_0$ input pin	$R7_0$ output pin
$R7_1$	The pin function is switched by the DCR7 DCR71 bit as shown below.		
	DCR71	0	1
	Pin function	$R7_1$ input pin	$R7_1$ output pin
$R7_2$	The pin function is switched by the DCR7 DCR72 bit as shown below.		
	DCR72	0	1
	Pin function	$R7_2$ input pin	$R7_2$ output pin

Table 12-8 R Port Pin Functions (cont)

Pin	Pin Functions and Selection Methods		
$R8_0$	The pin function is switched by the DCR8 DCR80 bit as shown below.		
	DCR80	0	1
	Pin function	$R8_0$ input pin	$R8_0$ output pin
$R8_1$	The pin function is switched by the DCR8 DCR81 bit as shown below.		
	DCR81	0	1
	Pin function	$R8_1$ input pin	$R8_1$ output pin
$R8_2$	The pin function is switched by the DCR8 DCR82 bit as shown below.		
	DCR82	0	1
	Pin function	$R8_2$ input pin	$R8_2$ output pin
$R8_3$	The pin function is switched by the DCR8 DCR83 bit as shown below.		
	DCR83	0	1
	Pin function	$R8_3$ input pin	$R8_3$ output pin
$R9_0$	The pin function is switched by the DCR9 DCR90 bit as shown below.		
	DCR90	0	1
	Pin function	$R9_0$ input pin	$R9_0$ output pin
$R9_1$	The pin function is switched by the DCR9 DCR91 bit as shown below.		
	DCR91	0	1
	Pin function	$R9_1$ input pin	$R9_1$ output pin
$R9_2$	The pin function is switched by the DCR9 DCR92 bit as shown below.		
	DCR92	0	1
	Pin function	$R9_2$ input pin	$R9_2$ output pin
$R9_3$	The pin function is switched by the DCR9 DCR93 bit as shown below.		
	DCR93	0	1
	Pin function	$R9_3$ input pin	$R9_3$ output pin

12.4 Usage Notes

Keep the following points in mind when using the I/O ports.

- When the MIS MIS2 bit is set to 1, the $R0_2$/SO pin will be an NMOS open drain output regardless of whether it is selected for use as the $R0_2$ pin or as the SO pin by the PMRA PMRA0 bit.

- I/O pins that are unused in user systems must be tied to a fixed potential, since floating I/O pins can cause noise that can interfere with LSI operation.

  The built-in pull-up MOS transistors can be used to pull up unused pins to V_{CC}. Alternatively, unused pins can be pulled up to V_{CC} with external resistors of about 100 kΩ.

  Application programs should maintain the PDR, DCD and DCR contents for unused pins at their reset state values. Also note that unused pins must not be selected for use as peripheral function I/O pins.

- When the MIS MIS3 bit is set to 1 (pull-up MOS transistors active) and the PDR for an R port/analog input shared function pin has the value 1, the MOS transistor for the corresponding pin will not be turned off by selecting the analog input function with the AMR1 or AMR2 register.

  To use an R port/analog input shared function pin as an analog input when the pull-up MOS transistors are active, always clear the PDR for the corresponding pin to 0 first and then turn off the pull-up MOS transistor. (Note that the PDR registers are set to 1 immediately following a reset.)

  Figure 12-3 shows the circuit for the R port/analog input shared function pins. AMR1 and AMR2 are used to set the port outputs to high impedance. ACR is used to switch the analog input channel.

  The states of the R port/analog input shared function pins are set, as shown in table 12-9, by the combination of the AMR1 or AMR2 register, the MIS3 bit, the DCR, and the PDR settings.

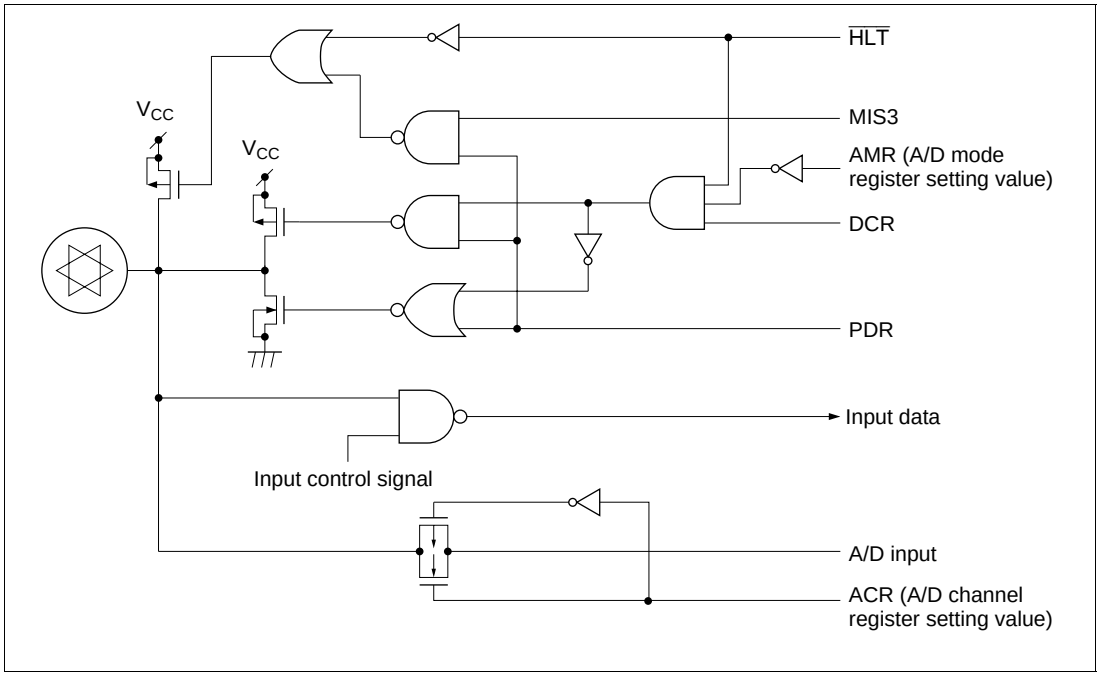


Figure 12-3 R Port/Analog Input Shared Function Pin Circuit

Table 12-9 Program Control of the R Port/Analog Input Shared Function Pins

Corresponding bit in AMR1 or AMR2		0 (R port selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

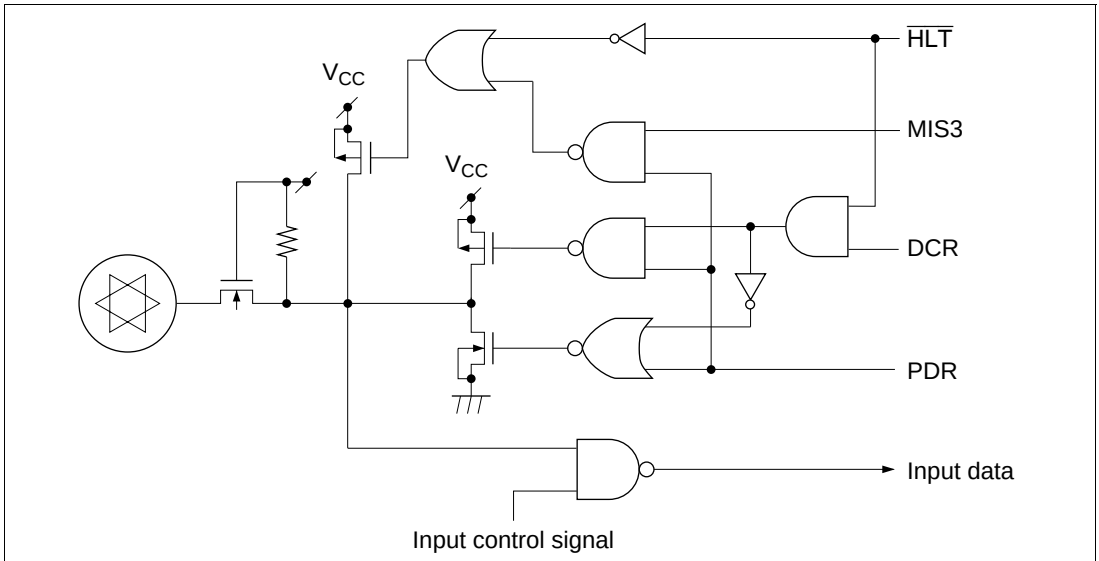
Note: —: off

Corresponding bit in AMR1 or AMR2		1 (analog input selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	—	—		—	—
	NMOS			—	—			—	—
Pull-up MOS transistor		—				—	On	—	On

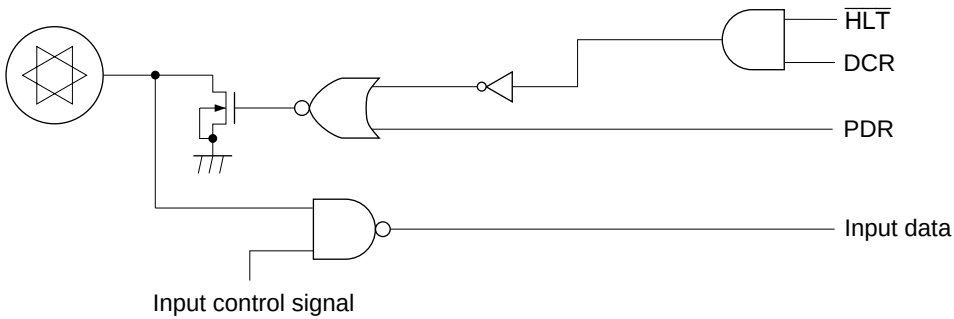
Note: —: off

- In the HD404369 Series evaluation chip set, the circuits for the medium voltage NMOS open drain pins (the R1 and R2 port pins) differ from the ZTAT™ and the mask ROM microcomputer versions as shown in figure 12-4. Although the outputs in both the ZTAT™ and mask ROM versions can be set to high impedance by the combinations listed in table 12-10, these outputs cannot be set to high impedance in the evaluation chip set. Please keep this in mind when using the evaluation chip set.

  Figure 12-4 shows the circuit for the medium voltage NMOS open drain pins.



(a) Evaluation Chip Pin Circuit Structure



(b) ZTAT™ and Mask ROM Pin Circuit Structure

Figure 12-4 Medium Voltage NMOS Open Drain Pin Circuits

Table 12-10 ZTAT™ and Mask ROM Microcomputer NMOS Open Drain Pin High Impedance Control

DCR	PDR	Description	
0	*	High impedance output	(initial value)
1	0	NMOS buffer on. Low level output	
	1	High impedance output	

Note: * Don't care

Section 13 Oscillator Circuits (HD404344R/HD404394/HD404318/HD404358/ HD404358R Series)

13.1 Overview

13.1.1 Features

The HD404344R, HD404394, HD404318, HD404358, and HD404358R Series microcomputers include a system clock oscillator circuit with the following features.

- The system clock oscillator circuit supports the use of a ceramic oscillator, a crystal oscillator, a resistor, or an external clock input. The system clock is generated by dividing the oscillator frequency by four internally (i.e., $f_{cyc} = f_{OSC}/4$). Note that $ø_{CPU} = ø_{PER} = f_{cyc}$.

  The following oscillator elements and external clock frequencies can be used.

  HD404344R Series

  Use an oscillator or an external clock with a frequency in the range 0.4 to 5.4 MHz*[1]. Alternately, for CR oscillation*[2] connect a resistor.

  HD404394 and HD404318 Series

  Use an oscillator or an external clock with a frequency in the range 0.4 to 4.5 MHz.

  HD404358 Series

  Use an oscillator or an external clock with a frequency in either the range 0.4 to 5.0 MHz*[3], or the range 0.4 to 8.5 MHz*[4].

  HD404358R series

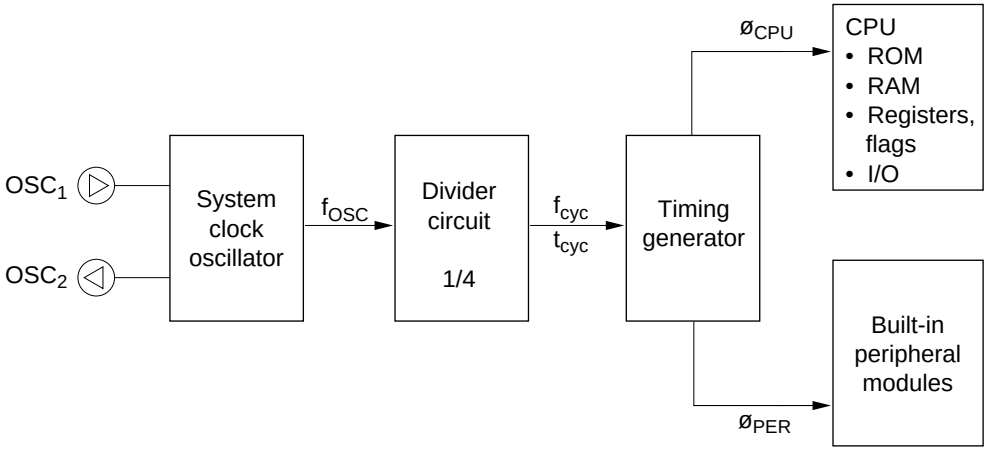
  Use an oscillator or an external clock with a frequency in the range 0.4 to 5.0 MHz*[5] or 0.4 to 8.5 MHz*[6]. Alternately, for CR oscillation*[7] connect a resistor.

Notes: 1. HD404341R, HD404342R, HD404344R, HD4074344
2. HD40C4341R, HD40C4342R, HD40C4344R
3. HD404354, HD404356, HD404358
4. HD40A4354, HD40A4356, HD40A4358, HD407A4359
5. HD404354R, HD404356R, HD404358R
6. HD40A4354R, HD40A4356R, HD40A4358R, HD407A4359R
7. HD40C4354R, HD40C4356R, HD40C4358R, HD407C4359R

- The built-in peripheral module operating clock ($ø_{PER}$) is input to an 11-bit prescaler (PSS) and divided to generate the clocks that are used as the counter operating clocks for the built-in peripheral modules. The divisors can be set individually using the mode registers for each built-in peripheral module.

13.1.2 Block Diagram

Figure 13-1 shows the block diagram of the oscillator circuit used in the HD404344R, HD404394, HD404318, HD404358, and HD404358R Series microcomputers.



Symbol	Description
f_{OSC}	The frequency of the ceramic or crystal oscillator or CR oscillator connected between the OSC_1 and OSC_2 oscillator pins
f_{cyc}	$f_{OSC}/4$
t_{cyc}	The clock period for the f_{cyc} frequency (This period is equal to one instruction cycle in active mode and also to one count period of prescaler S (PSS).)
$ø_{CPU}$	The system clock (the operating clock in active mode)
$ø_{PER}$	The system clock (the built-in peripheral module and interrupt clock)

Figure 13-1 Oscillator Circuit Block Diagram (HD404344R/HD404394/HD404318/HD404358/HD404358R Series)

13.1.3 Oscillator Circuit Pins

Table 13-1 lists the pins used by the oscillator circuit.

Table 13-1 Oscillator Circuit Pins

Pin	Symbol	I/O	Function
System clock oscillator pin 1	OSC_1	Input	Connections for the system clock oscillator element* (An external clock can be input to OSC_1.)
System clock oscillator pin 2	OSC_2	Output	

Note: * HD404344R Series

Connect a ceramic oscillator with a frequency in the range 0.4 to 4.5 MHz or a resistor.

HD404394 and HD404318 Series

Use a ceramic or crystal oscillator element with a frequency in the range 0.4 to 4.5 MHz.

HD404358 Series

Use a ceramic or crystal oscillator element with a frequency in either the range 0.4 to 5.0 MHz, or the range 0.4 to 8.5 MHz.

HD404358R Series

Connect a ceramic or crystal oscillator with a frequency in the range 0.4 to 5.0 MHz or 0.4 to 8.5 MHz, or a resistor.

13.2 Oscillator Connection and External Clock Input

The system clock oscillator circuit supports the use of a ceramic oscillator, a crystal oscillator, a resistor, or an external clock input. Table 13-2 shows sample oscillator circuits.

Table 13-2 Oscillator Circuit Examples

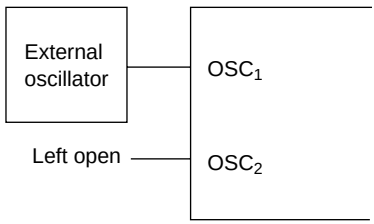
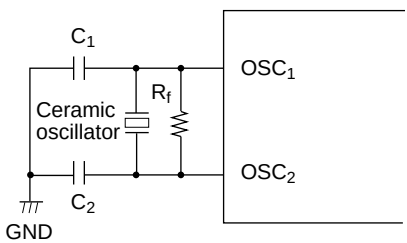
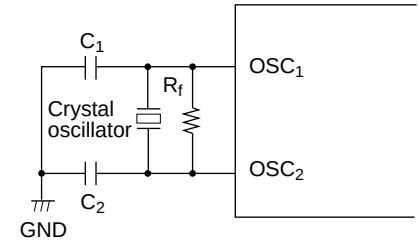
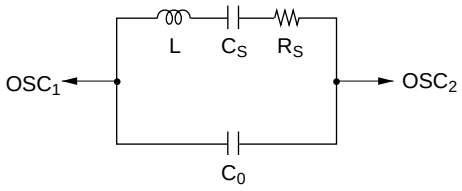
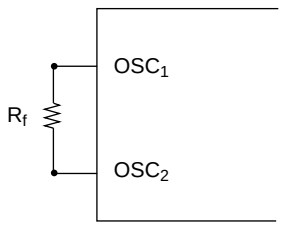
Circuit	Circuit Constants
External clock 	—
Ceramic oscillator (OSC_1, OSC_2) 	Ceramic oscillator: CSA 4.00MG (Murata Manufacturing) R_f = 1 MΩ ±20% $C_1 = C_2$ = 30 pF ±20%

Table 13-2 Oscillator Circuit Examples (cont)

Circuit	Circuit Constants
Crystal oscillator*[1] (OSC_1, OSC_2)  Cut parallel resonator type crystal oscillator 	R_f = 1 MΩ ±20% $C_1 = C_2$ = 10 to 22 pF ±20% Crystal oscillator: Equivalent circuit shown at left C_0 = 7 pF max R_S = 100 Ω max f = 1.0 to 4.5 MHz
CR oscillator*[2] (OSC_1, OSC_2) 	R_f = 20 kΩ ± 1%

Notes: 1. Applies to the HD404318, HD404358, and HD404358R Series.
2. Applies to the HD404344R and HD404358R Series.

13.3 Usage Notes

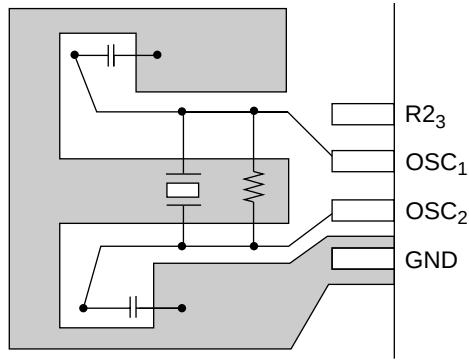
Keep the following points in mind when designing and implementing the oscillator circuit.

- When using a crystal or ceramic oscillator the circuit constants will differ depending on the device actually used, the stray capacitances in the mounted circuit and other factors. Therefore, these circuit parameters should be determined in consultation with the manufacturer of the crystal or ceramic oscillator element used.

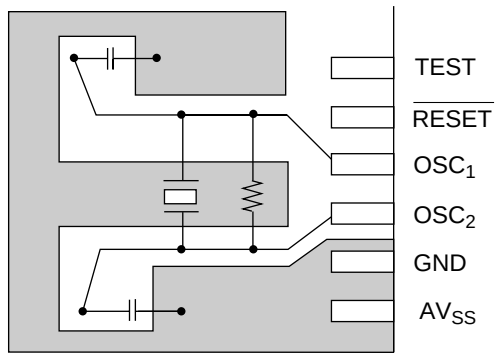
- The distance between the OSC_1 and OSC_2 pins and the devices connected to those pins should be kept as short as possible. Do not allow any other lines to cross those lines. (See figure 13-2.) Correct oscillation may become impossible due to induced signals if any lines cross.

- In like manner, the distance between the OSC_1 and OSC_2 terminals, on the one hand, and the oscillator resistor, on the other, should be as short as possible. Do not allow any other lines to cross them.

HD404344R/HD404394 Series



HD404318/HD404358/HD404358R Series



GND

Figure 13-2 Wiring Examples for Crystal and Ceramic Oscillators

Section 14 Oscillator Circuits (HD404339 and HD404369 Series)

14.1 Overview

14.1.1 Features

The microcomputers in the HD404339 and HD404369 Series include a system clock oscillator circuit and a subsystem clock oscillator circuit with the following features.

- The system clock oscillator circuit supports the use of a ceramic or crystal oscillator or an external clock input. The system clock is generated by dividing the oscillator frequency by either 4, 8, 16, or 32 internally (i.e., $f_{cyc} = f_{OSC}/4$, $f_{OSC}/8$, $f_{OSC}/16$, or $f_{OSC}/32$: the divisor is software selectable). Note that $ø_{CPU} = ø_{PER} = f_{cyc}$.

  The following oscillator elements and external clock frequencies can be used.

  HD404339 Series

  Use an oscillator element or an external clock with a frequency in the range 0.4 to 4.5 MHz.

  HD404369 Series

  Use an oscillator element or an external clock with a frequency in either the range 0.4 to 5.0 MHz*[1], or the range 0.4 to 8.5 MHz*[2].

  Notes: 1. HD404364, HD404368, HD4043612, HD404369
  2. HD40A4364, HD40A4368, HD40A43612, HD40A4369, HD407A4369

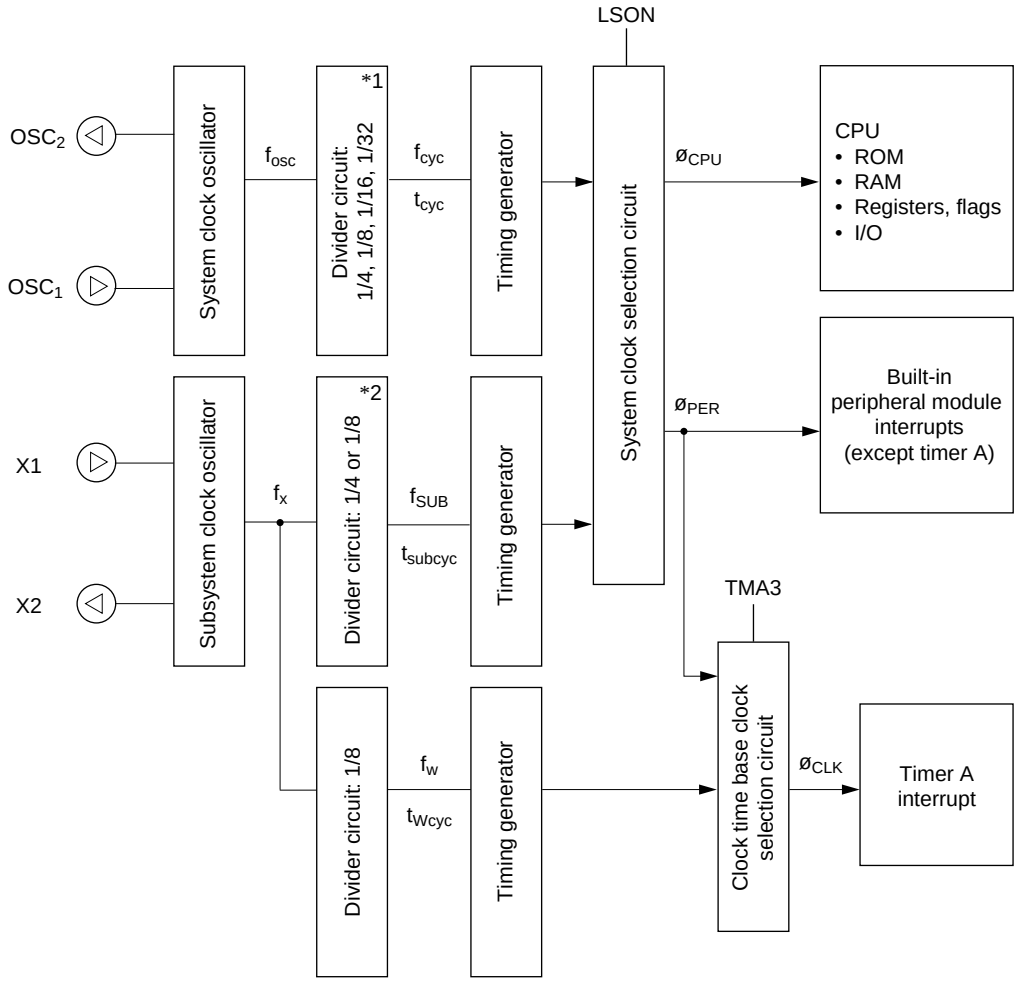
- The built-in peripheral module operating clock ($ø_{PER}$) is input to an 11-bit prescaler (PSS) and divided to generate the clocks that are used as the counter operating clocks for the built-in peripheral modules. The divisors can be set individually using the mode registers for each built-in peripheral module.

- A 32.768 kHz crystal oscillator is used as the subsystem clock oscillator. A clock generated by dividing this frequency by four or eight ($f_{SUB} = f_X/4$ or $f_X/8$) with an internal divider circuit is used as the system clock in subactive mode. The divisor can be selected by setting a register.

- In all operating modes, a clock generated by dividing the subsystem clock frequency by eight is input to prescaler W (PSW). A clock generated by PSW division is used in timer A clock time base operation.

14.1.2 Block Diagram

Figure 14-1 shows the block diagram of the oscillator circuits used in the HD404339 and HD404369 Series microcomputers.



Notes: Symbols are described on the following page.

1. The divisor is selected by the system clock selection register 2 (SSR2: $028) SSR21 and SSR20 bits.
2. The divisor is selected by the system clock selection register 1 (SSR1: $027) SSR12 bit.

Figure 14-1 Oscillator Circuit Block Diagram (HD404339/HD404369 Series)

Symbol	Description
f_{OSC}	The frequency of the ceramic or crystal oscillator connected between the OSC_1 and OSC_2 oscillator pins
f_X	The frequency of the crystal oscillator connected between the X1 and X2 oscillator pins (32.768 kHz)
f_{cyc}	$f_{OSC}/4$, $f_{OSC}/8$, $f_{OSC}/16$, or $f_{OSC}/32$
t_{cyc}	The clock period for the f_{cyc} frequency (This period is equal to one instruction cycle in active mode and also to one count period for prescaler S (PSS).)
f_W	$f_X/8$
t_{Wcyc}	The clock period for the f_W frequency (one count period for prescaler W (PSW))
f_{SUB}	$f_X/4$ or $f_X/8$
t_{subcyc}	The clock period for the f_W frequency (one instruction cycle in subactive mode)
$ø_{CPU}$	The system clock (the CPU operating clock)
$ø_{CLK}$	The clock used for timer A and interrupt frame generation (Supplied from PSS when the TMA3 bit is 0, and from PSW when the TMA3 bit is 1.)
$ø_{PER}$	The system clock (the built-in peripheral module and interrupt clock)

14.1.3 Oscillator Circuit Pins

Table 14-1 lists the pins used by the oscillator circuit.

Table 14-1 Oscillator Circuit Pins

Pin	Symbol	I/O	Function
System clock oscillator pin 1	OSC_1	Input	Connections for the system clock oscillator element* (An external clock can be input to OSC_1.)
System clock oscillator pin 2	OSC_2	Output	
Subsystem clock oscillator pin 1	X1	Input	Connections for the 32.768 kHz crystal oscillator.
Subsystem clock oscillator pin 2	X2	Output	

Note: * HD404339 Series

Use a ceramic or crystal oscillator element with a frequency in the range 0.4 to 4.5 MHz.

HD404369 Series

Use a ceramic or crystal oscillator element with a frequency in either the range 0.4 to 5.0 MHz, or the range 0.4 to 8.5 MHz.

14.1.4 Register and Flag Configuration

Table 14-2 lists the registers and flag used in oscillator circuit control.

Table 14-2 Register and Flag Configuration

Address	Item	Symbol	R/W	Initial value
$027	System clock selection register 1	SSR1	W	$0
$028	System clock selection register 2	SSR2	W	$0
$020, 0	Low speed on flag	LSON	R/W	0

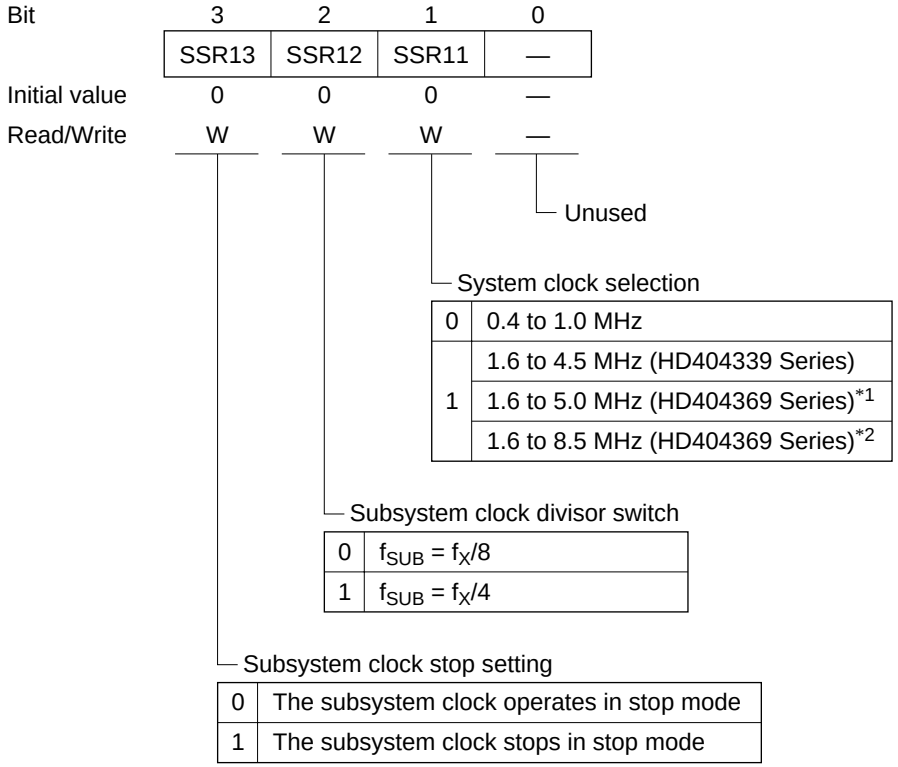
Note: * LSON is a control bit allocated in the register flag area. It can only be manipulated by the RAM bit manipulation instructions.

14.2 Register and Flag Descriptions

14.2.1 System Clock Selection Register 1 (SSR1: $027)

SSR1 is a 4-bit write-only register that is used to specify the system clock oscillator frequency (f_{OSC}) actually used, to select the subsystem clock frequency (f_{SUB}) divisor, and to set the subsystem clock oscillator operating state in stop mode.

The SSR1 SSR12 and SSR11 bits are initialized to zero on reset and in stop mode.



Notes: 1. HD404364, HD404368, HD4043612, HD404369
2. HD40A4364, HD40A4368, HD40A43612, HD40A4369, HD407A4369

Bit 3—Subsystem Clock Stop Setting (SSR13): Selects whether the subsystem clock (32.768 kHz) operates or stops in stop mode.

This bit is initialized to 0 only on reset.

SSR13	Description	
0	The subsystem clock operates in stop mode	(initial value)
1	The subsystem clock stops in stop mode	

Bit 2—Subsystem Clock Divisor Switch (SSR12): Specifies the divisor for the subsystem clock that is supplied to the CPU and the built-in peripheral modules in subactive mode. However, note that the divisor for the subsystem clock supplied to PSW is fixed at eight, i.e., $f_W = f_X/8$. Thus the clock used for timer A in clock time base mode is not affected by the setting of this bit.

This bit must be set in active mode. The microcomputer may operate incorrectly if this bit is changed in subactive mode. Also, note that this bit is initialized to 0 on reset and in stop mode.

SSR12	Description
0	f_{SUB} will be 1/8 of the subsystem clock oscillator frequency f_X ($f_{SUB} = f_X/8$) and the CPU single instruction cycle time will be 244.14 µs (when f_X = 32.768 kHz). (initial value)
1	f_{SUB} will be 1/4 of the subsystem clock oscillator frequency f_X ($f_{SUB} = f_X/4$) and the CPU single instruction cycle time will be 122.07 µs (when f_X = 32.768 kHz).

Bit 1—System Clock Selection (SSR11): The SSR11 bit must be set to match the frequency of the system clock.

This bit is initialized to 0 on reset and in stop mode.

SSR11	Description	
0	The system clock frequency is between 0.4 and 1.0 MHz	(initial value)
1	The system clock frequency is between 1.6 and 4.5 MHz (HD404339 Series)	
	The system clock frequency is between 1.6 and 5.0 MHz (HD404369 Series)*[1]	
	The system clock frequency is between 1.6 and 8.5 MHz (HD404369 Series)*[2]	

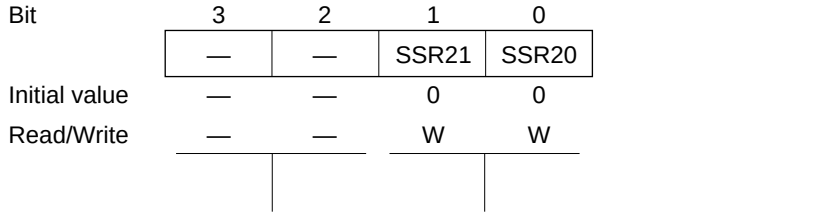
Notes: If these register settings do not match the frequency of the system oscillator, the subsystem using the 32 kHz oscillator will not operate correctly. If the subsystem clock is used, then the system clock frequency must either be between 0.4 and 1.0 MHz or between 1.6 and 4.5 MHz (or 1.6 and 5.0 MHz, or 1.6 and 8.5 MHz).

1. HD404364, HD404368, HD4043612, HD404369
2. HD40A4364, HD40A4368, HD40A43612, HD40A4369, HD407A4369

14.2.2 System Clock Selection Register 2 (SSR2: $028)

SSR2 is a 2-bit write-only register that selects the system clock divisor.

SSR2 is initialized to $0 on reset and in stop mode.



0	0	Division by 4 ($f_{cyc} = f_{OSC}/4$)
	1	Division by 8 ($f_{cyc} = f_{OSC}/8$)
1	0	Division by 16 ($f_{cyc} = f_{OSC}/16$)
	1	Division by 32 ($f_{cyc} = f_{OSC}/32$)

Bits 1 and 0—System Clock Selection (SSR21, SSR20): These bits set the system clock divisor to be 4, 8, 16, or 32, i.e., the system oscillator frequency is divided by 4, 8, 16, or 32. ($f_{cyc} = f_{OSC}/4$, $f_{OSC}/8$, $f_{OSC}/16$, or $f_{OSC}/32$) This setting only takes effect when watch mode is entered. That is, the system clock must be stopped to change the divisor.

SSR21	SSR20	Description	
0	0	The system clock divisor is 4 ($f_{cyc} = f_{OSC}/4$)	(initial value)
	1	The system clock divisor is 8 ($f_{cyc} = f_{OSC}/8$)	
1	0	The system clock divisor is 16 ($f_{cyc} = f_{OSC}/16$)	
	1	The system clock divisor is 32 ($f_{cyc} = f_{OSC}/32$)	

There are two methods for changing the system clock divisor as follows.

1. In active mode, set the divisor by writing the SSR21 and SSR20 bits. At this point the immediately prior divisor setting remains in effect. Now, switch to watch mode and then return to active mode. When the system returns to active mode the new clock divisor will be in effect.

2. In subactive mode, set the divisor by writing the SSR21 and SSR20 bits. Then, return to active mode by passing through watch mode. When the system returns to active mode the new clock divisor will be in effect. (The change will also take effect for direct transition to active mode.)

14.2.3 Low Speed On Flag (LSON: $020, 0)

LSON selects whether the system operating clock is taken from the system clock or from the subsystem clock when switching modes between active mode, watch mode, and subactive mode. See section 6.2.5, “Low Speed On Flag (LSON)”, for details.

14.3 Oscillator Connection and External Clock Input

The system clock oscillator circuit supports the use of a ceramic or crystal oscillator with a frequency between 0.4 and 4.5 MHz (or between 0.4 and 8.5 MHz) or an external clock input. A 32.768 MHz crystal oscillator must be used as the subsystem clock oscillator. Table 14-3 shows sample oscillator circuits.

Table 14-3 Oscillator Circuit Examples

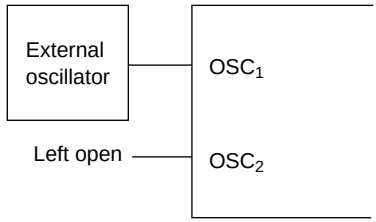
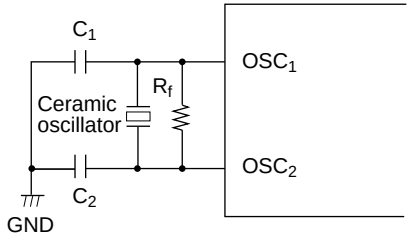
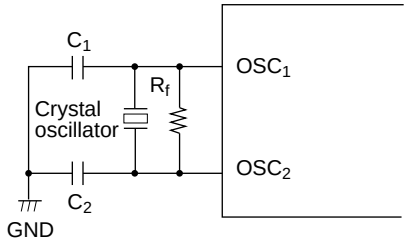
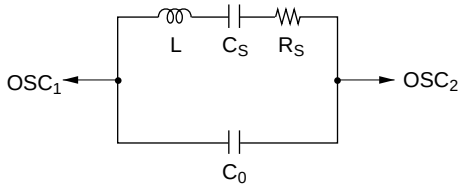
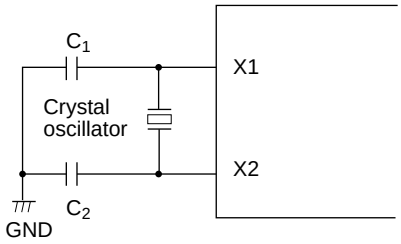
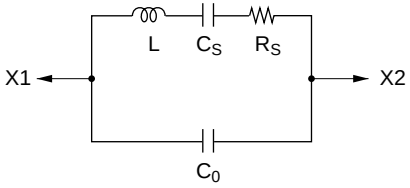
	Circuit	Circuit Constants
External clock		—
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSA 4.00MG (Murata Manufacturing) R_f = 1 MΩ ±20% $C_1 = C_2$ = 30 pF ±20%
Crystal oscillator (OSC_1, OSC_2)	 Cut parallel resonator type crystal oscillator 	R_f = 1 MΩ ±20% $C_1 = C_2$ = 10 to 22 pF ±20% Crystal oscillator: Equivalent circuit shown at left C_0 = 7 pF max R_S = 100 Ω max f = 1.0 to 4.5 MHz

Table 14-3 Oscillator Circuit Examples (cont)

Circuit	Circuit Constants
Crystal oscillator (X1, X2)  Cut parallel resonator type crystal oscillator  	Crystal oscillator: 32.768 kHz; MX38T (Nippon Denpa Kogyo, Ltd.) C1 = C2 = 20 pF ±20% RS = 14 kΩ C0 = 1.5 pF

14.4 Usage Notes

Keep the following points in mind when designing and implementing clock oscillator circuits.

- When using a crystal or ceramic oscillator the circuit constants will differ depending on the device actually used, the stray capacitances in the mounted circuit and other factors. Therefore, these circuit parameters should be determined in consultation with the manufacturer of the crystal or ceramic oscillator element used.
- The distance between the OSC_1 and OSC_2 pins (and X1 and X2 pins) and the devices connected to those pins should be kept as short as possible. Do not allow any other lines to cross those lines. (See figure 14-2.) Correct oscillation may become impossible due to induced signals if any lines cross.
- If the subsystem clock (the 32.768 kHz oscillator) is not used, connect the X1 pin to ground and leave the X2 pin open.

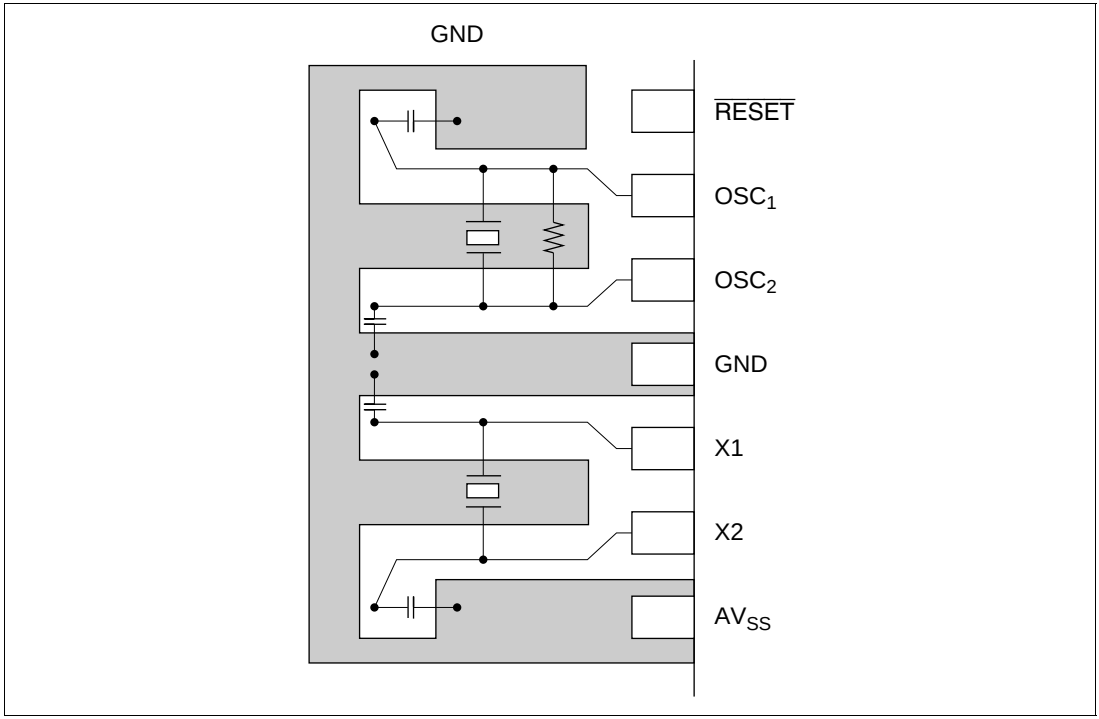


Figure 14-2 Wiring Example for Crystal and Ceramic Oscillators

Section 15 A/D Converter

15.1 Overview

The HMCS43XX family microcomputers include a built-in resistor ladder successive approximations A/D converter.

15.1.1 Features

The A/D converter has the following features.

- Eight bit resolution (1/256 of the reference voltage)
- Input channels

Series	Number of Channels
HD404344R	4
HD404394	3
HD404318	8
HD404358	
HD404358R	
HD404339	12
HD404369	

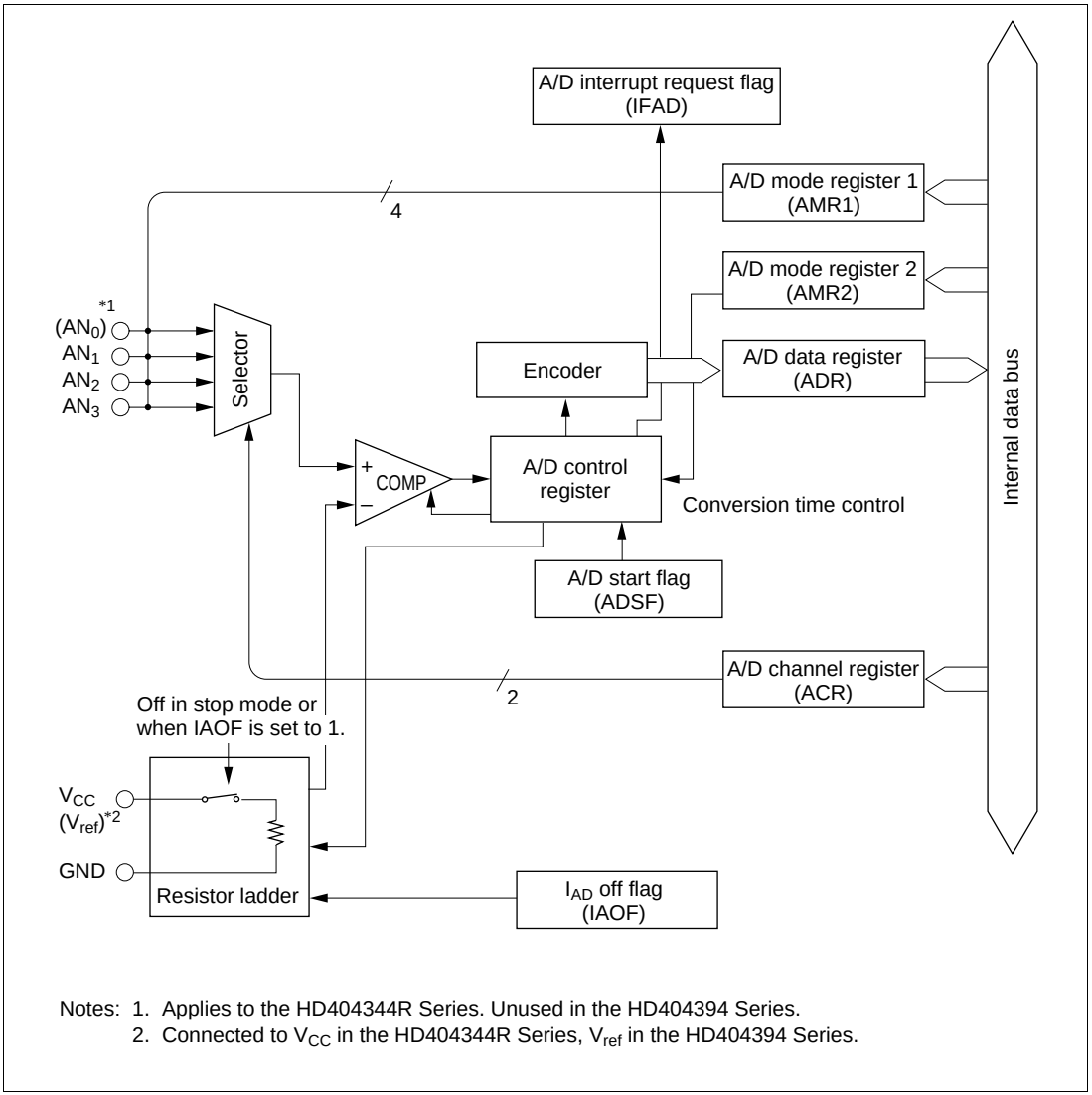
- Analog power supply

Series	Analog Reference Power Supply
HD404344R	V_{CC} (internal connection)
HD404394	V_{ref}
HD404318	AV_{CC}
HD404358	
HD404358R	
HD404339	
HD404369	

- Conversion time: $34t_{cyc}$ or $67t_{cyc}$ (t_{cyc}: system clock period)
- An interrupt is generated at the completion of an A/D conversion.

15.1.2 Block Diagram

Figures 15-1 (a), (b), and (c) show the block diagrams of the A/D converter circuits used in the HD404344R/HD404394 Series, HD404318/HD404358/HD404358R Series, and HD404339/HD404369 Series microcomputers, respectively.



Notes: 1. Applies to the HD404344R Series. Unused in the HD404394 Series.
2. Connected to V_{CC} in the HD404344R Series, V_{ref} in the HD404394 Series.

Figure 15-1 (a) A/D Converter Block Diagram (HD404344R/HD404394 Series)

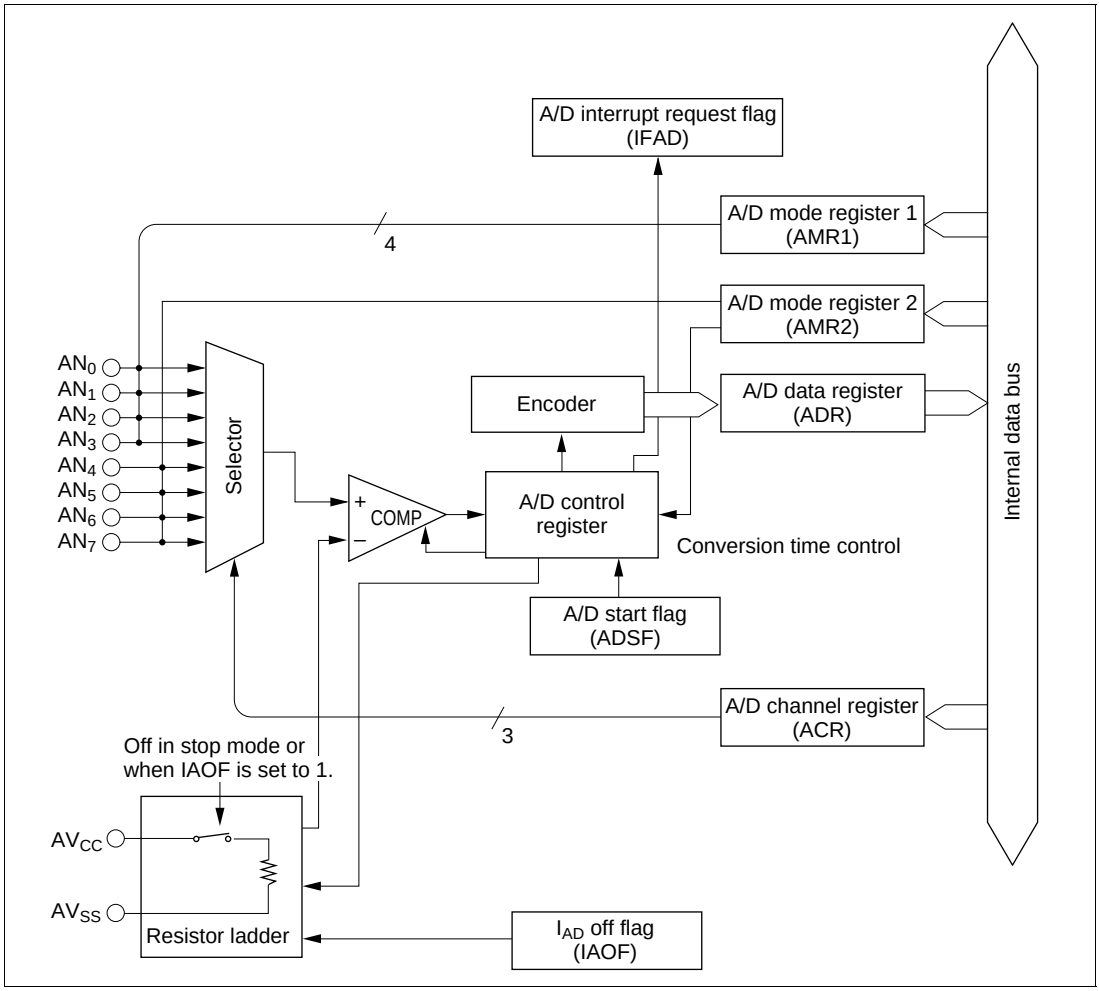


Figure 15-1 (b) A/D Converter Block Diagram (HD404318/HD404358/HD404358R Series)

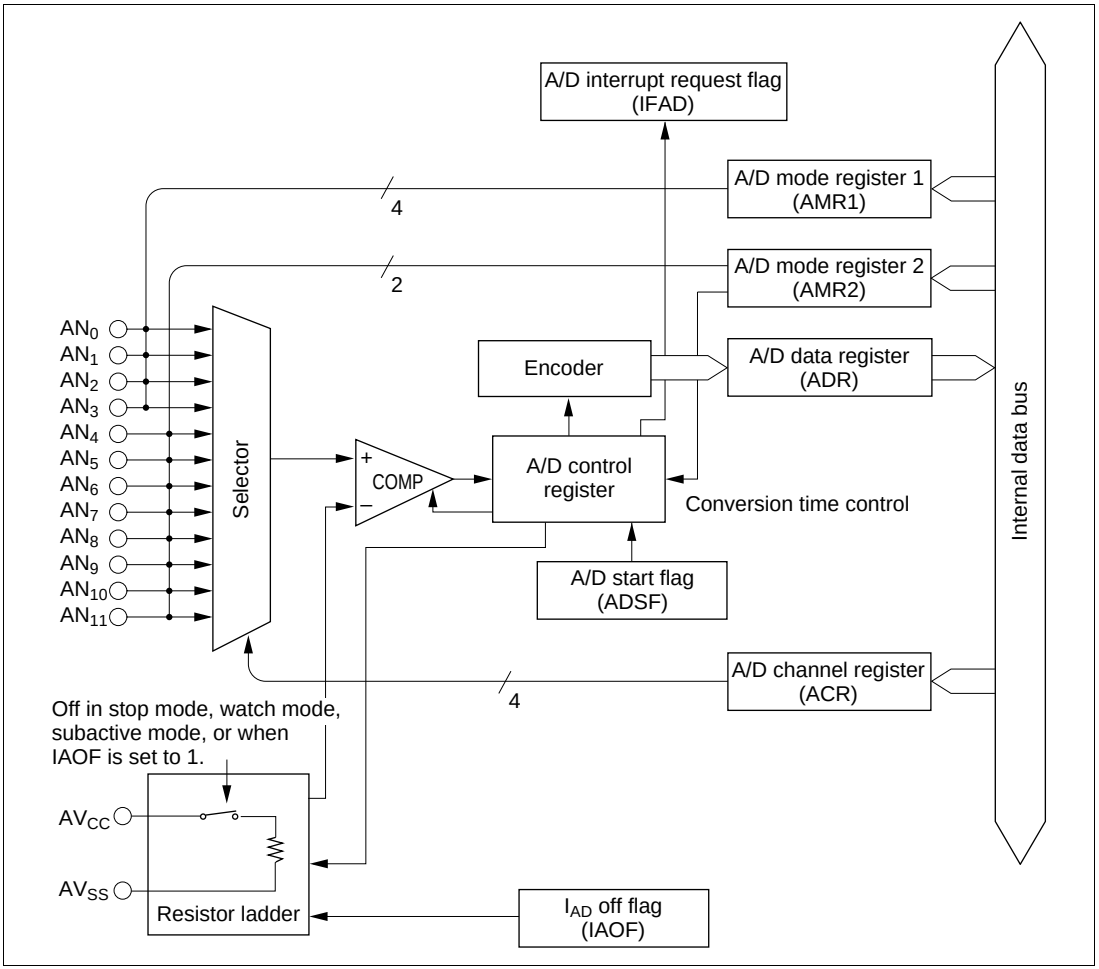


Figure 15-1 (c) A/D Converter Block Diagram (HD404339/HD404369 Series)

15.1.3 Pin Configuration

Table 15-1 shows the configuration of the A/D converter pins.

Table 15-1 Pin Configuration

HD404344R Series

Pin	Symbol	I/O	Function
Analog input channel 0	$R3_0/AN_0$	I/O or input	Shared function: Analog input channel 0 or $R3_0$
Analog input channel 1	$R3_1/AN_1$	I/O or input	Shared function: Analog input channel 1 or $R3_1$
Analog input channel 2	$R3_2/AN_2$	I/O or input	Shared function: Analog input channel 2 or $R3_2$
Analog input channel 3	$R3_3/AN_3$	I/O or input	Shared function: Analog input channel 3 or $R3_3$

HD404394 Series

Pin	Symbol	I/O	Function
Analog reference power supply	V_{ref}	—	Analog reference power supply
Analog input channel 1	$R3_1/AN_1$	I/O or input	Shared function: Analog input channel 1 or $R3_1$
Analog input channel 2	$R3_2/AN_2$	I/O or input	Shared function: Analog input channel 2 or $R3_2$
Analog input channel 3	$R3_3/AN_3$	I/O or input	Shared function: Analog input channel 3 or $R3_3$

Table 15-1 Pin Configuration (cont)

HD404318/HD404358/HD404358R Series

Pin	Symbol	I/O	Function
Analog power supply	AV_{CC}		Power supply for the analog block
Analog ground	AV_{SS}	—	Ground for the analog block
Analog input channel 0	$R3_0/AN_0$	I/O or input	Shared function: Analog input channel 0 or $R3_0$
Analog input channel 1	$R3_1/AN_1$	I/O or input	Shared function: Analog input channel 1 or $R3_1$
Analog input channel 2	$R3_2/AN_2$	I/O or input	Shared function: Analog input channel 2 or $R3_2$
Analog input channel 3	$R3_3/AN_3$	I/O or input	Shared function: Analog input channel 3 or $R3_3$
Analog input channel 4	$R4_0/AN_4$	I/O or input	Shared function: Analog input channel 4 or $R4_0$
Analog input channel 5	$R4_1/AN_5$	I/O or input	Shared function: Analog input channel 5 or $R4_1$
Analog input channel 6	$R4_2/AN_6$	I/O or input	Shared function: Analog input channel 6 or $R4_2$
Analog input channel 7	$R4_3/AN_7$	I/O or input	Shared function: Analog input channel 7 or $R4_3$

Table 15-1 Pin Configuration (cont)

HD404339/HD404369 Series

Pin	Symbol	I/O	Function
Analog power supply	AV_{CC}	—	Power supply for the analog block
Analog ground	AV_{SS}	—	Ground for the analog block
Analog input channel 0	$R3_0/AN_0$	I/O or input	Shared function: Analog input channel 0 or $R3_0$
Analog input channel 1	$R3_1/AN_1$	I/O or input	Shared function: Analog input channel 1 or $R3_1$
Analog input channel 2	$R3_2/AN_2$	I/O or input	Shared function: Analog input channel 2 or $R3_2$
Analog input channel 3	$R3_3/AN_3$	I/O or input	Shared function: Analog input channel 3 or $R3_3$
Analog input channel 4	$R4_0/AN_4$	I/O or input	Shared function: Analog input channel 4 or $R4_0$
Analog input channel 5	$R4_1/AN_5$	I/O or input	Shared function: Analog input channel 5 or $R4_1$
Analog input channel 6	$R4_2/AN_6$	I/O or input	Shared function: Analog input channel 6 or $R4_2$
Analog input channel 7	$R4_3/AN_7$	I/O or input	Shared function: Analog input channel 7 or $R4_3$
Analog input channel 8	$R5_0/AN_8$	I/O or input	Shared function: Analog input channel 8 or $R5_0$
Analog input channel 9	$R5_1/AN_9$	I/O or input	Shared function: Analog input channel 9 or $R5_1$
Analog input channel 10	$R5_2/AN_{10}$	I/O or input	Shared function: Analog input channel 10 or $R5_2$
Analog input channel 11	$R5_3/AN_{11}$	I/O or input	Shared function: Analog input channel 11 or $R5_3$

15.1.4 Register and Flag Configuration

Table 15-2 shows the configuration of the registers and flags used by the A/D converter.

Table 15-2 Register and Flag Configuration

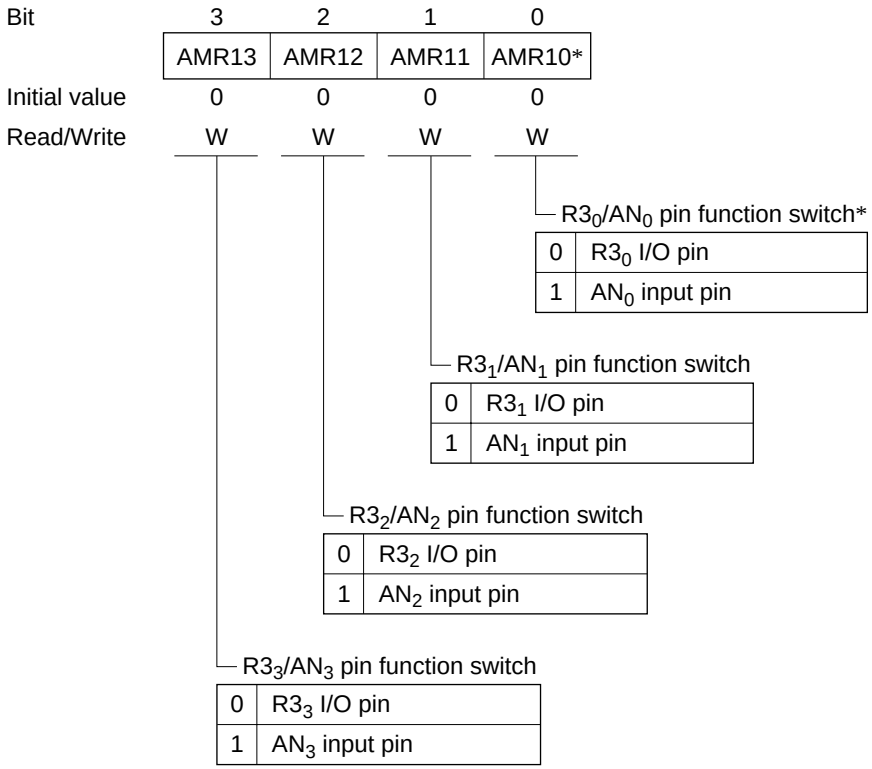
Address	Item	Symbol	R/W	Initial Value
$019	A/D mode register 1	AMR1	W	$0
$01A	A/D mode register 2	AMR2	W	$0
$017	A/D data register L	ADRL	R	$0
$018	A/D data register U	ADRU	R	$8
$016	A/D channel register	ACR	W	$0
$020, 2	A/D start flag	ADSF	R/W*	0
$021, 2	IAD off flag	IAOF	R/W*	0

Note: * ADSF and IAOF are allocated in the register flag area and can only be manipulated with the RAM bit manipulation instructions. Only a 1 can be written to the ADSF flag, i.e., it can only be set to 1, it cannot be cleared to 0.

15.2 Register and Flag Descriptions

15.2.1 A/D Mode Register 1 (AMR1: $019)

AMR1 is a 4-bit write-only register that switches the functions of the R3 port shared function pins.



Note: * Applies to the HD404344R, HD404318, HD404358, HD404358R, HD404339, and HD404369 Series.
The AMR10 bit is unused in the HD404394 Series.

Bit 3—R3$_3$/AN$_3$ Pin Function Switch (AMR13): Selects whether the R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin or as the A/D converter channel 3 input pin AN$_3$.

AMR13	Description	
0	The R3$_3$/AN$_3$ pin functions as the R3$_3$ I/O pin.	(initial value)
1	The R3$_3$/AN$_3$ pin functions as the AN$_3$ input pin.	

Bit 2—$R3_2/AN_2$ Pin Function Switch (AMR12): Selects whether the $R3_2/AN_2$ pin functions as the $R3_2$ I/O pin or as the A/D converter channel 2 input pin AN_2.

AMR12	Description	
0	The $R3_2/AN_2$ pin functions as the $R3_2$ I/O pin.	(initial value)
1	The $R3_2/AN_2$ pin functions as the AN_2 input pin.	

Bit 1—$R3_1/AN_1$ Pin Function Switch (AMR11): Selects whether the $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin or as the A/D converter channel 1 input pin AN_1.

AMR11	Description	
0	The $R3_1/AN_1$ pin functions as the $R3_1$ I/O pin.	(initial value)
1	The $R3_1/AN_1$ pin functions as the AN_1 input pin.	

HD404344R/HD404318/HD404358/HD404358R/HD404339/HD404369 Series

Bit 0—$R3_0/AN_0$ Pin Function Switch (AMR10): Selects whether the $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin or as the A/D converter channel 0 input pin AN_0.

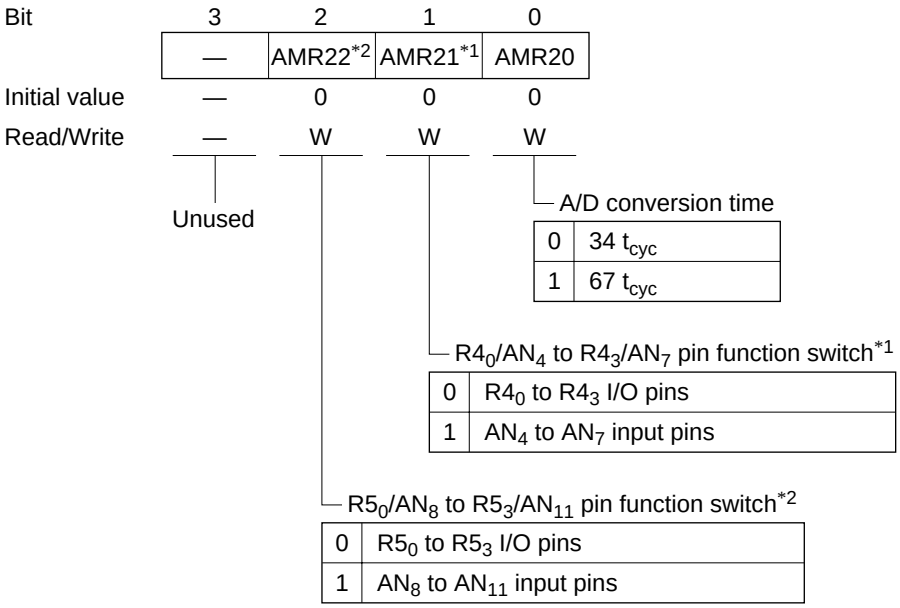
AMR10	Description	
0	The $R3_0/AN_0$ pin functions as the $R3_0$ I/O pin.	(initial value)
1	The $R3_0/AN_0$ pin functions as the AN_0 input pin.	

HD404394 Series

Bit 0—Reserved Bit: This bit is unused.

15.2.2 A/D Mode Register 2 (AMR2: $01A)

AMR2 is a 4-bit write-only register that sets the A/D conversion time and switches the functions of certain R port shared function pins.



Notes: 1. Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The AMR21 bit is unused in the HD404344R and HD404394 Series.
2. Applies to the HD404339 and HD404369 Series. The AMR22 bit is unused in the HD404344R, HD404394, HD404318, HD404358, and HD404358R Series.

HD404339/HD404369 Series

Bit 2—$R5_0/AN_8$ to $R5_3/AN_{11}$ Pin Function Switch (AMR22): Selects whether the $R5_0/AN_8$ to $R5_3/AN_{11}$ pins function as the $R5_0$ to $R5_3$ I/O pins or as the A/D converter channel 8 to 11 input pins (AN_8 to AN_{11}).

AMR22	Description	
0	The $R5_0/AN_8$ to $R5_3/AN_{11}$ pins function as the $R5_0$ to $R5_3$ I/O pins.	(initial value)
1	The $R5_0/AN_8$ to $R5_3/AN_{11}$ pins function as the AN_8 to AN_{11} input pins.	

HD404344R/HD404394/HD404318/HD404358/HD404358R Series

Bit 2—Reserved Bit: This bit is unused.

Bit 1—$R4_0/AN_4$ to $R4_3/AN_7$ Pin Function Switch (AMR21): Selects whether the $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins or as the A/D converter channel 4 to 7 input pins (AN_4 to AN_7).

AMR21	Description	
0	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the $R4_0$ to $R4_3$ I/O pins.	(initial value)
1	The $R4_0/AN_4$ to $R4_3/AN_7$ pins function as the AN_4 to AN_7 input pins.	

HD404344R/HD404394 Series

Bit 1—Reserved Bit: This bit is unused.

Bit 0—A/D Conversion Time Selection (AMR20): Selects the A/D conversion time.

AMR20	Description	
0	Conversion time = $34t_{cyc}$	(initial value)
1	Conversion time = $67t_{cyc}$	

Note: t_{cyc} is the system clock period.

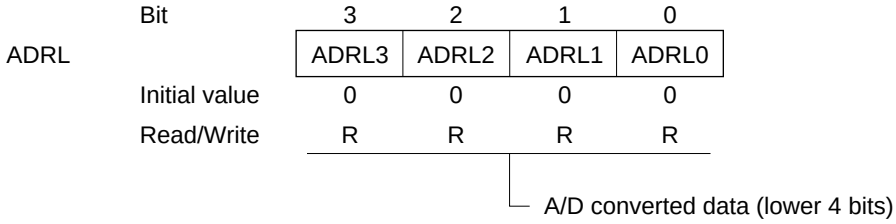
15.2.3 A/D Data Register L, U (ADRL: $017, ADRU: $018)

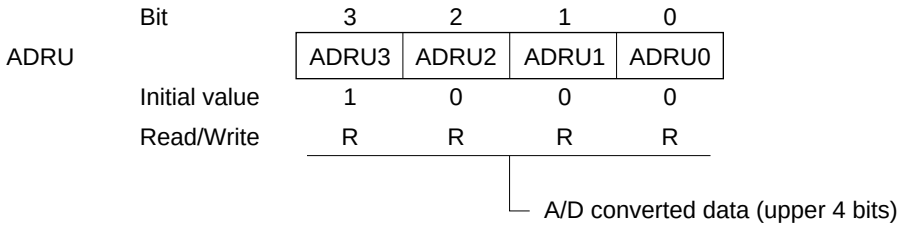
The ADRL/U pair (ADRL and ADRU) forms an 8-bit read-only register in which ADRL is the lower digit and ADRU is the upper digit.

The 8-bit A/D converted data is transferred to the ADRL/U pair and held until the start of the next conversion.

The contents of this register is not guaranteed during A/D converter operation.

The ADRL/U pair is not cleared on reset.





15.2.4 A/D Channel Register (ACR: $016)

ACR is a 4-bit write-only register that selects the input channel for which A/D conversion will be performed.

Bit	3	2	1	0
	ACR3	ACR2	ACR1	ACR0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Analog input channel selection

ACR3	ACR2	ACR1	ACR0	Input channel			
				HD404344R	HD404394	HD404318/ HD404358/ HD404358R	HD404339/ HD404369
0	0	0	0	AN_0		AN_0	AN_0
			1	AN_1	AN_1	AN_1	AN_1
		1	0	AN_2	AN_2	AN_2	AN_2
			1	AN_3	AN_3	AN_3	AN_3
	1	0	0			AN_4	AN_4
			1			AN_5	AN_5
		1	0			AN_6	AN_6
			1			AN_7	AN_7
1	0	0	0				AN_8
			1				AN_9
		1	0				AN_{10}
			1				AN_{11}
	1	*	*				

Note: * Don't care

: Unused

Bits 3 to 0—Analog Input Channel Selection (ACR3 to ACR0): These bits select the analog input channel.

HD404344R Series

ACR3	ACR2	ACR1	ACR0	Description	
0	0	0	0	Analog input channel 0 (AN0) selected.	(initial value)
			1	Analog input channel 1 (AN1) selected.	
		1	0	Analog input channel 2 (AN2) selected.	
			1	Analog input channel 3 (AN3) selected.	
	1	*	*	Unused	
1	*	*	*		

Note: * Don't care

HD404394 Series

ACR3	ACR2	ACR1	ACR0	Description	
0	0	0	0	Unused	(initial value)
			1	Analog input channel 1 (AN1) selected.	
		1	0	Analog input channel 2 (AN2) selected.	
			1	Analog input channel 3 (AN3) selected.	
	1	*	*	Unused	
1	*	*	*		

Note: * Don't care

HD404318/HD404358/HD404358R Series

ACR3	ACR2	ACR1	ACR0	Description	
0	0	0	0	Analog input channel 0 (AN0) selected.	(initial value)
			1	Analog input channel 1 (AN1) selected.	
		1	0	Analog input channel 2 (AN2) selected.	
			1	Analog input channel 3 (AN3) selected.	
	1	0	0	Analog input channel 4 (AN4) selected.	
			1	Analog input channel 5 (AN5) selected.	
		1	0	Analog input channel 6 (AN6) selected.	
			1	Analog input channel 7 (AN7) selected.	
1	*	*	*	Unused	

Note: * Don't care

ACR3	ACR2	ACR1	ACR0	Description	
0	0	0	0	Analog input channel 0 (AN0) selected.	(initial value)
			1	Analog input channel 1 (AN1) selected.	
		1	0	Analog input channel 2 (AN2) selected.	
			1	Analog input channel 3 (AN3) selected.	
	1	0	0	Analog input channel 4 (AN4) selected.	
			1	Analog input channel 5 (AN5) selected.	
		1	0	Analog input channel 6 (AN6) selected.	
			1	Analog input channel 7 (AN7) selected.	
1	0	0	0	Analog input channel 8 (AN8) selected.	
			1	Analog input channel 9 (AN9) selected.	
		1	0	Analog input channel 10 (AN10) selected.	
			1	Analog input channel 11 (AN11) selected.	
	1	*	*	Unused	

Note: * Don't care

15.2.5 A/D Start Flag (ADSF: $020, 2)

ADSF starts the A/D conversion process. When ADSF is set to 1, the A/D converter starts. When the conversion completes, the converted data is transferred to the ADRL/U pair and ADSF is cleared to 0.

ADSF can be read and written using the RAM bit manipulation instructions.

ADSF is cleared to 0 on reset and in stop mode.

ADSF	Description	
0	(Read) Indicates that the A/D conversion had completed. (Write) The value 0 cannot be written.	(initial value)
1	(Read) An A/D conversion is in progress. (Write) Starts the A/D converter.	

15.2.6 IAD Off Flag (IAOF: $021, 2)

The current flow through the resistor ladder can be cut off by setting IAOF to 1 in either standby mode or active mode. However, the A/D converter will not operate correctly in this state. Do not use the A/D converter when IAOF is set to 1.

IAOF	Description	
0	Current flows in the resistor ladder.	(initial value)
1	No current flows in the resistor ladder.	

15.3 A/D Converter Operation

15.3.1 A/D Conversion Operation

Figure 15-2 shows the A/D conversion operation sequence.

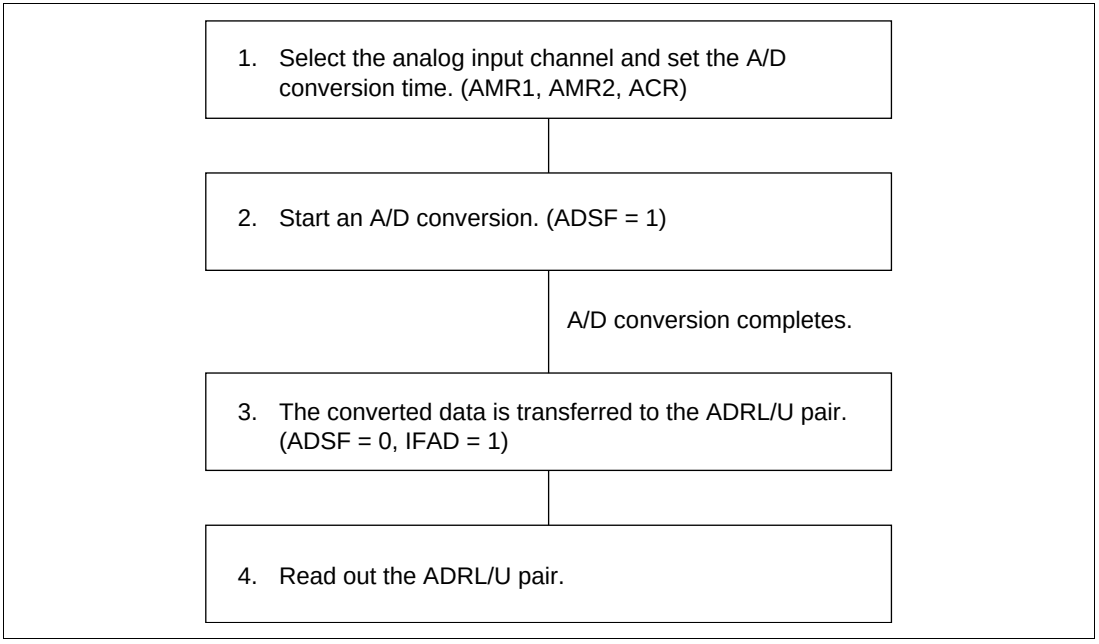


Figure 15-2 A/D Conversion Operation Sequence

An A/D converter operation proceeds as follows.

1. Select the analog input channel and set the A/D conversion time using the AMR register (AMR1, AMR2, and ACR).
2. Start an A/D conversion by setting ADSF to 1.
3. When the A/D conversion completes, the converted data is transferred to the ADRL/U pair, and ADSF is cleared to 0. At the same time, IFAD is set to 1.
4. Read out the data from the ADRL/U pair.

Figure 15-3 shows the timing chart for A/D converter operation.

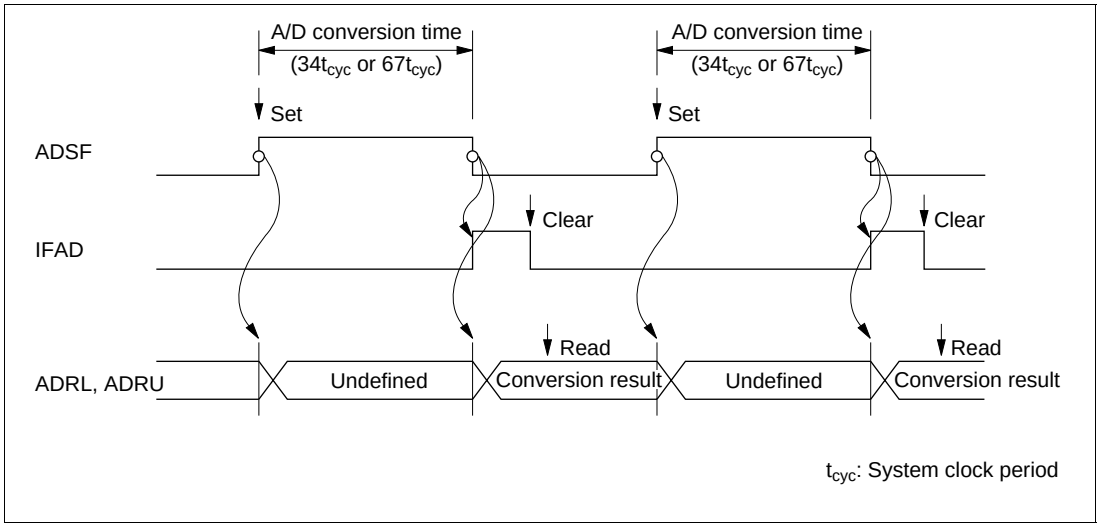


Figure 15-3 A/D Converter Operation Timing Chart

15.3.2 Low Power Mode Operation

The current supplied to the resistor ladder is cut off in stop mode, watch mode*, and subactive mode. As a result, the A/D converter does not operate in these modes.

Note: * Applies to the HD404339 and HD404369 Series.

15.3.3 A/D Converter Precision

Since an A/D converter converts an analog signal to a digital code, there is, in principle, a quantization error (defined to be 1/2 the LSB) associated with the conversion. Figure 15-4 shows the correspondence between an eight-bit resolution A/D converter's analog input voltage and the result of the conversion.

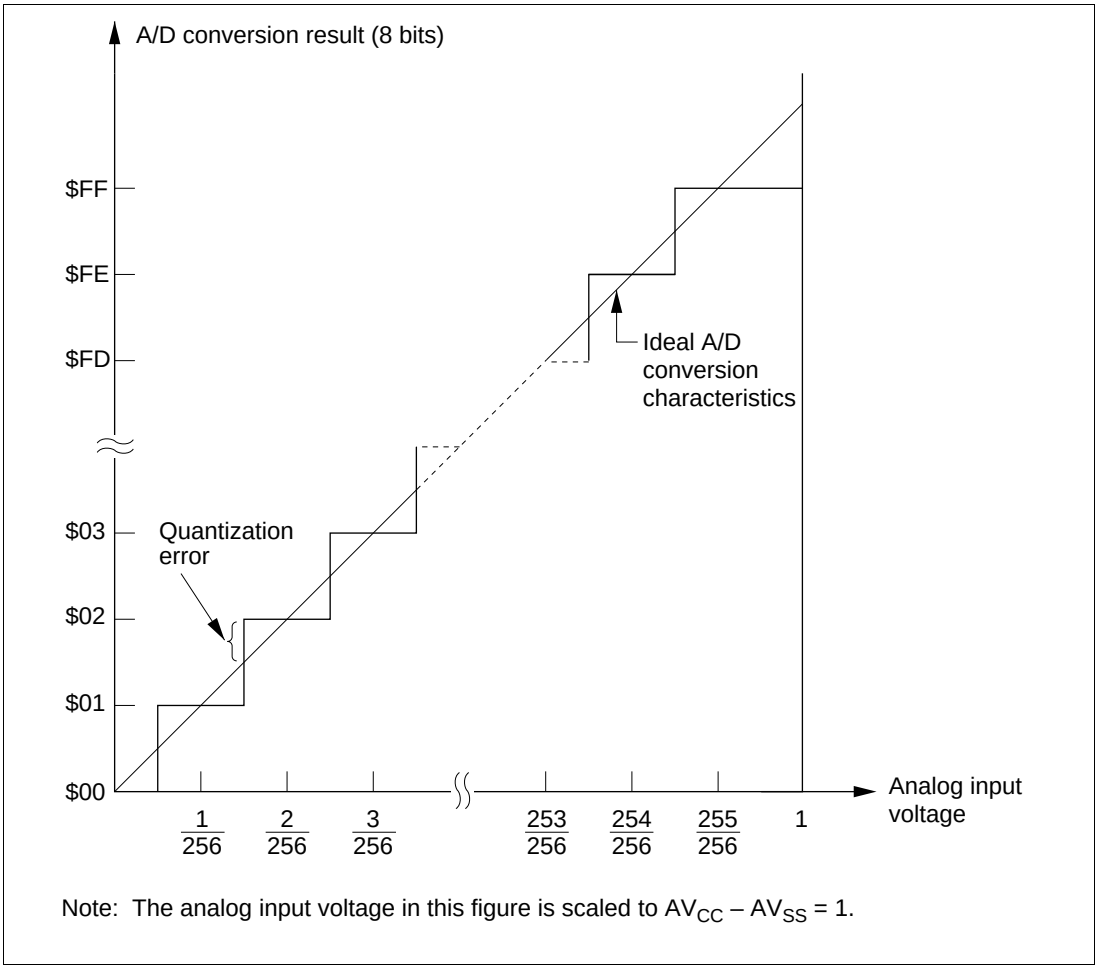


Figure 15-4 Correspondence between A/D Converter Analog Input and Digital Output

The difference between the result of an A/D conversion and the analog input is called the absolute precision. See the "A/D Converter Characteristics" item for each series in section 25, "Electrical Characteristics", for the absolute precision provided by these A/D converters.

15.3.4 Notes on the Analog Reference Power Supply

In products in which the A/D converter reference voltage is fixed at AV_{CC} or V_{CC} (the HD404344R, HD404318, HD404358, HD404358R, HD404339, and HD404369 Series), the resolution is fixed at $AV_{CC}/256$ or $V_{CC}/256$. (Note that a reference voltage in the range $V_{CC} - 0.3 \leq AV_{CC} \leq V_{CC} + 0.3$ must be used even in products that provide an AV_{CC} pin.)

The HD404394 Series microcomputers, which include a V_{ref} pin, support A/D conversions with an even higher resolution ($V_{ref}/256$) by varying the V_{ref} pin voltage. However, the voltage applied to the V_{ref} pin must be in the range $V_{CC}/2 \leq V_{ref} \leq V_{CC}$.

15.4 Interrupts

The A/D converter interrupt source is the completion of A/D conversion.

When A/D conversion completes, the IFAD bit in the interrupt control bit area is set to 1.

IFAD is never cleared automatically, even if the interrupt is accepted. The interrupt handling routine should clear IFAD to 0.

The A/D interrupt can be independently enabled or masked with the A/D interrupt mask (IMAD) in the interrupt control bit area.

15.5 Usage Notes

Keep the following points in mind when using the A/D converter.

- ADSF is allocated in the register flag area. Use the SEM and SEMD instructions to set ADSF. Do not attempt to write a 0 to ADSF.
- Do not write ADSF during an A/D conversion.
- The contents of the ADRL/U pair are undefined during an A/D conversion.
- Do not write a 1 to IAOF during an A/D conversion.
- The pull-up MOS transistors on R port/analog input shared function pins are not turned off by selecting the pin for use as an analog input pin with AMR1 if the MIS MIS3 bit is set to 1 (pull-up MOS transistors active) and the PDR for the corresponding pin is set to 1. If the pull-up MOS transistors are activated, always be sure to turn off the pull-up MOS transistor for the pin being used as an analog input pin by clearing to 0 the PDR for that pin. Note that the PDRs are set to 1 immediately following a reset.

Figure 15-5 shows the circuit structure of the R port/analog input shared function pins.

AMR1 is a register that is used to set the port output to the high impedance state. ACR is used to switch the pin function to the analog input function.

Table 15-3 lists the states of the R port/analog input shared function pins that can be set by combinations of the AMR1 (AMR2), MIS3 bit, DCR, and PDR settings.

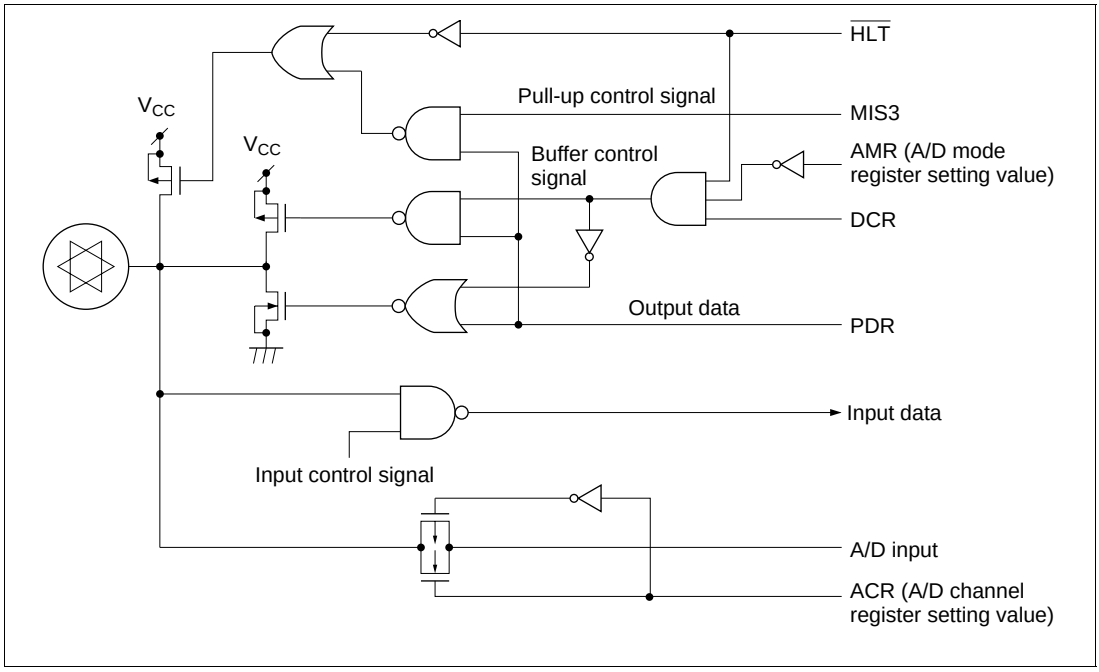


Figure 15-5 R Port/Analog Input Shared Function Pin Circuit

Table 15-3 Program Control of R Port/Analog Input Shared Function Pin States

Corresponding bit in AMR1 or AMR2		0 (R port selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	On	—		—	On
	NMOS			On	—			On	—
Pull-up MOS transistor		—				—	On	—	On

Note: —: off

Corresponding bit in AMR1 or AMR2		1 (analog input selected)							
MIS3 bit		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—		—	—	—		—	—
	NMOS			—	—			—	—
Pull-up MOS transistor		—				—	On	—	On

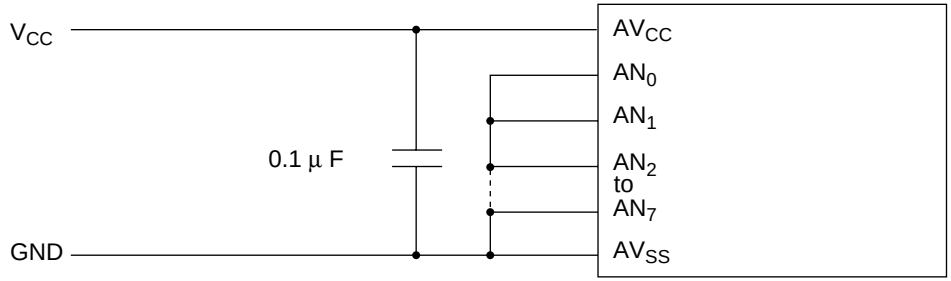
Note: —: off

15.6 Notes on Mounting Built-in A/D Converter Microcomputers (HD404318 and HD404339 Series Only)

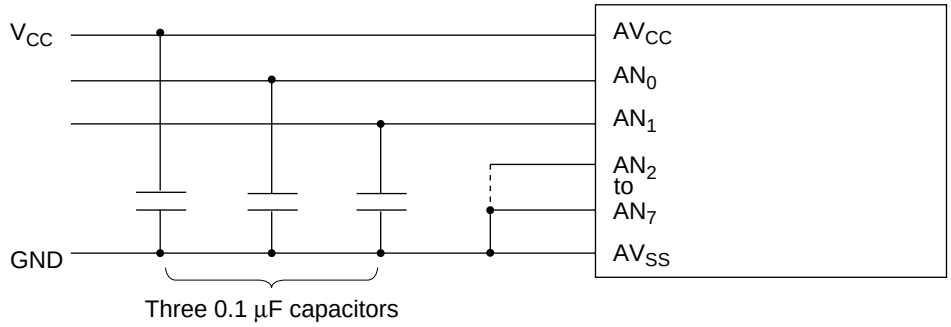
Observe the following points when designing and implementing built-in A/D converter microcomputers circuits.

- Insert bypass capacitors (laminated ceramic type) of about 0.1 µF between AV_{CC} and AV_{SS} and between pins used as analog pins and AV_{SS}. Also, connect unused analog pins to AV_{SS}. Figure 15-6 (a) shows connection examples for the HD404318 series, and figure 15-6 (b) shows connection examples for the HD404339 series.

When AN_0 to AN_7 are unused and the R3 and R4 ports are also unused



When AN_0 and AN_1 are used, and AN_2 to AN_7 are unused



When AN_0 to AN_7 (all the analog pins) are used

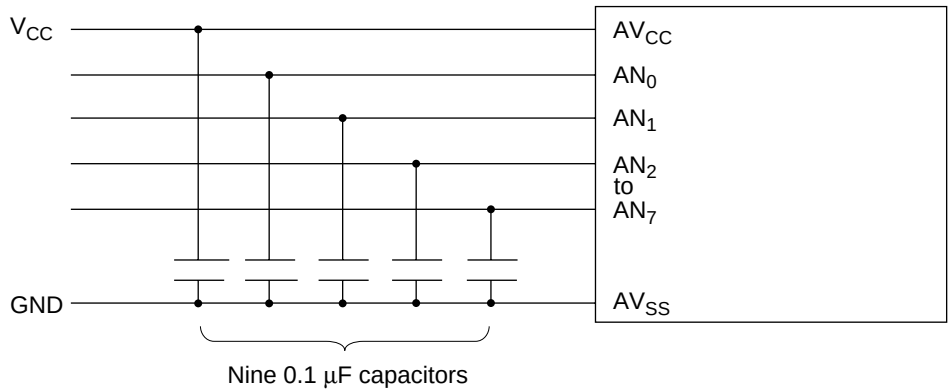
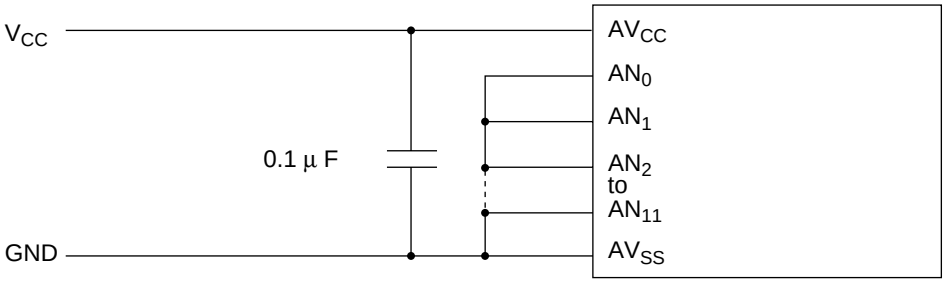
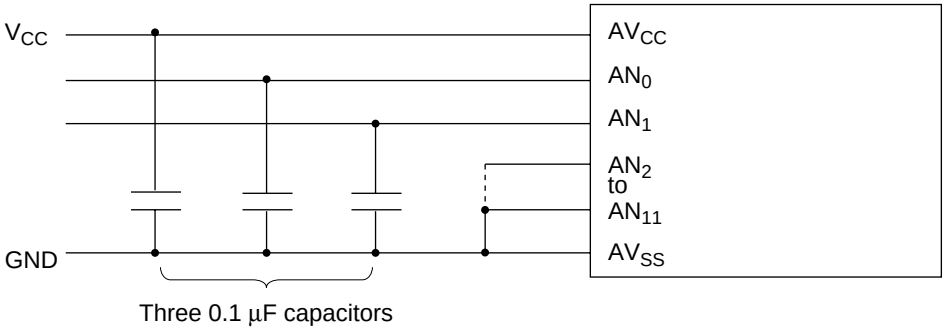


Figure 15-6 (a) Connection Examples for AV_{CC}/AV_{SS} and AV_{SS} and the Used Analog Pins (HD404318 Series)

When AN_0 to AN_{11} are unused and the R3 to R5 ports are also unused



When AN_0 and AN_1 are used, and AN_2 to AN_{11} are unused



When AN_0 to AN_{11} (all the analog pins) are used

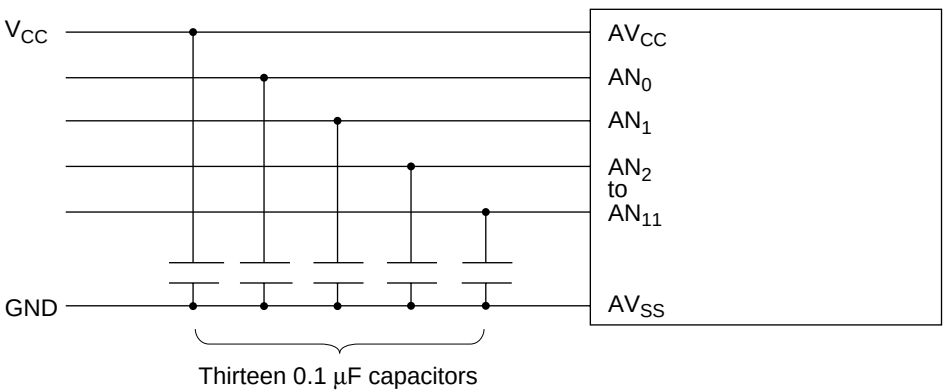


Figure 15-6 (b) Connection Examples for AV_{CC}/AV_{SS} and AV_{SS} and the Used Analog Pins (HD404339 Series)

- Connect the capacitor used in normal power supply circuit design between V_{CC} and ground. Since there will be no resistors inserted in series in the power supply circuit, the capacitors are connected in parallel. Thus a total of two capacitors, a large capacitor (C1) and a small capacitor (C2) are used. Figure 15-7 shows this circuit.

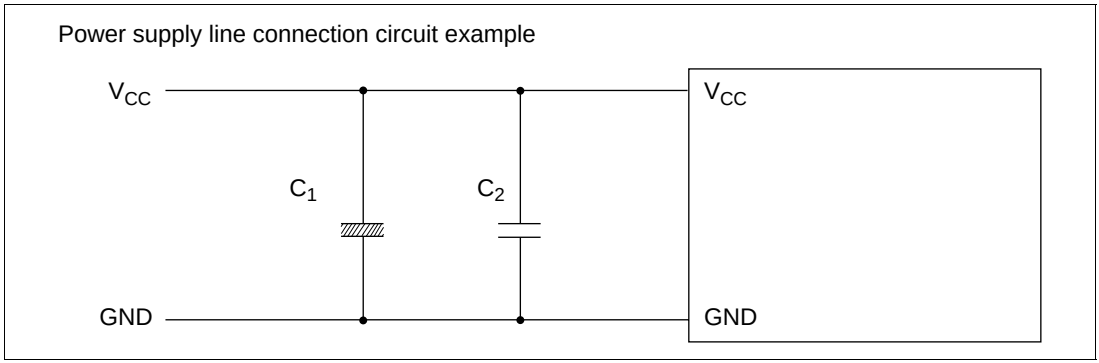


Figure 15-7 V_{CC} to Ground Circuit Example

Section 16 Prescalers

16.1 Overview

The microcomputers in the HMCS43XX family include one or two built-in prescalers. The prescaler(s) provided differ between product series.

	Series	
Prescaler	**HD404344R/HD404394/HD404318/HD404358/ HD404358R**	**HD404339/HD404369**
Prescaler S (PSS)	◯	◯
Prescaler W (PSW)	—	◯

The internal clocks for timers A to C and the operating clocks for each built-in peripheral module are selected from the prescaler outputs by the mode registers for the built-in peripheral modules.

Table 16-1 lists the input clocks and operating conditions for the prescalers.

Table 16-1 Prescaler Input Clocks and Operating Conditions

HD404344R/HD404394/HD404318/HD404358/HD404358R Series

Item	Input Clock	Reset Condition	Stop Condition
Prescaler S	• System clock	• System reset	• System reset • Stop mode

HD404339/HD404369 Series

Item	Input Clock	Reset Condition	Stop Condition
Prescaler S	• In active mode and standby mode: system clock • In subactive mode: subsystem clock	• System reset	• System reset • Stop mode • Watch mode
Prescaler W	• A clock generated by dividing the 32.768 kHz subsystem clock by eight.	• System reset • Software*	• System reset • Stop mode

Note: * PSW is cleared to 0 when all the bits TMA3 to TMA1 in timer mode register A (TMA) are set to 1.

Figure 16-1 (a) shows the prescaler output destinations for the HD404344R and HD404394 Series, figure 16-1 (b) shows the destinations for the HD404318, HD404358, and HD404358R Series, and figure 16-1 (c) shows the destinations for the HD404339 and HD404369 Series.

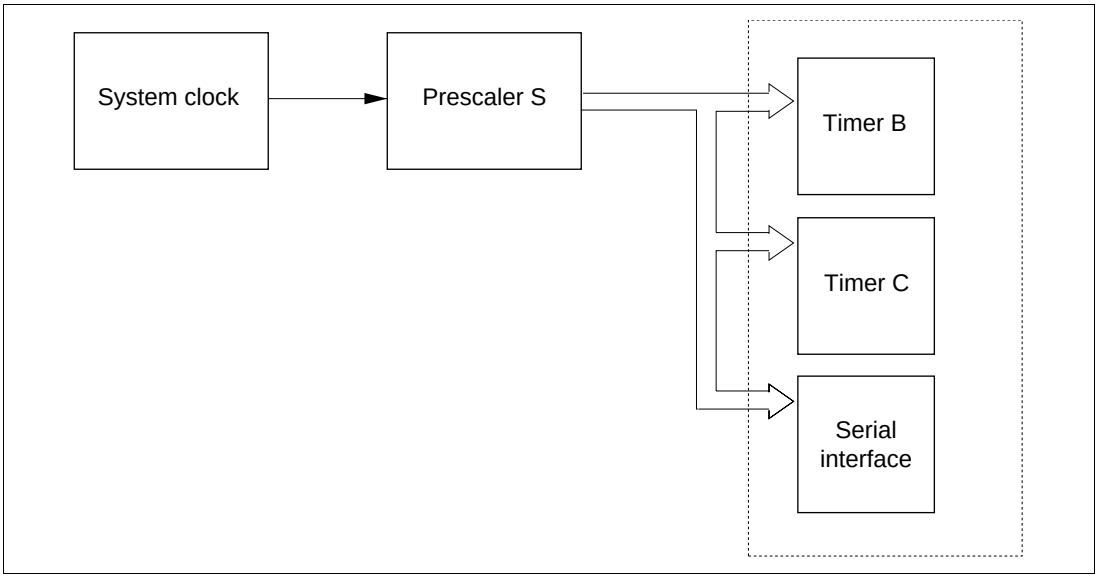


Figure 16-1 (a) Prescaler Output Destinations (HD404344R and HD404394 Series)

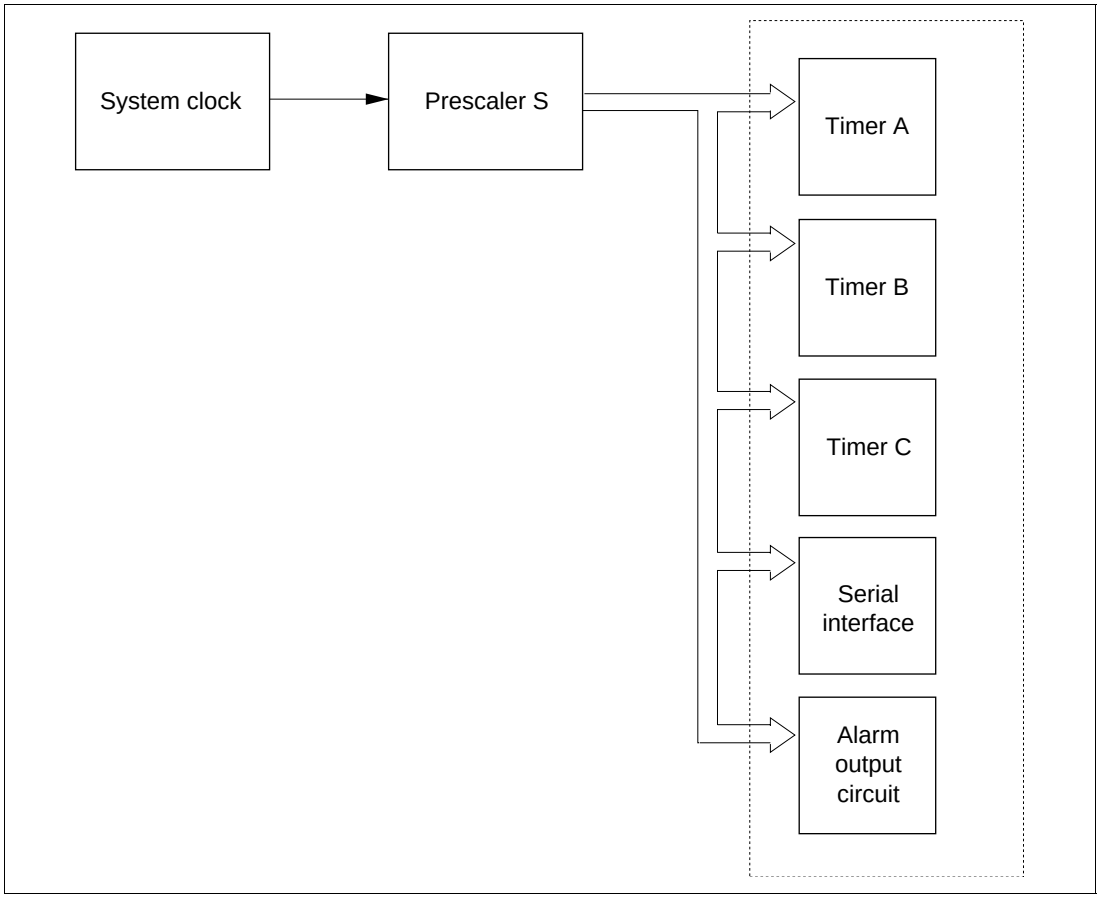


Figure 16-1 (b) Prescaler Output Destinations (HD404318, HD404358, and HD404358R Series)

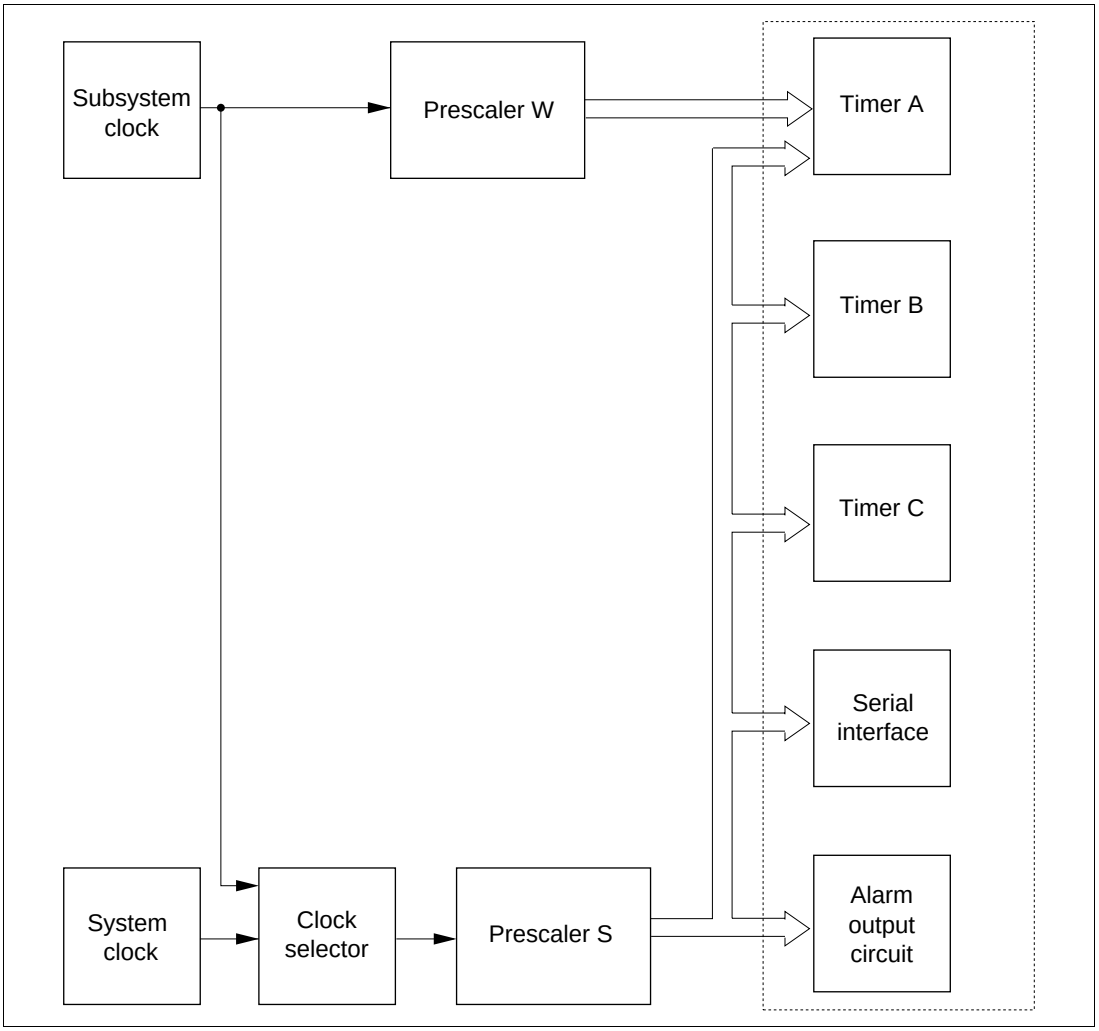


Figure 16-1 (c) Prescaler Output Destinations (HD404339 and HD404369 Series)

16.2 Prescaler S (PSS)

PSS is an 11-bit counter that takes the system clock as its input in active mode and standby mode, and the subsystem clock in subactive mode*.

PSS is initialized to $000 on reset, and divides the system clock after the reset is cleared.

Although PSS operation stops during reset, in stop mode, and in watch mode*, it continues to operate in all other operating modes. Although the PSS output is supplied to all the built-in peripheral modules, the divisor it implements can be selected independently for each built-in peripheral module.

Note: * Applies to the HD404339 and HD404369 Series.

16.3 Prescaler W (PSW) (HD404339 and HD404369 Series Only)

PSW is a 5-bit counter that takes as its input a clock generated by dividing the 32.768 kHz subsystem clock by eight.

PSW is initialized to $00 on reset, and divides the subsystem clock after the reset is cleared. Although PSW stops during reset and in stop mode, it continues to operate in all other operating modes. PSW can be reset in software.

Only timer A uses the PSW output.

Section 17 Timer A (HD404318/HD404358/HD404358R/HD404339 /HD404369 Series)

17.1 Overview

The microcomputers in the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series include the timer A peripheral module. (The microcomputers in the HD404344R and HD404394 Series do not include timer A.)

17.1.1 Features

Timer A is an eight-bit free-running timer.

Timer A can also be used as a clock time base in microcomputers in the HD404339 and HD404369 Series, which include the 32.768 kHz subsystem clock oscillator.

HD404318/HD404358/HD404358RSeries

- The timer clock can be selected from one of eight internal clock signals ($2048t_{cyc}$, $1024t_{cyc}$, $512t_{cyc}$, $128t_{cyc}$, $32t_{cyc}$, $8t_{cyc}$, $4t_{cyc}$, and $2t_{cyc}$) generated by prescaler S (PSS).
- Interrupts can be generated on timer counter A (TCA) overflow.

HD404339/HD404369 Series

- The timer clock can be selected from one of eight internal clock signals (with periods of $2048t_{cyc}$, $1024t_{cyc}$, $512t_{cyc}$, $128t_{cyc}$, $32t_{cyc}$, $8t_{cyc}$, $4t_{cyc}$, and $2t_{cyc}$) when prescaler S (PSS) is used.
- The timer clock can be selected from one of five internal clock signals (with periods of $32t_{Wcyc}$, $16t_{Wcyc}$, $8t_{Wcyc}$, $2t_{Wcyc}$, and $1/2t_{Wcyc}$) when prescaler W (PSW) is used (when timer A is used as a clock time base).
- Interrupts can be generated by the overflow of the timer counter A (TCA) register.

Note: t_{cyc} (which is $1/ø_{PER}$) is the period of one PSS count cycle, and t_{Wcyc} (which is 244.24 µs) is the period of one PSW count cycle.

17.1.2 Block Diagram

Figures 17-1 (a) and (b) show the block diagrams of timer A in the HD404318, HD404358, and HD404358R Series and in the HD404339 and HD404369 Series, respectively.

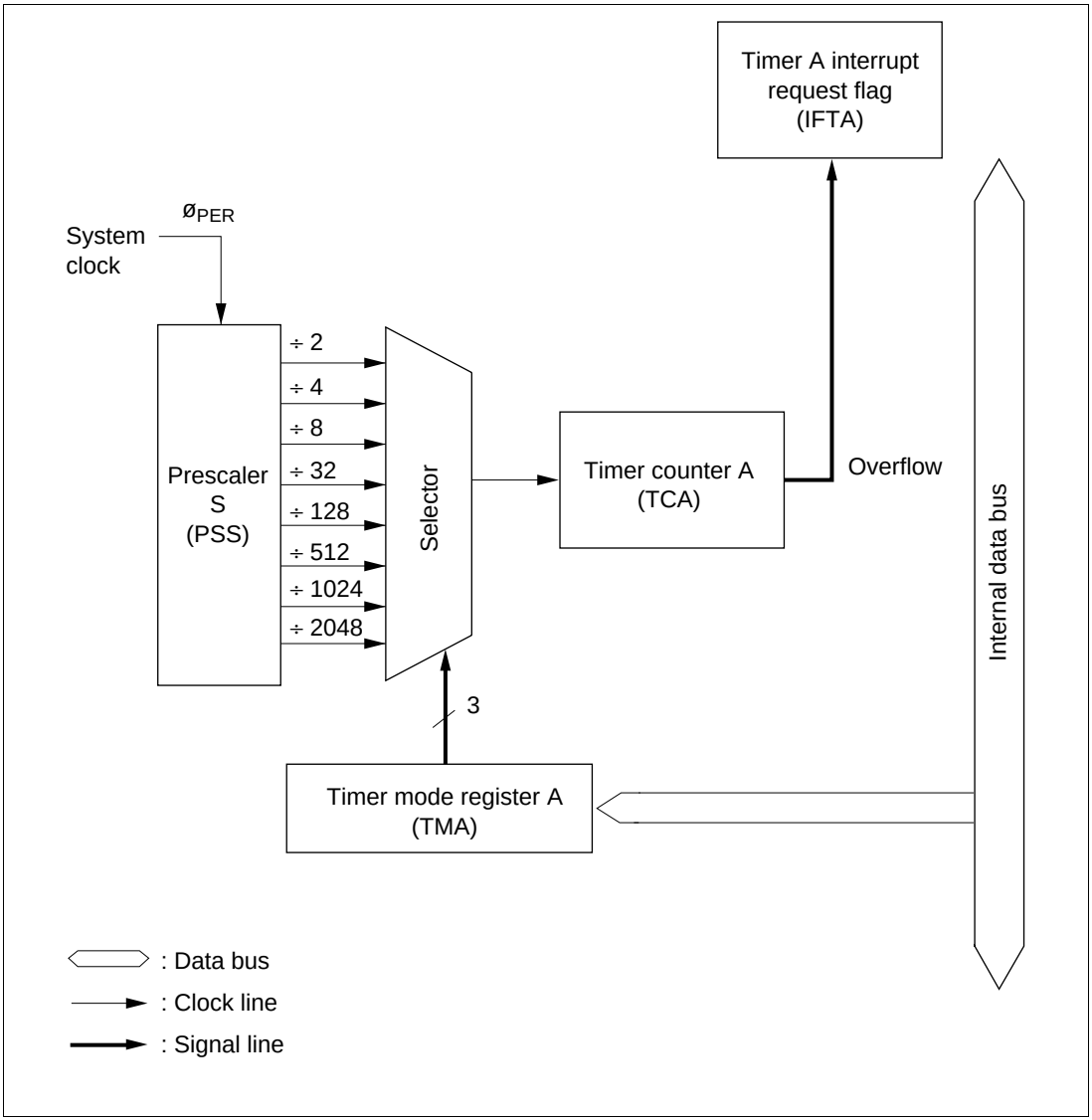


Figure 17-1 (a) Timer A Block Diagram (HD404318, HD404358, and HD404358R Series)

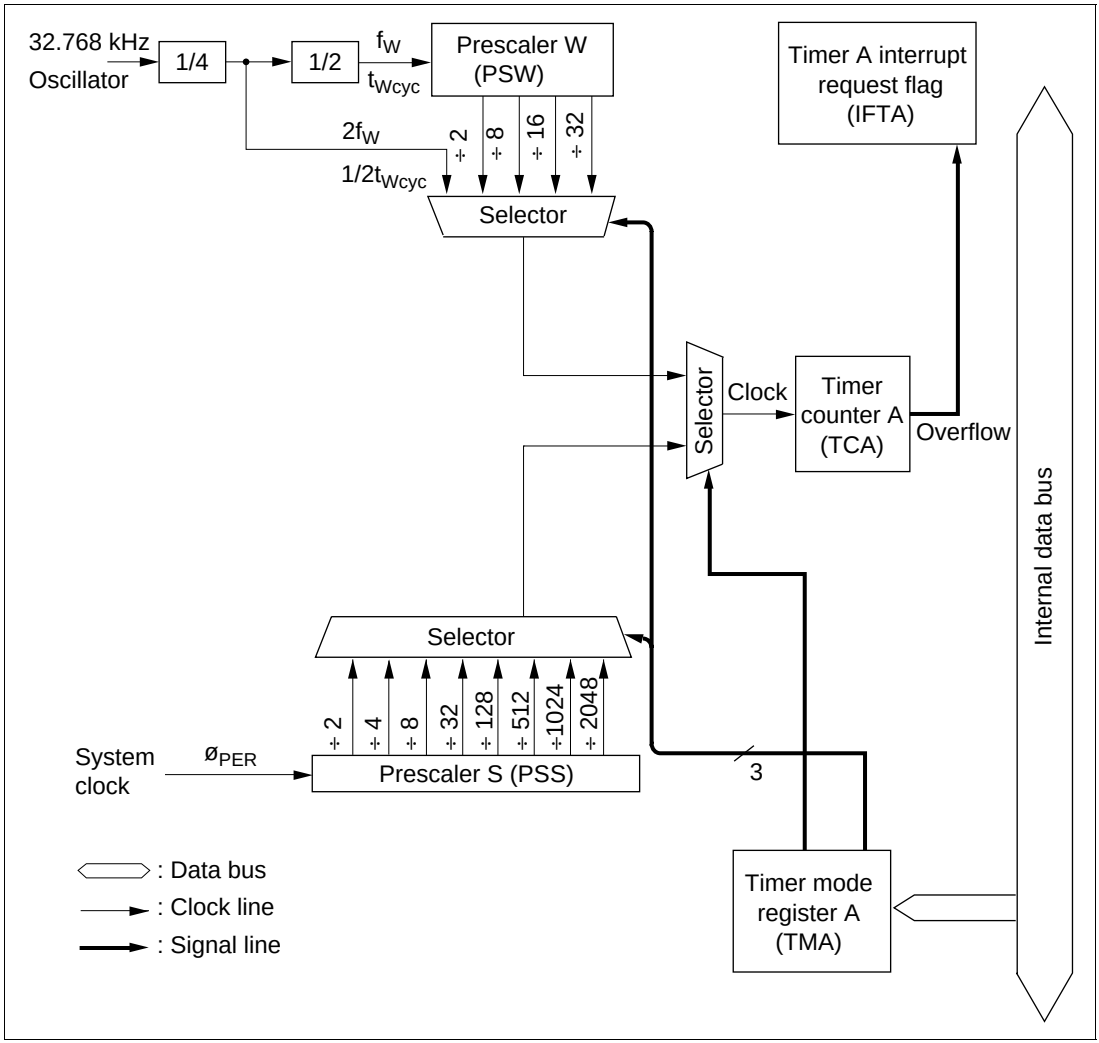


Figure 17-1 (b) Timer A Block Diagram (HD404339 and HD404369 Series)

17.1.3 Register Configuration

Table 17-1 lists the registers associated with timer A.

Table 17-1 Timer A Register Structure

Address	Register	Symbol	R/W	Initial Value
$008	Timer mode register A	TMA	W	$0
—	Timer counter A	TCA	—	$00

17.2 Register Descriptions

17.2.1 Timer Mode Register A (TMA: $008)

HD404318/HD404358/HD404358R Series

TMA is a 4-bit write-only register that selects the divisor for prescaler S, which is used as the timer A clock source.

TMA is initialized to $0 on reset and in stop mode.

Bit	3	2	1	0
	—	TMA2	TMA1	TMA0
Initial value	—	0	0	0
Read/Write	—	W	W	W

Unused

Timer A clock selection

TMA2	TMA1	TMA0	Input clock period
0	0	0	2048 t_{cyc}
		1	1024 t_{cyc}
	1	0	512 t_{cyc}
		1	128 t_{cyc}
1	0	0	32 t_{cyc}
		1	8 t_{cyc}
	1	0	4 t_{cyc}
		1	2 t_{cyc}

Note: $t_{cyc} = f_{OSC}/4$

Bits 2 to 0—Timer A Clock Selection (TMA2 to TMA0): These bits select the timer A clock source divisor.

			Description					
				Input Clock Period				
TMA2	TMA1	TMA0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
		1	PSS	$1024t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
	1	0	PSS	$512t_{cyc}$	5.12 ms	2.56 ms	1.024 ms	512 µs
		1	PSS	$128t_{cyc}$	1.28 ms	640 µs	256 µs	128 µs
1	0	0	PSS	$32t_{cyc}$	320 µs	160 µs	64 µs	32 µs
		1	PSS	$8t_{cyc}$	80 µs	40 µs	16 µs	8 µs
	1	0	PSS	$4t_{cyc}$	40 µs	20 µs	8 µs	4 µs
		1	PSS	$2t_{cyc}$	20 µs	10 µs	4 µs	2 µs

TMA is a 4-bit write-only register that selects the prescaler to be used as the timer A clock source (PSS or PSW) and the divisor used.

TMA is initialized to $0 on reset and in stop mode.

Bit	3	2	1	0
	TMA3	TMA2	TMA1	TMA0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Timer A clock selection

TMA3	TMA2	TMA1	TMA0	Prescaler	Input clock period	Mode
0	0	0	0	PSS	2048 t_{cyc} *1	Free-running timer mode
			1	PSS	1024 t_{cyc}	
		1	0	PSS	512 t_{cyc}	
			1	PSS	128 t_{cyc}	
	1	0	0	PSS	32 t_{cyc}	
			1	PSS	8 t_{cyc}	
		1	0	PSS	4 t_{cyc}	
			1	PSS	2 t_{cyc}	
1	0	0	0	PSW	32 t_{Wcyc} *2	Clock time base mode
			1	PSW	16 t_{Wcyc}	
		1	0	PSW	8 t_{Wcyc}	
			1	PSW	2 t_{Wcyc}	
	1	0	0	—	1/2 t_{Wcyc}	
			1	—	Unused	
		1	*	—	Clears PSW and TCA	

Notes: 1. $t_{cyc} = f_{OSC}/4$, $f_{OSC}/8$, $f_{OSC}/16$, or $f_{OSC}/32$
2. $t_{Wcyc} = f_X/8$

* Don't care

Bit 3—Timer A Source Prescaler Selection (TMA3): Selects PSS or PSW as the timer A clock source.

TMA3	Description	
0	PSS is used as the timer A clock source.	(initial value)
1	PSW is used as the timer A clock source.	

Bits 2 to 0—Timer A Clock Selection (TMA2 to TMA0): These bits select the timer A clock source period. The period selected depends on the combination with TMA3 as follows.

- Free-running mode

a. System Clock Divisor: 4 (SSR21, SSR20* = 00)

				Description					
					Input Clock Period				
TMA3	TMA2	TMA1	TMA0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	0	PSS	$2048t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
			1	PSS	$1024t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
		1	0	PSS	$512t_{cyc}$	5.12 ms	2.56 ms	1.024 ms	512 µs
			1	PSS	$128t_{cyc}$	1.28 ms	640 µs	256 µs	128 µs
	1	0	0	PSS	$32t_{cyc}$	320 µs	160 µs	64 µs	32 µs
			1	PSS	$8t_{cyc}$	80 µs	40 µs	16 µs	8 µs
		1	0	PSS	$4t_{cyc}$	40 µs	20 µs	8 µs	4 µs
			1	PSS	$2t_{cyc}$	20 µs	10 µs	4 µs	2 µs

Note: * System clock selection register 2 (SSR2) bits 1 and 0

b. System Clock Divisor: 8 (SSR21, SSR20* = 01)

				Description					
					Input Clock Period				
TMA3	TMA2	TMA1	TMA0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	0	PSS	$2048t_{cyc}$	40.96 ms	20.48 ms	8.192 ms	4.096 ms
			1	PSS	$1024t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
		1	0	PSS	$512t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
			1	PSS	$128t_{cyc}$	2.56 ms	1.28 ms	512 µs	256 µs
	1	0	0	PSS	$32t_{cyc}$	640 µs	320 µs	128 µs	64 µs
			1	PSS	$8t_{cyc}$	160 µs	80 µs	32 µs	16 µs
		1	0	PSS	$4t_{cyc}$	80 µs	40 µs	16 µs	8 µs
			1	PSS	$2t_{cyc}$	40 µs	20 µs	8 µs	4 µs

Note: * System clock selection register 2 (SSR2) bits 1 and 0

c. System Clock Divisor: 16 (SSR21, SSR20* = 10)

				Description					
						Input Clock Period			
TMA3	TMA2	TMA1	TMA0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	0	PSS	$2048t_{cyc}$	81.92 ms	40.96 ms	16.384 ms	8.192 ms
			1	PSS	$1024t_{cyc}$	40.96 ms	20.48 ms	8.192 ms	4.096 ms
		1	0	PSS	$512t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
			1	PSS	$128t_{cyc}$	5.12 ms	2.56 ms	1.024 ms	512 µs
	1	0	0	PSS	$32t_{cyc}$	1.28 ms	640 µs	256 µs	128 µs
			1	PSS	$8t_{cyc}$	320 µs	160 µs	64 µs	32 µs
		1	0	PSS	$4t_{cyc}$	160 µs	80 µs	32 µs	16 µs
			1	PSS	$2t_{cyc}$	80 µs	40 µs	16 µs	8 µs

Note: * System clock selection register 2 (SSR2) bits 1 and 0

d. System Clock Divisor: 32 (SSR21, SSR20* = 11)

				Description					
						Input Clock Period			
TMA3	TMA2	TMA1	TMA0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	0	PSS	$2048t_{cyc}$	163.84 ms	81.92 ms	32.768 ms	16.384 ms
			1	PSS	$1024t_{cyc}$	81.92 ms	40.96 ms	16.384 ms	8.192 ms
		1	0	PSS	$512t_{cyc}$	40.96 ms	20.48 ms	8.192 ms	4.096 ms
			1	PSS	$128t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
	1	0	0	PSS	$32t_{cyc}$	2.56 ms	1.28 ms	512 µs	256 µs
			1	PSS	$8t_{cyc}$	640 µs	320 µs	128 µs	64 µs
		1	0	PSS	$4t_{cyc}$	320 µs	160 µs	64 µs	32 µs
			1	PSS	$2t_{cyc}$	160 µs	80 µs	32 µs	16 µs

Note: * System clock selection register 2 (SSR2) bits 1 and 0

- Clock time base mode

				Description		
					Input Clock Period	
TMA3	TMA2	TMA1	TMA0	Source Prescaler	Symbol	f_x = 32.768 kHz
1	0	0	0	PSW	$32t_{Wcyc}$	7.8125 ms
			1	PSW	$16t_{Wcyc}$	3.9063 ms
		1	0	PSW	$8t_{Wcyc}$	1.9531 ms
			1	PSW	$2t_{Wcyc}$	488.28 µs
	1	0	0	—	$1/2t_{Wcyc}$	122.07 µs
			1	Unused		
		1	*	Clears PSW and TCA.		

Note: * Don't care

17.2.2 Timer Counter A (TCA)

TCA is an 8-bit increment-only counter that is incremented by the input internal clock. The input clock period is selected by the TMA register*. It is not possible to read or write TCA. When TCA overflows the timer A interrupt request flag (IFTA) is set to 1.

TCA is initialized to $00 on reset and in stop mode.

Bit	7	6	5	4	3	2	1	0
	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Counter value

Note: * HD404318/HD404358/HD404358R Series

The PSS output is selected by the TMA TMA2 to TMA0 bits. The TMA TMA3 bit is unused. The frequency of the system clock ($ø_{PER}$) divided by PSS is fixed at 1/4 the oscillator frequency ($ø_{PER} = f_{OSC}/4$).

HD404339/HD404369 Series

The PSS or PSW output is selected by the TMA TMA3 to TMA0 bits. The frequency of the system clock ($ø_{PER}$) divided by PSS can be selected to be 1/4, 1/8, 1/16, or 1/32 of the oscillator frequency, i.e., $ø_{PER} = f_{OSC}/4$, $f_{OSC}/8$, $f_{OSC}/16$, or $f_{OSC}/32$ by system clock selection register 2 (SSR2). The frequency of the subsystem clock (f_W) divided by PSW is fixed at 1/8 the oscillator frequency ($f_W = f_X/8$).

Writing 111 to bits TMA3 to TMA1 of TMA clears PSW and TCA.

17.3 Timer A Operation

17.3.1 Free-Running Timer Operation

Timer A can be used as an 8-bit free-running timer.

HD404318/HD404358/HD404358R Series

Timer A is incremented continuously immediately following a reset.

HD404339/HD404369 Series

Timer A operates as a free-running timer when the TMA TMA3 bit is set to 0. Since TCA is cleared to $00 and TMA3 is cleared to 0 on reset, timer A is incremented continuously immediately following a reset and thus functions as a free-running timer.

TCA cannot be cleared when timer A is operating as a free-running timer, i.e., when the TMA3 bit is 0.

The following describes the free-running timer operation common to the microcomputers in the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series.

Timer A operates on one of eight internal clocks output from PSS and selected by the TMA TMA2 to TMA0 bits.

Timer A overflows on the next clock input after the TCA counter reaches $FF and IFTA is set to 1. A CPU interrupt is generated if the timer A interrupt mask is 0 at that time. See section 4, “Exception Handling”, for details on interrupts.

On an overflow, the TCA value returns to $00, and TCA begins to count up once again. Thus timer A functions as an interval timer that outputs an overflow periodically every 256 input clock periods.

17.3.2 Clock Time Base Operation

HD404339/HD404369 Series

When the TMA TMA3 bit is set to 1 timer A functions as a clock time base.

The TMA TMA2 to TMA0 bits select the timer A operating clock to be one of five internal clocks: four clocks output from PSW and a clock that is not modified by PSW.

Clock time base operation generates interrupts with a precise timing by using the 32.768 kHz crystal oscillator as the base clock.

In clock time base operation (when the TMA3 bit is 1) TCA and PSW can be cleared to $00 by setting both TMA2 and TMA1 to 1.

Clock time base mode is used when switching to and clearing watch and subactive modes. See section 6, “Low Power Modes”, for details.

17.4 Interrupts

The timer A interrupt source is generated by TCA overflow.

When TCA overflows, IFTA in the interrupt control bit area is set to 1. IFTA is never cleared automatically, even if the interrupt is accepted. The interrupt handling routine should clear IFTA to 0.

The timer A interrupt can be independently enabled or disabled by IMTA in the interrupt control bit area. See section 4, “Exception Handling”, for details.

17.5 Usage Notes

Errors in the overflow period can occur if the divisor is changed during operation in time base mode. Do not change the divisor during timer operation.

Section 18 Timer B

18.1 Overview

18.1.1 Features

Timer B is an 8-bit multifunction (free-running/event counter/reload timer/input capture*) timer with the following features.

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. Timer B in the HD404344R and HD404394 Series does not support the input capture function.

HD404344R/HD404394 Series

- The timer clock can be selected from one of seven internal clocks ($2048t_{cyc}$, $512t_{cyc}$, $128t_{cyc}$, $32t_{cyc}$, $8t_{cyc}$, $4t_{cyc}$, and $2t_{cyc}$), from prescaler S (PSS), or taken from an external event input.
- An interrupt can be generated on timer counter B (TCB) overflow.

HD404318/HD404358/HD404358R/HD404339/HD404369 Series

- The timer clock can be selected from one of seven internal clocks ($2048t_{cyc}$, $512t_{cyc}$, $128t_{cyc}$, $32t_{cyc}$, $8t_{cyc}$, $4t_{cyc}$, and $2t_{cyc}$) from prescaler S (PSS), or taken from an external event input.
- An interrupt can be generated on timer counter B (TCB) overflow.
- Timer B also supports input capture operation triggered by an external event input.
- Interrupts can be generated on input capture events.

18.1.2 Block Diagram

Figure 18-1 shows the block diagram for timer B during free-running and reload timer operation.

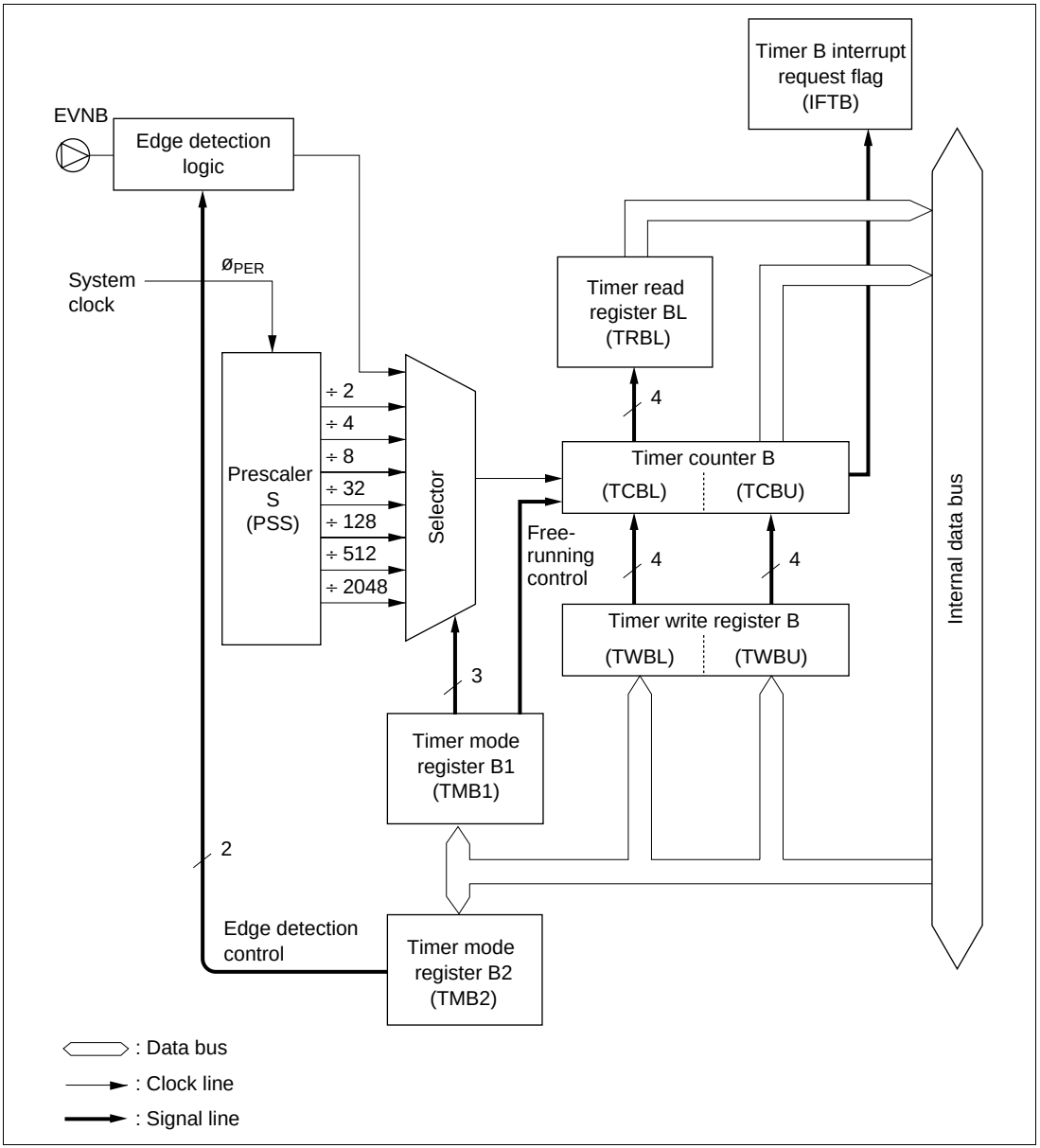


Figure 18-1 Timer B Block Diagram (Free-Running and Reload Timer)

Figure 18-2 shows the block diagram for timer B during input capture operation. (HD404318, HD404358, HD404358R, HD404339, and HD404369 Series)

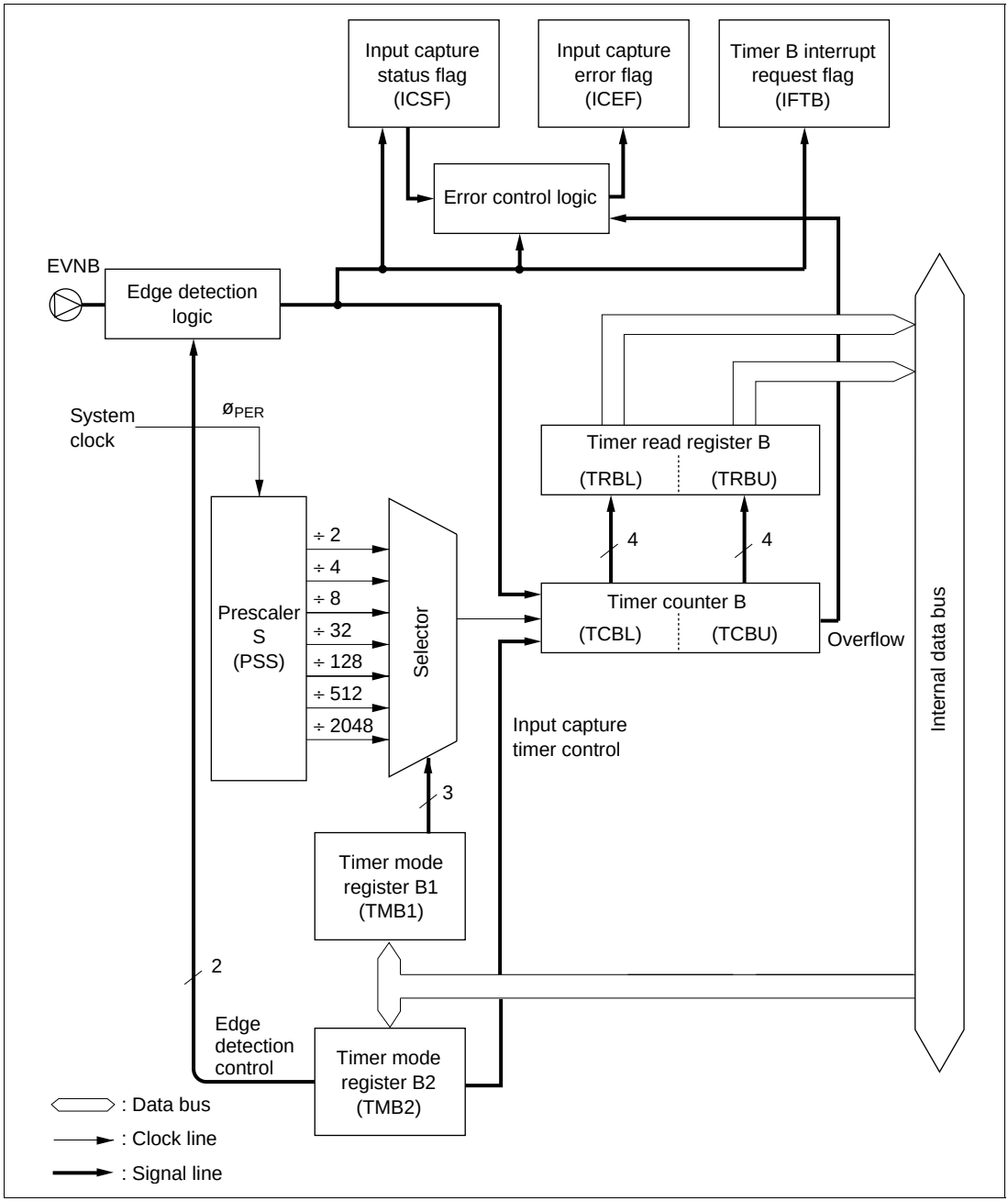


Figure 18-2 Timer B Block Diagram (HD404318, HD404358, HD404358R, HD404339, and HD404369 Series) (Input Capture Timer)

18.1.3 Timer B Pins

Table 18-1 lists the timer B pins.

Table 18-1 Timer B Pins

Pin	Symbol	I/O	Function
Timer B event input	EVNB	Input	Timer B event input and input capture timer trigger input pin*

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. Timer B in the HD404344R and HD404394 Series does not support the input capture function.

18.1.4 Register Configuration

Table 18-2 lists the registers used by timer B.

Table 18-2 Register Configuration

Address	Register	Symbol	R/W	Initial Value
$009	Timer mode register B1	TMB1	W	$0
$026	Timer mode register B2	TMB2	W	$0
—	Timer counter B	TCB	—	$00
$00A	Timer write register BL	TWBL	W	$0
$00B	Timer write register BU	TWBU	W	Undefined
$00A	Timer read register BL	TRBL	R	Undefined
$00B	Timer read register BU	TRBU	R	Undefined
$024	Port mode register B	PMRB	W	$0
$021, 0	Input capture status flag*	ICSF*	R/W*	0
$021, 1	Input capture error flag*	ICEF*	R/W*	0

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. Timer B in the HD404344R and HD404394 Series does not support the input capture function.

ICSF and ICEF are allocated in the register flag area and can be manipulated with the RAM bit manipulation instructions. A value of 1 can be written to these flags to set them, but they cannot be cleared to 0 by program instructions. See section 2, “Memory”, for details.

18.2 Register Descriptions

18.2.1 Timer Mode Register B1 (TMB1: $009)

TMB1 is a 4-bit write-only register that selects the timer B function (free-running or reload timer) and the operating clock.

TMB1 is cleared to $0 on reset and in stop mode.

Bit	3	2	1	0
	TMB13	TMB12	TMB11	TMB10
Initial value	0	0	0	0
Read/Write	W	W	W	W

Timer B clock selection

TMB12	TMB11	TMB10	Input clock source
0	0	0	2048 t_{cyc}
		1	512 t_{cyc}
	1	0	128 t_{cyc}
		1	32 t_{cyc}
1	0	0	8 t_{cyc}
		1	4 t_{cyc}
	1	0	2 t_{cyc}
		1	EVNB (external event input pin)

Note: Set port mode register B to the values shown below when the timer B clock is taken from external event input.

HD404344R and HD404394 Series: Set the PMRB0 bit to 1.
HD404318, HD404358, HD404358R, HD404339, and HD404369 Series: Set the PMRB2 bit to 1.

Timer B function selection

0	Free-running timer
1	Reload timer

Bit 3—Timer B Function Selection (TMB13): Selects the timer B function.

TMB13	Description	
0	Selects the free-running timer function.	(initial value)
1	Selects the reload timer function.	

Bits 2 to 0—Timer B Clock Selection (TMB12 to TMB10): These bits select the timer B input clock.

- Active mode

HD404344R/HD404394/HD404318/HD404358/HD404358R Series

			Description					
				Input Clock Period				
TMB12	TMB11	TMB10	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
		1	PSS	$512t_{cyc}$	5.12 ms	2.56 ms	1.024 ms	512 µs
	1	0	PSS	$128t_{cyc}$	1.28 ms	640 µs	256 µs	128 µs
		1	PSS	$32t_{cyc}$	320 µs	160 µs	64 µs	32 µs
1	0	0	PSS	$8t_{cyc}$	80 µs	40 µs	16 µs	8 µs
		1	PSS	$4t_{cyc}$	40 µs	20 µs	8 µs	4 µs
	1	0	PSS	$2t_{cyc}$	20 µs	10 µs	4 µs	2 µs
		1	—	External event input (EVNB pin)				

HD404339/HD404369 Series

1. System Clock Divisor: 4 (SSR21, SSR20* = 00)

			Description					
				Input Clock Period				
TMB12	TMB11	TMB10	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
		1	PSS	$512t_{cyc}$	5.12 ms	2.56 ms	1.024 ms	512 µs
	1	0	PSS	$128t_{cyc}$	1.28 ms	640 µs	256 µs	128 µs
		1	PSS	$32t_{cyc}$	320 µs	160 µs	64 µs	32 µs
1	0	0	PSS	$8t_{cyc}$	80 µs	40 µs	16 µs	8 µs
		1	PSS	$4t_{cyc}$	40 µs	20 µs	8 µs	4 µs
	1	0	PSS	$2t_{cyc}$	20 µs	10 µs	4 µs	2 µs
		1	—	External event input (EVNB pin)				

Note: * System clock selection register 2 (SSR2) bits 1 and 0

2. System Clock Divisor: 8 (SSR21, SSR20* = 01)

			Description				
				Input Clock Period			
TMB12	TMB11	TMB10	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	40.96 ms	20.48 ms	8.192 ms	4.096 ms
		1	PSS	$512t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
	1	0	PSS	$128t_{cyc}$	2.56 ms	1.28 ms	512 µs	256 µs
		1	PSS	$32t_{cyc}$	640 µs	320 µs	128 µs	64 µs
1	0	0	PSS	$8t_{cyc}$	160 µs	80 µs	32 µs	16 µs
		1	PSS	$4t_{cyc}$	80 µs	40 µs	16 µs	8 µs
	1	0	PSS	$2t_{cyc}$	40 µs	20 µs	8 µs	4 µs
		1	—	External event input (EVNB pin)				

Note: * System clock selection register 2 (SSR2) bits 1 and 0

3. System Clock Divisor: 16 (SSR21, SSR20* = 10)

			Description				
				Input Clock Period			
TMB12	TMB11	TMB10	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	81.92 ms	40.96 ms	16.384 ms	8.192 ms
		1	PSS	$512t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
	1	0	PSS	$128t_{cyc}$	5.12 ms	2.56 ms	1.024 ms	512 µs
		1	PSS	$32t_{cyc}$	1.28 ms	640 µs	256 µs	128 µs
1	0	0	PSS	$8t_{cyc}$	320 µs	160 µs	64 µs	32 µs
		1	PSS	$4t_{cyc}$	160 µs	80 µs	32 µs	16 µs
	1	0	PSS	$2t_{cyc}$	80 µs	40 µs	16 µs	8 µs
		1	—	External event input (EVNB pin)				

Note: * System clock selection register 2 (SSR2) bits 1 and 0

4. System Clock Divisor: 32 (SSR21, SSR20* = 11)

			Description				
				Input Clock Period			
TMB12	TMB11	TMB10	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	163.84 ms	81.92 ms	32.768 ms	16.384 ms
		1	PSS	$512t_{cyc}$	40.96 ms	20.48 ms	8.192 ms	4.096 ms
	1	0	PSS	$128t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
		1	PSS	$32t_{cyc}$	2.56 ms	1.28 ms	512 µs	256 µs
1	0	0	PSS	$8t_{cyc}$	640 µs	320 µs	128 µs	64 µs
		1	PSS	$4t_{cyc}$	320 µs	160 µs	64 µs	32 µs
	1	0	PSS	$2t_{cyc}$	160 µs	80 µs	32 µs	16 µs
		1	—	External event input (EVNB pin)				

Note: * System clock selection register 2 (SSR2) bits 1 and 0

- Subactive mode

HD404339/HD404369 Series

			Description			
				Input Clock Period		
					f_x = 32.768 kHz (in Subactive Mode)	
TMB12	TMB11	TMB10	Source Prescaler	Symbol	SSR12* = 0	SSR12* = 1
0	0	0	PSS	$2048t_{cyc}$	500 ms	250 ms
		1	PSS	$512t_{cyc}$	125 ms	62.5 ms
	1	0	PSS	$128t_{cyc}$	31.25 ms	15.625 ms
		1	PSS	$32t_{cyc}$	7.8125 ms	3.9063 ms
1	0	0	PSS	$8t_{cyc}$	1.9531 ms	976.56 µs
		1	PSS	$4t_{cyc}$	976.56 µs	488.28 µs
	1	0	PSS	$2t_{cyc}$	488.28 µs	244.14 µs
		1	PSS	—	External event input (EVNB pin)	

Note: * System clock selection register 1 (SSR1) bit 2

18.2.2 Timer Mode Register B2 (TMB2: $026)

TMB2 is a 3-bit write-only register that selects the input capture function and the EVNB pin input edge detection type.

TMB2 is initialized to $0 on reset and in stop mode.

Bit	3	2	1	0
	—	TMB22*	TMB21	TMB20
Initial value		0	0	0
Read/Write	—	W	W	W

EVNB pin edge detection selection

TMB21	TMB20	EVNB pin edge detection
0	0	No detection
	1	Falling edge detection
1	0	Rising edge detection
	1	Falling/rising edge pair detection

Input capture setting*

0	Free-running/reload timer
1	Input capture timer

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. TMB22 is unused in the HD404344R and HD404394 Series.

Bit 2—Input Capture Setting (TMB22)

HD404318/HD404358/HD404358R/HD404339/HD404369 Series

Selects the timer B function. When this bit is 0, the TMB1 TMB13 bit selects either the free-running timer or the reload timer function.

TMB22	Description	
0	Selects the free-running/reload timer function.	(initial value)
1	Selects the input capture timer function.	

Bits 1 and 0—EVNB Pin Edge Detection Selection (TMB21, TMB20)

TMB21	TMB20	Description	
0	0	No edges are detected on the EVNB pin input.	(initial value)
	1	Falling edges are detected on the EVNB pin input.	
1	0	Rising edges are detected on the EVNB pin input.	
	1	Falling/rising edge pairs are detected on the EVNB pin input.	

18.2.3 Timer Counter B (TCB)

TCB is an 8-bit up counter that is incremented by the input internal clock.

Bit	7	6	5	4	3	2	1	0
	TCB7	TCB6	TCB5	TCB4	TCB3	TCB2	TCB1	TCB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Counter value

The TCB input clock is selected by the TMB1 TMB12 to TMB10 bits.

The value in TCB can be read by reading out the TRBL/U pair, and TCB can be written by writing to the TWBL/U pair.

The timer B interrupt request flag (IFTB) is set to 1 when TCB overflows.

If the free-running timer function is selected for timer B (TMB13 = 0) at this time, TCB will be cleared to $00 and start to count again. If the reload timer function is selected for timer B (TMB13 = 1), the value in the TWBL/U pair will be written to TCB and TCB will start counting from that value.

TCB is initialized to $00 on reset and in stop mode.

18.2.4 Timer Write Register TWBL/U (TWBL: $00A, TWBU: $00B)

The TWBL/U pair form an 8-bit write-only register in which TWBL is the upper digit and TWBU is the lower digit. The TWBL/U pair is used to set the initial value of TCB, i.e., to set the reload value in reload operation.

	Bit	3	2	1	0
TWBU		TWBU3	TWBU2	TWBU1	TWBU0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	W	W	W	W

	Bit	3	2	1	0
TWBL		TWBL3	TWBL2	TWBL1	TWBL0
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

Data must be written in the order TWBL first and then TWBU. When TWBL is written, the value in TCB does not change. Next, when TWBU is written, the value in TWBU is transferred to the upper digit of TCB and the value in TWBL is transferred to the lower digit of TCB.

When the TWBL/U pair is being written for the second or later time and there is no need to change the TWBL reload value, timer B can be initialized by writing only TWBU.

TWBL is initialized to $0 and TWBU is undefined on reset and in stop mode.

18.2.5 Timer Read Register TRBL/U (TRBL: $00A, TRBU: $00B)

The TRBL/U pair form an 8-bit read-only register in which TRBL and TRBU directly read out the upper and lower digits respectively of TCB in timer B operating modes other than input capture operation*. That is, the TRBL/U pair is used to read out the value in TCB.

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. Timer B in the HD404344R and HD404394 Series does not support the input capture function.

	Bit	3	2	1	0
TRBU		TRBU3	TRBU2	TRBU1	TRBU0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	R	R	R	R

	Bit	3	2	1	0
TRBL		TRBL3	TRBL2	TRBL1	TRBL0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	R	R	R	R

Data must be read in the order TRBU first and then TRBL. When TRBU is read out, the current value of the upper digit in TCB is returned and at the same time the value of the lower digit is latched into TRBL. Then, reading out the value in TRBL returns that latched value. This means that the exact value of TCB at the point TRBU was read is acquired.

In input capture operation in HD404318, HD404358, HD404358R, HD404339, and HD404369 Series microcomputers, TRBL and TRBU form an 8-bit register that latches the value in TCB, and can be read in any order.

TRBL and TRBU are undefined on reset and in stop mode.

18.2.6 Port Mode Register B (PMRB: $024)

HD404344R/HD404394 Series

PMRB is a 2-bit write-only register whose PMRB0 bit switches an I/O pin for use as an event counter.

This section describes the PMRB0 bit. See the “Port Mode Register B” item in sections 7 and 8, “I/O Ports”, for details on the switching performed by the PMRB3 bit.

Bit	3	2	1	0
	PMRB3	—	—	PMRB0
Initial value	0	—	—	0
Read/Write	W	—	—	W

Unused

$D_0/\overline{INT_0}$/EVNB pin function switch

0	D_0 I/O pin
1	$\overline{INT_0}$/EVNB input pin

$D_4/\overline{STOPC}$ pin function switch

0	D_4 I/O pin
1	$\overline{STOPC}$ input pin

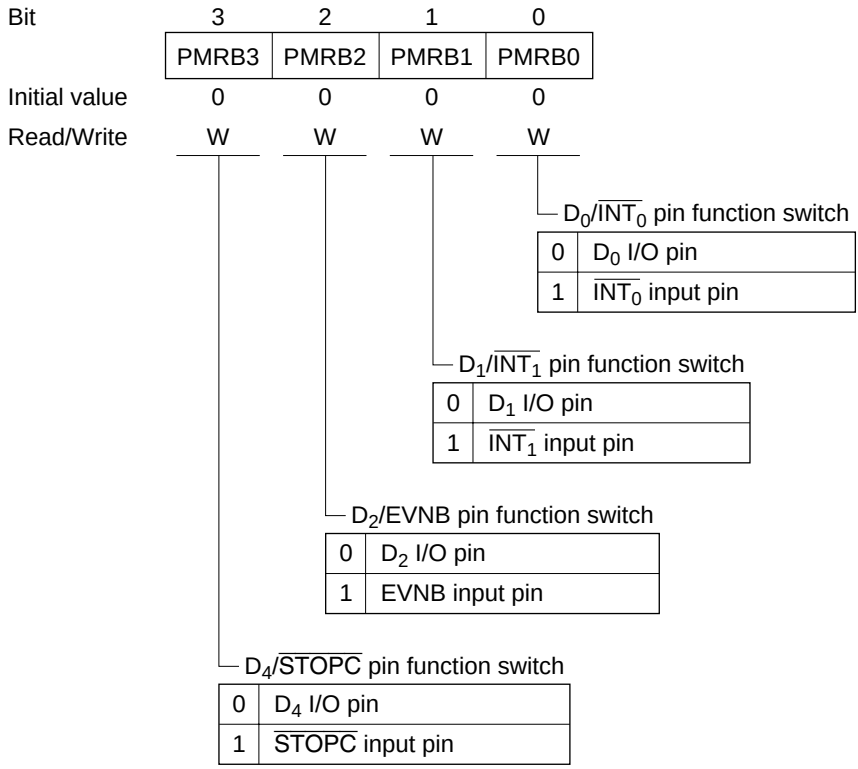
Bit 0—$D_0/\overline{INT_0}$/EVNB Pin Function Switch (PMRB0): Selects whether the $D_0/\overline{INT_0}$/EVNB pin functions as the D0 I/O pin or as the external interrupt 0/timer B event ($\overline{INT_0}$/EVNB) input pin.

PMRB0	Description	
0	The $D_0/\overline{INT_0}$/EVNB pin functions as the D_0 I/O pin.	(initial value)
1	The D0/$\overline{INT_0}$/EVNB pin functions as the $\overline{INT_0}$/EVNB input pin.	

Set the PMRB0 bit to 1 when this pin is to be used as the EVNB pin. Also, set the TMB1 TMB12 to TMB10 bits to 111, and select the edge detection type with the TMB2 TMB21 and TMB20 bits. Note that the $\overline{INT_0}$ interrupt should normally be masked at this time. See section 18.2.1, “Timer Mode Register B1 (TMB1)”, for more details.

PMRB is a 4-bit write-only register whose PMRB2 bit switches an I/O pin to be used for event counting or input capture.

This section describes the PMRB2 bit. See the “Port Mode Register” items in sections 9 to 12, “I/O Ports”, for details on the switching performed by the PMRB3, PMRB1, and PMRB0 bits.



Bit 2—D_2/EVNB Pin Function Switch (PMRB2): Selects whether the D_2/EVNB pin functions as the D_2 I/O pin or as the timer B event input pin (EVNB).

PMRB2	Description	
0	The D_2/EVNB pin functions as the D_2 I/O pin.	(initial value)
1	The D_2/EVNB pin functions as the EVNB input pin.	

Set the PMRB0 bit to 1 when this pin is to be used as the EVNB pin. Also, set the TMB1 TMB12 to TMB10 bits to 111, and select the edge detection type with the TMB2 TMB21 and TMB20 bits. See section 18.2.1, “Timer Mode Register B1 (TMB1)”, for more details.

18.2.7 Input Capture Status Flag (ICSF: $021, 0)

HD404318/HD404358/HD404358R/HD404339/HD404369 Series

ICSF is set to 1 when the edge specified by bits TMB21 to TMB20 is detected on the EVNB pin in input capture operation, i.e., when TMB22 is set to 1.

ICSF can be read and written (only 0 can be written) only by the RAM bit manipulation instructions.

ICSF is cleared to 0 on reset and in stop mode.

ICSF	Description
0	Indicates that no edge was detected in the input capture trigger input (EVNB). (initial value)
1	Indicates that an edge was detected in the input capture trigger input (EVNB).

18.2.8 Input Capture Error Flag (ICEF: $021, 1)

HD404318/HD404358/HD404358R/HD404339/HD404369 Series

ICEF is set to 1 if the next input capture event is detected when ICSF is set to 1, or if TCB overflows when ICSF is set to 1.

ICEF can be read and written (only 0 can be written) only by the RAM bit manipulation instructions.

ICEF is cleared to 0 on reset and in stop mode.

ICEF	Description
0	Indicates that no input capture operating error has occurred. (initial value)
1	Indicates that either the next input capture trigger was detected with ICSF = 1, or that TCB overflowed with ICSF = 1.

18.3 Timer B Operation

Timer B is an 8-bit multifunction timer. Table 18-3 lists the functions supported for each series in the HMCS43XX family. The functions are selected by timer mode register B.

Table 18-3 Timer B Functions

	Series	
Function	**HD404344R/HD404394**	**HD404318/HD404358/HD404358R/ HD404339/HD404369**
Free-running timer	◯	◯
Reload timer	◯	◯
External event counter	◯	◯
Input capture timer	—	◯

18.3.1 Free-Running Timer

Timer B can be used as an 8-bit free-running timer.

When the TMB TMB22* bit is 0 and furthermore the TMB1 TMB13 bit is 0, timer B operates as an 8-bit free-running timer.

Since TCB is cleared to $00 and the TMB22* and TMB13 bits are cleared to 0 on reset, timer B is incremented continuously as a free-running timer immediately following a reset. The timer B operating clock is selected by TMB TMB12 to TMB10 to be one of seven internal clocks output from PSS.

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. This bit is unused in the HD404344R and HD404394 Series.

On the clock input after the count value in TCB reaches $FF, timer B overflows and IFTB is set to 1. If the timer B interrupt mask (IMTB) is 0 at this time, a CPU interrupt is generated. See section 4, “Exception Handling”, for details on interrupts.

On an overflow, the TCB count returns to $00 and timer B begins to count again.

18.3.2 Reload Timer Operation

When the TMB TMB22* bit is 0 and furthermore the TMB1 TMB13 bit is 1, timer B operates as an 8-bit reload timer. When a reload value is loaded into the TWBL/U pair, that value is loaded into TCB and timer B begins to count up from that value.

On the clock input after the count value in TCB reaches $FF, timer B overflows, the value in the TWBL/U pair is loaded into TCB, and timer B continues counting from that value. This means that the timer B overflow period can be set to be any value in the range 1 to 256 times the input clock period.

The operating clock and interrupt operation during reload timer operation are identical to those for free-running timer operation.

When a new reload value is loaded into the TWBL/U pair that value is immediately written to TCB.

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The TMB22 bit is unused in the HD404344R and HD404394 Series.

18.3.3 External Event Counter Operation

When the TMB1 TMB12 to TMB10 bits are set to 111, TCB is incremented by the EVNB pin input signal edges specified by the TMB21 and TMB20 bits.

Other aspects of timer B operation in this mode are identical to either free-running or reload timer operation depending on the setting of the TMB1 TMB13 bit.

18.3.4 Input Capture Timer Operation

HD404318/HD404358/HD404358R/HD404339/HD404369 Series

The input capture timer function measures the period between EVNB input pin edge detection events. An internal clock must be selected as the TCB operating clock when timer B is used as an input capture timer.

Timer B operates as an input capture timer when the TMB2 TMB22 bit is set to 1. TCB will be cleared to $00 at that point.

The TMB2 TMB21 and TMB20 bits select the edge detection event type, which can be either a falling edge, a rising edge, or a falling/rising edge pair on the EVNB input pin.

When an edge is detected on the EVNB pin, the value of TCB at that time is written to the TRBL/U pair and IFTB and ICSF are both set to 1. At the same time TCB is cleared to $00 and continues to count up from $00.

ICEF is set to 1 if the next edge is detected when ICSF is set to 1 or if TCB overflows.

When timer B is used as an input capture timer (when the TMB22 bit is 1) TRBL and TRBU can be read in any order. (See figure 18-2.)

18.4 Interrupts

Timer B interrupts are generated on TCB overflow and on EVNB pin edge detections during input capture timer operation*.

When an interrupt is generated, IFTB in the interrupt control bit area is set to 1.

Timer B in the HD404344R and HD404394 Series does not support the input capture function. IFTB is never cleared automatically, even if the interrupt is accepted. The interrupt handling routine should clear IFTB to 0.

The timer B interrupt can be independently enabled or disabled by IMTB in the interrupt control bit area.

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. Timer B in the HD404344R and HD404394 Series does not support the input capture function.

18.5 Usage Notes

Keep the following points in mind when using timer B.

- Be sure to write TWBL first and then TWBU when using the TWBL/U pair to set the TCB reload value or to initialize TCB. The value in the TWBL/U pair is written to TCB at the point that TWBU is written. Thus if TWBL has been set and only the value in the upper digit is to be changed, it is only necessary to write TWBU.
- Be sure to read TRBU first and then TRBL when reading the TCB value using the TRBL/U pair. The value in the lower digit of TCB is latched into TRBL when TRBU is read. Thus reading TRBL returns the value of the TCB lower digit at the point TRBU was last read. However, the TRBL/U pair can be read in any order during input capture timer operation.
- When changing the value of TMB1, the new value becomes valid two instructions after the execution of the instruction that wrote TMB1. Therefore it is necessary for programs that initialize timer B (set the reload value or initialize TCB) by writing to the TWBL/U pair to perform this initialization only after the mode changed by TMB1 has become valid.
- When detection of falling/rising edge pairs on the EVNB pin is selected by the TMB2 setting, the falling edge and the rising edge must be separated by at least $2t_{cyc}$.

Section 19 Timer C

19.1 Overview

19.1.1 Features

Timer C is an 8-bit multifunction timer (free-running/reload timer) with the following features.

- The timer clock can be selected from one of eight internal clocks ($2048t_{cyc}$, $1024t_{cyc}$, $512t_{cyc}$, $128t_{cyc}$, $32t_{cyc}$, $8t_{cyc}$, $4t_{cyc}$, and $2t_{cyc}$), from prescaler S (PSS).
- Timer C can be used as a watchdog timer.
- Timer C can be used to generate waveform (PWM) output.
- An interrupt can be generated on timer counter C (TCC) overflow.

19.1.2 Block Diagram

Figure 19-1 shows the block diagram for timer C.

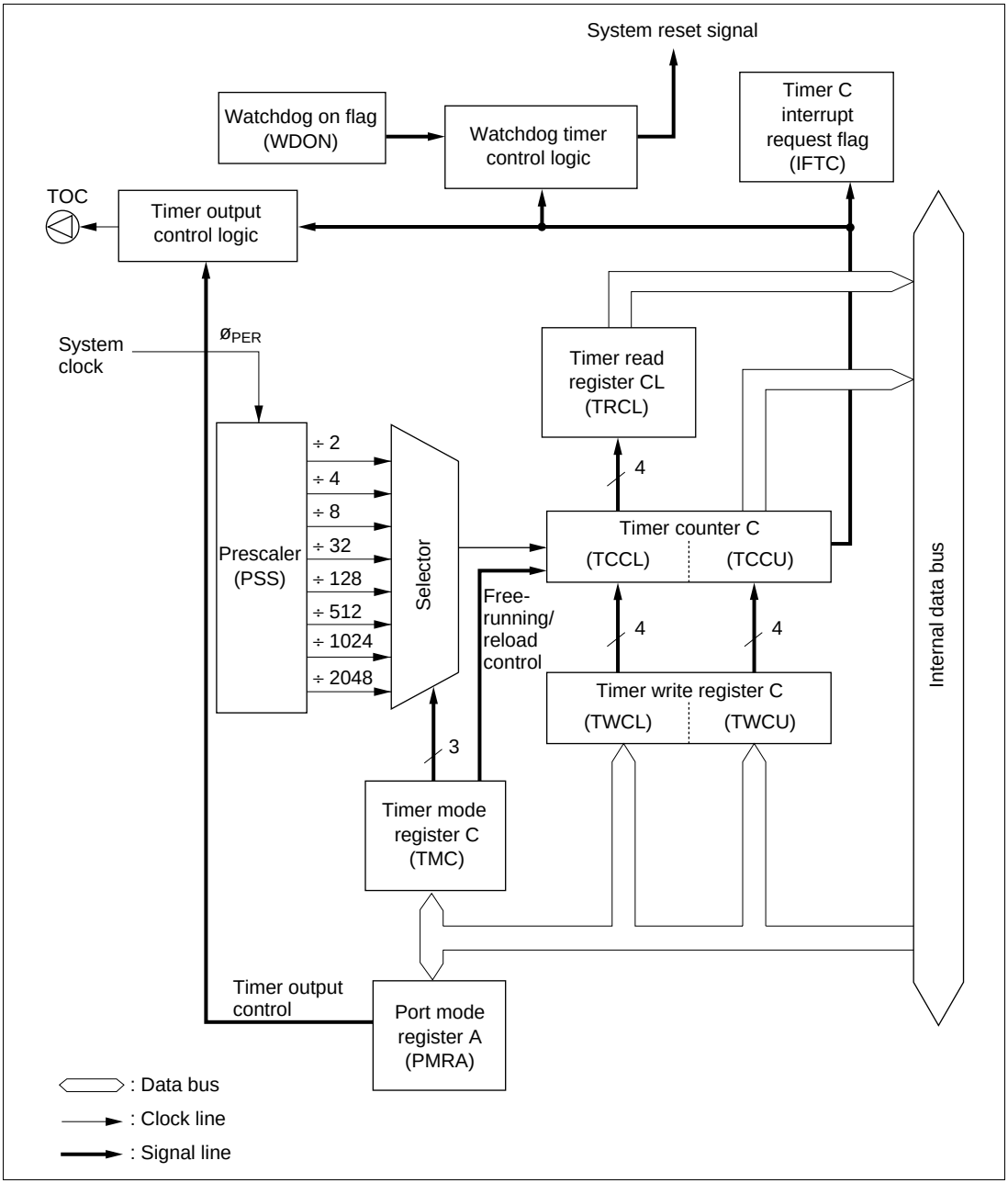


Figure 19-1 Timer C Block Diagram

19.1.3 Timer C Pins

Table 19-1 lists the timer C pins.

Table 19-1 Timer C Pins

Pin	Symbol	I/O	Function
Timer C output	TOC	Output	Timer C output pin

19.1.4 Register Configuration

Table 19-2 lists the registers used by timer C.

Table 19-2 Register Configuration

Address	Register	Symbol	R/W	Initial Value
$00D	Timer mode register C	TMC	W	$0
$004	Port mode register A	PMRA	W	$0
—	Timer counter C	TCC	—	$00
$00E	Timer write register CL	TWCL	W	$0
$00F	Timer write register CU	TWCU	W	Undefined
$00E	Timer read register CL	TRCL	R	Undefined
$00F	Timer read register CU	TRCU	R	Undefined
$020, 1	Watchdog on flag	WDON*	R/W*	0

Note: * WDON is allocated in the register flag area and can be manipulated only with the RAM bit manipulation instructions. A value of 1 can be written to set this flag, but it cannot be cleared to 0 by program instructions. See section 2, “Memory”, for details.

19.2 Register Descriptions

19.2.1 Timer Mode Register C (TMC: $00D)

TMC is a 4-bit write-only register that selects the timer C function (free-running or reload timer) and the operating clock.

TMC is cleared to $0 on reset and in stop mode.

Bit	3	2	1	0
	TMC3	TMC2	TMC1	TMC0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Timer C clock selection

TMC2	TMC1	TMC0	Input clock cource
0	0	0	2048 t_{cyc}
		1	1024 t_{cyc}
	1	0	512 t_{cyc}
		1	128 t_{cyc}
1	0	0	32 t_{cyc}
		1	8 t_{cyc}
	1	0	4 t_{cyc}
		1	2 t_{cyc}

Timer C function selection

0	Free-running timer
1	Reload timer

Bit 3—Timer C Function Selection (TMC3): Selects the timer C function.

TMC3	Description	
0	Selects the free-running timer function.	(initial value)
1	Selects the reload timer function.	

Bits 2 to 0—Timer C Clock Selection (TMC2 to TMC0): These bits select the timer C input clock.

- Active mode

HD404344R/HD404394/HD404318/HD404358/HD404358R Series

			Description					
				Input Clock Period				
TMC2	TMC1	TMC0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
		1	PSS	$1024t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
	1	0	PSS	$512t_{cyc}$	5.12 ms	2.56 ms	1.024 ms	512 µs
		1	PSS	$128t_{cyc}$	1.28 ms	640 µs	256 µs	128 µs
1	0	0	PSS	$32t_{cyc}$	320 µs	160 µs	64 µs	32 µs
		1	PSS	$8t_{cyc}$	80 µs	40 µs	16 µs	8 µs
	1	0	PSS	$4t_{cyc}$	40 µs	20 µs	8 µs	4 µs
		1	PSS	$2t_{cyc}$	20 µs	10 µs	4 µs	2 µs

HD404339/HD404369 Series

1. System Clock Divisor: 4 (SSR21, SSR20* = 00)

			Description					
				Input Clock Period				
TMC2	TMC1	TMC0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
		1	PSS	$1024t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
	1	0	PSS	$512t_{cyc}$	5.12 ms	2.56 ms	1.024 ms	512 µs
		1	PSS	$128t_{cyc}$	1.28 ms	640 µs	256 µs	128 µs
1	0	0	PSS	$32t_{cyc}$	320 µs	160 µs	64 µs	32 µs
		1	PSS	$8t_{cyc}$	80 µs	40 µs	16 µs	8 µs
	1	0	PSS	$4t_{cyc}$	40 µs	20 µs	8 µs	4 µs
		1	PSS	$2t_{cyc}$	20 µs	10 µs	4 µs	2 µs

Note: * System clock selection register 2 (SSR2) bits 1 and 0

2. System Clock Divisor: 8 (SSR21, SSR20* = 01)

			Description				
				Input Clock Period			
TMC2	TMC1	TMC0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	40.96 ms	20.48 ms	8.192 ms	4.096 ms
		1	PSS	$1024t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
	1	0	PSS	$512t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
		1	PSS	$128t_{cyc}$	2.56 ms	1.28 ms	512 µs	256 µs
1	0	0	PSS	$32t_{cyc}$	640 µs	320 µs	128 µs	64 µs
		1	PSS	$8t_{cyc}$	160 µs	80 µs	32 µs	16 µs
	1	0	PSS	$4t_{cyc}$	80 µs	40 µs	16 µs	8 µs
		1	PSS	$2t_{cyc}$	40 µs	20 µs	8 µs	4 µs

Note: * System clock selection register 2 (SSR2) bits 1 and 0

3. System Clock Divisor: 16 (SSR21, SSR20* = 10)

			Description				
				Input Clock Period			
TMC2	TMC1	TMC0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	81.92 ms	40.96 ms	16.384 ms	8.192 ms
		1	PSS	$1024t_{cyc}$	40.96 ms	20.48 ms	8.192 ms	4.096 ms
	1	0	PSS	$512t_{cyc}$	20.48 ms	10.24 ms	4.096 ms	2.048 ms
		1	PSS	$128t_{cyc}$	5.12 ms	2.56 ms	1.024 ms	512 µs
1	0	0	PSS	$32t_{cyc}$	1.28 ms	640 µs	256 µs	128 µs
		1	PSS	$8t_{cyc}$	320 µs	160 µs	64 µs	32 µs
	1	0	PSS	$4t_{cyc}$	160 µs	80 µs	32 µs	16 µs
		1	PSS	$2t_{cyc}$	80 µs	40 µs	16 µs	8 µs

Note: * System clock selection register 2 (SSR2) bits 1 and 0

4. System Clock Divisor: 32 (SSR21, SSR20* = 11)

			Description				
				Input Clock Period			
TMC2	TMC1	TMC0	Source Prescaler	Symbol	f_{osc} = 400 kHz	f_{osc} = 800 kHz	f_{osc} = 2 MHz	f_{osc} = 4 MHz
0	0	0	PSS	$2048t_{cyc}$	163.84 ms	81.92 ms	32.768 ms	16.384 ms
		1	PSS	$1024t_{cyc}$	81.92 ms	40.96 ms	16.384 ms	8.192 ms
	1	0	PSS	$512t_{cyc}$	40.96 ms	20.48 ms	8.192 ms	4.096 ms
		1	PSS	$128t_{cyc}$	10.24 ms	5.12 ms	2.048 ms	1.024 ms
1	0	0	PSS	$32t_{cyc}$	2.56 ms	1.28 ms	512 µs	256 µs
		1	PSS	$8t_{cyc}$	640 µs	320 µs	128 µs	64 µs
	1	0	PSS	$4t_{cyc}$	320 µs	160 µs	64 µs	32 µs
		1	PSS	$2t_{cyc}$	160 µs	80 µs	32 µs	16 µs

Note: * System clock selection register 2 (SSR2) bits 1 and 0

- Subactive mode

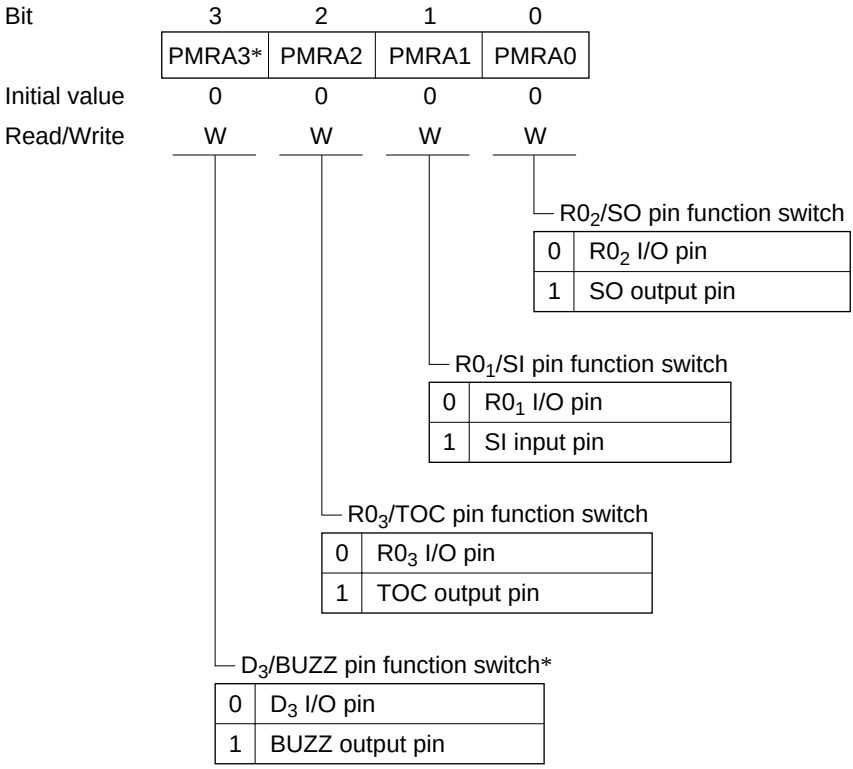
HD404339/HD404369 Series

			Description			
				Input Clock Period		
					f_x = 32.768 kHz	
TMC2	TMC1	TMC0	Source Prescaler	Symbol	SSR12* = 0	SSR12* = 1
0	0	0	PSS	$2048t_{cyc}$	500 ms	250 ms
		1	PSS	$1024t_{cyc}$	250 ms	125 ms
	1	0	PSS	$512t_{cyc}$	125 ms	62.5 ms
		1	PSS	$128t_{cyc}$	31.25 ms	15.625 ms
1	0	0	PSS	$32t_{cyc}$	7.8125 ms	3.9063 ms
		1	PSS	$8t_{cyc}$	1.9531 ms	976.56 µs
	1	0	PSS	$4t_{cyc}$	976.56 µs	488.28 µs
		1	PSS	$2t_{cyc}$	488.28 µs	244.14 µs

Note: * System clock selection register 1 (SSR1) bit 2

19.2.2 Port Mode Register A (PMRA: $004)

PMRA is a 4-bit write-only register whose PMRA2 bit switches the $R0_3$/TOC pin function. This section describes the PMRA2 bit. See sections 20.2.4 and 21.2.1, “Port Mode Register A (PMRA)”, for details on the PMRA3, PMRA1, and PMRA0 bits.



Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The PMRA3 bit is unused in the HD404344R and HD404394 Series.

Bit 2—$R0_3$/TOC Pin Function Switch (PMRA2): Selects whether the $R0_3$/TOC pin functions as the $R0_3$ I/O pin or as the timer C output pin (TOC).

PMRA2	Description	
0	The $R0_3$/TOC pin functions as the $R0_3$ I/O pin.	(initial value)
1	The $R0_3$/TOC pin functions as the TOC output pin.	

19.2.3 Timer Counter C (TCC)

TCC is an 8-bit up counter that is incremented by the input internal clock.

Bit	7	6	5	4	3	2	1	0
	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	—	—	—	—

Counter value

The TCC input clock is selected by the TMC TMC2 to TMC0 bits.

The value in TCC can be read by reading out the TRCL/U pair, and TCC can be written by writing to the TWCL/U pair.

The timer C interrupt request flag (IFTC) is set to 1 when TCC overflows.

If the free-running timer function is selected for timer C (TMC3 = 0) at this time, TCC will be cleared to $00 and start to count again. If the reload timer function is selected for timer C (TMC3 = 1), the value in the TWCL/U pair will be written to TCC and TCC will start counting from that value.

TCC is initialized to $00 on reset and in stop mode.

19.2.4 Timer Write Register TWCL/U (TWCL: $00E, TWCU: $00F)

The TWCL/U pair form an 8-bit write-only register in which TWCL is the lower digit and TWCU is the upper digit. The TWCL/U pair is used to set the initial value of TCC, i.e., to set the reload value in reload operation.

	Bit	3	2	1	0
TWCU		TWCU3	TWCU2	TWCU1	TWCU0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	W	W	W	W

	Bit	3	2	1	0
TWCL		TWCL3	TWCL2	TWCL1	TWCL0
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

Data must be written in the order TWCL first and then TWCU. When TWCL is written, the value in TCC does not change. Next, when TWCU is written, the value in TWCU is transferred to the upper digit of TCC and the value in TWCL is transferred to the lower digit of TCC.

When the TWCL/U pair is being written for the second or later time and there is no need to change the TWCL reload value, timer C can be initialized by writing only TWCU.

TWCL is initialized to $0 and TWCU is undefined on reset and in stop mode.

19.2.5 Timer Read Register TRCL/U (TRCL: $00E, TRCU: $00F)

The TRCL/U pair form an 8-bit read-only register in which TRCL and TRCU directly read out the lower and upper digits respectively of TCC. That is, the TRCL/U pair is used to read out the value in TCC.

	Bit	3	2	1	0
TRCU		TRCU3	TRCU2	TRCU1	TRCU0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	R	R	R	R

	Bit	3	2	1	0
TRCL		TRCL3	TRCL2	TRCL1	TRCL0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	R	R	R	R

Data must be read in the order TRCU first and then TRCL. When TRCU is read out, the current value of the upper digit in TCC is returned and at the same time the value of the lower digit is latched into TRCL. Then, reading out the value in TRCL returns that latched value. This means that the exact value of TCC at the point TRCU was read is acquired.

TRCL and TRCU are undefined on reset and in stop mode.

19.2.6 Watchdog On Flag (WDON: $020, 1)

WDON selects whether timer C functions as a watchdog timer. WDON is allocated in the register flag area and can only by manipulated by the RAM bit manipulation instructions. Only a value of 1 can be written to this flag. It cannot be cleared to 0 by program instructions.

WDON is cleared to 0 on reset and in stop mode.

WDON	Description
0	Timer C functions normally. (initial value)
1	Timer C functions as a watchdog timer. When timer C overflows the system goes to the reset state and reset exception handling begins.

19.3 Timer C Operation

Timer C is an 8-bit multifunction timer with the following functions.

- Free-running timer
- Reload timer
- PWM output
- Watchdog timer

19.3.1 Free-Running Timer Operation

When the TMC TMC3 bit is 0, timer C operates as an 8-bit free-running timer.

Since TCC is cleared to $00 and the TMC3 bit is cleared to 0 on reset, timer C is incremented continuously as a free-running timer immediately following a reset. The timer C operating clock is selected by TMC TMC2 to TMC0 to be one of eight internal clocks output from PSS.

On the clock input after the count value in TCC reaches $FF, timer C overflows and IFTC is set to 1. If the timer C interrupt mask (IMTC) is 0 at this time, a CPU interrupt is generated. See section 4, “Exception Handling”, for details on interrupts.

On an overflow, the TCC count returns to $00 and timer C begins to count again.

19.3.2 Reload Timer Operation

When the TMC TMC3 bit is 1, timer C operates as an 8-bit reload timer. When a reload value is loaded into the TWCL/U pair, that value is loaded into TCC and timer C begins to count up from that value.

On the clock input after the count value in TCC reaches $FF, timer C overflows, the value in the TWCL/U pair is loaded into TCC, and timer C continues counting from that value. This means that the timer C overflow period can be set to be any value in the range 1 to 256 times the input clock period.

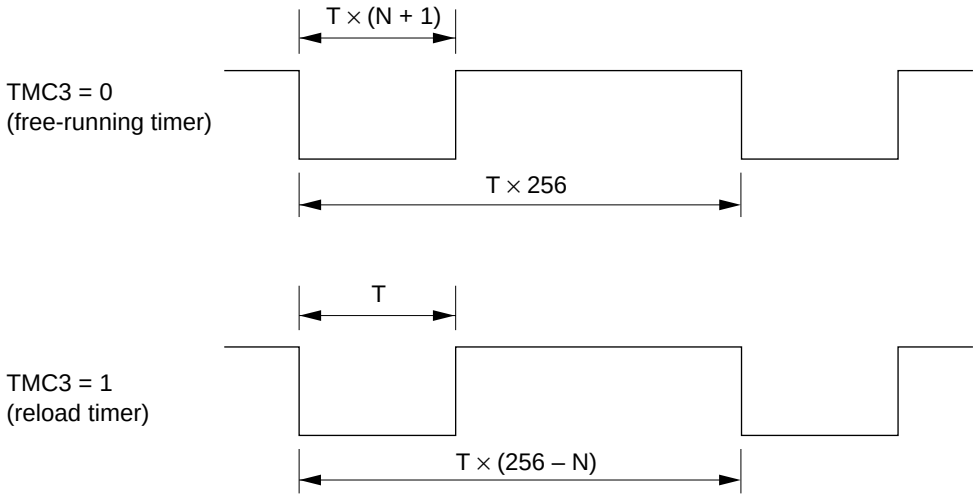
The operating clock and interrupt operation during reload timer operation are identical to those for free-running timer operation.

When a new reload value is loaded into the TWCL/U pair that value is immediately written to TCC.

19.3.3 PWM Output Operation

When the PMRA PMRA2 bit is set to 1, the $R0_3$/TOC pin functions as the TOC output pin and timer C generates a PWM output signal.

PWM output operation is a function that generates a variable duty pulse output. The output waveform is controlled by the contents of TMC and the TWCL/U pair as shown in figure 19-2.



Note: T: The period of the timer counter C (TCC) input clock. Controlled by timer mode register C.
N: The value in the TWCL/U pair. When N is 255 the PWM output will be a constant low level signal.

Figure 19-2 PWM Output Waveform

19.3.4 Watchdog Timer Operation

When WDON is set to 1 timer C functions as a watchdog timer. A watchdog timer is used to detect program runaway.

In watchdog timer operation, when timer C overflows the system goes to the reset state and reset exception handling begins. Therefore, the application program must reset TCC before its value becomes $FF so that overflows do not occur in normal operation.

19.4 Interrupts

The timer C interrupt is generated on TCC overflow.

When TCC overflows, IFTC in the interrupt control bit area is set to 1. IFTC is never cleared automatically, even if the interrupt is accepted. The interrupt handling routine should clear IFTC to 0.

The timer C interrupt can be independently enabled or disabled by IMTC in the interrupt control bit area.

19.5 Usage Notes

Keep the following points in mind when using timer C.

- Be sure to write TWCL first and then TWCU when using the TWCL/U pair to initialize TCC. The value in the TWCL/U pair is written to TCC at the point that TWCU is written. Thus if TWCL has been set and only the value in the upper digit is to be changed, it is only necessary to write TWCU.

  However, when using PWM output with the reload timer setting (i.e., with the PMRA2 bit set to 1 and the TMC3 bit set to 0) in HD404358, HD404358R, and HD404369 Series microcomputers, after the TWCL/U pair has been written, the contents of the TWCL/U pair are written to TCC when TCC overflows. Also, if only the upper digit needs to be changed, first write TWCL and then write TWCU.

- Be sure to read TRCU first and then TRCL when reading the TCC value using the TRCL/U pair. The value in the lower digit of TCC is latched into TRCL when TRCU is read. Thus reading TRCL returns the value of the TCC lower digit at the point TRCU was last read.

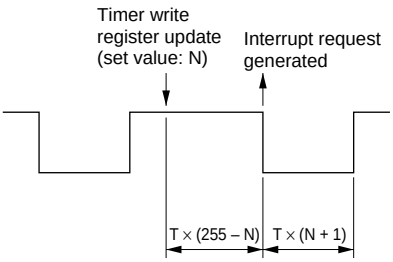
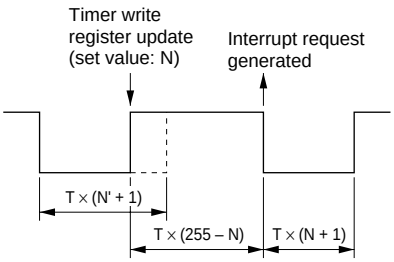
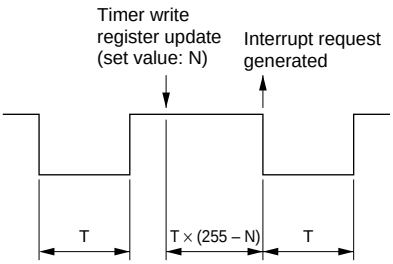
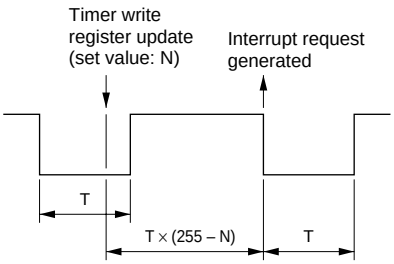
- When changing the value of TMC, the new value becomes valid two instructions after the execution of the instruction that wrote TMC. Therefore it is necessary for programs that initialize timer C (set the reload value or initialize TCC) by writing to the TWCL/U pair to perform this initialization only after the mode changed by TMC has become valid.

- Keep the following points in mind when using the timer output as PWM output.

  In PWM output mode, the duty and the period between the point when the timer write register is updated and the point when the next overflow interrupt is generated differ from the set values as shown in table 19-3.

  Therefore, when using PWM output, only use the output following the overflow interrupt generated after the timer write register was updated. The PWM output following the first overflow will have the duty and period specified by the settings.

Table 19-3 PWM Output Immediately Following Timer Write Register Update

Mode	PWM Output: Timer Write Register Updated during High Level Output	PWM Output: Timer Write Register Updated during Low Level Output
Free-running (HD404344R, HD404394, HD404318, HD404339 Series)		
Reload (all series)		

Section 20 Serial Interface

20.1 Overview

The HMCS43XX microcomputers include a built-in single-channel serial interface. This serial interface is a built-in peripheral module that implements serial data communication with other LSIs. In particular, this serial interface implements 8-bit clock synchronous communication.

20.1.1 Features

The serial interface has the following features.

- The clock source can be selected from one of 13 internal clocks: either the system clock or one of the prescaler S (PSS*) outputs divided by 2 or 4. Alternatively, an external clock can be used as the clock source.
- During idle periods, the transfer output pin can be set to either high or low.
- Interrupts can be generated on transfer complete and transfer errors.

Note: * See section 16, “Prescalers”, for details.

20.1.2 Block Diagram

Figure 20-1 shows the block diagram of the serial interface.

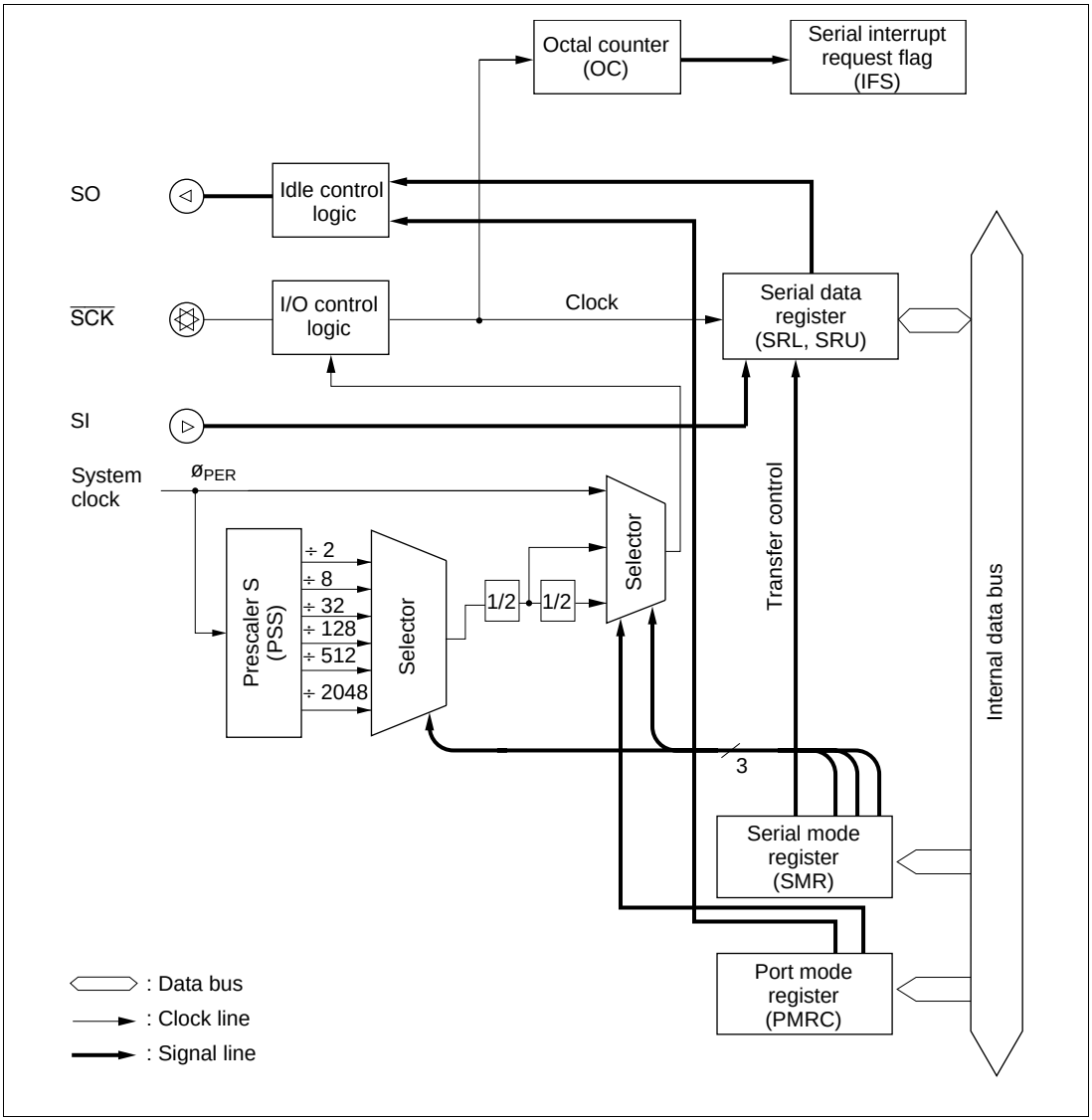


Figure 20-1 Serial Interface Block Diagram

20.1.3 Serial Interface Pins

Table 20-1 lists the pins used by the serial interface.

Table 20-1 Serial Interface Pins

Pin	Symbol	I/O	Function
Serial clock I/O	$\overline{SCK}$	I/O	Transfer clock input and output
Serial reception data input	SI	Input	Serial reception data input
Serial transmission data output	SO	Output	Serial transmission data output

20.1.4 Register Configuration

Table 20-2 lists the registers used by the serial interface.

Table 20-2 Register Configuration

Address	Register	Symbol	R/W	Initial Value
$005	Serial mode register	SMR	W	$0
$006	Serial data register L	SRL	R/W	Undefined
$007	Serial data register U	SRU	R/W	Undefined
	Octal counter	OC	—	000
$004	Port mode register A	PMRA	W	$0
$025	Port mode register C	PMRC	W	00-0
$00C	Miscellaneous register	MIS	W	$0

20.2 Register Descriptions

20.2.1 Serial Mode Register (SMR: $005)

SMR is a 4-bit write-only register that switches the R port and serial clock pin function, selects the transfer clock, and controls serial interface initialization.

The serial interface is initialized by write operations to the SMR. Clock supply to the serial data register and the octal counter stops and the octal counter is cleared to 0.

If a program writes to SMR during a data transfer, the data transmission or reception is aborted and the serial interrupt request flag is set to 1.

SMR is initialized to $0 on reset and in stop mode.

Bit	3	2	1	0
	SMR3	SMR2	SMR1	SMR0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Transfer clock selection

SMR2	SMR1	SMR0	$\overline{SCK}$ pin	Clock source	Prescaler divisor*
0	0	0	Output	PSS	$ø_{PER}$/2048
		1	Output	PSS	$ø_{PER}$/512
	1	0	Output	PSS	$ø_{PER}$/128
		1	Output	PSS	$ø_{PER}$/32
1	0	0	Output	PSS	$ø_{PER}$/8
		1	Output	PSS	$ø_{PER}$/2
	1	0	Output	System clock	$ø_{PER}$
		1	Input	External clock	—

$R0_0/\overline{SCK}$ pin function switch

0	R0 port I/O pin
1	$\overline{SCK}$ clock I/O pin

Note: * The transfer clock divisor is determined by the combination of the prescaler divisor set by the SMR2 to SMR0 bits and the prescaler output divisor (2 or 4) set by the PMRC PMRC0 bit.

Bit 3—$R0_0/\overline{SCK}$ Pin Function Switch (SMR3): Selects whether the $R0_0/\overline{SCK}$ pin functions as the $R0_0$ I/O pin or as the serial interface transfer clock I/O pin.

SMR3	Description	
0	The $R0_0/\overline{SCK}$ pin functions as the $R0_0$ I/O pin.	(initial value)
1	The $R0_0/\overline{SCK}$ pin functions as the $\overline{SCK}$ I/O pin.	

Bits 2 to 0—Transfer Clock Selection (SMR2 to SMR0, PMRC0): These bits select the serial interface transfer clock source to be either an external clock, the system clock, or a prescaler S (PSS) output. If PSS output is selected, the PMRC PMRC0 bit selects whether the PSS output will be divided by 2 or 4.

PMRC	SMR				Transfer Clock Source	Transfer Clock Divisor (a PSS Divisor of 2 or 4)	Transfer Clock Period
PMRC0	SMR2	SMR1	SMR0	$\overline{SCK}$ Pin			
0	0	0	0	Output	PSS	$(ø_{PER}/2048) \div 2$	4096 t_{cyc} (initial value)
			1	Output	PSS	$(ø_{PER}/512) \div 2$	1024 t_{cyc}
		1	0	Output	PSS	$(ø_{PER}/128) \div 2$	256 t_{cyc}
			1	Output	PSS	$(ø_{PER}/32) \div 2$	64 t_{cyc}
	1	0	0	Output	PSS	$(ø_{PER}/8) \div 2$	16 t_{cyc}
			1	Output	PSS	$(ø_{PER}/2) \div 2$	4 t_{cyc}
		1	0	Output	System clock	$ø_{PER}$	t_{cyc}
			1	Input	External clock	—	—
1	0	0	0	Output	PSS	$(ø_{PER}/2048) \div 4$	8192 t_{cyc} (initial value)
			1	Output	PSS	$(ø_{PER}/512) \div 4$	2048 t_{cyc}
		1	0	Output	PSS	$(ø_{PER}/128) \div 4$	512 t_{cyc}
			1	Output	PSS	$(ø_{PER}/32) \div 4$	128 t_{cyc}
	1	0	0	Output	PSS	$(ø_{PER}/8) \div 4$	32 t_{cyc}
			1	Output	PSS	$(ø_{PER}/2) \div 4$	8 t_{cyc}
		1	0	Output	System clock	$ø_{PER}$	t_{cyc}
			1	Input	External clock	—	—

Notes: $ø_{PER}$: The built-in peripheral module operating clock
t_{cyc}: System clock period

20.2.2 Serial Data Register SRL/U (SRL: $006, SRU: $007)

The SRL/U pair form an 8-bit read/write register in which SRU is the upper digit and SRL is the lower digit. Data to be transmitted is written to this register and received data is read from this register.

Data written to the SRL/U pair is shifted right (from upper bit positions to lower bit positions) one bit at a time on the falling edge of the transfer clock and the LSB data is output from the SO pin. Similarly, external data that was transferred LSB first is input from the SI pin. This data is acquired by shifting the SRL/U pair right one bit at a time. (See figure 20-2.)

The SRL/U pair can only be read or written after the last data transmission or reception operation has completed. Data integrity is not guaranteed if data is read or written during a data transmission or reception operation.

The SRL/U pair is undefined on reset and in stop mode.

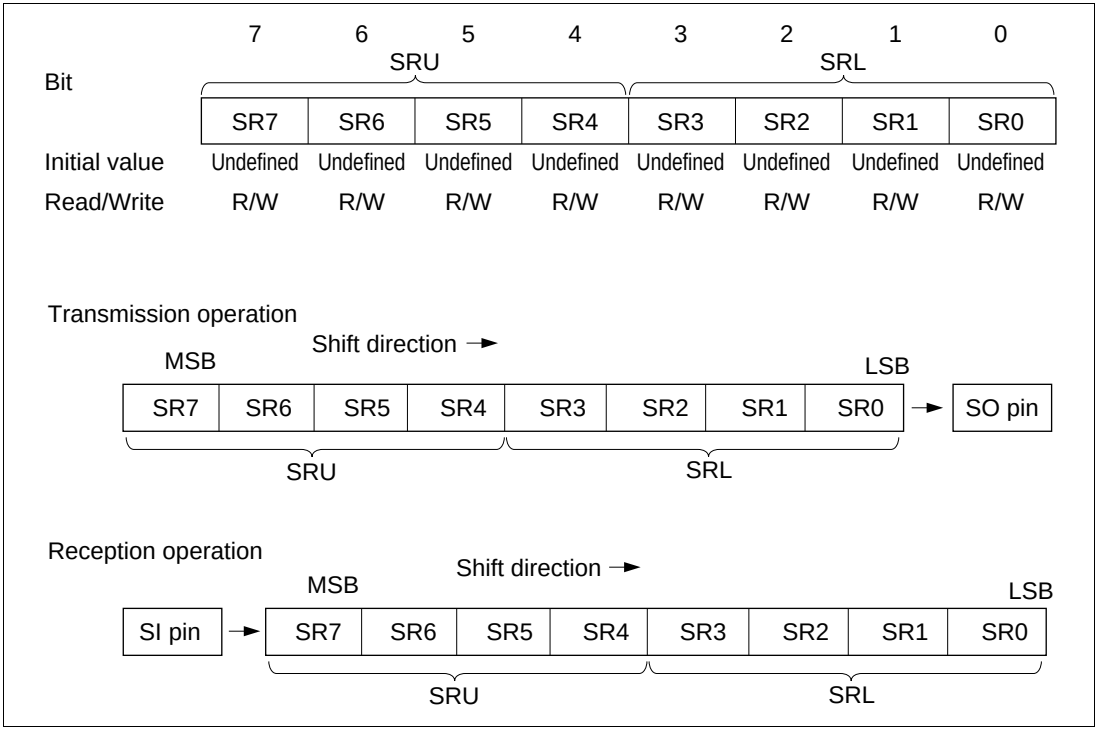


Figure 20-2 Shift Operations During Data Transmission and Reception

20.2.3 Octal Counter (OC)

Bit	2	1	0
	OC2	OC1	OC0
Initial value	0	0	0
Read/Write	—	—	—

OC is a 3-bit counter that controls the serial interface operating state transitions. When an STS instruction is executed in the STS instruction wait state, OC is initialized to 000, and after the serial interface switches to the transfer state the OC is incremented by 1 on each rising edge of the transfer clock. When either eight transfer clock cycles complete or the transmission or reception is aborted, OC is cleared to 000 and the serial interface switches from the transfer state to the STS instruction wait state or the transfer clock wait state. At the same time IFS is set to 1.

OC is initialized to 000 on reset and in stop mode.

See section 20.3.4, “Operating States”, for details on the OC and operating state transitions.

20.2.4 Port Mode Register A (PMRA: $004)

PMRA is a 4-bit write-only register whose PMRA2 to PMRA0 bits switch the R0 port pin function. PMRA3 switches the function of the D port D_3/BUZZ pin.

This section describes the PMRA1 and PMRA0 bits. See sections 19.2.2 and 21.2.1, “Port Mode Register A (PMRA)”, for details on the PMRA3 and PMRA2 bits.

Bit	3	2	1	0
	PMRA3*	PMRA2	PMRA1	PMRA0
Initial value	0	0	0	0
Read/Write	W	W	W	W

$R0_2$/SO pin function switch

0	$R0_2$ I/O pin
1	SO output pin

$R0_1$/SI pin function switch

0	$R0_1$ I/O pin
1	SI input pin

$R0_3$/TOC pin function switch

0	$R0_3$ I/O pin
1	TOC output pin

D_3/BUZZ pin function switch*

0	D_3 I/O pin
1	BUZZ output pin

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The PMRA3 bit is unused in the HD404344R and HD404394 Series.

Bit 1— $R0_1$/SI Pin Function Switch (PMRA1): Selects whether the $R0_1$/SI pin functions as the $R0_1$ I/O pin or as the serial reception data input pin (SI).

PMRA1	Description	
0	The $R0_1$/SI pin functions as the $R0_1$ I/O pin.	(initial value)
1	The $R0_1$/SI pin functions as the SI input pin.	

Bit 0—$R0_2$/SO Pin Function Switch (PMRA0): Selects whether the $R0_2$/SO pin functions as the $R0_2$ I/O pin or as the serial transmission data output pin (SO).

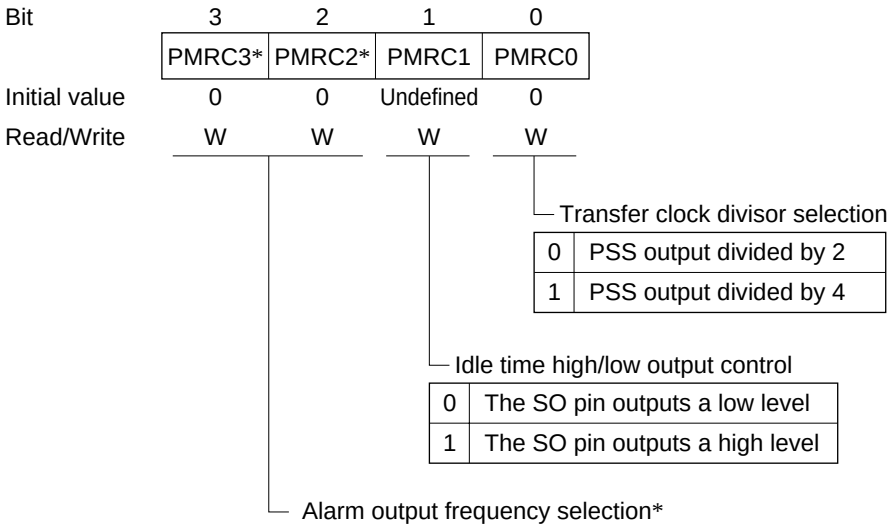
PMRA0	Description	
0	The $R0_2$/SO pin functions as the $R0_2$ I/O pin.	(initial value)
1	The $R0_2$/SO pin functions as the SO output pin.	

20.2.5 Port Mode Register C (PMRC: $025)

PMRC is a 4-bit write-only register that selects the high/low level output state during serial interface idle and sets the divisor for the PSS output used as the transfer clock. This register also sets the alarm frequency,

Do not update or write to this register during serial interface transfers. Writing to this register during a transfer can cause the serial interface to operate incorrectly.

This section describes the PMRC1 and PMRC0 bits. See section 21.2.2, “Port Mode Register C”, for details on the PMRC3 and PMRC2 bits.



Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The PMRC3 and PMRC2 bits are unused in the HD404344R and HD404394 Series.

Bit 1—Idle Time High/Low Output Control (PMRC1): Controls the state of the SO pin during serial interface idle. The SO pin changes state when this bit is written.

PMRC1 is undefined on reset and in stop mode.

PMRC1	Description	
0	The SO pin outputs a low level during idle.	(initial value)
1	The SO pin outputs a high level during idle.	

Bit 0—Transfer Clock Divisor Selection (PMRC0): Selects whether the PSS output divided by 2 or 4 is used as the transfer clock. This bit, along with the SMR SMR2 to SMR0 bits, controls the corresponding serial interface transfer clock.

PMRC0 is initialized to 0 on reset and in stop mode.

PMRC0	Description	
0	The PSS output divided by 2 is used as the transfer clock.	(initial value)
1	The PSS output divided by 4 is used as the transfer clock.	

20.2.6 Miscellaneous Register (MIS: $00C)

MIS is a 4-bit write-only register that controls the port pull-up MOS transistor on/off states, controls the $R0_2$/SO pin output buffer PMOS transistor on/off state, sets the interrupt frame period (T) in watch mode and subactive mode, and sets the oscillator stabilization time (t_{RC}) when low power modes are cleared.

MIS is initialized to $0 on reset and in stop mode.

Bit	3	2	1	0
	MIS3	MIS2	MIS1*1	MIS0*1
Initial value	0	0	0	0
Read/Write	W	W	W	W

Interrupt frame period and oscillator stabilization time setting*1

MIS1	MIS0	Interrupt frame period	Oscillator stabilization period	Oscillator circuit conditions
0	0	0.24414 ms	0.12207 (0.24414) ms*2	External clock
	1	15.625 ms	7.8125 ms	Ceramic oscillator
1	0	125 ms	62.5 ms	Crystal oscillator
	1	Unused		—

$R0_2$/SO pin output buffer control

0	PMOS transistor active (CMOS output)
1	PMOS off (NMOS open drain output)

Pull-up MOS transistor control

0	Pull-up MOS transistors all off
1	Pull-up MOS transistors active

Notes: 1. Applies to the HD404339 and HD404369 Series. The MIS1 and MIS0 bits are unused in the HD404344R, HD404394, HD404318, HD404358, and HD404358R Series.
2. Values in parentheses are direct transition times.

This section describes the MIS2 bit. See sections 11.1.2(4), 12.1.2(4) and 6.2.1, “Miscellaneous Register (MIS)”, for details on the MIS3, MIS1, and MIS0 bits.

Bit 2—$R0_2$/SO Pin Output Buffer Control (MIS2): Controls the $R0_2$/SO pin output buffer PMOS transistor on/off state.

MIS2	Description	
0	The $R0_2$/SO pin functions as a CMOS output.	(initial value)
1	The $R0_2$/SO pin functions as an NMOS open drain output.	

20.3 Operation

20.3.1 Operating Modes

The serial interface performs 8-bit clock synchronization communication. The serial interface has the four operating modes listed in table 20-3. These modes are selected by the SMR SMR3 bit and the PMRA PMRA1 and PMRA0 bits.

Table 20-3 Serial Interface Operating Modes

SMR	PMRA		
SMR3	**PMRA1**	**PMRA0**	**Operating Mode**
1	0	0	Transfer clock continuous output mode
		1	Transmission mode
	1	0	Reception mode
		1	Transmission/reception mode

20.3.2 Serial Data Format

Figure 20-3 shows the transfer format for clock synchronous serial data. Eight bits of data can be transmitted or received in a single operation. Data is transmitted (or received) in an LSB first format. Transmitted data is output from one falling edge of the transfer clock to the next falling edge, and received data is input on the rising edge of the transfer clock.

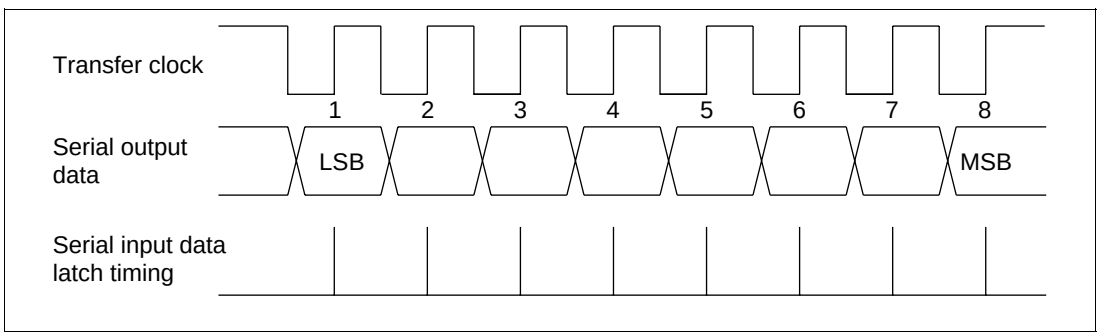


Figure 20-3 Clock Synchronous Serial Data Transfer Format

20.3.3 Transfer Clock

Either an internal clock or an external clock can be used as the transfer clock. The internal clock can be set to be either the system clock or one of 12 clocks generated by dividing PSS output by 2 or 4, for a total of 13 internal clock options. When an internal clock is used, the $\overline{\text{SCK}}$ pin functions as the transfer clock output pin.

20.3.4 Operating States

Serial interface transfer operations are initiated by the STS instruction. When an STS instruction is executed, OC is cleared to 000 and is incremented on each transfer clock rising edge. OC is cleared to 000 and IFS is set to 1 when eight transfer clock cycles have completed or when a transmission or reception is aborted.

The serial interface has four operating states as follows.

- STS instruction wait state
- Transfer clock wait state
- Serial state
- Transfer clock continuous output state (internal clock mode only)

Figure 20-4 shows the state transition diagram for the serial interface.

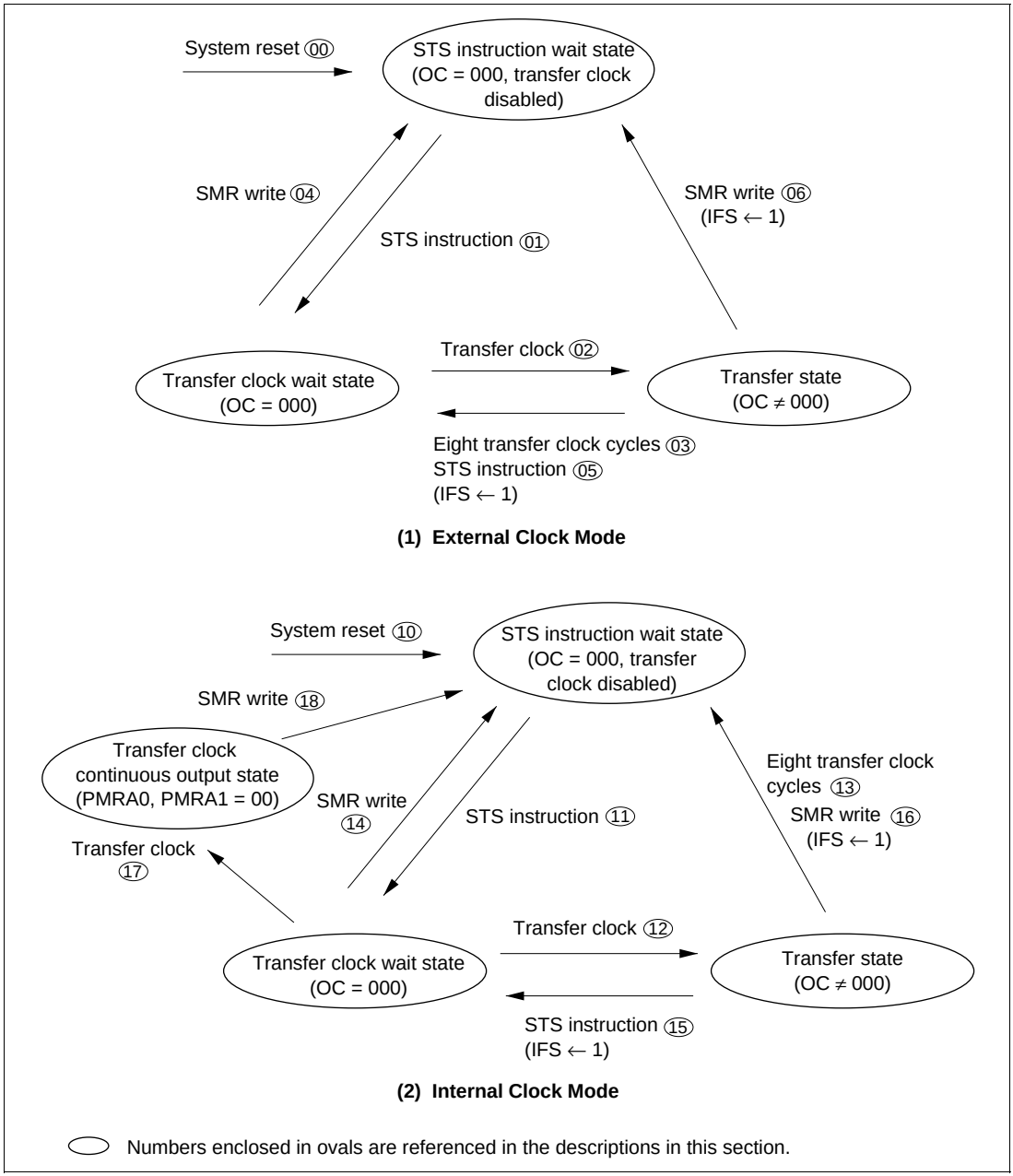


Figure 20-4 Serial Interface State Transition Diagram

(1) STS Instruction Wait State: The serial interface enters the STS instruction wait state on a system reset (items ⓪⓪ and ⑩ in figure 20-4).

The STS instruction wait state is the state in which the serial interface internal state is initialized. In this state, the serial interface will not operate even if a transfer clock is applied. When an STS instruction is executed (⓪① or ⑪) the serial interface switches to the transfer clock wait state.

(2) Transfer Clock Wait State: The transfer clock wait state is the period between the execution of an STS instruction and the first transfer clock falling edge.

When the transfer clock is applied (⓪② or ⑫) with the serial interface in the transfer clock wait state, the OC counter is incremented, the SRL/U pair shift operation starts, and the serial interface switches to the transfer state. However, when transfer clock continuous output mode is selected in internal clock mode, the serial interface does not switch to the transfer state, but rather it switches to the transfer clock continuous output state (⑰).

If SMR is written when the serial interface is in the transfer clock wait state, the serial interface switches to the STS instruction wait state (⓪④ or ⑭).

(3) Transfer State: Transfer state is the period between the first transfer clock falling edge and the eighth transfer clock rising edge.

If either an STS instruction is executed or eight transfer clock cycles are applied, OC is cleared to 000 and the serial interface state switches. If an STS instruction was executed (⓪⑤ or ⑮), the serial interface switches to the transfer clock wait state. If eight transfer clock cycles were applied, the serial interface transfers to either the transfer clock wait state (⓪③) if it was in external clock mode, or the STS instruction wait state (⑬) if it was in internal clock mode.

In internal clock mode, the transfer clock stops after eight clock cycles.

If SMR is written in the transfer state (⓪⑥ or ⑯), the serial interface is initialized and it switches to the STS instruction wait state.

When a transition from transfer state to any other state occurs, OC is cleared to 000 and IFS is set to 1.

(4) Transfer Clock Continuous Output State (Internal Clock Mode Only): Transfer clock continuous output state is a state in which no data transfer is performed but the transfer clock is output continuously from the $\overline{\text{SCK}}$ pin. When the PMRA PMRA1 and PMRA0 bits are set to 00 and the serial interface is in the transfer clock wait state, if the transfer clock is applied (⑰), the serial interface switches to the transfer clock continuous output state. If SMR is written in the transfer clock continuous output state (⑱), the serial interface is initialized and it switches to the STS instruction wait state.

20.3.5 Transmission and Reception Operations

(1) Serial Interface Initialization: The first step in data transmission or reception operation is initialization of the serial interface by software. This is performed by either resetting the system or writing to the SMR register.

(2) Data Transmission

a. Data transmission procedure in external clock mode

Figure 20-5 shows the data transmission procedure in external clock mode.

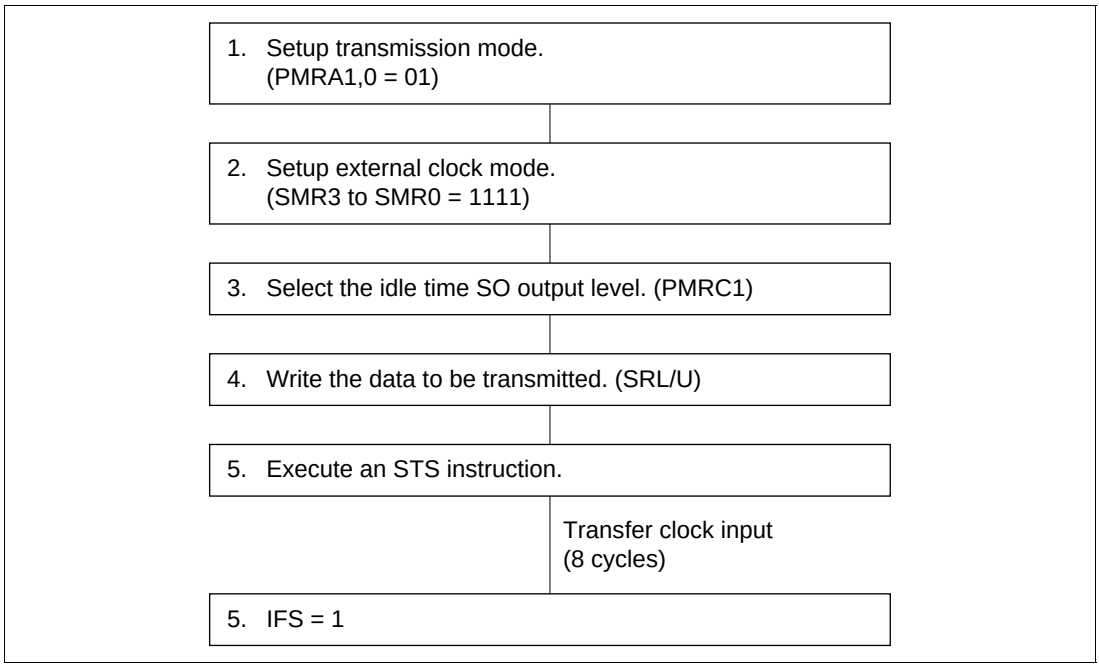


Figure 20-5 Data Transmission Procedure (External Clock Mode)

Use the following procedure for data transmission in external clock mode.

1. Setup transmission mode by setting the PMRA1 and PMRA0 bits to 01.

2. Setup external clock mode by setting the SMR3 to SMR0 bits to 1111.

   The serial interface internal states are initialized when SMR is written.

3 Select either a low or high level SO pin idle output by setting the PMRC1 bit. The SO pin will immediately go to either the high or low level when PMRC1 is written.

4 Write the data to be transmitted to the SRL/U pair.

5 Execute an STS instruction. The serial interface will switch from the STS instruction wait state to the transfer clock wait state.

   When the external clock is applied, the serial interface will switch from the transfer clock wait state to the transfer state on the first transfer clock falling edge, and the serial interface will begin the transmission operation.

6. When eight transfer clock cycles have been input, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches from the transfer state to the transfer clock wait state thus completing the transmission operation.

After the transfer completes, the SO pin holds the value of the MSB of the transmitted data. The output value on the SO pin can be changed by setting the PMRC1 bit.

In the transfer clock wait state, if the transfer clock continues to be input, data transmission operations are repeated. Also, the serial interface can be returned to the STS instruction wait state to prepare for the next transmission by performing a dummy write to the SMR register.

If the SMR register is written during a transmission operation, OC is cleared to 0 and IFS is set to 1. At the same time the serial interface switches to the STS instruction wait state and the transmission is aborted.

Figure 20-6 shows the operation sequence for data transmission in external clock mode.

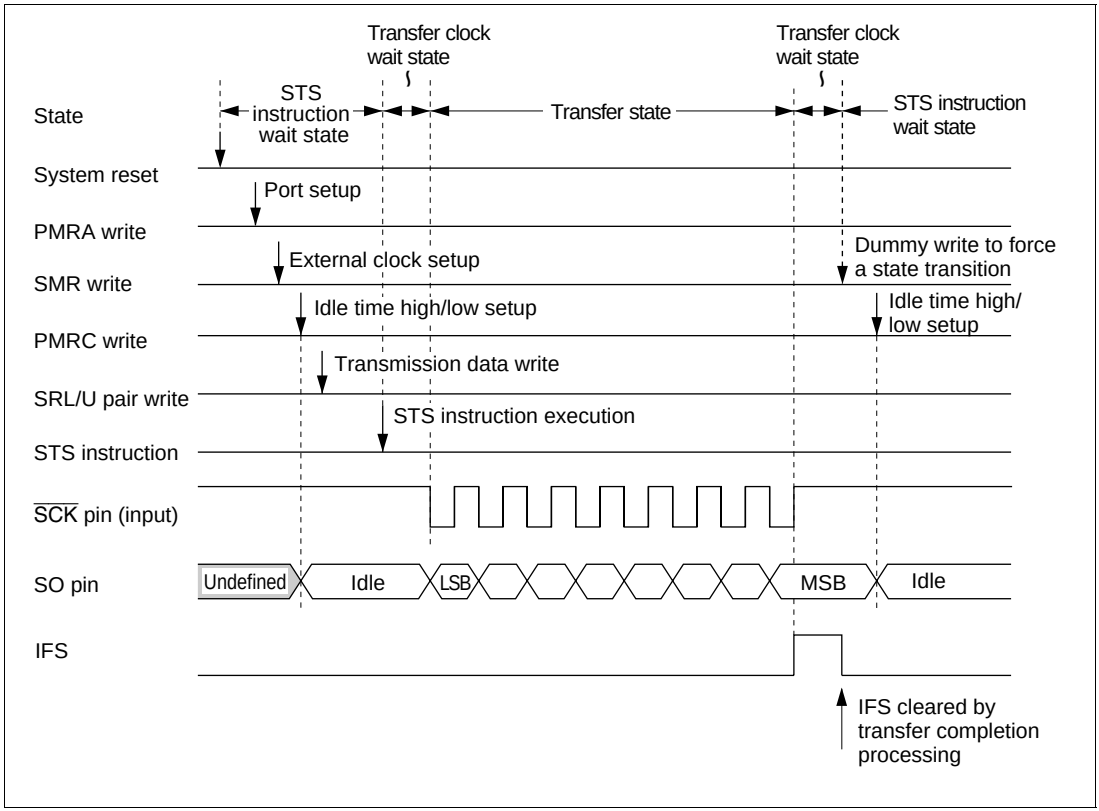


Figure 20-6 Serial Transmission Operation Sequence (External Clock Mode)

b. Data transmission procedure in internal clock mode

Figure 20-7 shows the data transmission procedure in internal clock mode.

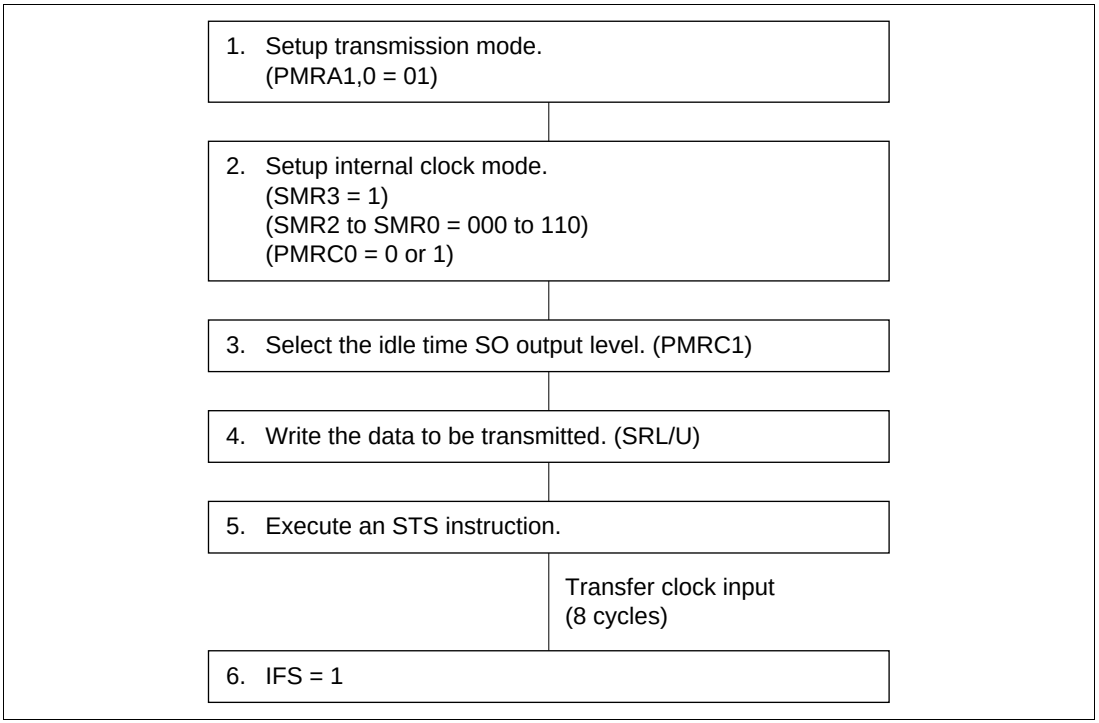


Figure 20-7 Data Transmission Procedure (Internal Clock Mode)

Use the following procedure for data transmission in internal clock mode.

1. Setup transmission mode by setting the PMRA1 and PMRA0 bits to 01.
2. Setup internal clock mode by setting the SMR2 to SMR0 bits.

   The serial interface internal states are initialized when SMR is written.

   Select a divisor of 2 or 4 transfer clock for the prescaler output by setting the PMRC0 bit.
3. Select either a low or high level SO pin idle output by setting the PMRC1 bit. The SO pin will immediately go to either the high or low level when PMRC1 is written.
4. Write the data to be transmitted to the SRL/U pair.
5. Execute an STS instruction. The serial interface will switch from the STS instruction wait state to the transfer clock wait state.

   When the internal clock is applied, the serial interface will switch from the transfer clock wait state to the transfer state on the first transfer clock falling edge, and the serial interface will begin the transfer operation.
6. When eight transfer clock cycles have been input, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches from the STS instruction wait state to the transfer clock wait state thus completing the transfer.

After the transfer completes, the SO pin holds the value of the MSB of the transmitted data. The output value on the SO pin can be changed by setting the PMRC1 bit.

In internal clock mode, the $\overline{\text{SCK}}$ pin functions as the transfer clock output pin and outputs the transfer clock, which is identical to the selected internal clock.

If the SMR register is written during a transmission operation, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches to the STS instruction wait state and the transmission is aborted.

Figure 20-8 shows the operation sequence for data transmission in internal clock mode.

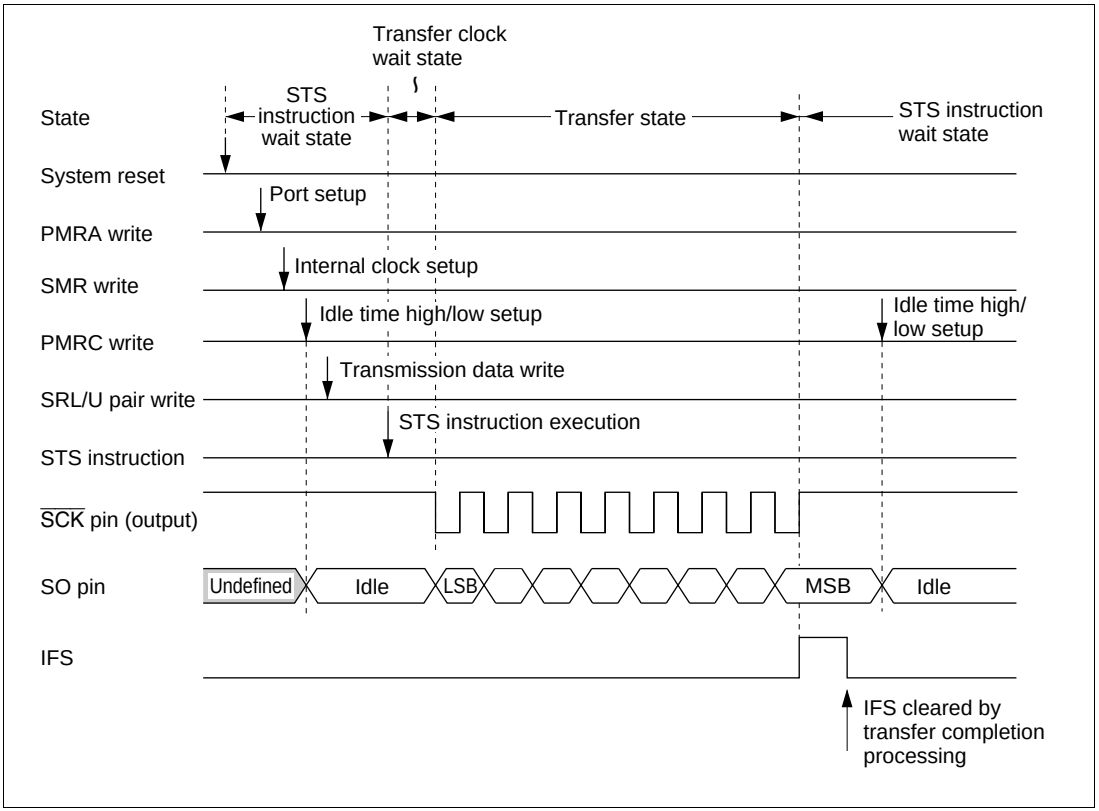


Figure 20-8 Serial Transmission Operation Sequence (Internal Clock Mode)

(3) Data Reception

a. Data reception procedure in external clock mode

Figure 20-9 shows the data reception procedure in external clock mode.

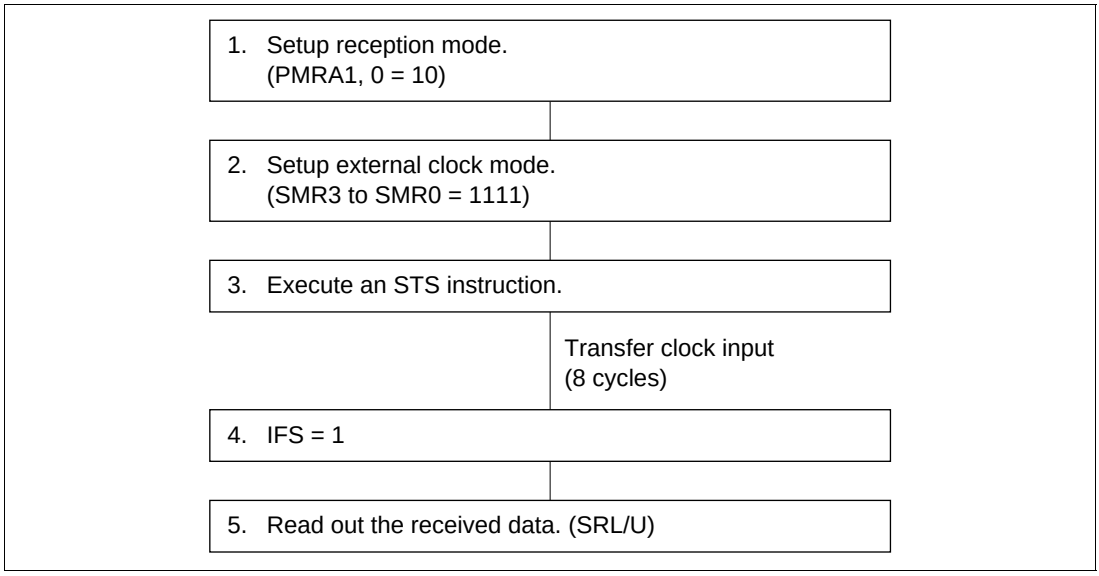


Figure 20-9 Data Reception Procedure (External Clock Mode)

Use the following procedure for data reception in external clock mode.

1. Setup reception mode by setting the PMRA1 and PMRA0 bits to 10.
2. Setup external clock mode by setting the SMR3 to SMR0 bits to 1111.

   The serial interface internal states are initialized when SMR is written.
3. Execute an STS instruction. The serial interface will switch from the STS instruction wait state to the transfer clock wait state.

   When the external clock is applied, the serial interface will switch from the transfer clock wait state to the transfer state on the first transfer clock falling edge, and the serial interface will begin the reception operation.
4. When eight transfer clock cycles have been input, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches from the transfer state to the transfer clock wait state thus completing the reception operation.
5. Read out the received data from the SRL/U pair.

After the completion of data reception with the serial interface in the transfer clock wait state, the reception operation will be repeated if the transfer clock continues to be input. Also, the serial interface can be returned to the STS instruction wait state to prepare for the next transmission by performing a dummy write to the SMR register.

If the SMR register is written during a reception operation, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches to the STS instruction wait state and the reception is aborted.

Figure 20-10 shows the operation sequence for data reception in external clock mode.

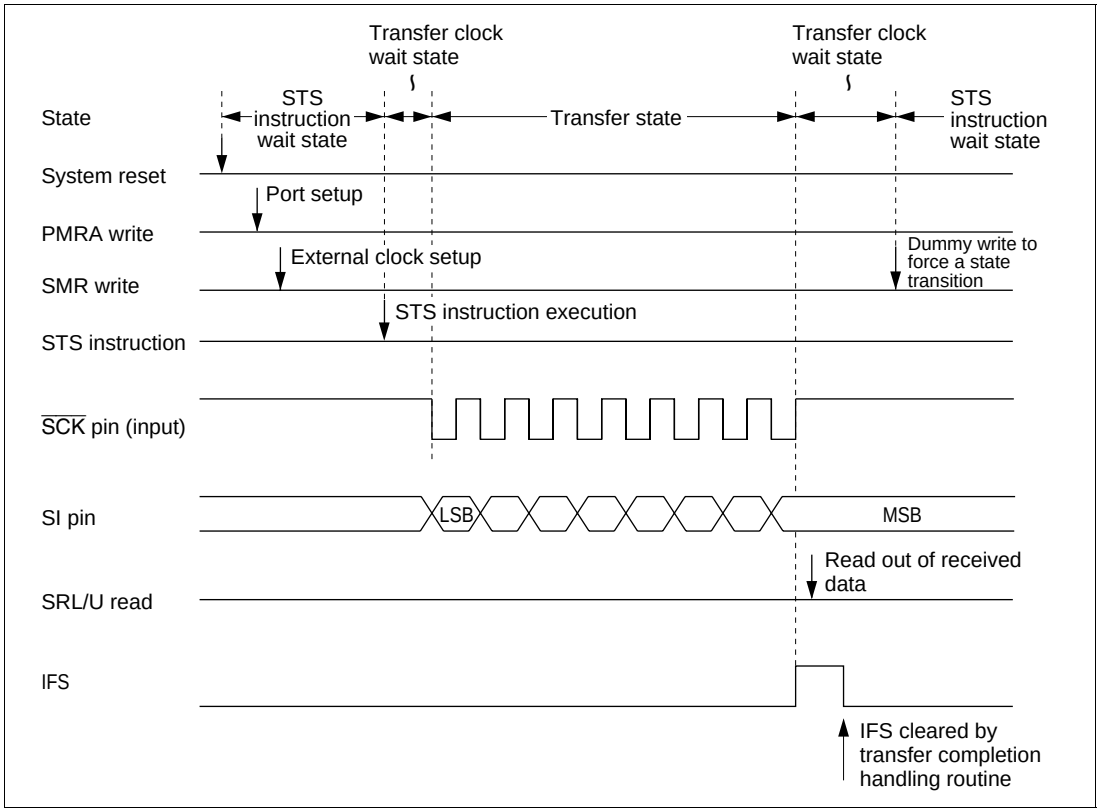


Figure 20-10 Serial Reception Operation Sequence (External Clock Mode)

b. Data reception procedure in internal clock mode

Figure 20-11 shows the data reception procedure in internal clock mode.

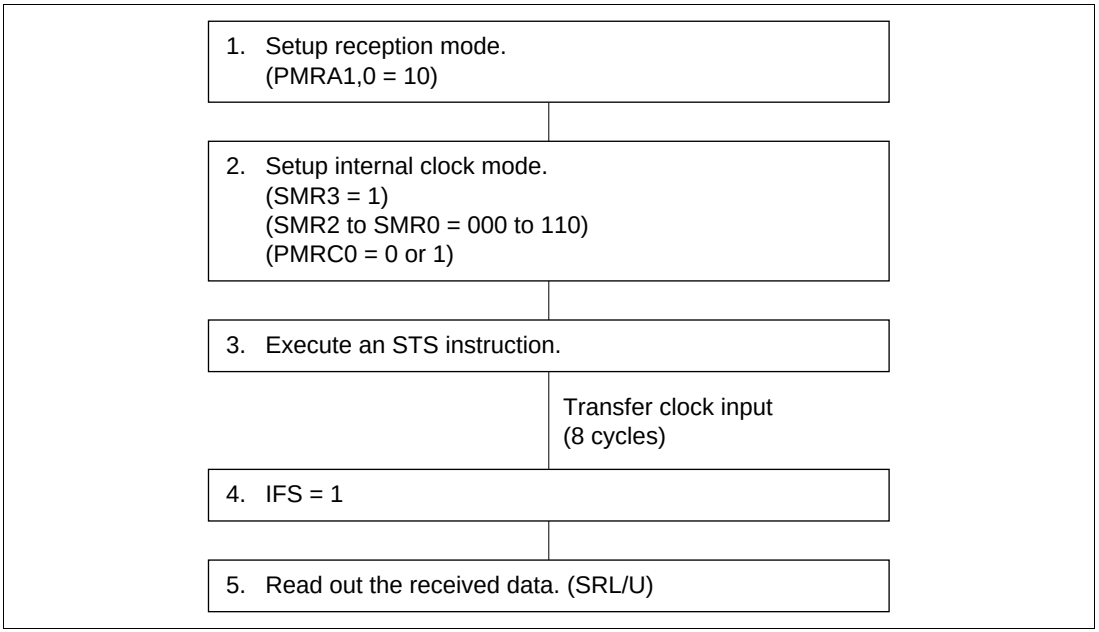


Figure 20-11 Data Reception Procedure (Internal Clock Mode)

Use the following procedure for data reception in internal clock mode.

1. Setup reception mode by setting the PMRA1 and PMRA0 bits to 10.
2. Setup internal clock mode by setting the SMR2 to SMR0 bits, and select the transfer clock.

   The serial interface internal states are initialized when SMR is written.

   Select a divisor of 2 or 4 for the prescaler output by setting the PMRC0 bit.
3. Execute an STS instruction. The serial interface will switch from the STS instruction wait state to the transfer clock wait state.

   When the internal clock is applied, the serial interface will switch from the transfer clock wait state to the transfer state on the first transfer clock falling edge, and the serial interface will begin the reception operation.
4. When eight transfer clock cycles have been input, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches from the transfer state to the STS instruction wait state thus completing the reception operation.
5. Read out the received data from the SRL/U pair.

If the SMR register is written during a reception operation, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches to the STS instruction wait state and the reception is aborted.

Figure 20-12 shows the operation sequence for data reception in internal clock mode.

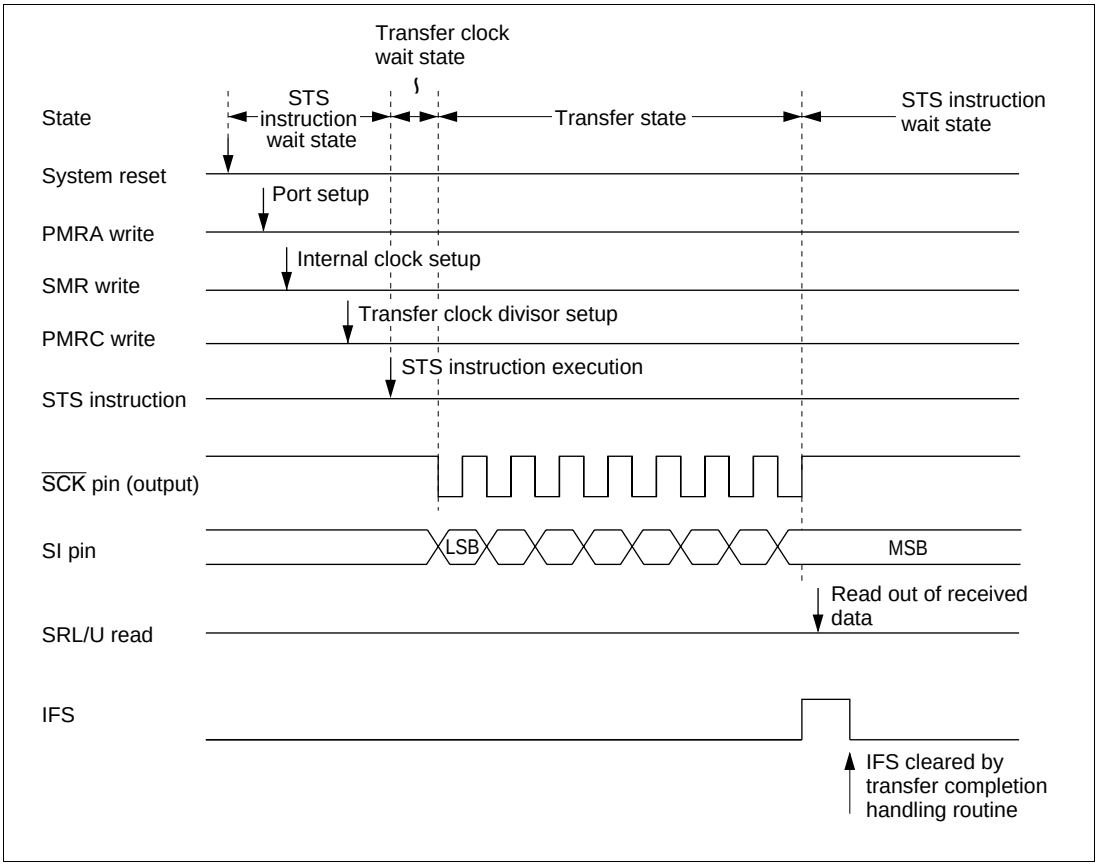


Figure 20-12 Serial Reception Operation Sequence (Internal Clock Mode)

(4) Simultaneous Transmission and Reception

a. Simultaneous transmission and reception in external clock mode

Figure 20-13 shows the simultaneous transmission and reception procedure in external clock mode.

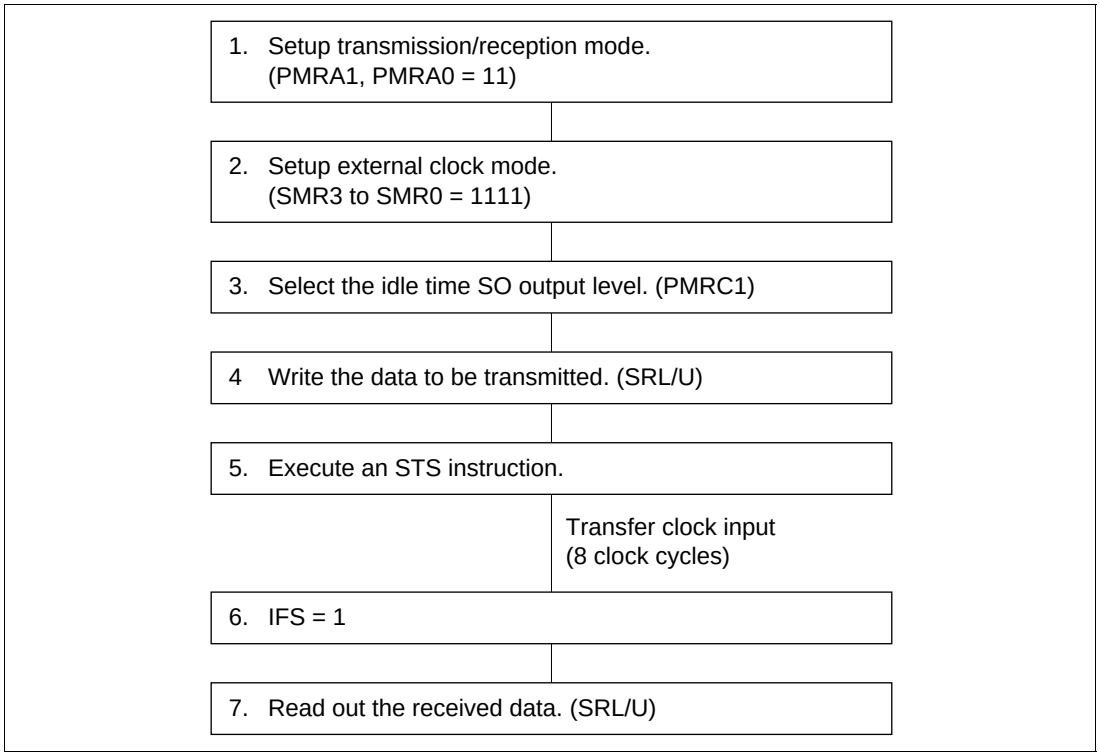


Figure 20-13 Simultaneous Transmission and Reception Procedure (External Clock Mode)

Use the following procedure for simultaneous transmission and reception in external clock mode.

1. Setup transmission/reception mode by setting the PMRA1 and PMRA0 bits to 11.
2. Setup external clock mode by setting the SMR3 to SMR0 bits to 1111.

   The serial interface internal states are initialized when SMR is written.
3. Select either a low or high level SO pin idle output by setting the PMRC1 bit. The SO pin will immediately go to either the high or low level when PMRC1 is written.
4. Write the data to be transmitted to the SRL/U pair.
5. Execute an STS instruction. The serial interface will switch from the STS instruction wait state to the transfer clock wait state.

   When the external clock is applied, the serial interface will switch from the transfer clock wait state to the transfer state on the first transfer clock falling edge, and the serial interface will begin the transmission/reception operation. The SRL/U pair will be shifted right (in the MSB to LSB direction) in synchronization with the transfer clock, received data will be acquired in the MSB, and transmitted data will be output from the LSB.
6. When eight transfer clock cycles have been input, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches from the transfer state to the transfer clock wait state thus completing the transmission/reception operation.
7. Read out the received data from the SRL/U pair.

After the transfer completes, the SO pin holds the value of the MSB of the transmitted data. The output value on the SO pin can be changed by setting the PMRC1 bit.

In the transfer clock wait state, if the transfer clock continues to be input, data transmission/

reception operations are repeated. Also, the serial interface can be returned to the STS instruction wait state to prepare for the next transmission/reception by performing a dummy write to the SMR register.

If the SMR register is written during a transmission/reception operation, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches to the STS instruction wait state and the transmission/reception operation is aborted.

See figures 20-6 and 20-10 for the transmission/reception operation in external clock mode.

b. Simultaneous transmission and reception in internal clock mode

Figure 20-14 shows the simultaneous transmission and reception procedure in internal clock mode.

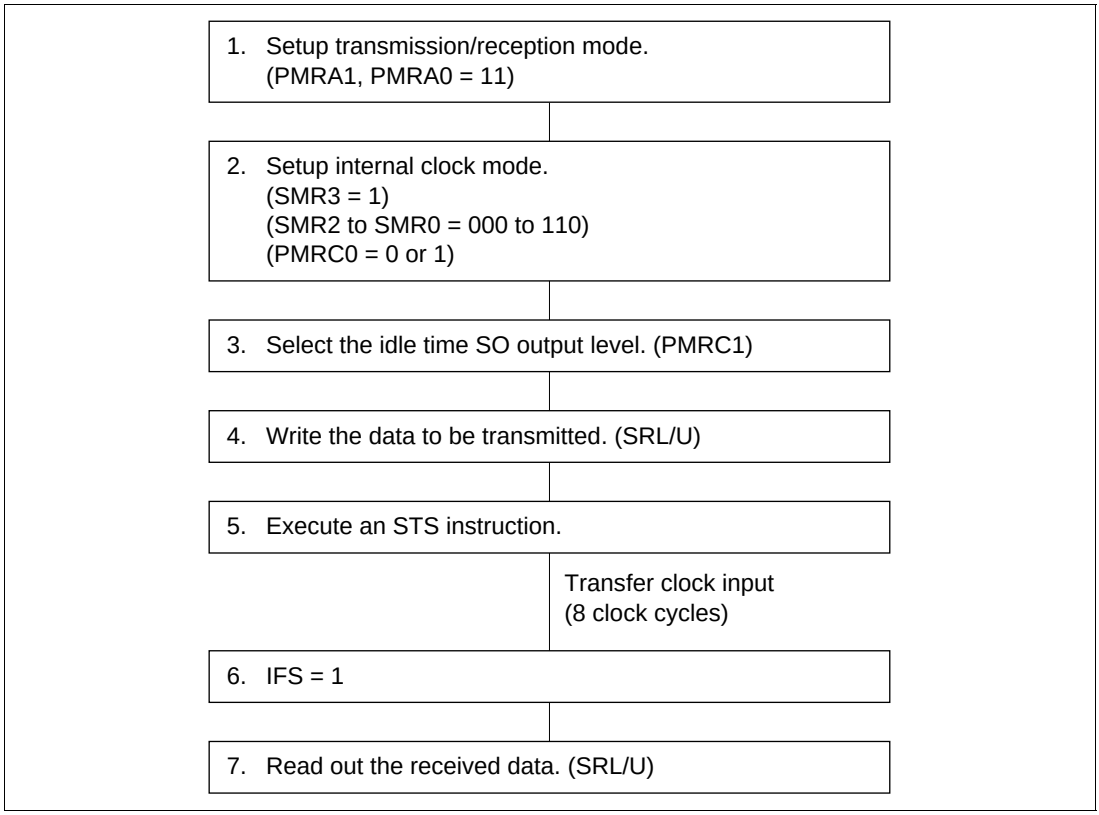


Figure 20-14 Simultaneous Transmission and Reception Procedure (Internal Clock Mode)

Use the following procedure for simultaneous transmission and reception in internal clock mode.

1. Setup transmission/reception mode by setting the PMRA1 and PMRA0 bits to 11.
2. Setup internal clock mode by setting the SMR2 to SMR0 bits, and select the transfer clock.

   The serial interface internal states are initialized when SMR is written.

   Select a divisor of 2 or 4 transfer clock for the prescaler output by setting the PMRC0 bit.
3. Select either a low or high level SO pin idle output by setting the PMRC1 bit. The SO pin will immediately go to either the high or low level when PMRC1 is written.
4. Write the data to be transmitted to the SRL/U pair.
5. Execute an STS instruction. The serial interface will switch from the STS instruction wait state to the transfer clock wait state.

   When the internal clock is applied, the serial interface will switch from the transfer clock wait state to the transfer state on the first transfer clock falling edge, and the serial interface will begin the transmission/reception operation.
6. When eight transfer clock cycles have been input, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches from the transfer state to the STS instruction wait state thus completing the transmission/reception operation.
7. Read out the received data from the SRL/U pair.

After the transfer completes, the SO pin holds the value of the MSB of the transmitted data. The output value on the SO pin can be changed by setting the PMRC1 bit.

In internal clock mode, the $\overline{\text{SCK}}$ pin functions as the transfer clock output pin and outputs the transfer clock, which is identical to the selected internal clock.

If the SMR register is written during a transmission/reception operation, OC is cleared to 000 and IFS is set to 1. At the same time the serial interface switches to the STS instruction wait state and the transmission/reception operation is aborted.

See figures 20-8 and 20-12 for the transmission/reception operation in internal clock mode.

(5) Transfer Clock Continuous Output Operation: Figure 20-15 shows the transfer clock continuous output operation procedure.

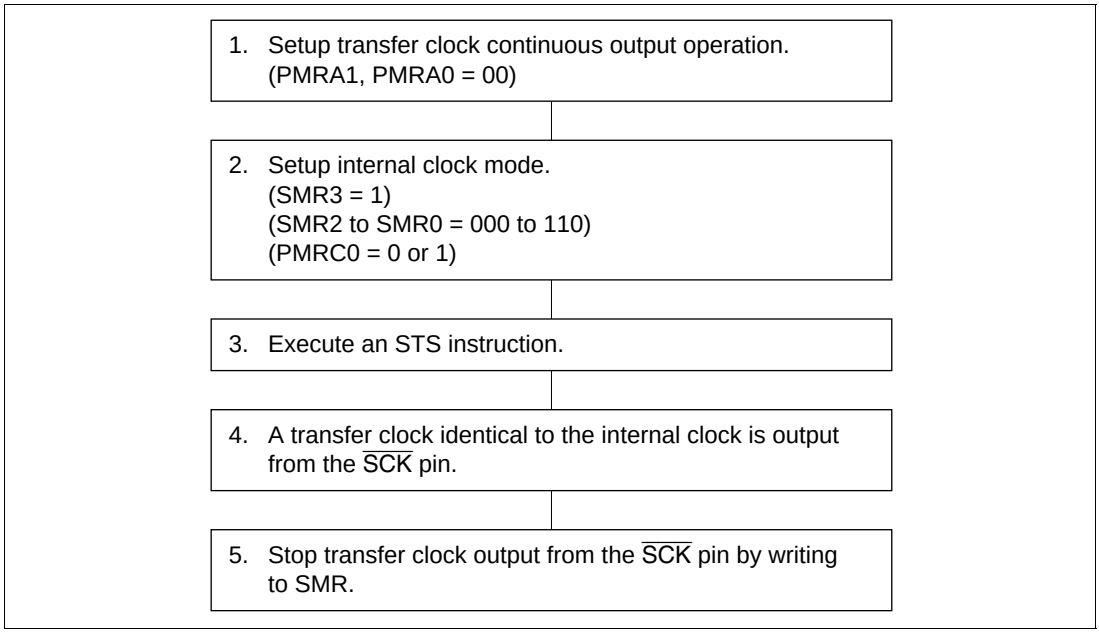


Figure 20-15 Transfer Clock Continuous Output Operation Procedure

Use the following procedure for transfer clock continuous output.

1. Setup transfer clock continuous output mode by setting the PMRA1 and PMRA0 bits to 00.
2. Setup internal clock mode by setting the SMR2 to SMR0 bits, and select the transfer clock.

   The serial interface internal states are initialized when SMR is written.

   Select a divisor of 2 or 4 for the prescaler output by setting the PMRC0 bit.
3. Execute an STS instruction. The serial interface will switch from the STS instruction wait state to the transfer clock wait state.
4. When the internal clock is applied, the serial interface will switch from the transfer clock wait state to the transfer state on the first transfer clock falling edge, and a transfer clock identical to the internal clock will be output from the $\overline{\text{SCK}}$ pin.
5. If the SMR is written in the transfer clock continuous output state, the serial interface will switch to the STS instruction wait state and transfer clock output will stop.

20.3.6 High- or Low-Level Output Selection during Idle

The serial interface allows user software to set the state of the SO pin arbitrarily during serial interface idle states, i.e., the STS instruction wait state and the transfer clock wait state. The output level during serial interface idle state is controlled by writing the PMRC PMRC1 bit. In the transfer state, the SO pin output level cannot be controlled.

20.3.7 Transfer Clock Error Detection (External Clock Mode)

The serial interface will operate incorrectly if external noise results in extraneous pulses being added to the transfer clock. The procedure shown in figures 20-16 and 20-17 allows such errors to be detected.

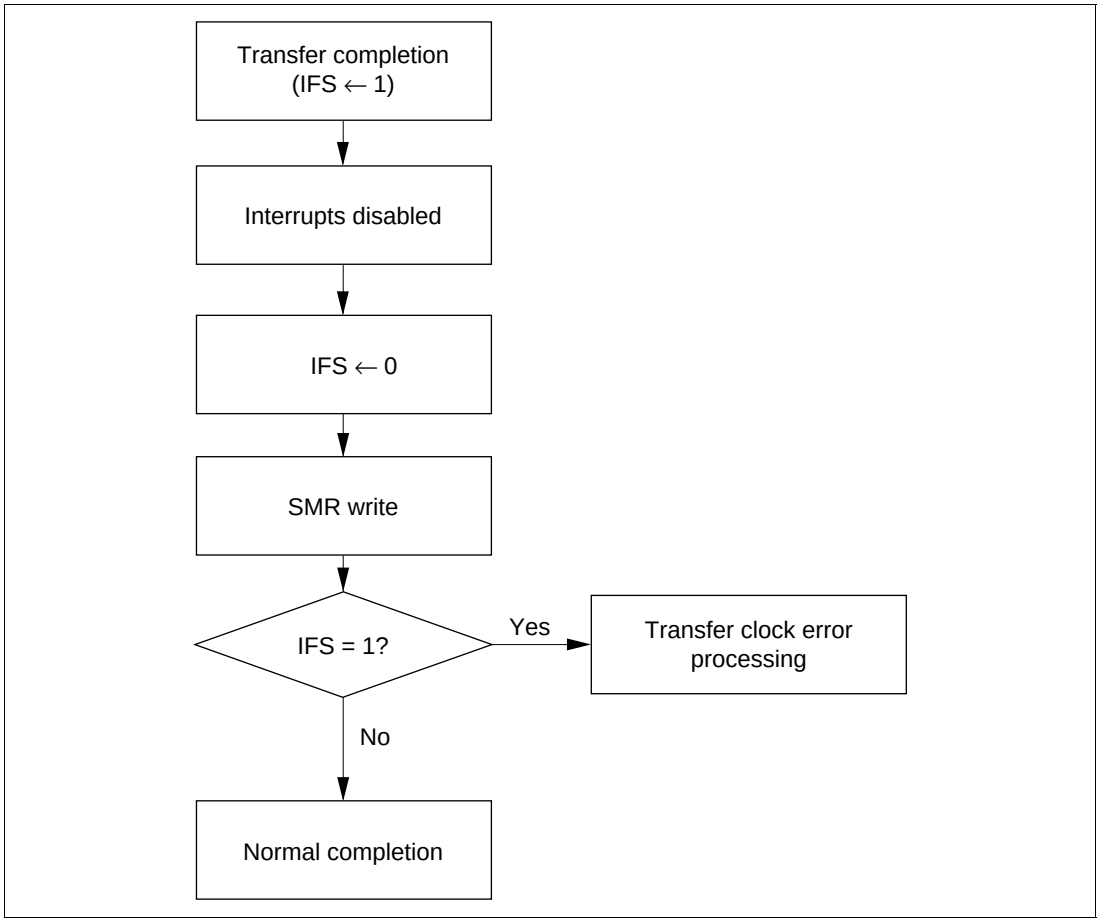


Figure 20-16 Transfer Clock Error Detection Flowchart

If more than 8 clock cycles are incorrectly applied in the transfer state, OC will be cleared to 000 and IFS set to 1 on the eighth (including noise) clock cycle. At the same time, the serial interface will switch from the transfer state to the transfer clock wait state. However, the serial interface will switch to the transfer state once again on the falling edge of the next clock pulse, which is a correct clock pulse.

At the same time, the interrupt processing routine will terminate the transfer, clear IFS to 0, and perform a dummy write to SMR. Since this dummy write causes the serial interface to switch from the transfer state to the STS instruction wait state, IFS will be set to 1 once again. (See figure 20-4.) Therefore, transfer clock errors can be detected by testing the IFS state after performing the SMR dummy write.

Figure 20-17 shows the transfer clock error detection sequence.

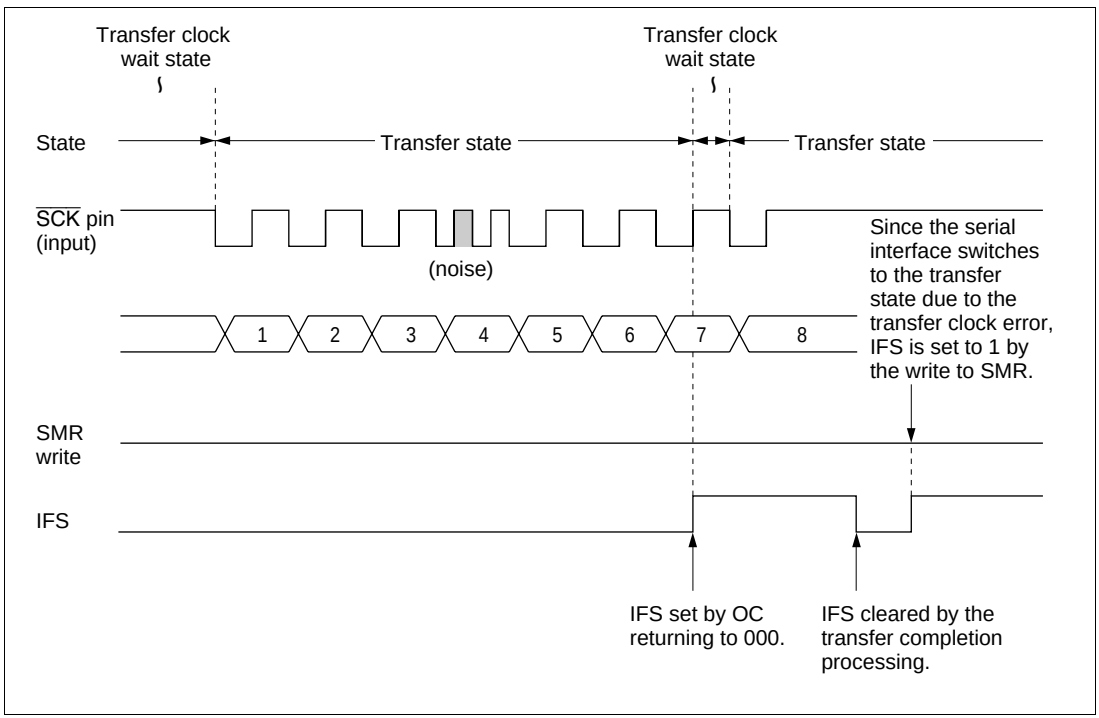


Figure 20-17 Transfer Clock Error Detection Sequence

20.4 Interrupts

The serial interface interrupt source is generated when the serial interface switches from the transfer state to any other state, i.e., when OC is cleared to 000. IFS is set to 1 when the serial interface interrupt source occurs.

IFS is never cleared automatically, even if the interrupt is accepted. The interrupt handling routine should clear IFS to 0.

The serial interrupt can be independently enabled or masked with the serial interrupt mask (IMS) in the interrupt control bit area.

20.5 Usage Notes

Keep the following points in mind when using the serial interface.

- If PMRA is to be written in either the transfer clock wait state or the transfer state, the serial interface should be re-initialized by writing to the SMR register.
- In the transfer state, IFS is not set to 1 by writing to SMR or switching to another state by executing an STS instruction during the first low level period of the transfer clock. To set the IFS flag reliably, execute an input instruction for the $R0_0$ pin, which will be assigned to be the $\overline{SCK}$ pin, and confirm that the $\overline{SCK}$ pin is at the high level. After this has been done, program software to write to SMR or to execute the STS instruction.
- Changes to the SMR register become valid two instruction cycles after the execution of the instruction that wrote the register. Therefore application programs must be written so that the STS instruction is executed only after a period of at least $2t_{cyc}$ has elapsed after the SMR register was written.
- MIS register control of the PMOS transistor on/off state is valid regardless of the PMRA register $R0_2$/SO pin function selection.

Section 21 Alarm Output (HD404318/HD404358/HD404358R/HD404339 /HD404369 Series)

21.1 Overview

The microcomputers in the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series include a built-in alarm output circuit.

21.1.1 Features

This circuit can output a signal generated by dividing the system clock to the BUZZ pin for use as an alarm drive signal. The alarm output circuit has the following features.

- The alarm output circuit can output one of four frequencies (these will be 488 Hz, 977 Hz, 1.95 kHz, and 3.91 kHz when f_{OSC} is 4 MHz) generated by dividing the system clock. The output waveform is a 50% duty square wave.

21.1.2 Block Diagram

Figure 21-1 shows the block diagram of the alarm output circuit.

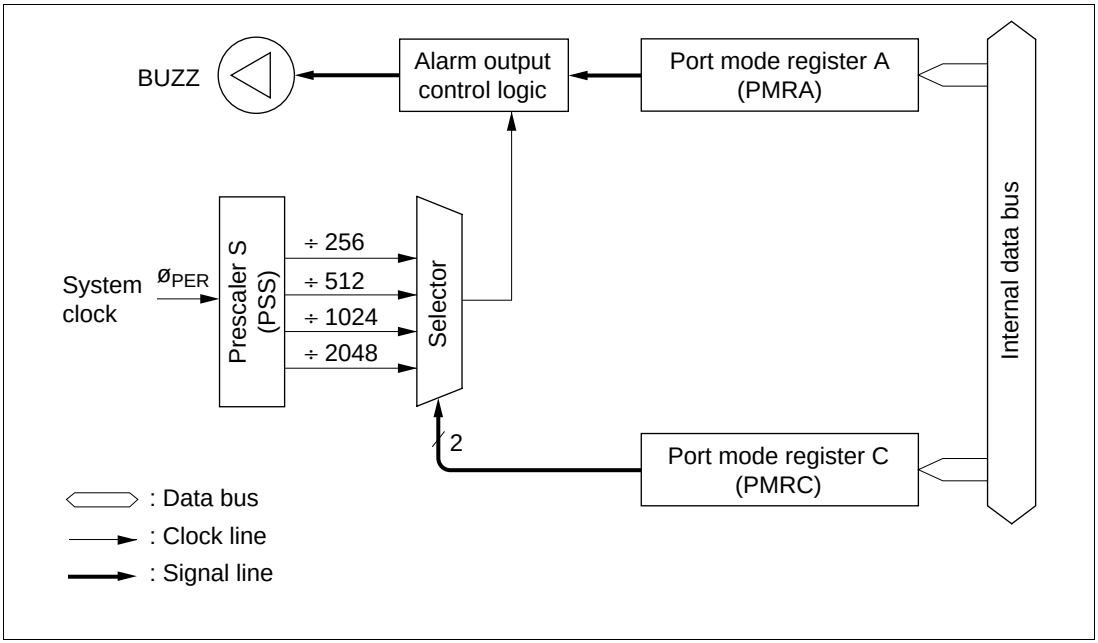


Figure 21-1 Alarm Output Circuit Block Diagram

21.1.3 Pin Functions

Table 21-1 lists the pins used by the alarm output circuit.

Table 21-1 Pin Configuration

Pin	Symbol	I/O	Function
Alarm output	BUZZ	Output	Alarm signal output

21.1.4 Register Configuration

Table 21-2 lists the registers used by the alarm output circuit.

Table 21-2 Register Configuration

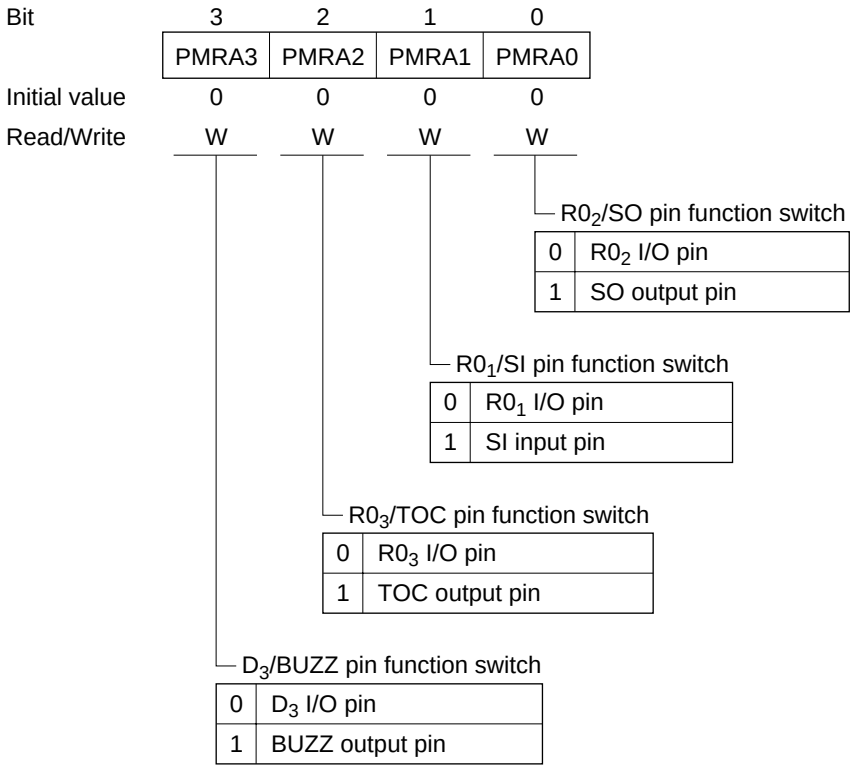
Address	Register	Symbol	R/W	Initial Value
$004	Port mode register A	PMRA	W	$0
$025	Port mode register C	PMRC	W	$0

21.2 Register Descriptions

21.2.1 Port Mode Register A (PMRA: $004)

PMRA is a 4-bit write-only register whose PMRA3 bit switches the function of the D_3/BUZZ pin and whose other bits switch the functions of the R0 port pins.

This section describes the PMRA3 bit. See the “Port Mode Register A (PMRA)” items in sections 9 to 12, “I/O Ports”, for details on the PMRA2 to PMRA0 bit in the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series microcomputers.



Bit 3—D_3/BUZZ Pin Function Switch (PMRA3): Selects whether the D_3/BUZZ pin functions as the D_3 I/O pin or as the alarm output pin (BUZZ).

PMRA3	Description	
0	The D_3/BUZZ pin functions as the D_3 I/O pin.	(initial value)
1	The D_3/BUZZ pin functions as the BUZZ output pin.	

21.2.2 Port Mode Register C (PMRC: $025)

PMRC is a 4-bit write-only register whose PMRC3 and PMRC2 bits select the alarm output frequency.

This section describes the PMRC3 and PMRC2 bits. See section 20.2.5, “Port Mode Register C (PMRC)” for details on the PMRC1 and PMRC0 bits.

Bit	3	2	1	0
	PMRC3	PMRC2	PMRC1	PMRC0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Transfer clock divisor selection

0	PSS output divided by 2
1	PSS output divided by 4

Idle time high/low output control

0	The SO pin outputs a low level
1	The SO pin outputs a high level

Alarm frequency selection

PMRC3	PMRC2	Alarm frequency
0	0	$ø_{PER}$/2048
	1	$ø_{PER}$/1024
1	0	$ø_{PER}$/512
	1	$ø_{PER}$/256

$ø_{PER}$: Built-in peripheral module operating clock

Bits 3 and 2—Alarm Frequency Selection (PMRC3, PMRC2): The PMRC3 and PMRC2 bits are initialized to 0 on reset and in stop mode.

PMRC3	PMRC2	Description	Alarm Frequency when $ø_{PER}$ = 1 MHz*
0	0	A signal with a frequency of $ø_{PER}$/2048 is output.	488 Hz
	1	A signal with a frequency of $ø_{PER}$/1024 is output.	977 Hz
1	0	A signal with a frequency of $ø_{PER}$/512 is output.	1.95 kHz
	1	A signal with a frequency of $ø_{PER}$/256 is output.	3.91 kHz

Note: * HD404318/HD404358/HD404358R Series: $ø_{PER} = f_{OSC}/4$
HD404339/HD404369 Series: $ø_{PER} = f_{OSC}/4$, $f_{OSC}/8$, $f_{OSC}/16$, or $f_{OSC}/32$

21.3 Operation

The alarm output circuit selects one of four frequencies generated by using prescaler S (PSS) to divide the system clock. Figure 21-2 shows the output waveform.

The output is a 50% duty square wave.

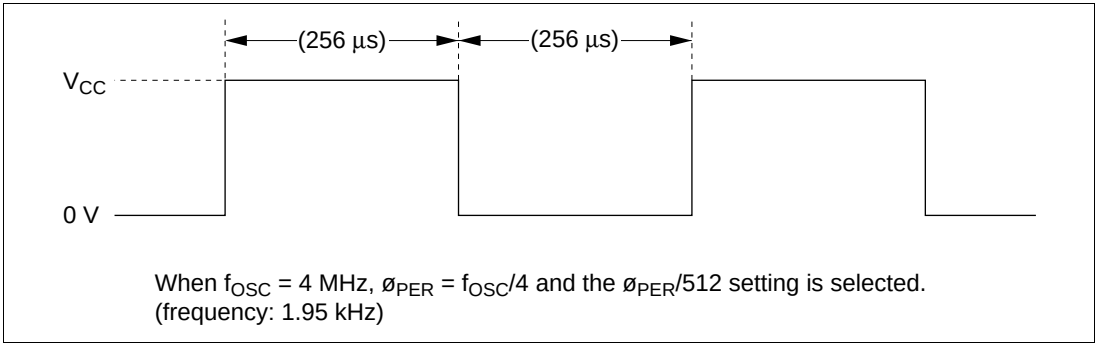


Figure 21-2 Alarm Output Waveform Example

Section 22 ROM

22.1 Overview

Table 22-1 lists the built-in ROM provided by the HMCS43XX Family microcomputers.

Table 22-1 Built-in ROM

HD404344R/HD404394 Series

Product Number			
HD404344R Series	**HD404394 Series**	**Capacity**	**ROM Type**
HD404341RS	HD404391S	1,024 words	Mask ROM
HD404341RFP	HD404391FP		
HD404341RFT	HD404391FT		
HD40C4341RS			
HD40C4341RFP			
HD40C4341RFT			
HD404342RS	HD404392S	2,048 words	
HD404342RFP	HD404392FP		
HD404342RFT	HD404392FT		
HD40C4342RS			
HD40C4342RFP			
HD40C4342RFT			
HD404344RS	HD404394S	4,096 words	
HD404344RFP	HD404394FP		
HD404344RFT	HD404394FT		
HD40C4344RS			
HD40C4344RFP			
HD40C4344RFT			
HD4074344S	HD4074394S	4,096 words	ZTAT™*
HD4074344FP	HD4074394FP		
HD4074344FT	HD4074394FT		

Note: * ZTAT™ is a registered trademark of Hitachi, Ltd.

Table 22-1 Built-in ROM (cont)

HD404318 Series

Product Number	Capacity	ROM Type
HD404314S	4,096 words	Mask ROM
HD404314H		
HD404316S	6,144 words	
HD404316H		
HD404318S	8,192 words	
HD404318H		
HD4074318S	8,192 words	ZTAT™*
HD4074318H		

Note: * ZTAT™ is a registered trademark of Hitachi, Ltd.

HD404358 Series

Product Number	Capacity	ROM Type
HD404354S/HD40A4354S	4,096 words	Mask ROM
HD404354H/HD40A4354H		
HD404356S/HD40A4356S	6,144 words	
HD404356H/HD40A4356H		
HD404358S/HD40A4358S	8,192 words	
HD404358H/HD40A4358H		
HD407A4359S	16,384 words	ZTAT™*
HD407A4359H		

Note: * ZTAT™ is a registered trademark of Hitachi, Ltd.

Table 22-1 Built-in ROM (cont)

HD404358R Series

Product Number	Capacity	ROM Type
HD404354RS/HD40A4354RS/HD40C4354RS	4,096 words	Mask ROM
HD404354RH/HD40A4354RH/HD40C4354RH		
HD404356RS/HD40A4356RS/HD40C4356RS	6,144 words	
HD404356RH/HD40A4356RH/HD40C4356RH		
HD404358RS/HD40A4358RS/HD40C4358RS	8,192 words	
HD404358RH/HD40A4358RH/HD40C4358RH		
HD407A4359RS/HD407C4359RS	16,384 words	ZTAT™*
HD407A4359RH/HD407C4359RH		

Note: * ZTAT™ is a registered trademark of Hitachi, Ltd.

HD404339 Series

Product Number	Capacity	ROM Type
HD404334S	4,096 words	Mask ROM
HD404334FS		
HD404336S	6,144 words	
HD404336FS		
HD404338S	8,192 words	
HD404338FS		
HD4043312S	12,288 words	
HD4043312FS		
HD404339S	16,384 words	
HD404339FS		
HD4074339S	16,384 words	ZTAT™*
HD4074339FS		

Note: * ZTAT™ is a registered trademark of Hitachi, Ltd.

Table 22-1 Built-in ROM (cont)

HD404369 Series

Product Number	Capacity	ROM Type
HD404364S/HD40A4364S	4,096 words	Mask ROM
HD404364F/HD40A4364F		
HD404368S/HD40A4368S	8,192 words	
HD404368F/HD40A4368F		
HD4043612S/HD40A43612S	12,288 words	
HD4043612F/HD40A43612F		
HD404369S/HD40A4369S	16,384 words	
HD404369F/HD40A4369F		
HD407A4369S	16,384 words	ZTAT™*
HD407A4369F		

Note: * ZTAT™ is a registered trademark of Hitachi, Ltd.

22.2 PROM Mode

22.2.1 PROM Mode

The HD4074344, HD4074394, HD4074318, HD407A4359, HD407A4359R, HD407C4359R, HD4074339, and HD407A4369 microcomputers support PROM mode. When these microcomputers are set to PROM mode, their microcomputer functions are stopped and they operate identically to the HN27C256 and HN27256 PROM products, thus allowing the internal PROM to be programmed.

Table 22-2 shows the method for switching these products to PROM mode.

Table 22-2 PROM Mode Setup Methods

HD4074344/HD4074394

Pin		Setting Level
Mode pin	$\overline{M}_0$ ($R3_1/AN_1$)	Low level
Reset pin	$\overline{RESET}$	

HD4074318/HD4074339

Pin		Setting Level
Mode pin	$\overline{M}_0$ ($D_0/\overline{INT}_0$)	High level
Mode pin	$\overline{M}_1$ ($D_1/\overline{INT}_1$)	
Reset pin	$\overline{RESET}$	Low level

HD407A4359/HD407A4359R/HD407C4359R/HD407A4369

Pin		Setting Level
Mode pin	$\overline{M}_0$ ($R4_1/AN_5$)	Low level
Mode pin	$\overline{M}_1$ ($R4_2/AN_6$)	
Reset pin	$\overline{RESET}$	

22.2.2 Socket Adapter Pin Correspondence and Memory Map

The on-chip PROM is programmed by using a socket adapter corresponding to the package type as shown in table 22-3. This converts the microcomputer to a 28-pin package thus allowing the use of a general-purpose PROM writer. Figures 22-1 to 22-5 show the socket adapter pin correspondences.

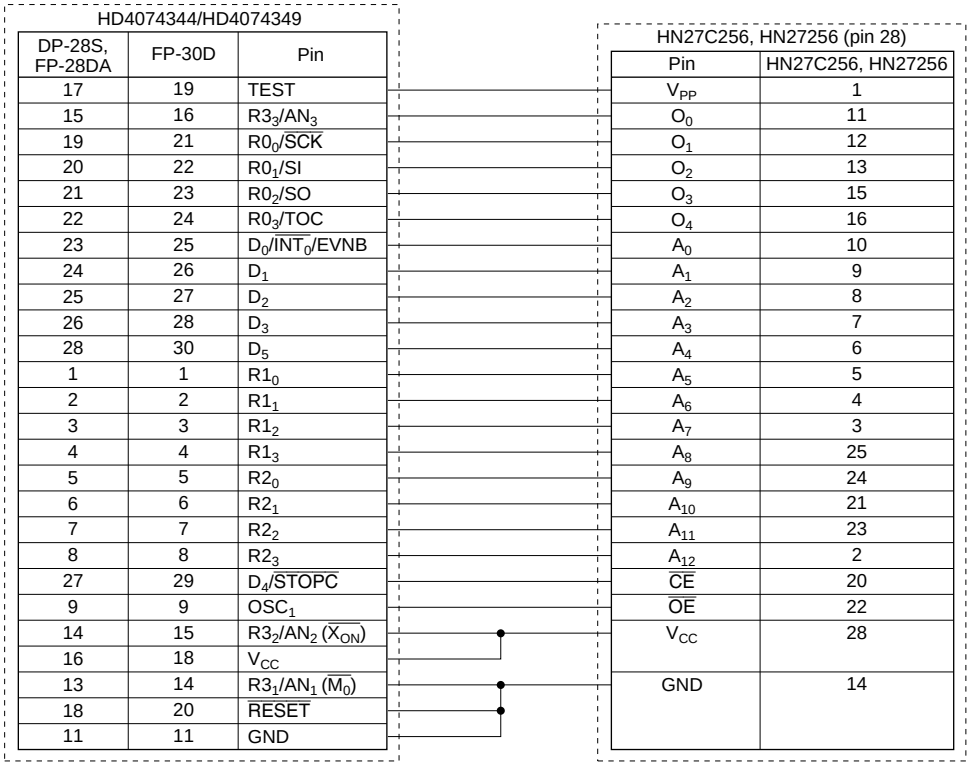
Since the HMCS400 Series instructions are 10-bit instructions, these products include an on-chip conversion circuit that allows a general-purpose PROM writer to be used. This circuit divides each instruction into upper and lower 5-bit segments and allows each segment to be programmed as a different address. Since the HD4074344 and HD4074394 have 4,096 words of PROM on chip, the PROM writer should be set for an 8-kbyte address space ($0000 to $1FFF). Since the HD4074318 has 8,192 words of PROM on chip, the PROM writer should be set for a 16-kbyte address space ($0000 to $3FFF). And since the HD407A4359, HD407A4359R, HD407C4359R, HD4074339, and HD407A4369 have 16,384 words of PROM on chip, the PROM writer should be set for a 32-kbyte address space ($0000 to $7FFF).

Figures 22-6 to 22-8 show the memory maps when these microcomputers are in PROM mode.

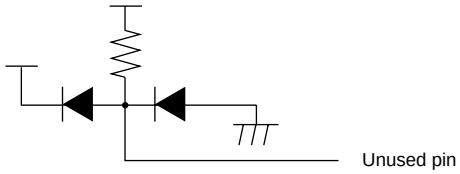
Table 22-3 Socket Adapters

Product Number	Package	Socket Adapter Product Number
HD4074344/HD4074394	DP-28S	HS4344ESS01H
	FP-28DA	HS4344ESP01H
	FP-30D	HS4344ESF01H
HD4074318	DP-42S	HS4318ESS01H
	FP-44A	HS4318ESH01H
HD407A4359/HD407A4359R/ HD407C4359R	DP-42S	HS4359ESS01H
	FP-44A	HS4359ESH01H
HD4074339	DP-64S	HS4339ESS01H
	FP-64B	HS4339ESF01H
HD407A4369	DP-64S	HS4369ESS01H
	FP-64B	HS4369ESF01H

Figure 22-1 shows the HD4074344 and HD4074394 socket adapter pin correspondence.



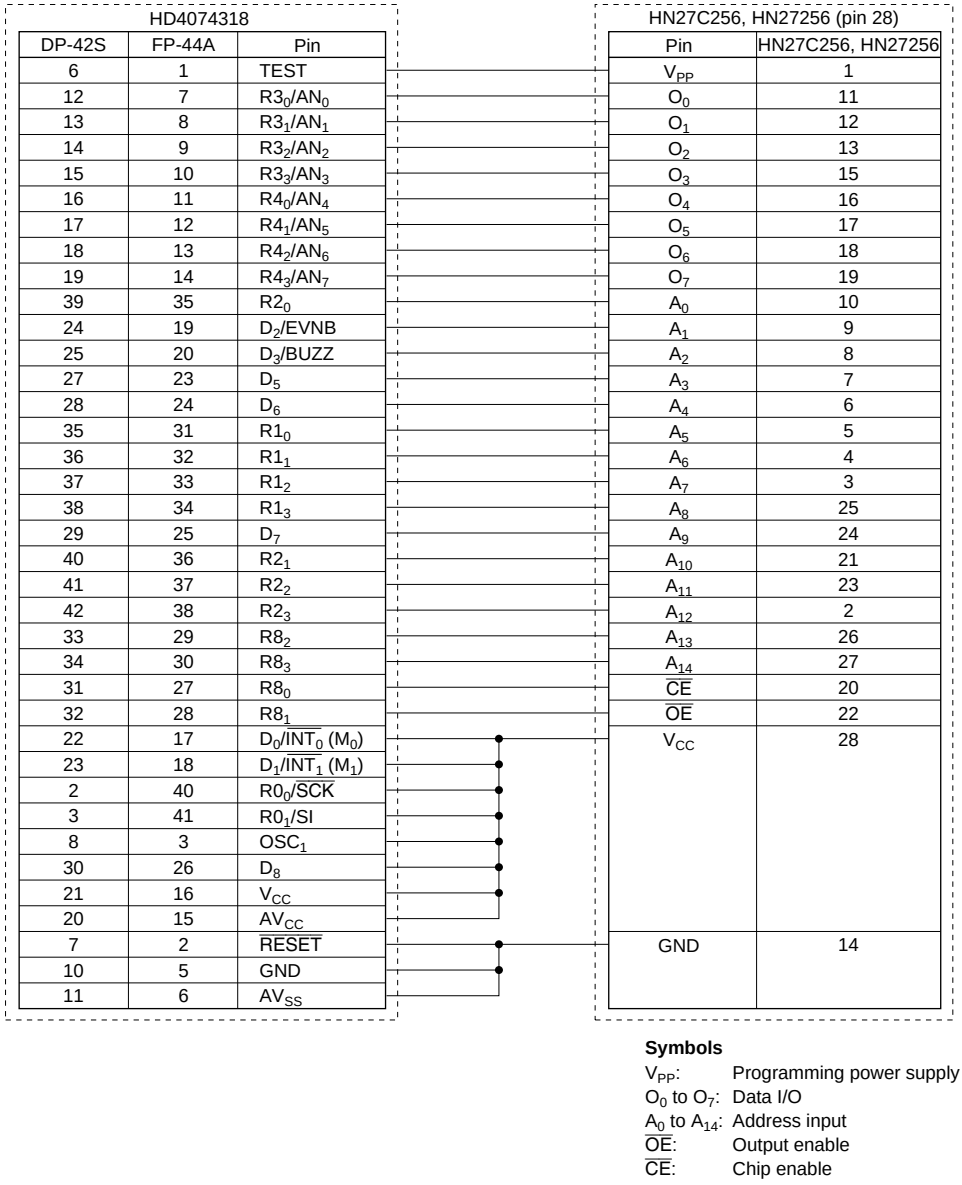
Notes: 1. The PROM adapter unused address pins (A_{13} and A_{14}) and unused data pins (O_5 to O_7) are connected inside the socket adapter with the circuit shown below.



2. Pins not specifically mentioned in the figure should be left open.

Figure 22-1 HD4074344 and HD4074394 Socket Adapter Pin Correspondence

Figure 22-2 shows the HD4074318 socket adapter pin correspondence.



Note: Pins not specifically mentioned in the figure should be left open.

Figure 22-2 HD4074318 Socket Adapter Pin Correspondence

Figure 22-3 shows the HD407A4359, HD407A4359R, and HD407C4359R socket adapter pin correspondence.

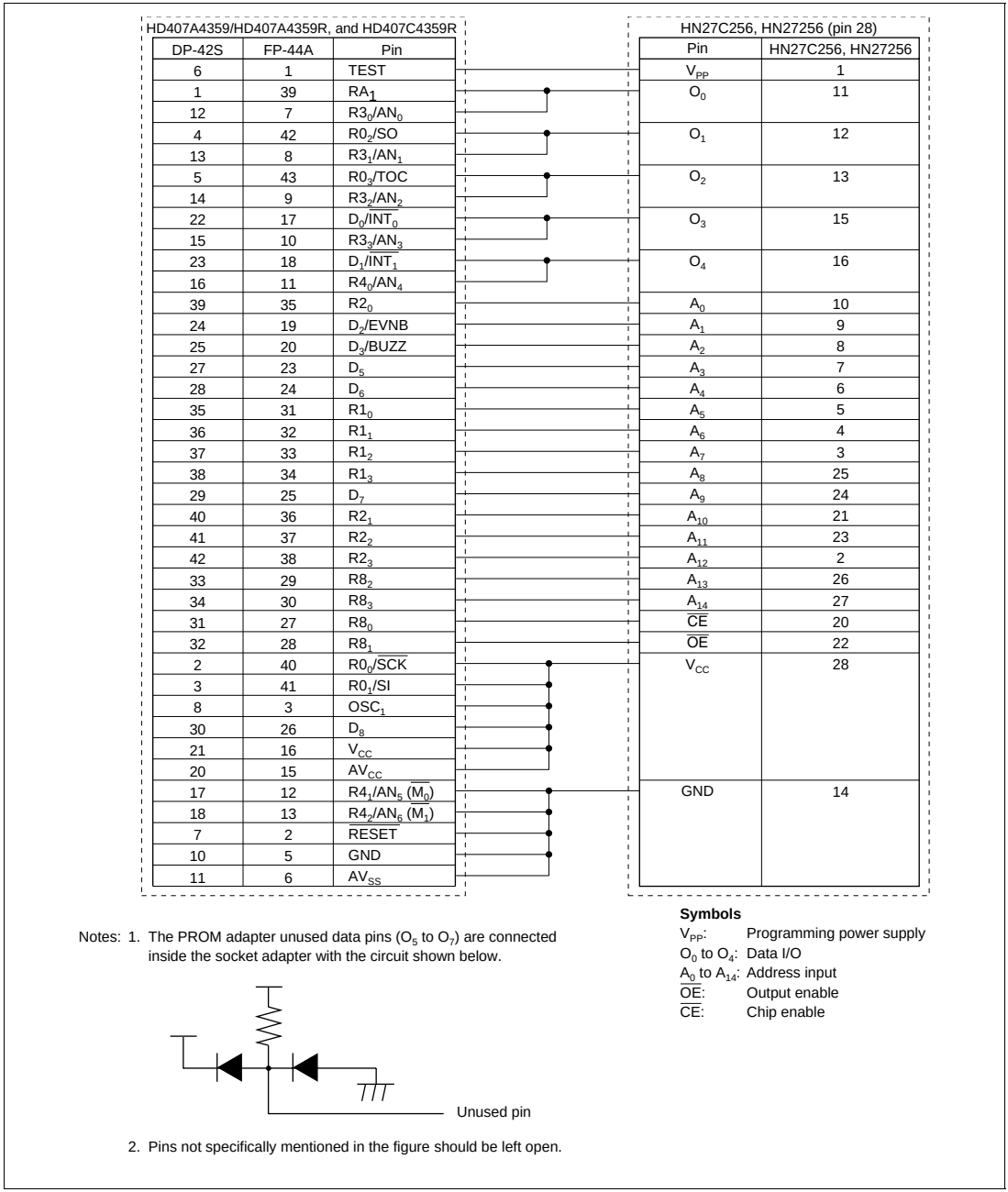
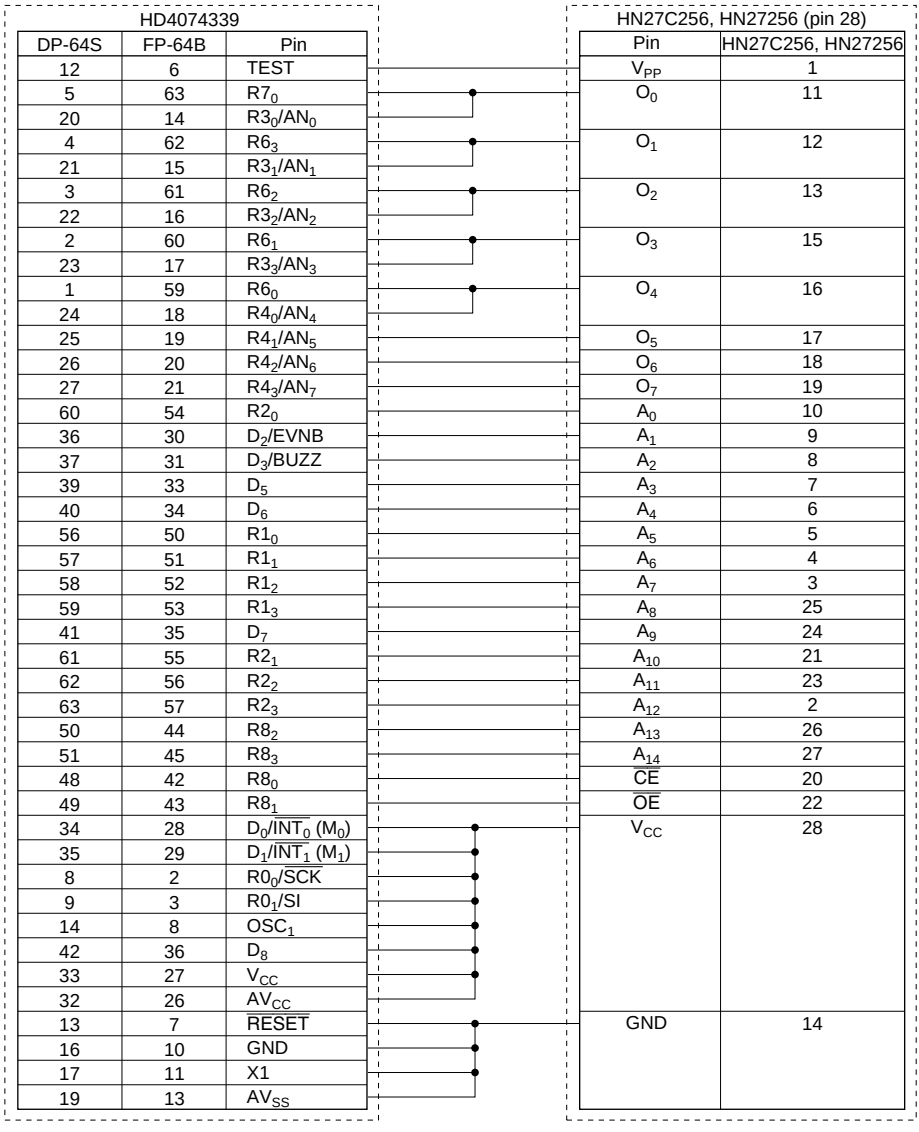


Figure 22-3 HD407A4359, HD407A4359R, and HD407C4359R Socket Adapter Pin Correspondence

Figure 22-4 shows the HD4074339 socket adapter pin correspondence.



HD4074339			HN27C256, HN27256 (pin 28)	
DP-64S	FP-64B	Pin	Pin	HN27C256, HN27256
12	6	TEST	V_{PP}	1
5	63	$R7_0$	O_0	11
20	14	$R3_0/AN_0$		
4	62	$R6_3$	O_1	12
21	15	$R3_1/AN_1$		
3	61	$R6_2$	O_2	13
22	16	$R3_2/AN_2$		
2	60	$R6_1$	O_3	15
23	17	$R3_3/AN_3$		
1	59	$R6_0$	O_4	16
24	18	$R4_0/AN_4$		
25	19	$R4_1/AN_5$	O_5	17
26	20	$R4_2/AN_6$	O_6	18
27	21	$R4_3/AN_7$	O_7	19
60	54	$R2_0$	A_0	10
36	30	D_2/EVNB	A_1	9
37	31	D_3/BUZZ	A_2	8
39	33	D_5	A_3	7
40	34	D_6	A_4	6
56	50	$R1_0$	A_5	5
57	51	$R1_1$	A_6	4
58	52	$R1_2$	A_7	3
59	53	$R1_3$	A_8	25
41	35	D_7	A_9	24
61	55	$R2_1$	A_{10}	21
62	56	$R2_2$	A_{11}	23
63	57	$R2_3$	A_{12}	2
50	44	$R8_2$	A_{13}	26
51	45	$R8_3$	A_{14}	27
48	42	$R8_0$	$\overline{CE}$	20
49	43	$R8_1$	$\overline{OE}$	22
34	28	$D_0/\overline{INT_0}$ (M_0)	V_{CC}	28
35	29	$D_1/\overline{INT_1}$ (M_1)		
8	2	$R0_0/\overline{SCK}$		
9	3	$R0_1$/SI		
14	8	OSC_1		
42	36	D_8		
33	27	V_{CC}		
32	26	AV_{CC}		
13	7	$\overline{RESET}$	GND	14
16	10	GND		
17	11	X1		
19	13	AV_{SS}		

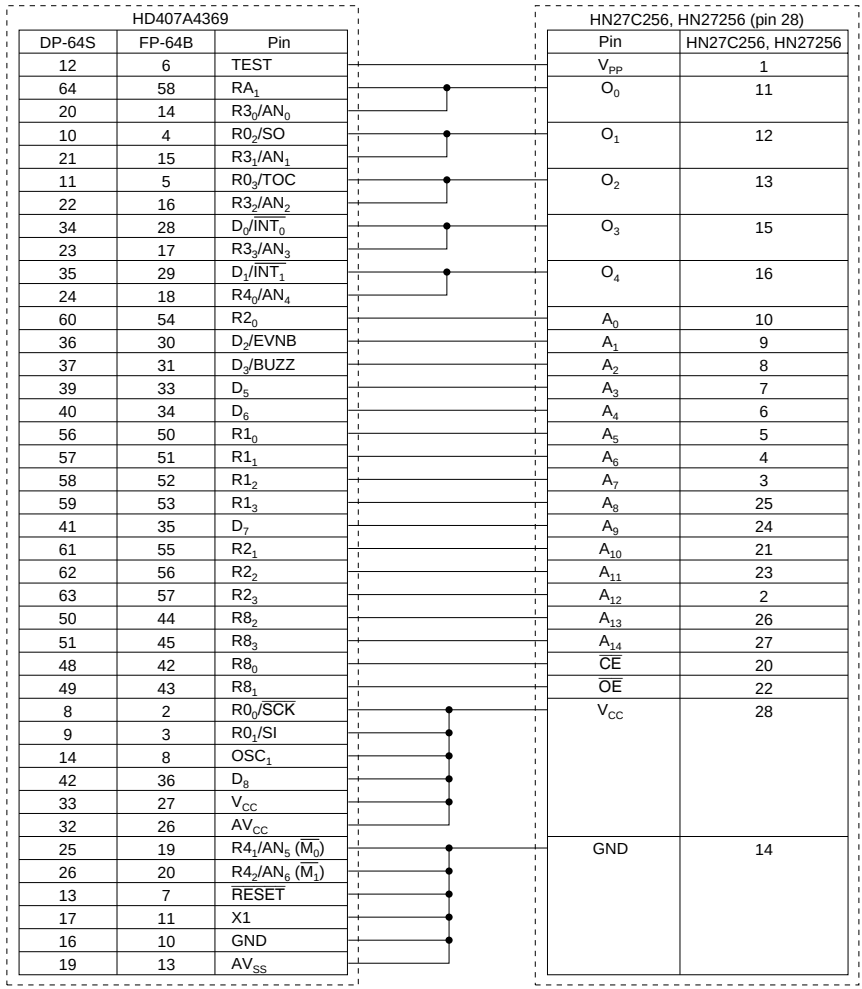
Symbols

V_{PP}:	Programming power supply
O_0 to O_7:	Data I/O
A_0 to A_{14}:	Address input
$\overline{OE}$:	Output enable
$\overline{CE}$:	Chip enable

Note: Pins not specifically mentioned in the figure should be left open.

Figure 22-4 HD4074339 Socket Adapter Pin Correspondence

Figure 22-5 shows the HD407A4369 socket adapter pin correspondence.

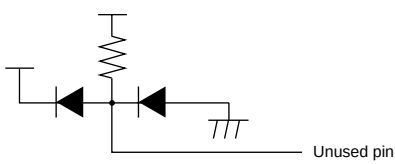


HD407A4369			HN27C256, HN27256 (pin 28)	
DP-64S	FP-64B	Pin	Pin	HN27C256, HN27256
12	6	TEST	V_{PP}	1
64	58	RA_1	O_0	11
20	14	$R3_0/AN_0$		
10	4	$R0_2/SO$	O_1	12
21	15	$R3_1/AN_1$		
11	5	$R0_3/TOC$	O_2	13
22	16	$R3_2/AN_2$		
34	28	$D_0/\overline{INT_0}$	O_3	15
23	17	$R3_3/AN_3$		
35	29	$D_1/\overline{INT_1}$	O_4	16
24	18	$R4_0/AN_4$		
60	54	$R2_0$	A_0	10
36	30	D_2/EVNB	A_1	9
37	31	D_3/BUZZ	A_2	8
39	33	D_5	A_3	7
40	34	D_6	A_4	6
56	50	$R1_0$	A_5	5
57	51	$R1_1$	A_6	4
58	52	$R1_2$	A_7	3
59	53	$R1_3$	A_8	25
41	35	D_7	A_9	24
61	55	$R2_1$	A_{10}	21
62	56	$R2_2$	A_{11}	23
63	57	$R2_3$	A_{12}	2
50	44	$R8_2$	A_{13}	26
51	45	$R8_3$	A_{14}	27
48	42	$R8_0$	$\overline{CE}$	20
49	43	$R8_1$	$\overline{OE}$	22
8	2	$R0_0/\overline{SCK}$	V_{CC}	28
9	3	$R0_1$/SI		
14	8	OSC_1		
42	36	D_8		
33	27	V_{CC}		
32	26	AV_{CC}		
25	19	$R4_1/AN_5$ ($\overline{M_0}$)	GND	14
26	20	$R4_2/AN_6$ ($\overline{M_1}$)		
13	7	$\overline{RESET}$		
17	11	X1		
16	10	GND		
19	13	AV_{SS}		

Symbols

V_{PP}:	Programming power supply
O_0 to O_4:	Data I/O
A_0 to A_{14}:	Address input
$\overline{OE}$:	Output enable
$\overline{CE}$:	Chip enable

Notes: 1. The PROM adapter unused data pins (O_5 to O_7) are connected inside the socket adapter with the circuit shown below.



2. Pins not specifically mentioned in the figure should be left open.

Figure 22-5 HD407A4369 Socket Adapter Pin Correspondence

Figure 22-6 shows the PROM mode memory map for the HD4074344 and the HD4074394.

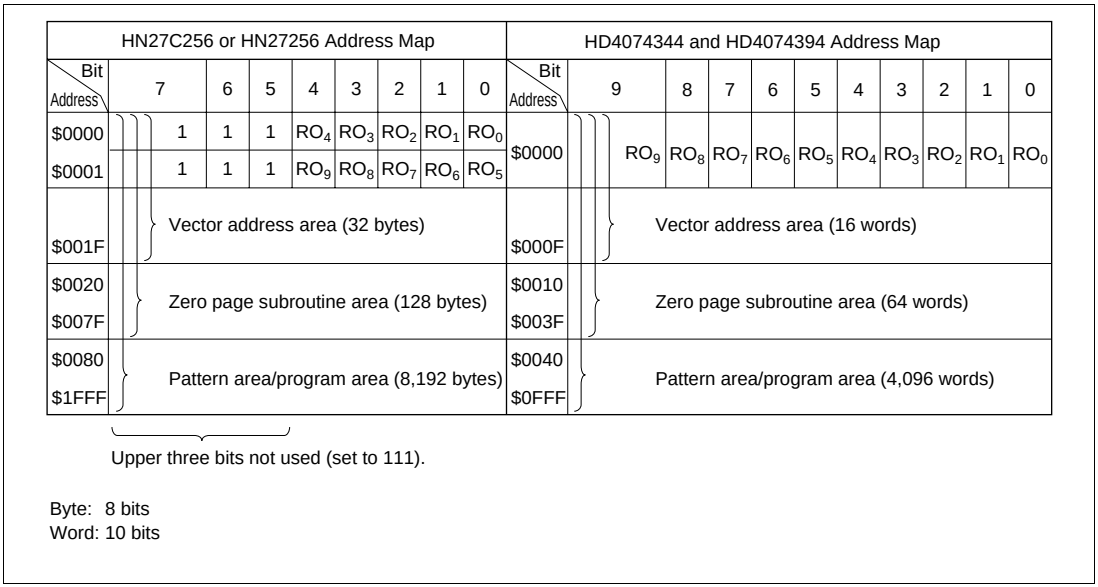


Figure 22-6 HD4074344 and HD4074394 PROM Mode Memory Map

Figure 22-7 shows the PROM mode memory map for the HD4074318.

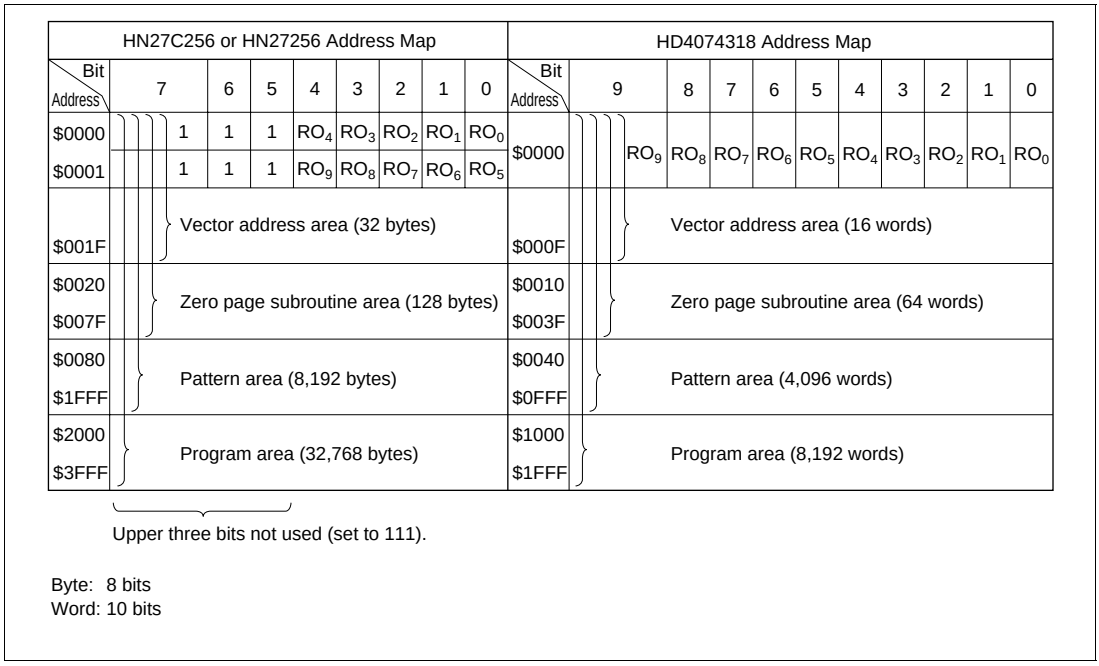


Figure 22-7 HD4074318 PROM Mode Memory Map

Figure 22-8 shows the PROM mode memory map for the HD407A4359, HD407A4359R, HD407C4359R, HD4074339, and HD407A4369.

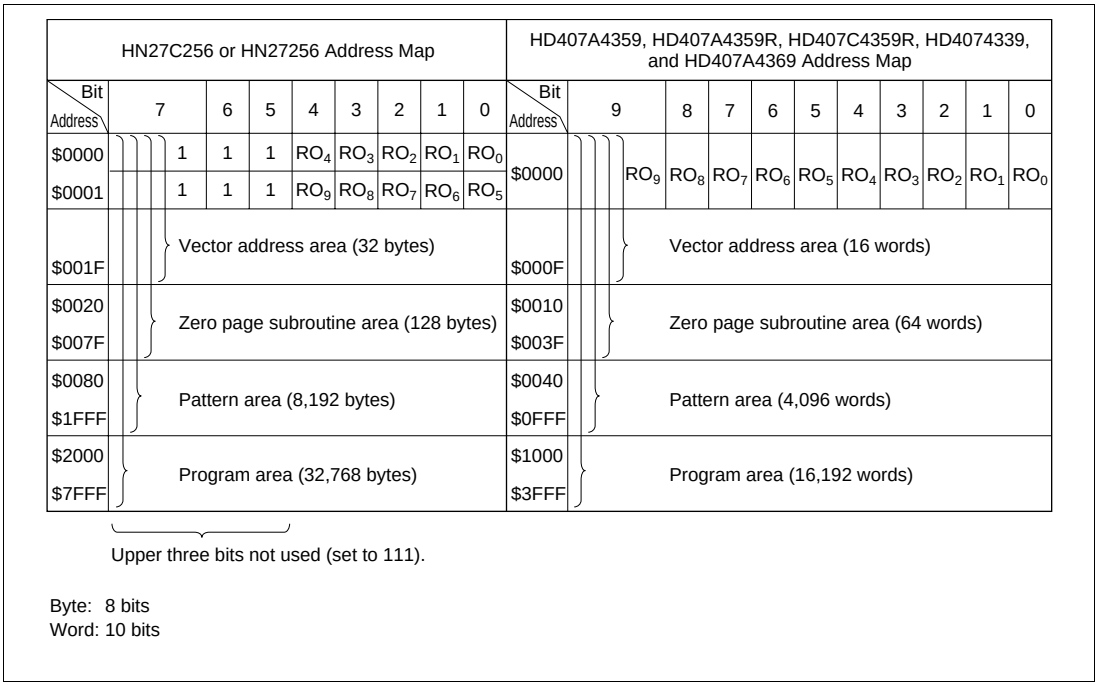


Figure 22-8 HD407A4359, HD407A4359R, HD407C4359R, HD4074339, and HD407A4369 PROM Mode Memory Map

22.3 Programming

Table 22-4 lists the settings used to select write, verify, and other modes when PROM programming.

Table 22-4 Write Mode Selection in PROM Mode

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	O_0 to O_7 (O_0 to O_4)*[1]	A_0 to A_{14} (A_0 to A_{12})*[2]
Write	L	H	Data input	Address input
Verify	H	L	Data output	Address input
Programming disable	H	H	High impedance	Address input

Symbols

L: Low level

H: High Level

Notes: 1. O_0 to O_7: Applies to the HD4074318 and HD4074339.
O_0 to O_4: Applies to the HD4074344, HD4074394, HD407A4359, HD407A4359R, HD407C4359R, and HD407A4369.

2. A_0 to A_{14}: Applies to the HD4074318, HD407A4359, HD407A4359R, HD407C4359R, HD4074339, and HD407A4369.
A_0 to A_{12}: Applies to the HD4074344 and HD4074394.

Note that write and read operations in PROM mode have the same specifications as the HN27C256 and HN27256 standard EPROM products.

22.3.1 Write/Verify

Write/verify mode provides efficient high-speed programming. With this method, high-speed writing can be performed without electrically stressing the device and without reducing data reliability. Data in unused regions is set to $FF. Figure 22-9 shows the basic flowchart for this high-speed programming technique. Tables 22-5 and 22-6 list the electrical characteristics during programming and figure 22-10 shows the timing.

Figure 22-9 shows the flowchart for high-speed programming.

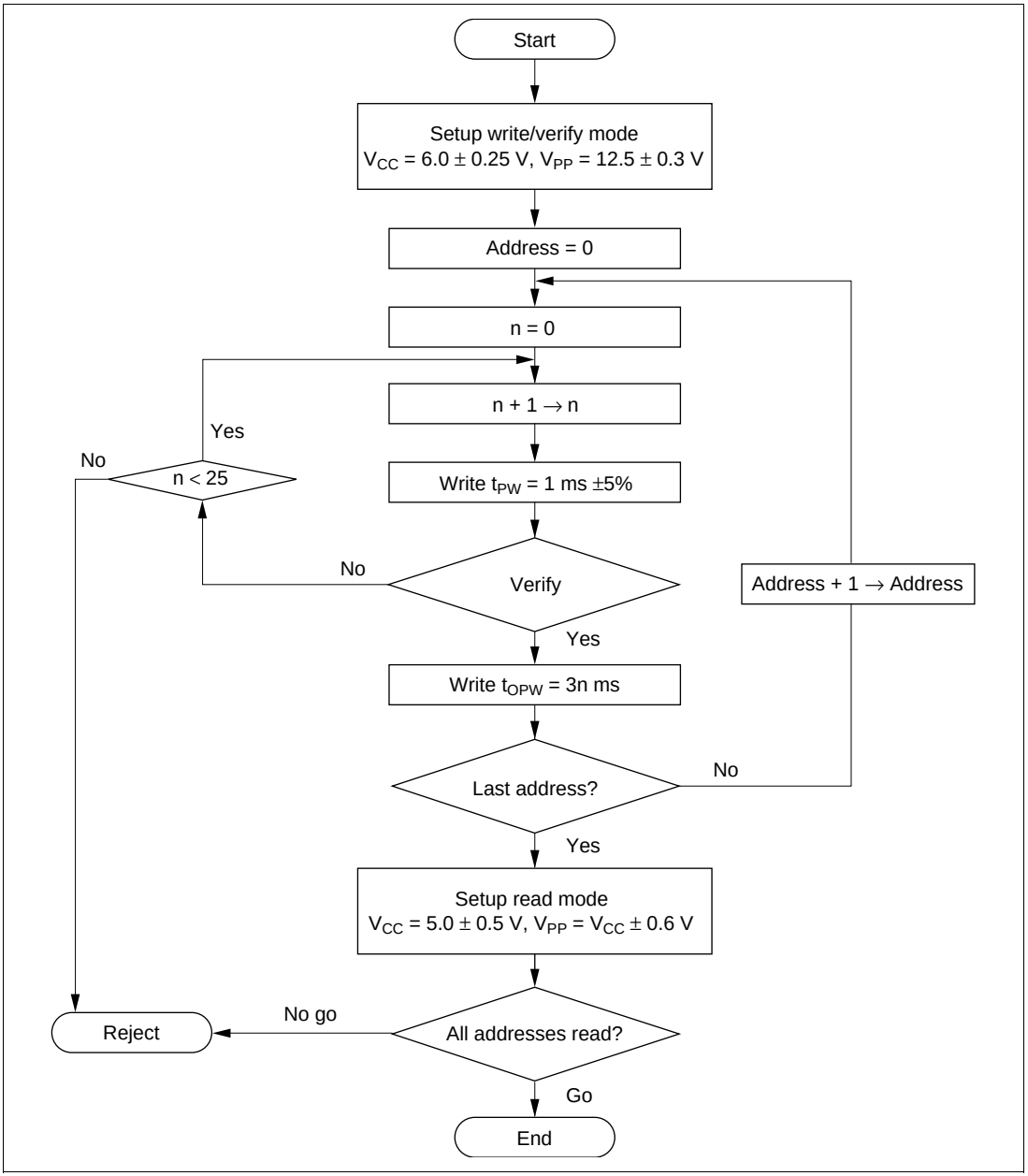


Figure 22-9 Flowchart for High-Speed Programming

Table 22-5 lists the DC characteristics and table 22-6 lists the AC characteristics.

Table 22-5 DC Characteristics

V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V, V_{SS} = 0 V, T_a = 25°C ±5°C, unless specified otherwise.

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input high level voltage	O_0 to O_7 (O_0 to O_4)*[1], A_0 to A_{14} (A_0 to A_{12})*[2], $\overline{OE}$, $\overline{CE}$	V_{IH}	2.2	—	V_{CC} + 0.3	V	
Input low level voltage	O_0 to O_7 (O_0 to O_4)*[1], A_0 to A_{14} (A_0 to A_{12})*[2], $\overline{OE}$, $\overline{CE}$	V_{IL}	–0.3	—	0.8	V	
Output high level voltage	O_0 to O_7 (O_0 to O_4)*[1]	V_{OH}	2.4	—	—	V	I_{OH} = –200 µA
Output low level voltage	O_0 to O_7 (O_0 to O_4)*[1]	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	O_0 to O_7 (O_0 to O_4)*[1], A_0 to A_{14} (A_0 to A_{12})*[2], $\overline{OE}$, $\overline{CE}$	$\lvert I_{IL} \rvert$	—	—	2	µA	V_{in} = 5.25 V/0.5 V
V_{CC} current		I_{CC}	—	—	30	mA	
V_{PP} current		I_{PP}	—	—	40	mA	

Notes: 1. O_0 to O_7: Applies to the HD4074318 and HD4074339.
O_0 to O_4: Applies to the HD4074344, HD4074394, HD407A4359, HD407A4359R, HD407C4359R, and HD407A4369.
2. A_0 to A_{14}: Applies to the HD4074318, HD407A4359, HD407A4359R, HD407C4359R, HD4074339, and HD407A4369.
A_0 to A_{12}: Applies to the HD4074344 and HD4074394.

Table 22-6 AC Characteristics

V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V, T_a = 25°C ±5°C, unless specified otherwise.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	µs	Figure 22-10*
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
Data output disable time	t_{DF}	—	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width during overprogramming	t_{OPW}	2.85	—	78.75	ms	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
Data output delay time	t_{OE}	0	—	500	ns	

Note: * Input pulse level: 0.8 to 2.2 V
Input rise/fall times ≤ 20 ns
Timing reference levels: Input: 1.0 V, 2.0 V
Output: 0.8 V, 2.0 V

Figure 22-10 shows the PROM write/verify timing.

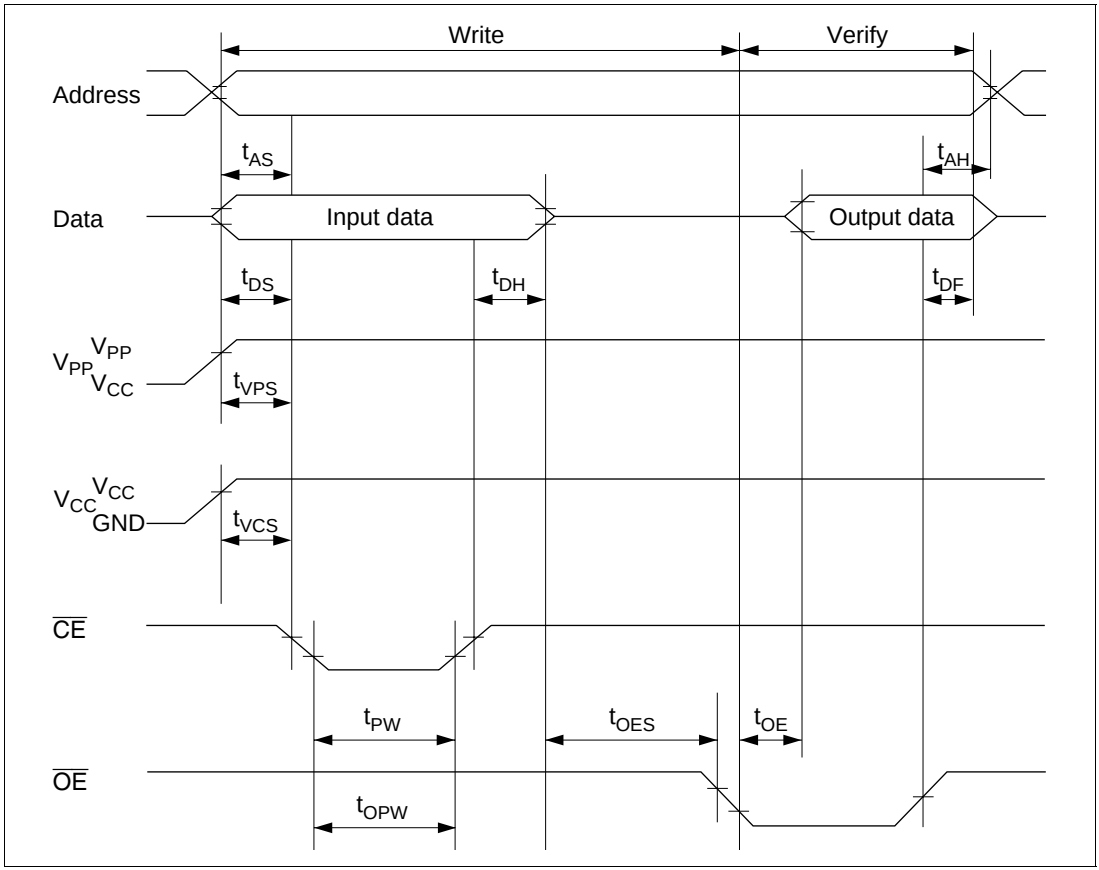


Figure 22-10 PROM Write/Verify Timing

22.3.2 PROM Programming Notes

- Use the stipulated voltages and times for PROM programming.

  The programming voltage (V_{PP}) in PROM mode is 12.5 V.

  The product may be permanently damaged if a voltage in excess of the rated voltage is applied. In particular, be especially careful of PROM writer overshoot.

  When the PROM writer is setup for either the Hitachi HN27256 or HN27C256, or the Intel specifications, V_{PP} will be 12.5 V.

- Make sure that the PROM writer, the socket adapter, and microcomputer chip are all aligned correctly, i.e., that their respective index marks match. Incorrect alignment can result in product damage due to overcurrents. Before writing, reconfirm that the product is correctly connected to the PROM writer.

- Do not touch the socket adapter or microcomputer during programming. This could cause contact faults that could result in programming failures.

22.3.3 Post-Programming Reliability

After programming, screening products by baking them at 150°C can be effective at improving data retention characteristics. Baking is one type of screening and allows early data retention failures in PROM memory cells to be caught in a short period.

Figure 22-11 shows the flowchart for the recommended screening procedure.

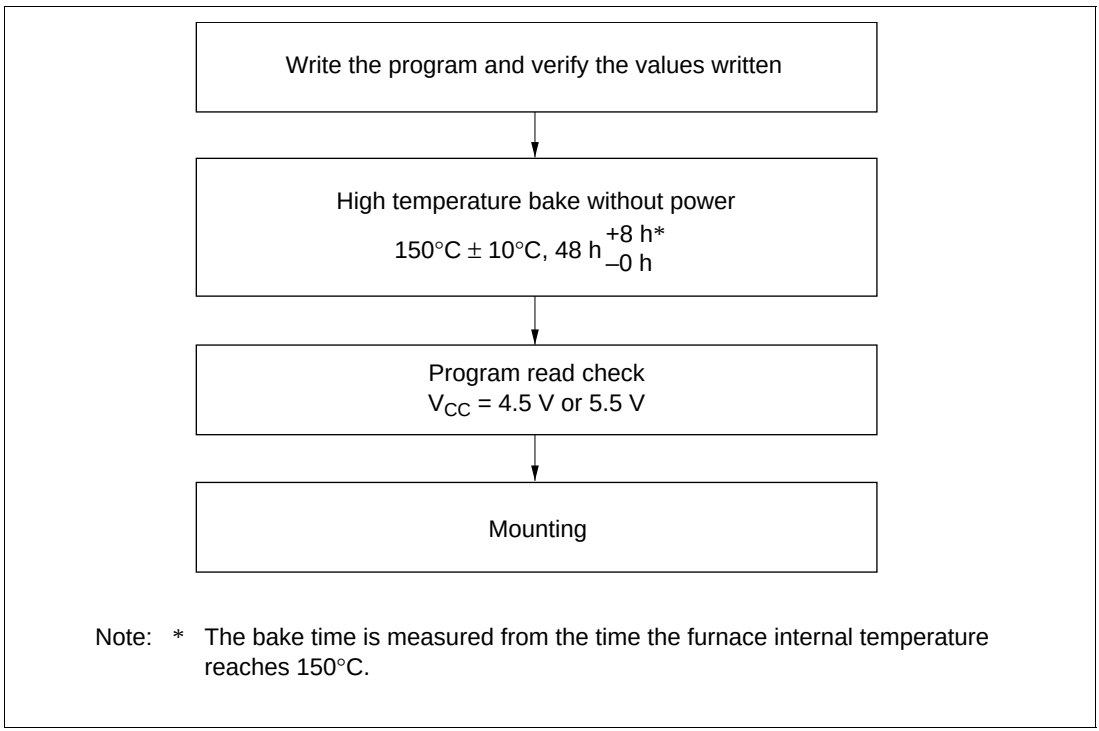


Figure 22-11 Recommended Screening Procedure

22.4 Notes on Ordering ROM

There are products in which data areas drawn on the mask and the ROM data actually used differ. Write 1s to the addresses in unused areas in the ROM data. This applies both when ordering using EPROMs and when ordering by sending data.

Figure 22-12 shows the ROM data configurations for the corresponding products.

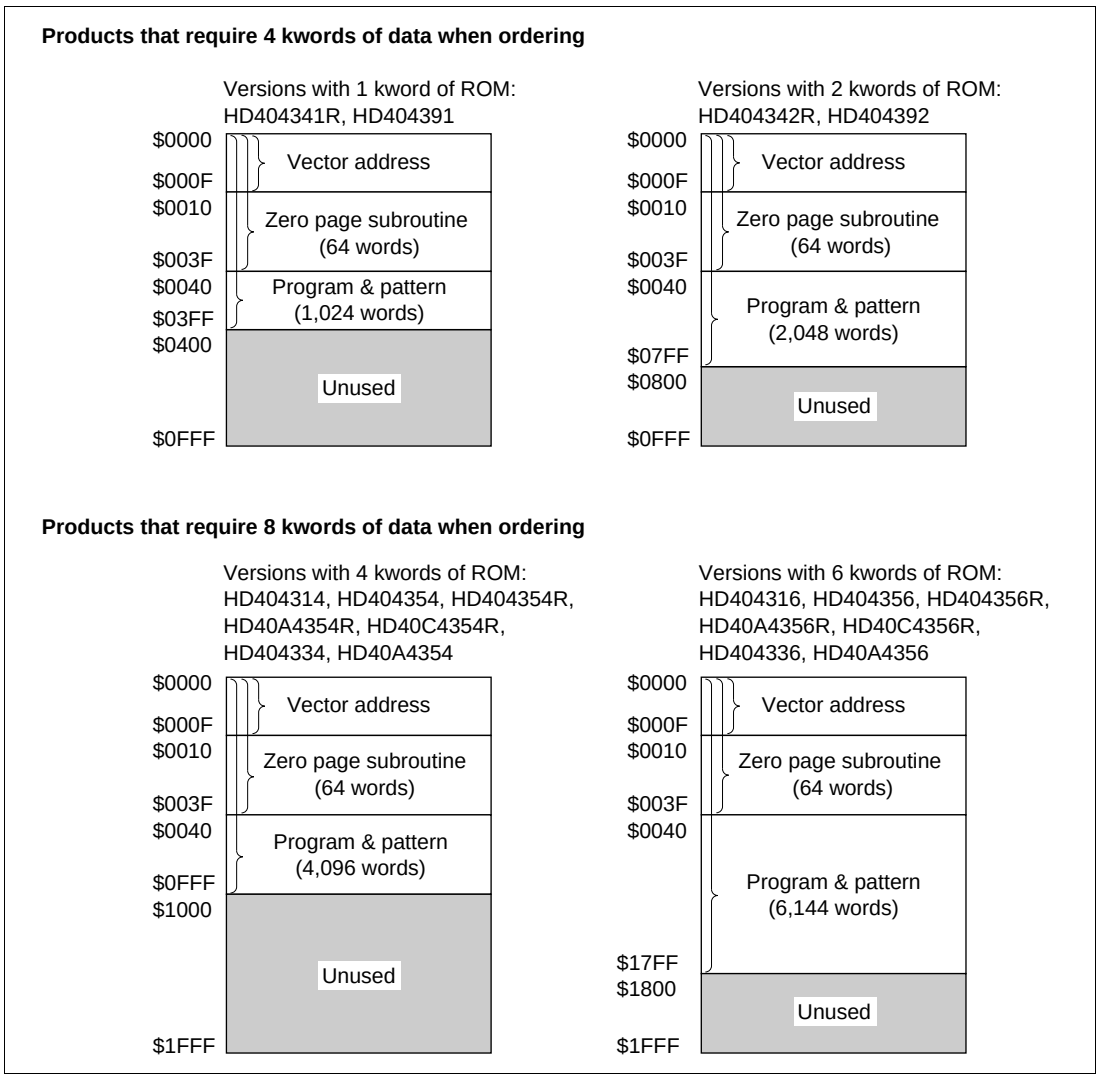


Figure 22-12 ROM Data Configurations (1)

Products that require 16 kwords of data when ordering

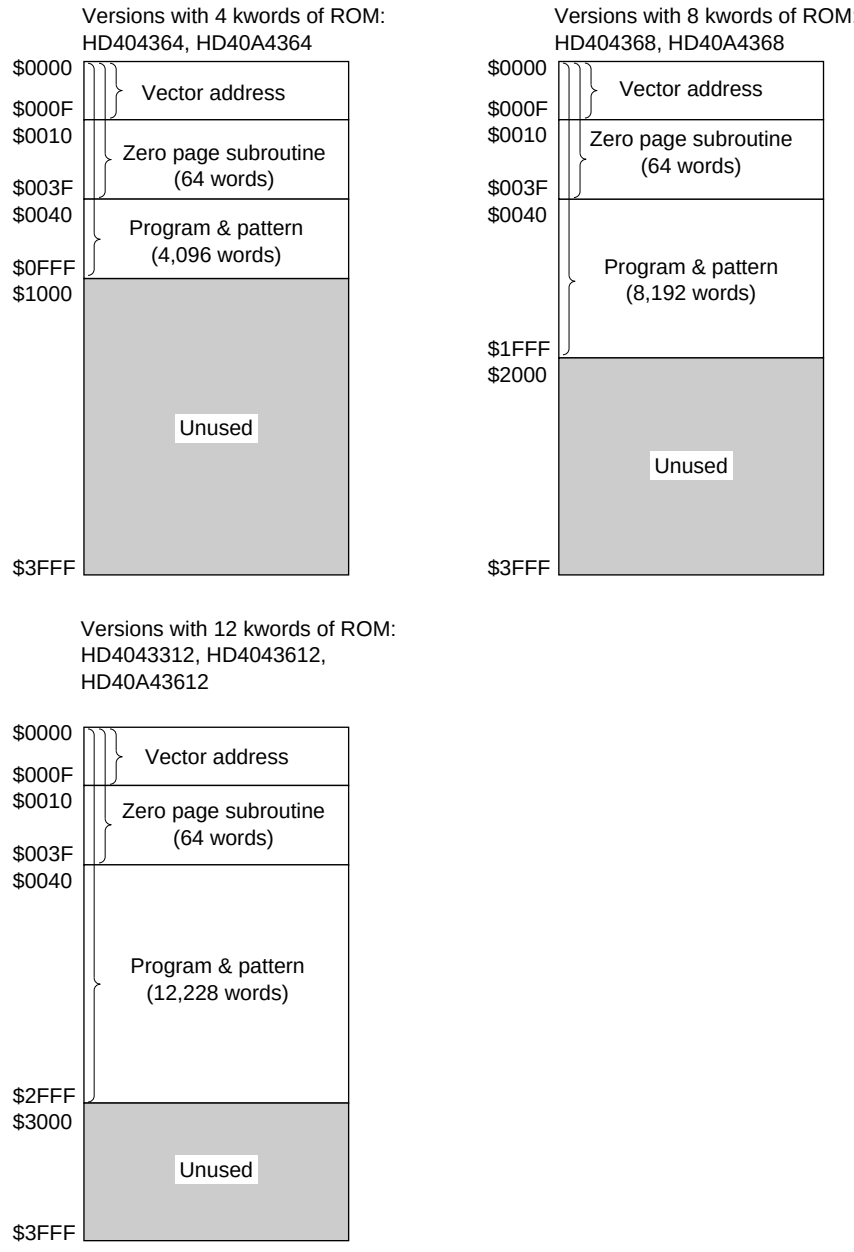


Figure 22-12 ROM Data Configurations (2)

Section 23 RAM

23.1 Overview

23.1.1 Features

The HMCS43XX Family RAM consists of three areas: the memory register area, the data area, and the stack area. The sizes of the memory register and stack areas are identical in all products in the HMCS43XX Family, but the size of the data areas differs between products.

Registers that control the system, interrupts, and the built-in peripheral modules are allocated in the RAM address space. This section describes the RAM areas other than the area used for these control registers.

The RAM areas have the following features.

- Memory register area (locations $040 to $04F)

  This is a 16 digit area that consists of the 16 memory registers (MR(0) to MR(15)). In addition to the usual RAM access instructions, the register to register instructions (LAMR and XMRA) can be used to access this area.

- Data area

  HD404344R/HD404394 Series

  The data area consists of 176 digits of memory at RAM addresses $050 to $0FF.

  HD404318 Series

  The data area consists of 304 digits of memory at RAM addresses $050 to $17F.

  HD404358 Series

  The data area consists of 304 digits of memory at RAM addresses $050 to $17F in products with 8,192 or fewer words of ROM, i.e., the HD404354, HD404356, HD404358, HD40A4354, HD40A4356, and HD40A4358.

  The data area consists of 432 digits of memory at RAM addresses $050 to $1FF in products with 12,288 or more words of ROM, i.e., the HD404359, HD40A4359, and HD407A4359.

  HD404358R Series

  The data area consists of 432 digits of memory at RAM addresses $050 to $1FF.

HD404339 Series

The data area consists of 432 digits of memory at RAM addresses $050 to $1FF.

HD404369 Series

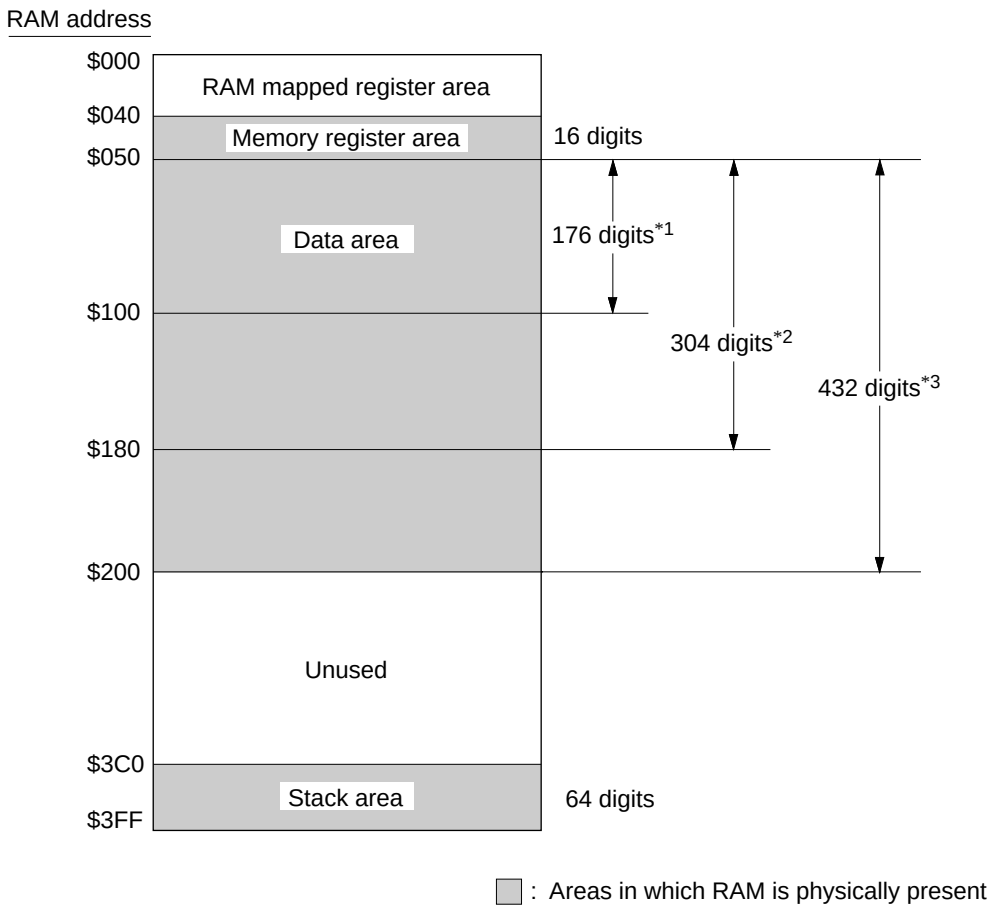
The data area consists of 432 digits of memory at RAM addresses $050 to $1FF.

- Stack area (locations $3C0 to $3FF)

  This area is used to save the program counter (PC), status (ST), and carry (CA) during subroutine calls and interrupt handling. Locations not used as stack area can be used as data area.

23.1.2 RAM Memory Map

Figure 23-1 shows the RAM memory map.



Notes: 1. Applies to the HD404344R and HD404394 Series.
2. Applies to all products in the HD404318 Series and to the HD404354, HD404356, HD404358, HD40A4354, HD40A4356, and HD40A4358 in the HD404358 Series.
3. Applies to all products in the HD404339 Series, to the HD407A4359 in the HD404358 Series, and to all products in the HD404358R Series, and to all products in the HD404369 Series.

Figure 23-1 RAM Memory Map

23.2 RAM Enable Flag (RAME: $021, 3)

The RAME flag shown in table 23-1 is a flag that indicates that the contents of RAM prior to the mode transition that cleared stop mode were maintained.

Table 23-1 RAM Enable Flag

Address	Flag	Symbol	R/W	Initial Value
$021, 3	RAM enable flag	RAME	R/W*	0

Note: * RAME is allocated in the register flag area and can only be manipulated with the RAM bit manipulation instructions. Only a value of 0 can be written to this flag, thus clearing it.

RAME is set to 1 when stop mode is cleared by a $\overline{\text{STOPC}}$ input. After clearing stop mode, a user program can be sure that the contents of RAM just before stop mode was entered were maintained by reading this flag and confirming that it was set to 1.

See the “RAM Enable Flag” items, sections 5.2.2 and 6.2.7, for more details on the RAME flag.

23.3 Usage Notes

Keep the following points in mind when using RAM.

- The contents of RAM are not guaranteed when power is first applied.
- The contents of RAM are not guaranteed after a reset.
- After power is turned on the values stored in the memory register area, data area, and stack area are undefined, regardless of whether a reset is input or not. It is essential to initialize these areas before use.

Section 24 Application Examples

24.1 Using the A/D Converter

This section describes the use of the A/D converter. Feel free to take advantage of the techniques presented here in user application systems.

This section has the following structure:

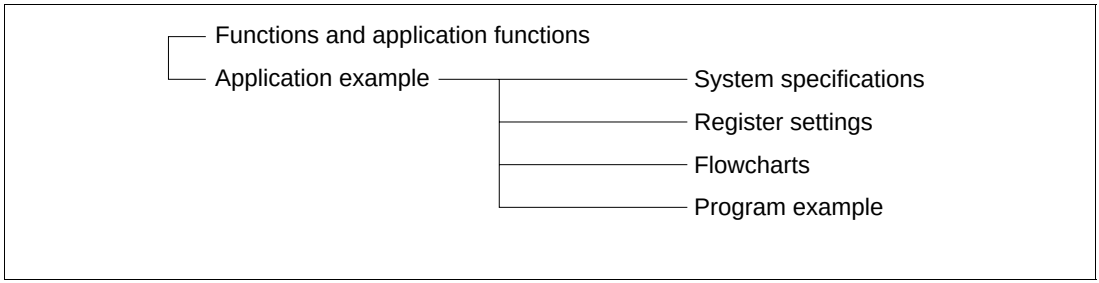


Figure 24-1 Application Example Organization

This application example uses an HD404339 Series microcomputer. While the techniques shown here apply equally to the HD404344R, HD404318, HD404358, HD404358R, and HD404369 Series microcomputers, the details of the register settings, clock settings, and pin arrangements would differ somewhat. See section 15, “A/D Converter”, for details.

Note: Although the operation of the program examples included in this section has been verified, their operation should be re-verified if they are used in an actual user system.

(1) Functions and Application Functions

- This application measures four analog input channels with an 8-bit resolution.
- This system can be used for various types of sensor detection applications (e.g., temperature or humidity) and key scan inputs.

(2) Application Example (Use of the 8-bit 4-Channel A/D Converter)

System Specifications

- The system stores the results of the 4-channel A/D conversions in RAM. Figure 24-2 shows the mapping of the RAM where the results are stored.

X \ Y	$3	$2	$1	$0
$A	(lower digit)			
$B	CH3 (upper digit)	CH2	CH1	CH0

Figure 24-2 RAM Mapping

- The completion of an A/D converter operation is detected by reading the A/D converter interrupt request flag. This application does not use interrupts.

Register Settings

- A/D mode register 1 (AMR1: $019)
- A/D mode register 2 (AMR2: $01A)
- A/D channel register (ACR: $016)
  The analog input pins and the A/D conversion time are specified by these three registers.

- A/D start flag (ADSF: $020, 2)
  Setting this flag starts an A/D conversion.
  1: A/D conversion start
  0: A/D conversion complete

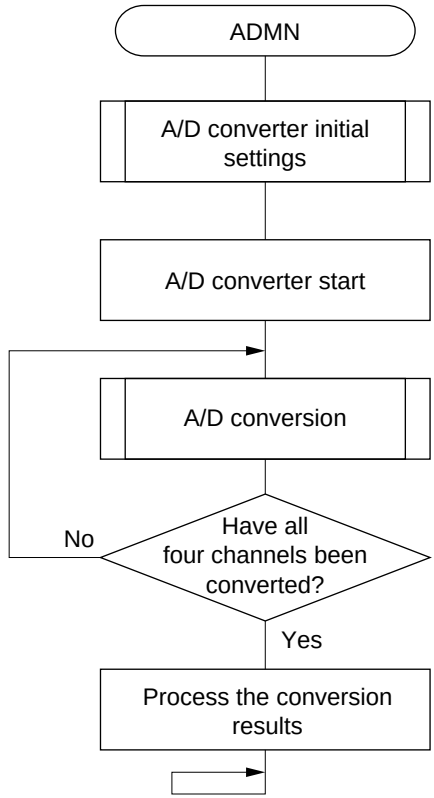
- A/D interrupt request flag (IFAD: $003, 0)
  Indicates that an A/D conversion has completed.
  1: A/D conversion complete
  0: A/D conversion in progress

- IAD off flag (IAOF: $021, 2)
  Controls the current in the A/D converter resistor ladder.

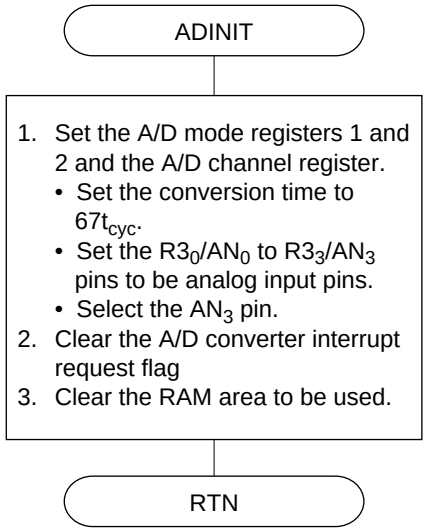
- A/D data register (ADRL: $017, ADRU: $018)
  Holds the result of an 8-bit A/D conversion.
  ADRL: Holds the lower 4 bits of an 8-bit A/D conversion.
  ADRU: Holds the upper 4 bits of an 8-bit A/D conversion.

Flowcharts

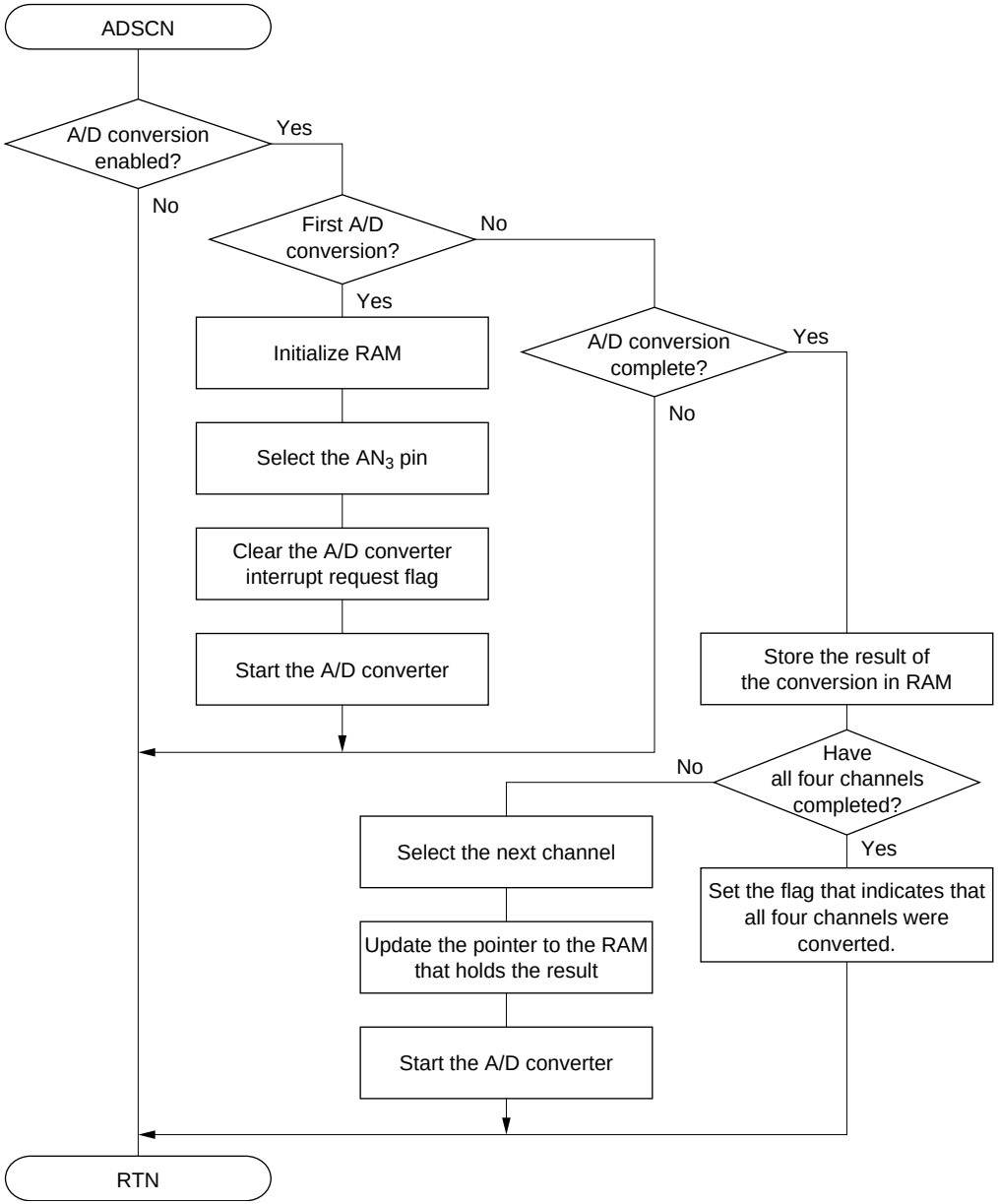
a. Main routine



b. A/D converter initial settings



c. A/D conversion



Sample Program

```
*  Symbol definitions
RSP     EQU     1,$000      * Stack pointer reset
IFAD    EQU     0,$003      * A/D interrupt request flag
ADSF    EQU     2,$020      * A/D start flag
IAOF    EQU     2,$021      * IAD off flag
AMR1    EQU     $019        * A/D mode register 1
AMR2    EQU     $01A        * A/D mode register 2
ACR     EQU     $016        * A/D channel register
ADRL    EQU     $017        * A/D data register (lower digit)
ADRU    EQU     $018        *  A/D data register (upper digit)

*  RAM mapping
ADCHNO  EQU     $0A4        * A/D conversion result storage address pointer
ADFLAG  EQU     $0B4        * Flag RAM
ADSTF   EQU     0,ADFLAG    * A/D start flag
AD1STF  EQU     1,ADFLAG    * A/D first flag
ADENDF  EQU     2,ADFLAG    * A/D end flag

*  Interrupt vector settings
        ORG     $0000
        JMPL    ADMN        * Reset vector address
        JMPL    ADMN        * INT0 interrupt vector address
        JMPL    ADMN        * INT1 interrupt vector address
        JMPL    ADMN        * Timer A interrupt vector address
        JMPL    ADMN        * Timer B interrupt vector address
        JMPL    ADMN        * Timer C interrupt vector address
        JMPL    ADMN        * A/D interrupt vector address
        JMPL    ADMN        * Serial interrupt vector address
```

* Main program

```
          ORG     $0100
ADMN      EQU     *
          REMD    RSP         * Stack pointer reset
          BR      *+1         * Status set
          CALL    ADINIT      * Call the ADINIT routine (Initializes the A/D
                                converter and RAM.)
          SEMD    ADSTF       * Start the A/D converter
ADMN01    CALL    ADSCN       * Call the ADSCN routine (Executes the A/D
                                conversions.)
          TMD     ADENDF      * A/D conversion completed?
          BRS     ADMN99      * If yes, branch to ADMN99.
          BRS     ADMN01      * If no, branch to ADMN01.
ADMN99    BRS     ADMN99
```

* ADINIT routine (Initializes the A/D converter and RAM.)

```
ADINIT    EQU     *
          LMID    $F,AMR1     * A/D mode register 1 (Sets the R3₀/AN₀ to R3₃/AN₃
                                pins to function as the AN₀ to AN₃ pins.)
          LMID    1, AMR2     * A/D mode register 2 (Sets the A/D conversion time
                                to be 67t_cyc.)
          LMID    3, ACR      * A/D channel register (Sets the analog input channel
                                to be AN₃.)
          REMD    IFAD        * Clear the A/D interrupt request flag.
          REMD    IAOF        * Clear the IAD off flag.
          LMID    0,ADFLAG    * Clear the usage flag.
          LMID    3,ADCHNO    * Initialize the pointer.
          RTN
```

* ADSCN routine (Executes the A/D conversions.)

```
ADSCN     EQU     *
          LWI     0           * Clear the W register.
          TMD     ADSTF       * Is ADSTF 1?
          BRS     ADSCN00     * If yes, branch to ADSCN00.
ADSCN99   RTN                 * If no, return to the main program.
ADSCN00   TMD     AD1STF      * Is AD1STF 1?
          BRS     ADSCN10     * If yes, branch to ADSCN10.
```

```
                *** First (channel 3) A/D conversion ***
                LMID    3,ACR       * A/D channel register
                REMD    IFAD        * A/D interrupt request flag
                SEMD    AD1STF      * Set AD1STF. (Indicates that the first A/D
                                      conversion is being performed.)
                LMID    3,ADCHNO    * Initialize the pointer.
                SEMD    ADSF        * Set the A/D start flag (Starts an A/D conversion.)
                BRS     ADSCN99     * Branch to ADSCN99.

                *** Channel 0 to 2 A/D conversions ***
ADSCN10         TMD     IFAD        * A/D interrupt request flag (Has the previous A/D
                                      conversion completed?)
                BRS     ADSCN11     * If yes, branch to ADSCN11.
                BRS     ADSCN99     * If no, branch to ADSCN99.

ADSCN11         REMD    IFAD        * Clear the A/D interrupt request flag.
                LXI     $A          * Specify the ADRL transfer destination RAM
                                      address (X).
                LAMD    ADCHNO      * Load the pointer.
                LYA                 * Specify the transfer destination RAM address (Y).
                LAMD    ADRL        * Move the ADRL value to the accumulator.
                LMA                 * Store the contents of the accumulator in RAM.
                LXI      $B         * Specify the ADRU transfer destination RAM
                                      address (X).
                LAMD    ADRU        * Move the ADRU value to the accumulator.
                LMADY               * Store the contents of the accumulator in RAM.
                                      Y ← Y — 1
                BRS     ADSCN12     * Branch to ADSCN12 if the A/D conversion has not
                                      completed.
                LMID    4,ADFLAG    * If the A/D conversion has completed, set ADENDF
                                      to 1, AD1STF to 0, and ADSTF to 0.
                BRS     ADSCN99     * Branch to ADSCN99.
```

```
ADSCN12  LAY                  * Move the next transfer destination RAM address
                                (Y) to the accumulator.
         LMAD     ADCHN0      * Update the pointer.
         LMAD     ACR         * Select the next A/D conversion channel.
         SEMD     ADSF        * Set the A/D start flag (Starts an A/D conversion.)
         BR       *+1         * Set the status.
         BRS      ADSCN99     * Branch to ADSCN99.
         END
```

24.2 Using Timer B

This section describes the use of timer B. Feel free to take advantage of the techniques presented here in user application systems.

This section has the following structure:

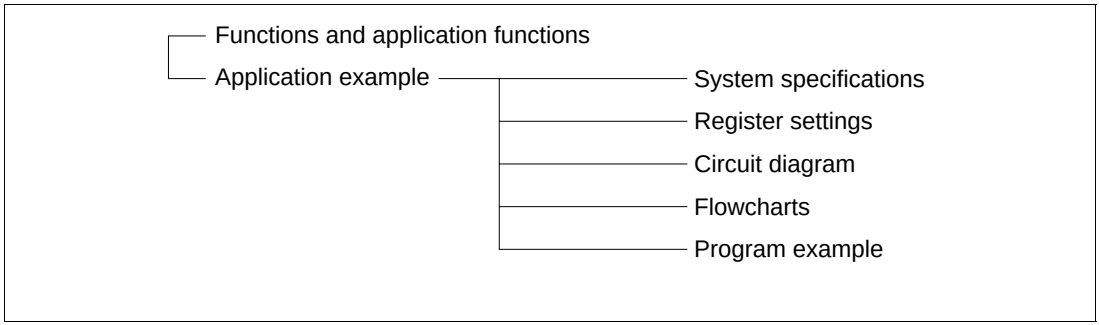


Figure 24-3 Application Example Organization

This application example uses an HD404339 Series microcomputer. While the techniques shown here apply equally to the HD404318, HD404358, HD404358R, and HD404369 Series microcomputers, the details of the register settings, clock settings, and pin arrangements would differ somewhat in the HD404318, HD404358, and HD404358R Series. See section 18, “Timer B”, for details.

Note: Although the operation of the program examples included in this section has been verified, their operation should be re-verified if they are used in an actual user system.

(1) Functions and Application Functions

- Free-running/reload timer ..... Key scan control, fixed time interrupts, and other functions
- External event counter ..... Pulse counter
- Input capture timer operation..... Measuring the time between trigger input edges.

(2) Application Example (Frequency Measurement Using Timer B)

This section presents an application that uses the HD4074339 timer B (in input capture timer mode) to determine the frequency of an input signal (square wave) and display the result in a pair of LEDs.

System Specifications

- The system clock used has a 1 MHz internal frequency based on a 4 MHz applied frequency.
- The signal to be measured is input to the EVNB pin, and the result of the frequency determination is output from the D port (pins D_5 and D_6) to be displayed on two LEDs connected to those pins.
- The input frequency is judged to be one of three levels as listed below, and the result is displayed in the LEDs.

  Overflow ..... Both LEDs off
  Under 1000 Hz..... One LED lit.
  1000 Hz or over ..... Two LEDs lit.

- Input capture mode is used for the timer B operating mode.

Register Settings

- A 4 MHz system clock oscillator frequency and a system clock divisor of 4 are used.

  The system clock selection register 1 (SSR1: $027) bit 1 is set.

  The system clock selection register 2 (SSR2: $028) is set to $0.

- The input clock period used is $8t_{cyc}$.

  Timer mode register B1 (TMB1: $009) is set to $4.

  This allows timer B to measure periods up to a maximum of 8 µs × 256 counts, which is 2040 µs (490 Hz), in 8 µs units.

- The timer is used in input capture mode and rising edge detection is used.

  Timer mode register B2 (TMB2: $026) is set to $6.

- The pull-up MOS transistors are set to be active by setting bit 3 in the miscellaneous register (MIS: $00C).

  Since the D_2/EVNB pin is used as the EVNB pin, the port mode register (PMRB: $024) bit 2 is set.

TMB1 Register Setting ($009)

Bit	TMB13	TMB12	TMB11	TMB10
Setting	0	1	0	0

TMB2 Register Setting ($026)

Bit	TMB23	TMB22	TMB21	TMB20
Setting	X	1	1	0

Figure 24-4 shows the timer B counter output.

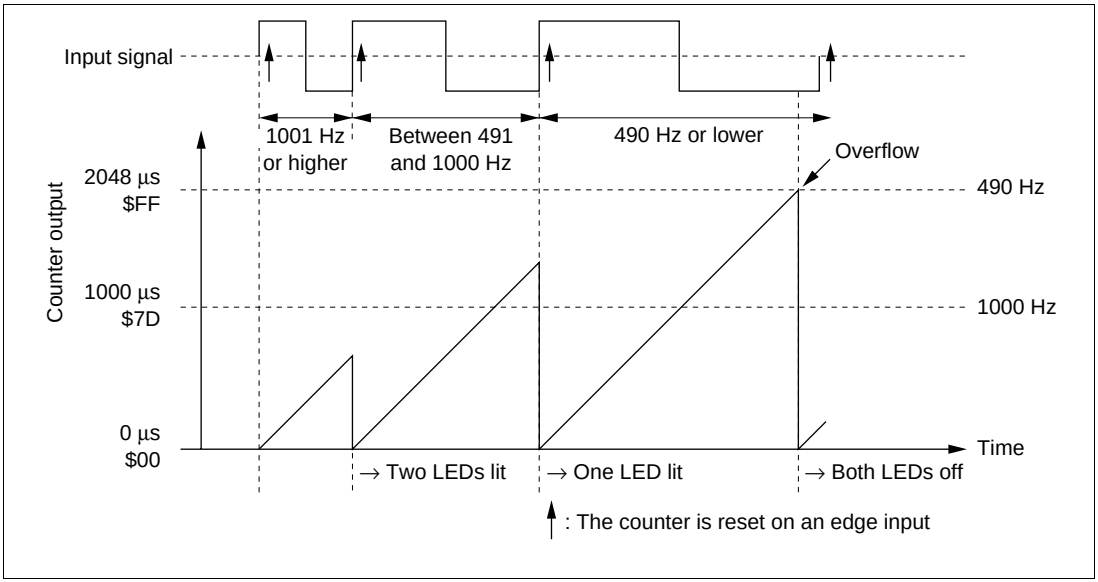


Figure 24-4 Timer B Counter Output

Frequency Determination Block Circuit Diagram: This circuit determines the frequency of a signal output from a pulse generator using an HD4074339.

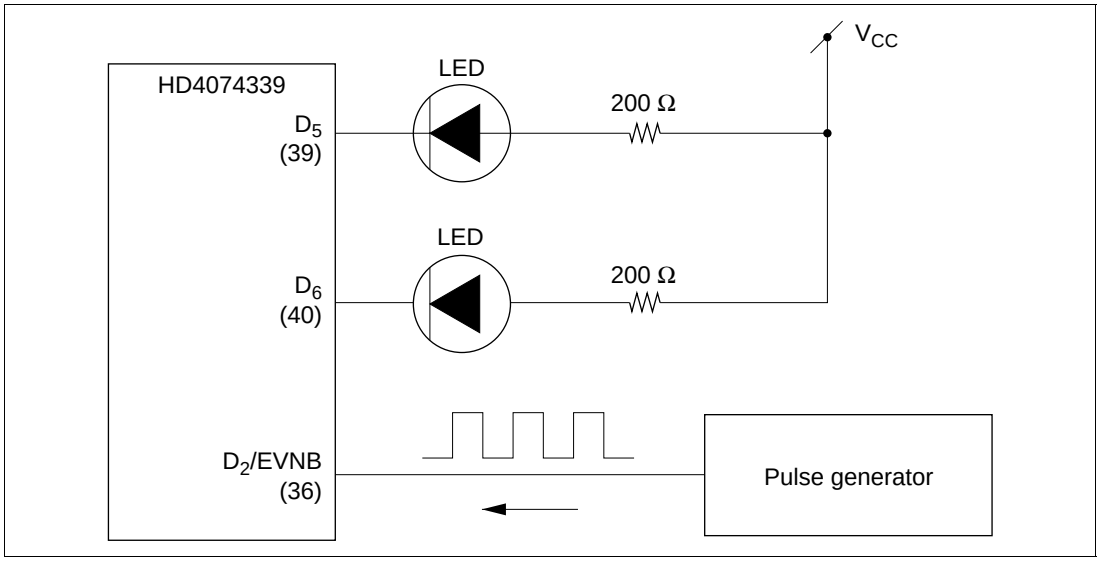
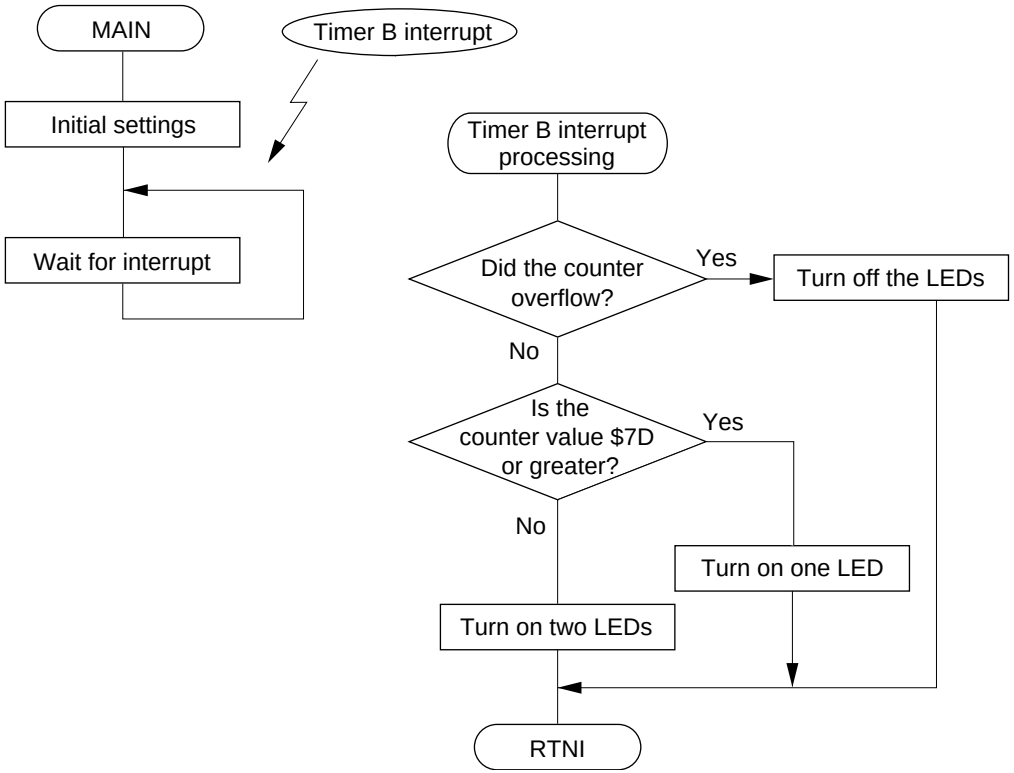


Figure 24-5 Frequency Determination Block Circuit Diagram

Flowcharts


MAIN
Timer B interrupt
Initial settings
Wait for interrupt
Timer B interrupt processing
Did the counter overflow?
Yes
Turn off the LEDs
No
Is the counter value $7D or greater?
Yes
No
Turn on one LED
Turn on two LEDs
RTNI

Sample Program

```
* Symbol definitions
  IE        EQU       $0,$000     * Interrupt enable flag
  IFTB      EQU       $0,$002     * Timer B interrupt flag
  IMTB      EQU       $1,$002     * Timer B interrupt mask
  MIS       EQU       $3,$00C     * Miscellaneous register
  TMB1      EQU       $009        * Timer mode register B1
  TRBL      EQU       $00A        * Timer read register BL
  TRBU      EQU       $00B        * Timer read register BU
  TMB2      EQU       $026        * Timer mode register B2
  ICEF      EQU       $1,$021     * ICT error flag
  ICSF      EQU       $0,$021     * ICT status flag
  PMRB      EQU       $024        * Port mode register B
  SSR1      EQU       $027        * System clock selection register 1
  SSR2      EQU       $028        * System clock selection register 2

* Interrupt vector settings
            ORG       $000
  STRV      JMPL      FDPROG      * Start vector address
            ORG       $008
  ICTV      JMPL      TBINT       * Timer B interrupt vector address

* Main program
            ORG       $1000
            LMID      $2,SSR1     * System clock: 4 MHz
            LMID      $0,SSR2     * System clock divisor: 4
            LMID      $4,TMB1     * Input clock period: 8tcyc
            LMID      $6,TMB2     * Set timer B to ICT mode with rising edge detection.

            LMID      $4,PMRB     * Pin mode: EVNB
            SEMD      MIS         * Pull-up MOS transistors active
            REMD      ICEF        * Reset the ICT error flag.
            REMD      ICSF        * Reset the ICT status flag.
            REMD      IMTB        * Reset the timer B interrupt mask.
            SEMD      IE          * IE = 1 (interrupts enabled)

  BINT      NOP                   * Interrupt wait loop
            JMPL      BINT
```

```
* Timer B interrupt handling routine
TBINT     REMD     IFTB       * Reset the timer B interrupt flag.
          TMD      ICEF       * If ICEF = 1
          BRL      SET0

COMPU     LAI      $7
          ALEMD    TRBU       * If $7 ≤ TRBU
          BRL      IFEQ
          JMPL     SET2
IFEQ      ANEMD    TRBU       * If $7 ≠ TRBU
          BRL      SET1
COMPL     LAI      $D
          ALEMD    TRBL       * If $D ≤ TRBL
          BRL      SET1
          JMPL     SET2
SET0      SEDD     $5         * Turn both LEDs off.
          SEDD     $6
          JMPL     TMEREND
SET1      REDD     $5         * Light one LED.
          SEDD     $6
          JMPL     TMEREND
SET2      REDD     $5         * Light both LEDs.
          REDD     $6

TMEREND   REMD     ICEF       * Reset the ICT error flag.
          REMD     ICSF       * Reset the ICT status flag.
          RTNI

          END
```

ICT: Input capture timer

$: Indicates a hexadecimal value.

25.1 HD404344R Series

25.1.1 Absolute Maximum Ratings

Table 25-1 lists the absolute maximum ratings of the HD404344R Series microcomputers.

Table 25-1 Absolute Maximum Ratings (HD404344R Series)

Item	Symbol	Rated Value	Unit	Notes
Power supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
Allowable total input current (current flowing in to the LSI)	$\sum I_0$	100	mA	3
Allowable total output current (current flowing out from the LSI)	$-\sum I_0$	30	mA	4
Allowable input current (current flowing in to the LSI)	I_0	30	mA	5, 6
		4	mA	5, 7
Allowable output current (current flowing out from the LSI)	$-I_0$	4	mA	8
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes:
1. Applies to the HD4074344 TEST (V_{PP}) pin.
2. Applies to D_0 to D_5, R0, R1, R2, and R3.
3. The allowable total input current is the sum of the currents flowing from all the I/O pins to ground at the same time.
4. The allowable total output current is the sum of the currents flowing from V_{CC} to all the I/O pins at the same time.
5. The allowable input current is the maximum value of the currents flowing from each I/O pin to ground.
6. Applies to D_1, D_2, R1, and R2.
7. Applies to D_0, D_3 to D_5, R0, and R3.
8. The allowable output current is the maximum value of the currents flowing from V_{CC} to each I/O pin.

Use of this LSI at levels that exceed the absolute maximum ratings can permanently damage the LSI. Also note that it is desirable to use this LSI within the conditions specified in the “Electrical Characteristics” section during normal operation. Exceeding those conditions can cause the LSI to operate incorrectly and may adversely affect LSI reliability.

All voltage values are referenced to ground.

25.1.2 Electrical Characteristics

(1) DC Characteristics

Tables 25-2 and 25-3 list the DC characteristics of the HD404344R Series microcomputers.

Table 25-2 DC Characteristics (HD404344R Series)

HD404344R, HD404342R, HD404341R, HD40C4344R,
HD40C4342R, HD40C4341R : V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD4074344 : V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{SCK}$, EVNB	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7 V_{CC}	—	V_{CC} + 0.3			
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3			
Input low level voltage	V_{IL}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{SCK}$, EVNB	–0.3	—	0.2 V_{CC}	V		
		SI	–0.3	—	0.3 V_{CC}			
		OSC_1	–0.3	—	0.5			
Output high level voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.5 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{SCK}$, SI, SO, EVNB, TOC, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Active mode current drain	I_{CC1}	V_{CC}	—	—	3.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2
	I_{CC2}		—	—	0.4		V_{CC} = 3 V, f_{OSC} = 400 kHz	2, 4
			—	—	0.5			2, 5

Table 25-2 DC Characteristics (HD404344R Series) (cont)

HD404344R, HD404342R, HD404341R, HD40C4344R,
HD40C4342R, HD40C4341R : V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD4074344 : V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Standby mode current drain	I_{SBY1}	V_{CC}	—	—	1.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3
	I_{SBY2}		—	—	0.2		V_{CC} = 3 V,	3, 4
			—	—	0.4		f_{OSC} = 400 kHz	3, 5
Stop mode current drain	I_{STOP}	V_{CC}	—	—	10	µA	V_{in} ($\overline{RESET}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (TEST) = 0 V to 0.3 V	
Stop mode data retention voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Except for the current flowing in the pull-up MOS transistors and output buffers.
2. The power supply current with the system in the reset state and no I/O currents flowing.

Test conditions	System state	Reset state
	Pin states	• RESET ..... At the ground potential • TEST ..... At the ground potential • D0 to D5, R0 to R3.. At the V_{CC} potential

3. The power supply current with the system timers operating and no I/O currents flowing.

Test conditions	System state	• I/O: The same as in the reset state • Standby mode
	Pin states	• $\overline{RESET}$ ..... At the V_{CC} potential • TEST ..... At the ground potential • D_0 to D_5, R0 to R3 .... At the V_{CC} potential

4. Applies to the HD4074344.
5. Applies to the HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, and HD40C4341R.

Table 25-3 Standard Pin I/O Characteristics (HD404344R Series)

HD404344R, HD404342R, HD404341R, HD40C4344R,
HD40C4342R, HD40C4341R : V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD4074344 : V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	D_0 to D_5, R0 to R3	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low level voltage	V_{IL}	D_0 to D_5, R0 to R3	–0.3	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	D_0 to D_5, R0 to R3	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	D_0 to D_5, R0 to R3	—	—	0.4	V	I_{OL} = 0.5 mA	
		D_1, D_2, R1, R2	—	—	2.0		I_{OL} = 15 mA, V_{CC} = 4.5 V to 5.5 V	
I/O leakage current	$\|I_{IL}\|$	D_0 to D_5, R0 to R3	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS transistor current	$-I_{PU}$	D_0 to D_5, R0 to R3	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	

Notes: 1. Except for the current flowing in the pull-up MOS transistors and output buffers.

(2) AC Characteristics

Tables 25-4 and 25-5 list the AC characteristics of the HD404344R Series microcomputers.

Table 25-4 AC Characteristics (HD404344R Series)

HD404344R, HD404342R, HD404341R, HD40C4344R,
HD40C4342R, HD40C4341R : V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD4074344 : V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Clock oscillator frequency (ceramic oscillator)	f_{OSC}	OSC_1, OSC_2	0.4	—	4.5	MHz	Clock divisor = 4	
Clock oscillator frequency (resistor oscillator)	f_{OSC}	OSC_1, OSC_2	1.0	2.0	3.5	MHz	Clock divisor = 4 R_f = 20 kΩ	
Instruction cycle time (ceramic oscillator, external clock)	t_{cyc}		0.89	—	10	µs	Clock divisor = 4	
Instruction cycle time (resistor oscillator)	t_{cyc}		1.14	—	4.0	µs	Clock divisor = 4 R_f = 20 kΩ	
Oscillator stabilization period (external clock)	t_{RC}	OSC_1, OSC_2	—	—	2.0	ms		1
Oscillator stabilization period (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	2.0	ms		1
Oscillator stabilization period (resistor oscillator)	t_{RC}	OSC_1, OSC_2	—	—	0.5	ms	R_f = 20 kΩ	1, 8
External clock high level width	t_{CPH}	OSC_1	92	—	—	ns		2

Table 25-4 AC Characteristics (HD404344R Series) (cont)

HD404344R, HD404342R, HD404341R, HD40C4344R,
HD40C4342R, HD40C4341R : V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD4074344 : V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
External clock low level width	t_{CPL}	OSC_1	92	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$, EVNB high level width	t_{IH}	$\overline{INT_0}$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT_0}$, EVNB low level width	t_{IL}	$\overline{INT_0}$, EVNB	2	—	—	t_{cyc}		3
Reset low level width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low level width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5
Reset rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		5
Input capacitance	C_{in}	All input pins other than TEST, and $R1_0$ to $R1_2$	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	15		f = 1 MHz, V_{in} = 0 V	6
			—	—	40			7
		$R1_0$ to $R1_2$	—	—	15		f = 1 MHz, V_{in} = 0 V	6
			—	—	30			7

Notes: 1. There are three cases where the oscillator stabilization period applies:

- When power is first applied, the time between the point when V_{CC} reaches $V_{CC\ min}$ and the point the oscillator is stable.
- When stop mode is cleared, the time between the point when the $\overline{RESET}$ input reaches the low level and the point the oscillator is stable.
- When stop mode is cleared, the time between the point when the $\overline{STOPC}$ input reaches the low level and the point the oscillator is stable.

To assure the time necessary to achieve stable oscillation at power on and when clearing stop mode, apply a low level to the $\overline{RESET}$ or $\overline{STOPC}$ input for at least t_{RC}.

Since the oscillator stabilization period varies with the details of the mounted circuit, stray capacitances, and other factors, this value should be determined based on thorough consultations with the manufacturer of the ceramic oscillator used.

2. See figure 25-1.
3. See figure 25-2.
4. See figure 25-3.
5. See figure 25-4.
6. Applies to the HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, and HD40C4341R.
7. Applies to the HD4074344.
8. Applies to the HD40C4344R, HD40C4342R, and HD40C4341R.

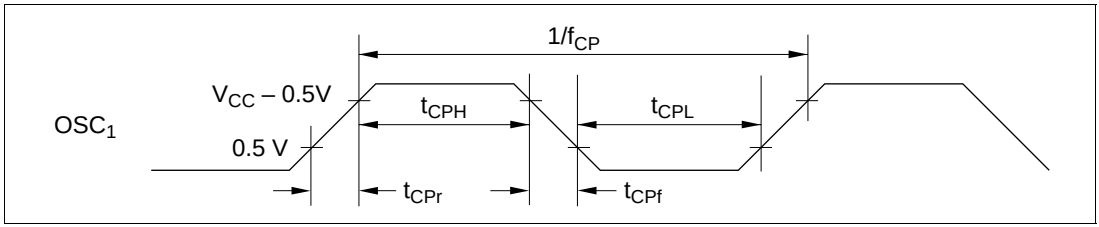


Figure 25-1 External Clock Timing (HD404344R Series)

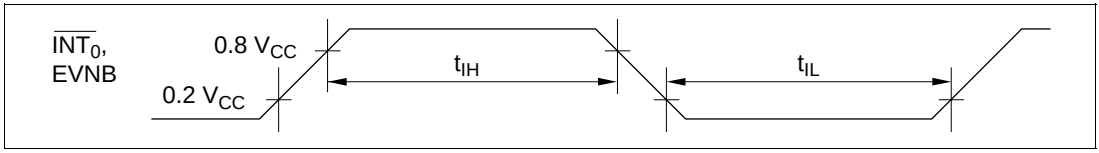


Figure 25-2 Interrupt Timing (HD404344R Series)

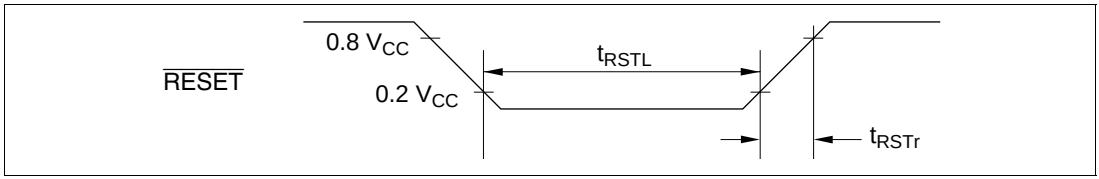


Figure 25-3 Reset Timing (HD404344R Series)

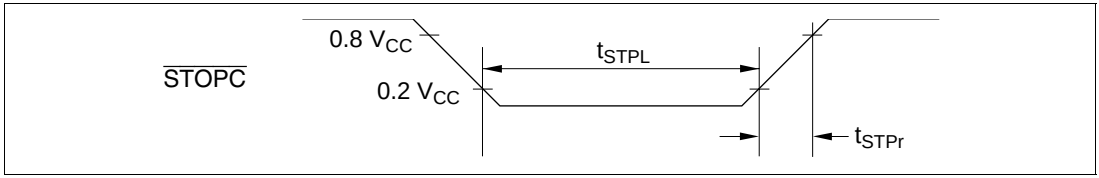


Figure 25-4 $\overline{\text{STOPC}}$ Timing (HD404344R Series)

Table 25-5 Serial Interface Timing Characteristics (HD404344R Series)

HD404344R, HD404342R, HD404341R, HD40C4344R,
HD40C4342R, HD40C4341R : V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD4074344 : V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

When the Transfer Clock is Output:

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	With the load shown in figure 25-6	1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-6	1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-6	1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-6	1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-6	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-6	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. See figure 25-5.

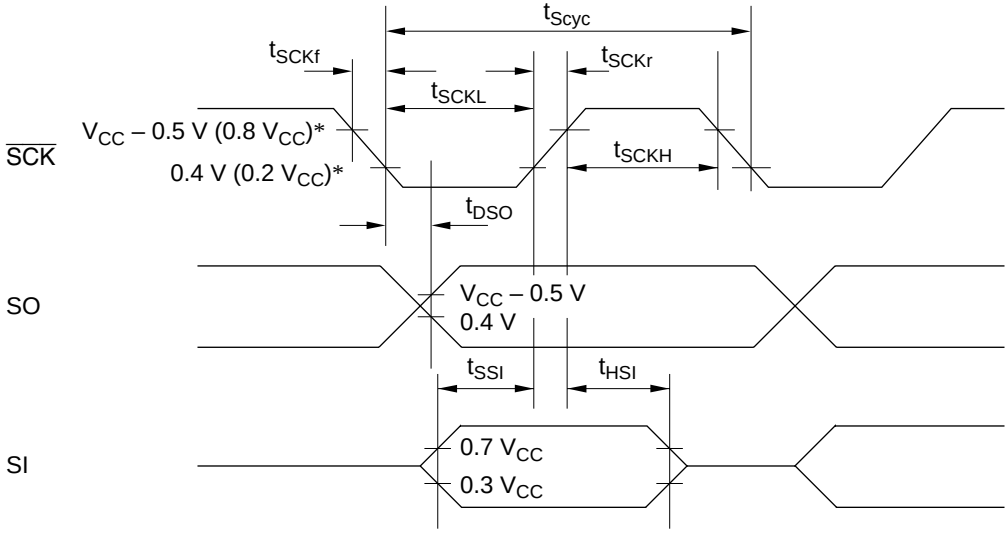
Table 25-5 Serial Interface Timing Characteristics (HD404344R Series) (cont)

HD404344R, HD404342R, HD404341R, HD40C4344R,
HD40C4342R, HD40C4341R : V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD4074344 : V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

When the Transfer Clock is Input:

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-6	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. See figure 25-5.



Note: * The values V_{CC} – 0.5 V and 0.4 V are the voltages for transfer clock output.
The values 0.8 V_{CC} and 0.2 V_{CC} are the voltages for transfer clock input.

Figure 25-5 Serial Interface Timing

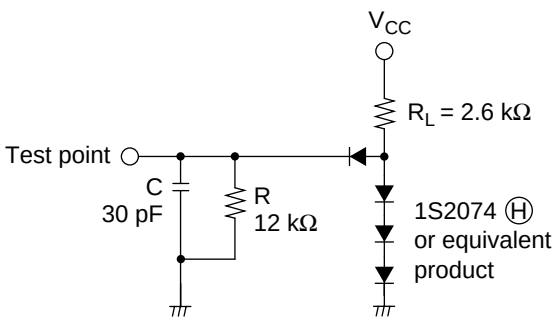


Figure 25-6 Timing Load Circuit

(3) A/D Converter Characteristics

Table 25-6 lists the characteristics of the HD404344R Series A/D converter.

Table 25-6 A/D Converter Characteristics (HD404344R Series)

HD404344R, HD404342R, HD404341R, HD40C4344R,
HD40C4342R, HD40C4341R : V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD4074344 : V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Analog input voltage	AV_{in}	AN_0 to AN_3	GND	—	V_{CC}	V		
Analog input capacitance	CA_{in}	AN_0 to AN_3	—	15	—	pF		
Resolution			—	8	—	Bits		
Number of inputs			0	—	4	Channels		
Absolute precision		AN_0 to AN_3	–2.0	—	2.0	LSB		1
			–2.5	—	2.5		T_a = 25°C, V_{CC} = 5.0 V	2
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0 to AN_3	1	—	—	MΩ	f_{OSC} = 1 Mhz, V_{in} = 0 V	

Notes: 1. Supplies to the HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, HD40C4341R.
2. Supplies to the HD4074344.

25.2 HD404394 Series

25.2.1 Absolute Maximum Ratings

Table 25-7 lists the absolute maximum ratings of the HD404394 Series microcomputers.

Table 25-7 Absolute Maximum Ratings (HD404394 Series)

Item	Symbol	Rated Value	Unit	Notes
Power supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		–0.3 to +15.0	V	3
Allowable total input current (current flowing in to the LSI)	$\sum I_0$	100	mA	4
Allowable total output current (current flowing in to the LSI)	$-\sum I_0$	30	mA	5
Allowable input current (current flowing in to the LSI)	I_0	30	mA	6, 7
		4	mA	6, 8
Allowable output current (current flowing out from the LSI)	$-I_0$	4	mA	9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes:
1. Applies to the HD4074394 TEST (V_{PP}) pin.
2. Applies to D_0 to D_5, R0, R13, R2, and $R3_1$ to $R3_3$.
3. Applies to $R1_0$ to $R1_2$.
4. The allowable total input current is the sum of the currents flowing from all the I/O pins to ground at the same time.
5. The allowable total output current is the sum of the currents flowing from V_{CC} to all the I/O pins at the same time.
6. The allowable input current is the maximum value of the currents flowing from each I/O pin to ground.
7. Applies to D_1, D_2, R1, and R2.
8. Applies to D_0, D_3 to D_5, R0, and $R3_1$ to $R3_3$.
9. The allowable output current is the maximum value of the currents flowing from V_{CC} to each I/O pin.

Use of this LSI at levels that exceed the absolute maximum ratings can permanently damage the LSI. Also note that it is desirable to use this LSI within the conditions specified in the “Electrical Characteristics” section during normal operation. Exceeding those conditions can cause the LSI to operate incorrectly and may adversely affect LSI reliability.

All voltage values are referenced to ground.

25.2.2 Electrical Characteristics

(1) DC Characteristics

Tables 25-8 to 25-10 list the DC characteristics of the HD404394 Series microcomputers.

Table 25-8 DC Characteristics (HD404394 Series)

V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{SCK}$, EVNB	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7 V_{CC}		V_{CC} + 0.3			
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3			
Input low level voltage	V_{IL}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{SCK}$, EVNB	–0.3	—	0.2 V_{CC}	V		
		SI	–0.3	—	0.3 V_{CC}			
		OSC_1	–0.3	—	0.5			
Output high level voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.5 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	$\overline{RESET}$, $\overline{STOPC}$, $\overline{SCK}$, $\overline{INT_0}$, SI, SO, EVNB, TOC, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Active mode current drain	I_{CC1}	V_{CC}	—	—	3.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2
	I_{CC2}		—	—	0.4		V_{CC} = 3 V, f_{OSC} = 400 kHz	

Table 25-8 DC Characteristics (HD404394 Series) (cont)

V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Standby mode current drain	I_{SBY1}	V_{CC}	—	—	1.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3
	I_{SBY2}		—	—	0.2		V_{CC} = 3 V, f_{OSC} = 400 kHz	
Stop mode current drain	I_{STOP}	V_{CC}	—	—	10	µA	V_{in} ($\overline{RESET}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (TEST) = 0 V to 0.3 V	
Stop mode data retention voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Except for the current flowing in the pull-up MOS transistors and output buffers.

2. The power supply current with the system in the reset state and no I/O currents flowing.

Test conditions	System state	Reset state
	Pin states	• $\overline{RESET}$ ..... At the ground potential • TEST ..... At the ground potential • D_0 to D_5, R_0 to R_3 ..... At the V_{CC} potential

3. The power supply current with the system timers operating and no I/O currents flowing.

Test conditions	System state	• I/O: The same as in the reset state • Standby mode
	Pin states	• $\overline{RESET}$ ..... At the V_{CC} potential • TEST ..... At the ground potential • D_0 to D_5, R0 to R3 .... At the V_{CC} potential

Table 25-9 Standard Pin I/O Characteristics (HD404394 Series)

V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	D_0 to D_5, R0, $R1_3$, R2, $R3_1$ to $R3_3$	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low level voltage	V_{IL}	D_0 to D_5, R0, $R1_3$, R2, $R3_1$ to $R3_3$	–0.3	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	D_0 to D_5, R0, $R3_1$ to $R3_3$	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
		$R1_3$, R2	V_{CC} – 0.5	—	—		500 kΩ at V_{CC}	
Output low level voltage	V_{OL}	D_0 to D_5, R0, $R1_3$, R2, $R3_1$ to $R3_3$	—	—	0.4	V	I_{OL} = 0.5 mA	
		D_1, D_2, $R1_3$, R2	—	—	2.0		I_{OL} = 15 mA, V_{CC} = 4.5 V to 5.5 V	
I/O leakage current	$\|I_{IL}\|$	D_0 to D_5, R0, $R1_3$, R2, $R3_1$ to $R3_3$	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS transistor current	$-I_{PU}$	D_0 to D_5, R0, $R3_1$ to $R3_3$	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	

Note: Except for the current flowing in the pull-up MOS transistors and output buffers.

Table 25-10 Medium Voltage NMOS Open Drain Pin I/O Characteristics (HD404394 Series)

V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	$R1_0$ to $R1_2$	0.7 V_{CC}	—	12.0	V		
Input low level voltage	V_{IL}	$R1_0$ to $R1_2$	–0.3	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	$R1_0$ to $R1_2$	11.5	—	—	V	500 kΩ at 12 V	
Output low level voltage	V_{OL}	$R1_0$ to $R1_2$	—	—	0.4	V	I_{OH} = 0.5 mA	
			—	—	2.0		I_{OL} = 15 mA, V_{CC} = 4.5 V to 5.5 V	
I/O leakage current	$\lvert I_{IL} \rvert$	$R1_0$ to $R1_2$	—	—	20	µA	V_{in} = 0 V to 12 V	1

Note: Except for the current flow in the output buffers.

(2) AC Characteristics

Tables 25-11 and 25-12 list the AC characteristics of the HD404394 Series microcomputers.

Table 25-11 AC Characteristics (HD404394 Series)

V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Clock oscillator frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz		
Instruction cycle time (ceramic oscillator)	t_{cyc}	—	0.89	1	10	µs	Clock divisor = 4	
Oscillator stabilization period	t_{RC}	OSC_1, OSC_2	—	—	2	ms		1
External clock high level width	t_{CPH}	OSC_1	92	—	—	ns		2
External clock low level width	t_{CPL}	OSC_1	92	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$, EVNB high level width	t_{IH}	$\overline{INT_0}$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT_0}$, EVNB low level width	t_{IL}	$\overline{INT_0}$, EVNB	2	—	—	t_{cyc}		3
Reset low level width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low level width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5
Reset rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		5

Table 25-11 AC Characteristics (HD404394 Series) (cont)

V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input capacitance	C_{in}	All input pins other than TEST, V_{ref}, and $R1_0$ to $R1_2$	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	15		f = 1 MHz, V_{in} = 0 V	6
			—	—	40			7
		V_{ref}	—	—	30		f = 1 MHz, V_{in} = 0 V	
		$R1_0$ to $R1_2$	—	—	30		f = 1 MHz, V_{in} = 0 V	

Notes: 1. There are three cases where the oscillator stabilization period applies:

- When power is first applied, the time between the point when V_{CC} reaches 2.7 V and the point the oscillator is stable.
- When stop mode is cleared, the time between the point when the $\overline{\text{RESET}}$ input reaches the low level and the point the oscillator is stable.
- When stop mode is cleared, the time between the point when the $\overline{\text{STOPC}}$ input reaches the low level and the point the oscillator is stable.

  To assure the time necessary to achieve stable oscillation at power on and when clearing stop mode, apply a low level to the $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input for at least t_{RC}.

  Since the oscillator stabilization period varies with the details of the mounted circuit, stray capacitances, and other factors, this value should be determined based on thorough consultations with the manufacturer of the ceramic oscillator used.

2. See figure 25-7.
3. See figure 25-8.
4. See figure 25-9.
5. See figure 25-10.
6. Applies to the HD404391, HD404392, and HD404394.
7. Applies to the HD4074394.

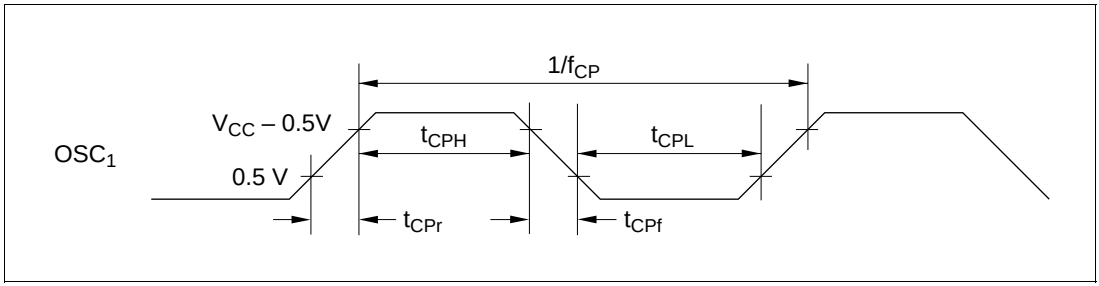


Figure 25-7 External Clock Timing (HD404394 Series)

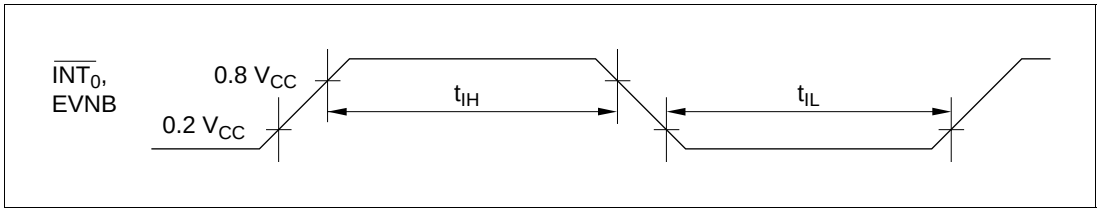


Figure 25-8 Interrupt Timing (HD404394 Series)

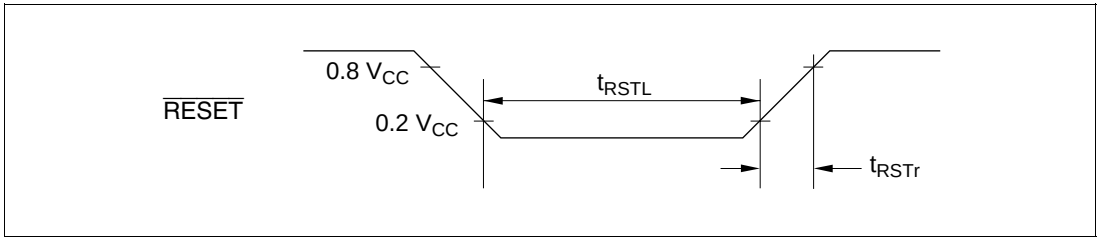


Figure 25-9 Reset Timing (HD404394 Series)

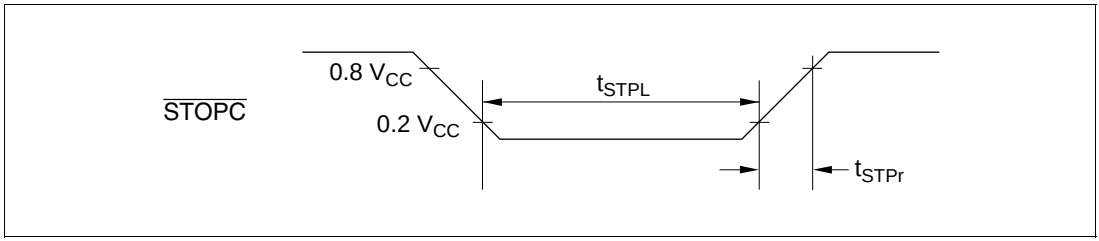


Figure 25-10 $\overline{\text{STOPC}}$ Timing (HD404394 Series)

Table 25-12 Serial Interface Timing Characteristics (HD404394 Series)

V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

When the Transfer Clock is Output:

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	With the load shown in figure 25-12	1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-12	1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-12	1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-12	1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-12	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-12	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: See figure 25-11.

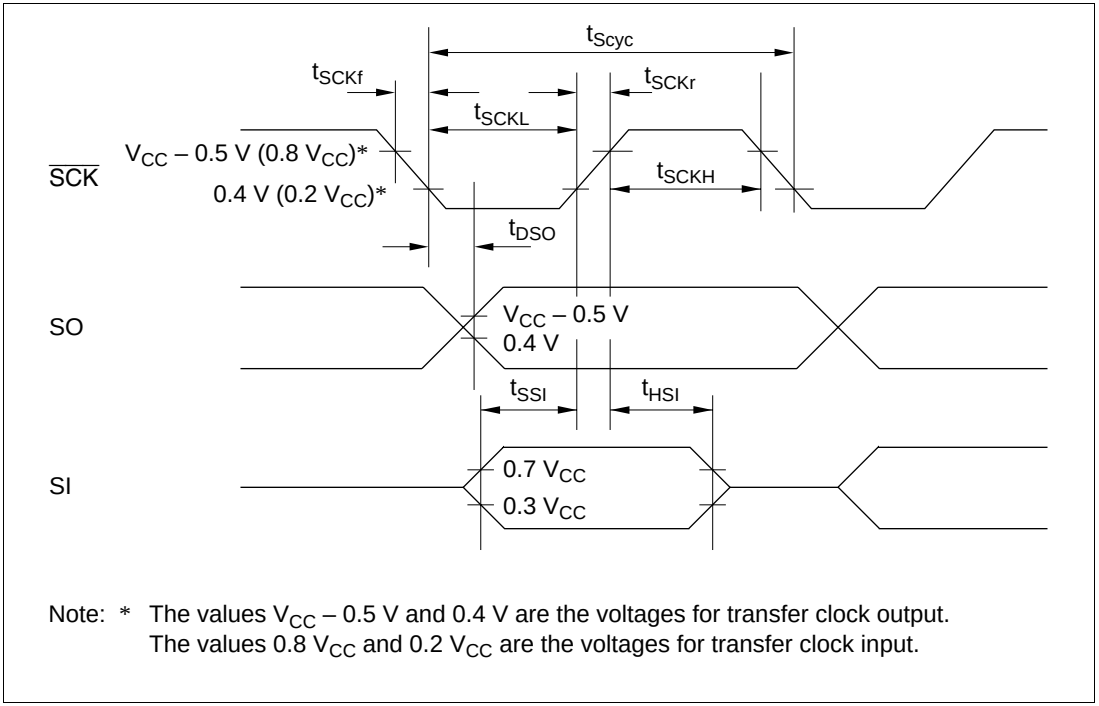
Table 25-12 Serial Interface Timing Characteristics (HD404394 Series) (cont)

V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

When the Transfer Clock is Input:

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-12	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: See figure 25-11.



Note: * The values V_{CC} – 0.5 V and 0.4 V are the voltages for transfer clock output.
The values 0.8 V_{CC} and 0.2 V_{CC} are the voltages for transfer clock input.

Figure 25-11 Serial Interface Timing

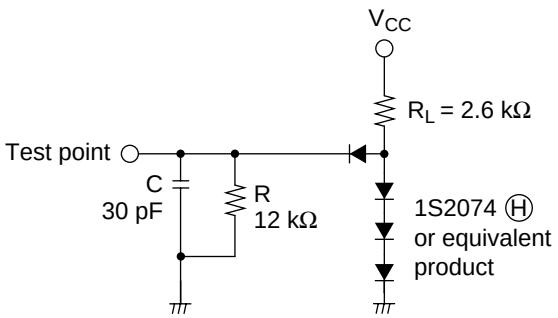


Figure 25-12 Timing Load Circuit

(3) A/D Converter Characteristics

Table 25-13 lists the characteristics of the HD404394 Series A/D converter.

Table 25-13 A/D Converter Characteristics (HD404394 Series)

V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Analog input reference voltage range	V_{ref}	V_{ref}	0.5 V_{CC}	—	V_{CC}	V		
Analog input voltage	AV_{in}	AN_1 to AN_3	GND	—	V_{ref}	V		
Current from V_{ref} to GND	I_{AD}		—	—	200	µA	V_{ref} = V_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_1 to AN_3	—	15	—	pF		
Resolution			—	8	—	Bits		
Number of inputs			0	—	3	Channels		
Absolute precision		AN_1 to AN_3	–3.0	—	3.0	LSB	T_a = 25°C, V_{ref} = V_{CC} = 5.0 V	
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_1 to AN_3	1	—	—	MΩ	f_{OSC} = 1 MHz, V_{in} = 0 V	

25.3 HD404318 Series

25.3.1 Absolute Maximum Ratings

Table 25-14 lists the absolute maximum ratings of the HD404318 Series microcomputers.

Table 25-14 Absolute Maximum Ratings (HD404318 Series)

Item	Symbol	Rated Value	Unit	Notes
Power supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		V_{CC} – 45 to V_{CC} + 0.3	V	3
Allowable total input current (current flowing in to the LSI)	$\sum I_0$	70	mA	4
Allowable total output current (current flowing out from the LSI)	$-\sum I_0$	150	mA	5
Allowable input current (current flowing in to the LSI)	I_0	4	mA	6, 7
		20	mA	6, 8
Allowable output current (current flowing out from the LSI)	$-I_0$	4	mA	9, 10
		30	mA	10, 11
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes:
1. Applies to the HD4074318 TEST (V_{PP}) pin.
2. Applies to all standard pins.
3. Applies to high voltage pins.
4. The allowable total input current is the sum of the currents flowing from all the I/O pins to ground at the same time.
5. The allowable total output current is the sum of the currents flowing from V_{CC} to all the I/O pins at the same time.
6. The allowable input current is the maximum value of the currents flowing from each I/O pin to ground.
7. Applies to R3 and R4.
8. Applies to R0.
9. Applies to R0, R3, and R4.
10. The allowable output current is the maximum value of the currents flowing from V_{CC} to each I/O pin.
11. Applies to D_0 to D_8, R1, R2, and R8.

Use of this LSI at levels that exceed the absolute maximum ratings can permanently damage the LSI. Also note that it is desirable to use this LSI within the conditions specified in the “Electrical Characteristics” section during normal operation. Exceeding those conditions can cause the LSI to operate incorrectly and may adversely affect LSI reliability.

25.3.2 Electrical Characteristics

(1) DC Characteristics

Tables 25-15 to 25-17 list the DC characteristics of the HD404318 Series microcomputers.

Table 25-15 DC Characteristics (HD404318 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, SI $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3			
Input low level voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, SI	–0.3	—	0.2 V_{CC}	V		
		$\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	V_{CC} – 40	—	0.2 V_{CC}			
		OSC_1	–0.3	—	0.5			
Output high level voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	$\overline{RESET}$, $\overline{SCK}$, SI, SO, TOC, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		$\overline{INT_0}$, $\overline{INT_1}$, STOPC, EVNB	—	—	20		V_{in} = V_{CC} – 40 V to V_{CC}	
Active mode current drain	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5
			—	—	8.0			2, 6

Table 25-15 DC Characteristics (HD404318 Series) (cont)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Standby mode current drain	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3
Stop mode current drain	I_{STOP}	V_{CC}	—	—	10	µA	V_{CC} = 5 V	4, 5
			—	—	20			4, 6
Stop mode data retention voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Except for the current flowing in the pull-up MOS transistors and output buffers.

2. The power supply current with the system in the reset state and no I/O currents flowing.

Test conditions	System state	Reset state
	Pin states	• $\overline{\text{RESET}}$, TEST..... At the ground potential • R0, R3, and R4 ..... At the V_{CC} potential • D_0 to D_8, R1, R2, R8, and RA_1 ..... At the V_{disp} potential

3. The power supply current with the system timers operating and no I/O currents flowing.

Test conditions	System state	• I/O: The same as in the reset state • Standby mode
	Pin states	• $\overline{\text{RESET}}$..... At the V_{CC} potential • TEST..... At the ground potential • R0, R3, and R4 ..... At the V_{CC} potential • D_0 to D_8, R1, R2, R8, and RA_1 ..... At the V_{disp} potential

4. The power supply current with no I/O currents flowing.

Test conditions	Pin states	• R0, R3, and R4 ..... At the V_{CC} potential • D_0 to D_8, R1, R2, R8, and RA_1 ..... At the ground potential

5. Applies to the HD404314, HD404316, and HD404318.
6. Applies to the HD4074318.

Table 25-16 Standard Pin I/O Characteristics (HD404318 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	R0, R3, R4	0.7 V_{CC}	—	V_{CC} + 0.3 V	V		
Input low level voltage	V_{IL}	R0, R3, R4	–0.3	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	R0, R3, R4	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	R3, R4	—	—	0.4	V	I_{OL} = 1.6 mA	
		R0	—	—	2.0		I_{OL} = 10 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	R0, R3, R4	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS transistor current	$-I_{PU}$	R0, R3, R4	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	2
			30	80	180			3

Notes: 1. Except for the current flowing in the output buffers.
2. Applies to the HD404314, HD404316, and HD404318.
3. Applies to the HD4074318.

Table 25-17 High Voltage Pin I/O Characteristics (HD404318 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	D_0 to D_8, R1, R2, R8, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low level voltage	V_{IL}	D_0 to D_8, R1, R2, R8, RA_1	V_{CC} – 40	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	D_0 to D_8, R1, R2 R8, BUZZ	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA	
			V_{CC} – 2.0	—	—		$-I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—		$-I_{OH}$ = 4 mA	
Output low level voltage	V_{OL}	D_0 to D_8, R1, R2 R8, BUZZ	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
			—	—	V_{CC} – 37		150 kΩ at V_{CC} – 40 V	2
I/O leakage current	$\|I_{IL}\|$	D_0 to D_8, R1, R2, R8 RA_1, BUZZ	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down resistor current	I_{PD}	D_0 to D_8, R1, R2, R8, BUZZ	200	600	1000	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applies to pins for which the pull-down resistor mask option was selected.
2. Applies to pins for which the no pull-down resistor mask option was selected.
3. Except for the current flow in the output buffers.

(2) AC Characteristics

Tables 25-18 and 25-19 list the AC characteristics of the HD404318 Series microcomputers.

Table 25-18 AC Characteristics (HD404318 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Clock oscillator frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	Clock divisor = 4	
Instruction cycle time	t_{cyc}		0.89	1	10	µs		
Oscillator stabilization period (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		1
Oscillator stabilization period (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		1
External clock high level width	t_{CPH}	OSC_1	92	—	—	ns		2
External clock low level width	t_{CPL}	OSC_1	92	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB high level width	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB low level width	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}		3
$\overline{RESET}$ low level width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low level width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5

Table 25-18 AC Characteristics (HD404318 Series) (cont)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
$\overline{\text{RESET}}$ rise time	t_{RSTr}	$\overline{\text{RESET}}$	—	—	20	ms		4
$\overline{\text{STOPC}}$ rise time	t_{STPr}	$\overline{\text{STOPC}}$	—	—	20	ms		5
Input capacitance	C_{in}	All input pins other than TEST	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	30		f = 1 MHz,	6
			—	—	180		V_{in} = 0 V	7

Notes: 1. There are three cases where the oscillator stabilization period applies:
- When power is first applied, the time between the point when V_{CC} reaches 4.0 V and the point the oscillator is stable.
- When stop mode is cleared, the time between the point when the $\overline{\text{RESET}}$ input reaches the low level and the point the oscillator is stable.
- When stop mode is cleared, the time between the point when the $\overline{\text{STOPC}}$ input reaches the low level and the point the oscillator is stable.

To assure the time necessary to achieve stable oscillation at power on and when clearing stop mode, apply a low level to the $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input for at least t_{RC}. Since the oscillator stabilization period varies with the details of the mounted circuit, stray capacitances, and other factors, this value should be determined based on thorough consultations with the manufacturer of the ceramic oscillator used.

2. See figure 25-13.
3. See figure 25-14.
4. See figure 25-15.
5. See figure 25-16.
6. Applies to the HD404314, HD404316, and HD404318.
7. Applies to the HD4074318.

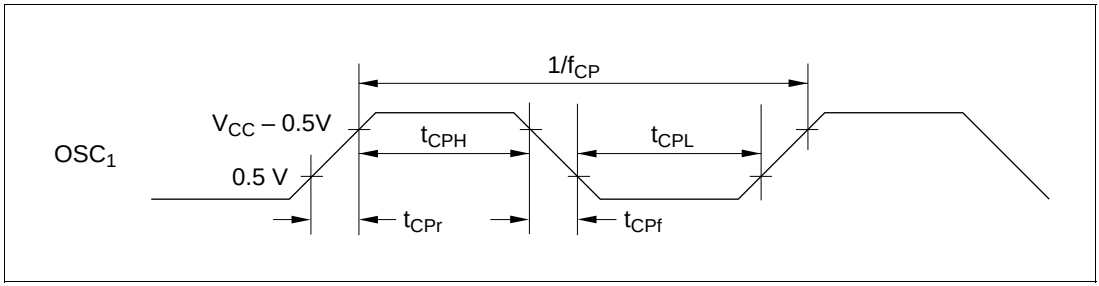


Figure 25-13 External Clock Timing (HD404318 Series)

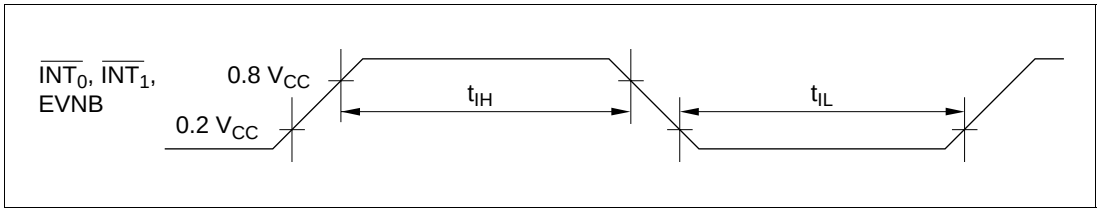


Figure 25-14 Interrupt Timing (HD404318 Series)

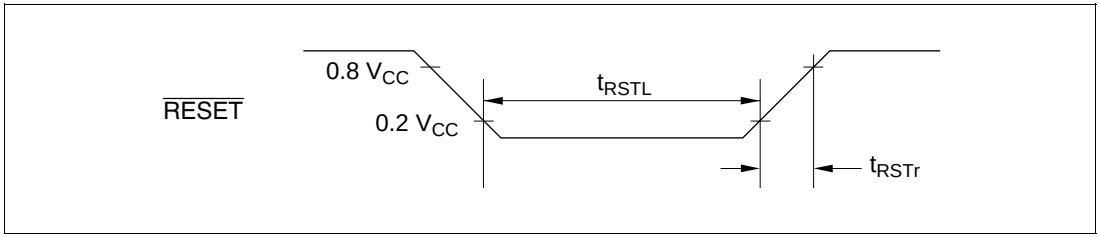


Figure 25-15 Reset Timing (HD404318 Series)

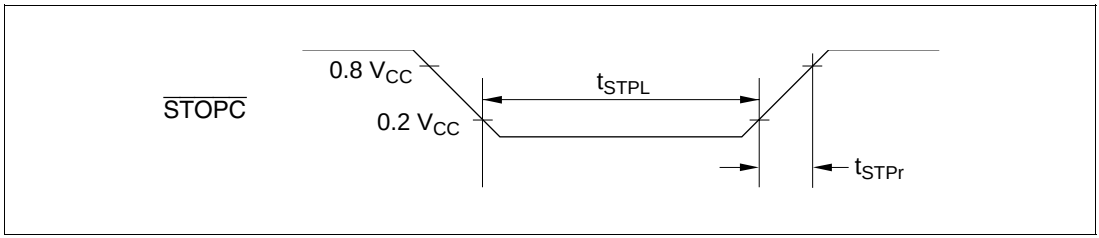


Figure 25-16 $\overline{\text{STOPC}}$ Timing (HD404318 Series)

Table 25-19 Serial Interface Timing Characteristics (HD404318 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

When the Transfer Clock is Output:

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	With the load shown in figure 25-18	1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-18	1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-18	1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-18	1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-18	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-18	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: See figure 25-17.

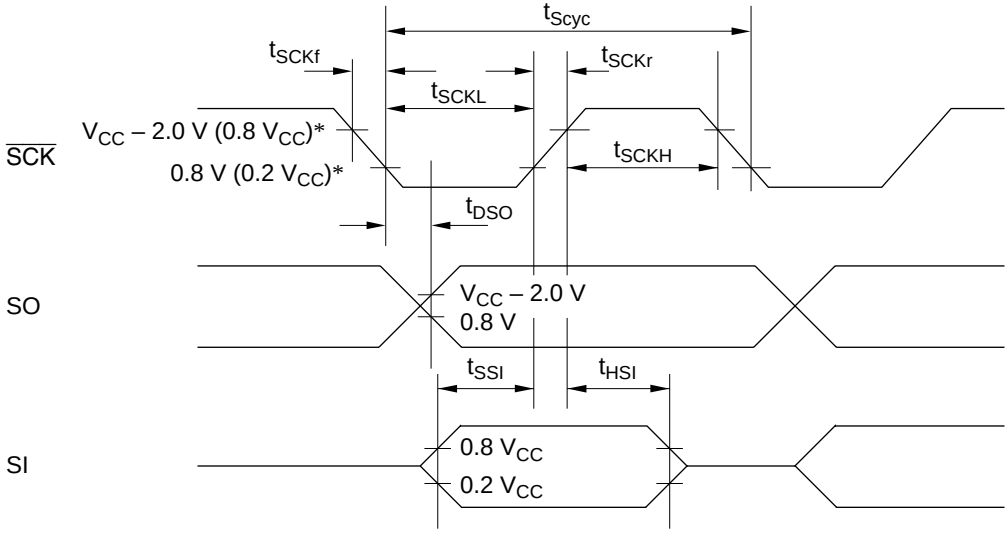
Table 25-19 Serial Interface Timing Characteristics (HD404318 Series) (cont)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

When the Transfer Clock is Input:

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-18	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: See figure 25-17.



Note: * The values V_{CC} – 2.0 V and 0.8 V are the voltages for transfer clock output.
The values 0.8 V_{CC} and 0.2 V_{CC} are the voltages for transfer clock input.

Figure 25-17 Serial Interface Timing (HD404318 Series)

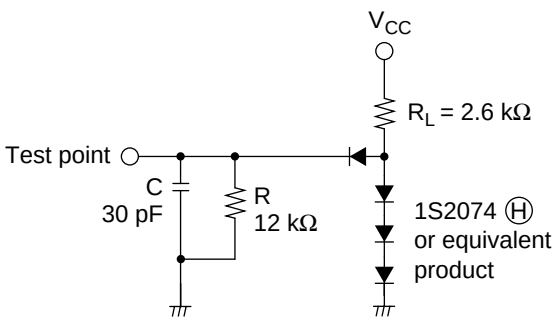


Figure 25-18 Timing Load Circuit

(3) A/D Converter Characteristics

Table 25-20 lists the characteristics of the HD404318 Series A/D converter.

Table 25-20 A/D Converter Characteristics (HD404318 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0 to AN_7	AV_{SS}	—	AV_{CC}	V		
Current from AV_{CC} to AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0 to AN_7	—	—	30	pF		
Resolution			8	8	8	Bits		
Number of inputs			0	—	8	Channels		
Absolute precision			—	—	±2.0	LSB		
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0 to AN_7	1	—	—	MΩ		

Note: Connect to the V_{CC} pin if the A/D converter is not used in the application.

25.4 HD404358/HD404358R Series

25.4.1 Absolute Maximum Ratings

Table 25-21 lists the absolute maximum ratings of the HD404358 and HD404358R Series microcomputers.

Table 25-21 Absolute Maximum Ratings (HD404358 and HD404358R Series)

		HD404358 Series	HD404358R Series		
Item	**Symbol**	**Rated Value**	**Rated Value**	**Unit**	**Notes**
Power supply voltage	V_{CC}	–0.3 to +7.0	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	–0.3 to V_{CC} + 0.3	V	2
		–0.3 to +15.0	—	V	3
Allowable total input current (current flowing in to the LSI)	$\sum I_0$	105	160	mA	4
Allowable total output current (current flowing out from the LSI)	$-\sum I_0$	50	50	mA	5
Allowable input current (current flowing in to the LSI)	I_0	4	4	mA	6, 7
		30	30	mA	6, 8
Allowable output current (current flowing out from the LSI)	$-I_0$	4	4	mA	9, 10
Operating temperature	T_{opr}	–20 to +75	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	–55 to +125	°C	

Notes:
1. Applies to the HD407A4359, HD407A4359R, and HD407C4359R TEST (V_{PP}) pin.
2. Applies to all standard pins.
3. Applies to the medium voltage pins.
4. The allowable total input current is the sum of the currents flowing from all the I/O pins to ground at the same time.
5. The allowable total output current is the sum of the currents flowing from V_{CC} to all the I/O pins at the same time.
6. The allowable input current is the maximum value of the currents flowing from each I/O pin to ground.
7. HD404358 Series: Applies to D_0 to D_8, R0, R1, R3, R4, and R8.
   HD404358R Series: Applies to D_0 to D_4, R3, and R4.
8. HD404358 Series: Applies to R2.
   HD404358R Series: Applies to D_5 to D_8, R0, R1, R2, and R8.
9. HD404358 Series: Applies to D_0 to D_8, R0, R1, R3, R4, and R8.
   HD404358R Series: Applies to D_0 to D_8, R0, R1, R2, R3, R4, and R8.
10. The allowable output current is the maximum value of the currents flowing from V_{CC} to each I/O pin.

Use of this LSI at levels that exceed the absolute maximum ratings can permanently damage the LSI. Also note that it is desirable to use this LSI within the conditions specified in the “Electrical Characteristics” section during normal operation. Exceeding those conditions can cause the LSI to operate incorrectly and may adversely affect LSI reliability.

All voltage values are referenced to ground.

25.4.2 Electrical Characteristics

(1) DC Characteristics

Tables 25-22 to 25-24 list the DC characteristics of the HD404358 and HD404358R Series microcomputers.

Table 25-22 DC Characteristics (HD404358 and HD404358R Series)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD404358R Series: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, EVNB	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7 V_{CC}	—	V_{CC} + 0.3			
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3			
Input low level voltage	V_{IL}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, EVNB	–0.3	—	0.2 V_{CC}	V		
		SI	–0.3	—	0.3 V_{CC}			
		OSC_1	–0.3	—	0.5			
Output high level voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI, SO, EVNB, TOC, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1

Table 25-22 DC Characteristics (HD404358 and HD404358R Series) (cont)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD404358R Series: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Active mode current drain	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2.5
	I_{CC1}		—	—	3.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2.6
	I_{CC2}		—	—	0.6	mA	V_{CC} = 3 V, f_{OSC} = 400 kHz	
	I_{CC3}		—	—	6.5	mA	V_{CC} = 5 V, f_{OSC} = 8 MHz	
Standby mode current drain	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3.5
	I_{SBY1}		—	—	1.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3.6
	I_{SBY2}		—	—	0.4	mA	V_{CC} = 3 V, f_{OSC} = 400 kHz	
	I_{SBY3}		—	—	2.5	mA	V_{CC} = 5 V, f_{OSC} = 8 MHz	
Stop mode current drain	I_{STOP}	V_{CC}	—	—	10	µA	V_{CC} = 5 V	4
Stop mode data retention voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Except for the current flowing in the pull-up MOS transistors and output buffers.
2. The power supply current with the system in the reset state and no I/O currents flowing.

Test conditions	System state	Reset state
	Pin states	• $\overline{\text{RESET}}$, TEST..... At the ground potential

3. The power supply current with the system timers operating and no I/O currents flowing.

Test conditions	System state	• I/O: The same as in the reset state • Standby mode
	Pin states	• $\overline{RESET}$ ..... At the V_{CC} potential • TEST ..... At the ground potential • D_0 to D_8, R0 to R4, R8, and RA_1 ..... At the V_{CC} potential

4. The power supply current with no I/O currents flowing.

Test conditions	Pin states	• $\overline{RESET}$ ..... At the V_{CC} potential • TEST ..... At the ground potential • D_0 to D_8, R0 to R4, R8, and RA_1 ..... At the V_{CC} potential

5. Applies to the HD404358 Series.
6. Applies to the HD404358R Series.

Table 25-23 Standard Pin I/O Characteristics (HD404358 and HD404358R Series)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD404358R Series: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	HD404358 Series D_0 to D_8, R0, R1, R3, R4, R8, RA_1 HD404358R Series D_0 to D_8, R0 to R4, R8, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low level voltage	V_{IL}	HD404358 Series D_0 to D_8, R0, R1, R3, R4, R8, RA_1 HD404358R Series D_0 to D_8, R0 to R4, R8, RA_1	–0.3	—	0.3 V_{CC}	V		

Table 25-23 Standard Pin I/O Characteristics (HD404358 and HD404358R Series) (cont)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD404358R Series: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Output high level voltage	V_{OH}	HD404358 Series D_0 to D_8, R0, R1, R3, R4, R8	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
		HD404358R Series D_0 to D_8, R0 to R4, R8	V_{CC} – 1.0	—	—			
Output low level voltage	V_{OL}	HD404358 Series D_0 to D_8, R0, R1, R3, R4, R8 HD404358R Series D_0 to D_4, R3, R4	—	—	0.4	V	I_{OL} = 1.6 mA	
		HD404358R Series D_5 to D_8, R0 to R2, R8	—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5 to 5.5 V	
I/O leakage current	$\|I_{IL}\|$	HD404358 Series D_0 to D_8, R0, R1, R3, R4, R8, RA_1 HD404358R Series D_0 to D_8, R0 to R4, R8, RA_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS transistor current	$–I_{PU}$	HD404358 Series D_0 to D_8, R0, R1, R3, R4, R8 HD404358R Series D_0 to D_8, R0 to R4, R8	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	

Note: 1. Except for the current flowing in the output buffers.

Table 25-24 Medium Voltage NMOS Open Drain Pin I/O Characteristics (HD404358 Series)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	R2	0.7 V_{CC}	—	12.0	V		
Input low level voltage	V_{IL}	R2	–0.3	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	R2	11.5	—	—	V	500 kΩ at 12 V	
Output low level voltage	V_{OL}	R2	—	—	0.4	V	I_{OL} = 0.4 mA	
			—	—	2.0		I_{OL} = 15 mA, V_{CC} = 4.5 V to 5.5 V	
I/O leakage current	$\lvert I_{IL} \rvert$	R2	—	—	20	µA	V_{in} = 0 V to V_{CC}	1

Note: 1. Except for the current flow in the output buffers.

(2) AC Characteristics

Tables 25-25 and 25-26 list the AC characteristics of the HD404358 and HD404358R Series microcomputers.

Table 25-25 AC Characteristics (HD404358 and HD404358R Series)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C
HD404354R, HD404356R, HD404358R, HD40A4354R, HD40A4356R, HD40A4358R, HD40C4354R, HD40C4356R, HD40C4358R, HD407A4359R, HD407C4359R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Clock oscillator frequency (ceramic oscillator, crystal oscillator)	f_{OSC}	OSC_1, OSC_2	0.4	4	5.0	MHz	Clock divisor = 4	
			0.4	4	8.5		Clock divisor = 4 V_{CC} = 4.0 to 5.5 V	6
			0.4	4	8.5		Clock divisor = 4 V_{CC} = 4.5 to 5.5 V	7
Clock oscillator frequency (resistor oscillator)	f_{OSC}	OSC_1, OSC_2	1.0	2.2	3.5	MHz	Clock divisor = 4	8
Instruction cycle time (ceramic oscillator, crystal oscillator, external clock input)	t_{cyc}		0.8	1	10	µs	Clock divisor = 4	
			0.47	1	10		Clock divisor = 4	6, 7
Instruction cycle time (resistor oscillator)	t_{cyc}		1.14	1.81	4.0	µs	Clock divisor = 4 R_f = 20 kΩ	8
Oscillator stabilization period (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		1
Oscillator stabilization period (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	30	ms		1,11
			—	—	40			1,12
Oscillator stabilization period (resistor oscillator)	t_{RC}	OSC_1, OSC_2	—	—	0.5	ms		1, 8

Table 25-25 AC Characteristics (HD404358 and HD404358R Series) (cont)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C
HD404354R, HD404356R, HD404358R, HD40A4354R, HD40A4356R, HD40A4358R, HD40C4354R, HD40C4356R, HD40C4358R, HD407A4359R, HD407C4359R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
External clock high level width	t_{CPH}	OSC_1	80	—	—	ns		2
			47	—	—		V_{CC} = 4.0 to 5.5 V	2, 6
			47	—	—		V_{CC} = 4.5 to 5.5 V	2, 7
External clock low level width	t_{CPL}	OSC_1	80	—	—	ns		2
			47	—	—		V_{CC} = 4.0 to 5.5 V	2, 6
			47	—	—		V_{CC} = 4.5 to 5.5 V	2, 7
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
			—	—	15		V_{CC} = 4.0 to 5.5 V	2, 6
			—	—	15		V_{CC} = 4.5 to 5.5 V	2, 7
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
			—	—	15		V_{CC} = 4.0 to 5.5 V	2, 6
			—	—	15		V_{CC} = 4.5 to 5.5 V	2, 7
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB high level width	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB low level width	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}		3
$\overline{RESET}$ low level width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low level width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		5

Table 25-25 AC Characteristics (HD404358 and HD404358R Series) (cont)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356,
HD40A4358: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to +75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C
HD404354R, HD404356R, HD404358R, HD40A4354R, HD40A4356R,
HD40A4358R, HD40C4354R, HD40C4356R, HD40C4358R, HD407A4359R,
HD407C4359R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input capacitance	C_{in}	All I/O pins other than TEST	—	—	15	pF	f = 1 MHz, V_{in} = 0V	11
		All I/O pins other than TEST, R2	—	—	15			12
		TEST	—	—	15			13
			—	—	40			9
			—	—	180			10
		R2	—	—	30			12

Notes: 1. There are three cases where the oscillator stabilization period applies:
- When power is first applied, the time between the point when V_{CC} reaches min and the point the oscillator is stable.
- When stop mode is cleared, the time between the point when the $\overline{\text{RESET}}$ input reaches the low level and the point the oscillator is stable.
- When stop mode is cleared, the time between the point when the $\overline{\text{STOPC}}$ input reaches the low level and the point the oscillator is stable.

To assure the time necessary to achieve stable oscillation at power on and when clearing stop mode, apply a low level to the $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input for at least t_{RC}.

Since the oscillator stabilization period varies with the details of the mounted circuit, stray capacitances, and other factors, this value should be determined based on thorough consultations with the manufacturer of the ceramic oscillator used.

2. See figure 25-19.
3. See figure 25-20.
4. See figure 25-21.
5. See figure 25-22.
6. Applies to the HD40A4354R, HD40A4356R, HD40A4358R, and HD407A4359R.
7. Applies to the HD40A4354, HD40A4356, HD40A4358, and HD407A4359.
8. Applies to the HD40C4354R, HD40C4356R, HD40C4358R, and HD407C4359R.
9. Applies to the HD407A4359R and HD407C4359R.
10. Applies to the HD407A4359.

11. Applies to the HD404358R.
12. Applies to the HD404358.
13. Applies to the HD404354R, HD404356R, HD404358R, HD40A4354R, HD40A4356R, HD40A4358R, HD40C4354R, HD40C4356R, and HD40C4358R

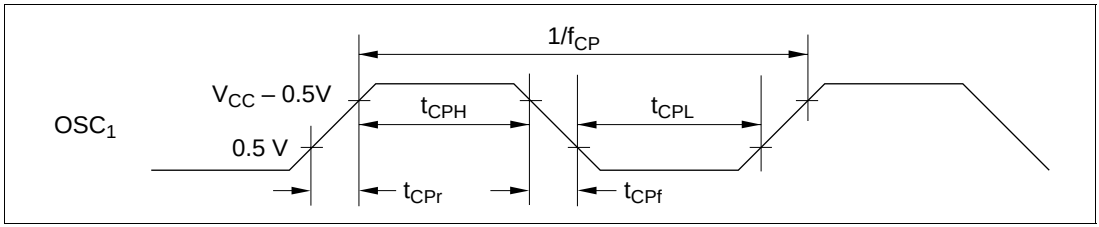


Figure 25-19 External Clock Timing (HD404358 and HD404358R Series)

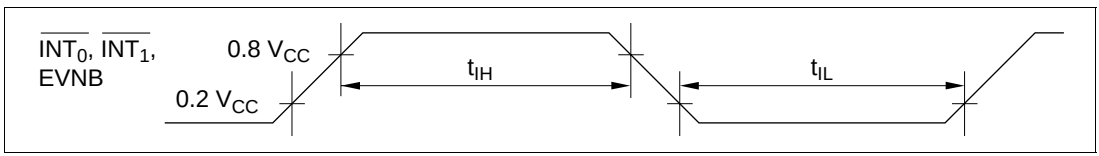


Figure 25-20 Interrupt Timing (HD404358 and HD404358R Series)

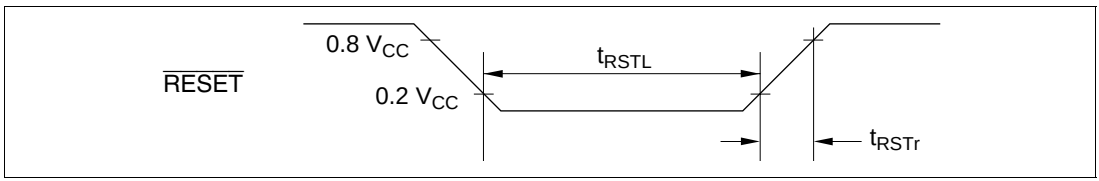


Figure 25-21 Reset Timing (HD404358 and HD404358R Series)

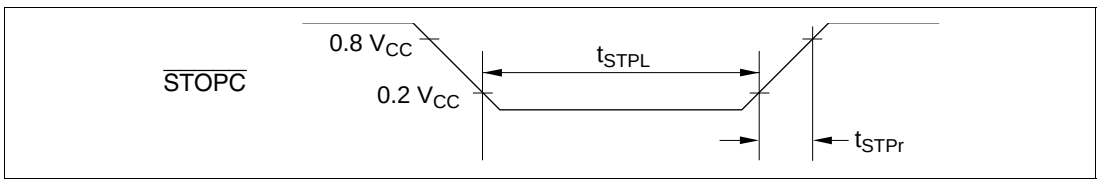


Figure 25-22 $\overline{STOPC}$ Timing (HD404358 and HD404358R Series)

Table 25-26 Serial Interface Timing Characteristics (HD404358 and HD404358R Series)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD404358R Series: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C,
unless specified otherwise.

When the Transfer Clock is Output:

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	With the load shown in figure 25-24	1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-24	1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-24	1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-24	1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-24	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-24	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. See figure 25-23.

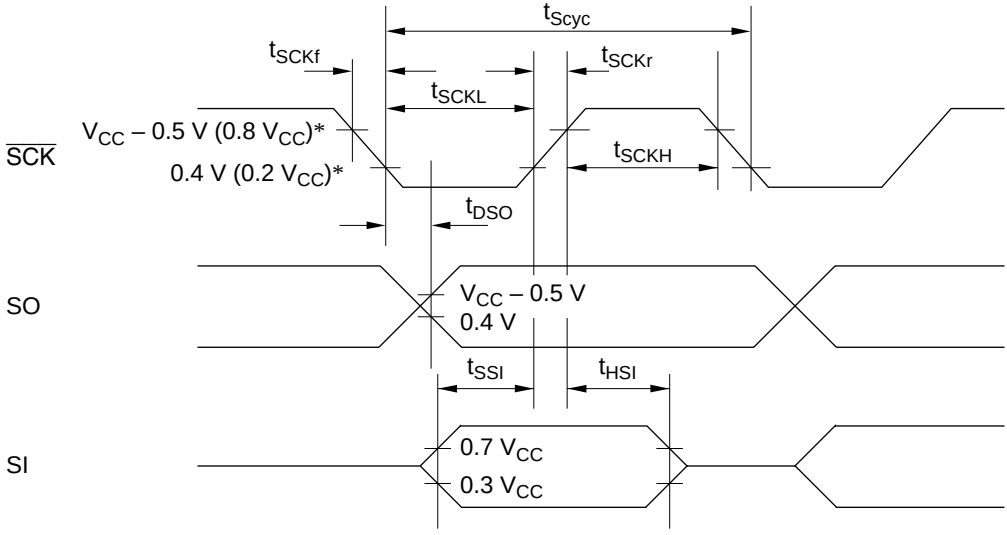
Table 25-26 Serial Interface Timing Characteristics (HD404358 Series) (cont)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD404358R Series: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C,
unless specified otherwise.

When the Transfer Clock is Input:

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-24	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: 1. See figure 25-23.



Note: * The values V_{CC} – 0.5 V and 0.4 V are the voltages for transfer clock output.
The values 0.8 V_{CC} and 0.2 V_{CC} are the voltages for transfer clock input.

Figure 25-23 Serial Interface Timing (HD404358 and HD404358R Series)

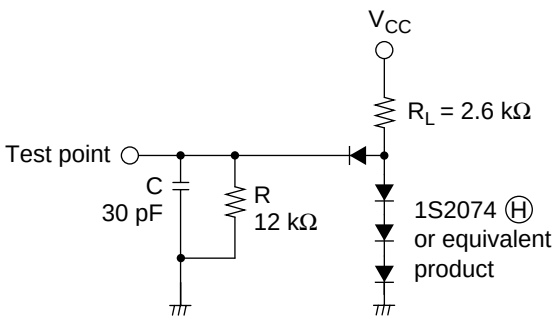


Figure 25-24 Timing Load Circuit

(3) A/D Converter Characteristics

Table 25-27 lists the characteristics of the HD404358 and HD404358R Series A/D converter.

Table 25-27 A/D Converter Characteristics (HD404358 and HD404358R Series)

HD404354, HD404356, HD404358, HD40A4354, HD40A4356, HD40A4358:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4359: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C
HD404358R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C,
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0 to AN_7	AV_{SS}	—	AV_{CC}	V		
Current from AV_{CC} to AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	2
			—	—	500			3
Analog input capacitance	CA_{in}	AN_0 to AN_7	—	—	30	pF		
Resolution			—	8	—	Bits		
Number of inputs			0	—	8	Channels		
Absolute precision			–2.0	—	2.0	LSB		
Conversion time			34	—	67	tcyc		
Input impedance		AN_0 to AN_7	1	—	—	MΩ		

Notes: 1. Connect to the V_{CC} pin if the A/D converter is not used in the application.
2. Applies to the HD404358.
3. Applies to the HD404358R.

25.5 HD404339 Series

25.5.1 Absolute Maximum Ratings

Table 25-28 lists the absolute maximum ratings of the HD404339 Series microcomputers.

Table 25-28 Absolute Maximum Ratings (HD404339 Series)

Item	Symbol	Rated Value	Unit	Notes
Power supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		V_{CC} – 45 to V_{CC} + 0.3	V	3
Allowable total input current (current flowing in to the LSI)	$\sum I_0$	70	mA	4
Allowable total output current (current flowing out from the LSI)	$-\sum I_0$	150	mA	5
Allowable input current (current flowing in to the LSI)	I_0	4	mA	6, 7
		20	mA	6, 8
Allowable output current (current flowing out from the LSI)	$-I_0$	4	mA	9, 10
		30	mA	10, 11
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes:
1. Applies to the HD4074339 TEST (V_{PP}) pin.
2. Applies to all standard pins.
3. Applies to high voltage pins.
4. The allowable total input current is the sum of the currents flowing from all the I/O pins to ground at the same time.
5. The allowable total output current is the sum of the currents flowing from V_{CC} to all the I/O pins at the same time.
6. The allowable input current is the maximum value of the currents flowing from each I/O pin to ground.
7. Applies to R3 to R5.
8. Applies to R0, R6, and R7.
9. Applies to R0, and $R3_0$ to $R7_2$.
10. The allowable output current is the maximum value of the currents flowing from V_{CC} to each I/O pin.
11. Applies to D_0 to D_{13}, R1, R2, R8 and R9.

Use of this LSI at levels that exceed the absolute maximum ratings can permanently damage the LSI. Also note that it is desirable to use this LSI within the conditions specified in the “Electrical Characteristics” section during normal operation. Exceeding those conditions can cause the LSI to operate incorrectly and may adversely affect LSI reliability.

All voltage values are referenced to ground.

25.5.2 Electrical Characteristics

(1) DC Characteristics

Tables 25-29 to 25-31 list the DC characteristics of the HD404339 Series microcomputers.

Table 25-29 DC Characteristics (HD404339 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, SI $\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3			
Input low level voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, SI	–0.3	—	0.2 V_{CC}	V		
		$\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	V_{CC} – 40	—	0.2 V_{CC}			
		OSC_1	–0.3	—	0.5			
Output high level voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	$\overline{RESET}$, $\overline{SCK}$, SI, SO, TOC, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		$\overline{INT_0}$, $\overline{INT_1}$, $\overline{STOPC}$, EVNB	—	—	20		V_{in} = V_{CC} – 40 V to V_{CC}	
Active mode current drain	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5, 6
			—	—	8.0			2, 5, 7

Table 25-29 DC Characteristics (HD404339 Series) (cont)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Standby mode current drain	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3, 5
Subactive mode current drain	I_{SUB}	V_{CC}	—	—	100	µA	V_{CC} = 5 V, using a 32 kHz oscillator	4, 6
			—	—	320			4, 7
Watch mode current drain	I_{WTC}	V_{CC}	—	—	20	µA	V_{CC} = 5 V, using a 32 kHz oscillator	4
Stop mode current drain	I_{STOP}	V_{CC}	—	—	10	µA	X1 = GND, X2 = OPEN	4, 6
			—	—	20			4, 7
Stop mode data retention voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Except for the current flowing in the pull-up MOS transistors and output buffers.

2. The power supply current with the system in the reset state and no I/O currents flowing.

Test conditions	System state	Reset state
	Pin states	• $\overline{\text{RESET}}$, TEST..... At the ground potential • R0, $R3_0$ to $R7_2$..... At the V_{CC} potential • D_0 to D_{13}, R1, R2, R8, R9, and RA_1..... At the V_{disp} potential

3. The power supply current with the system timers operating and no I/O currents flowing.

Test conditions	System state	• I/O: The same as in the reset state • Standby mode
	Pin states	• $\overline{\text{RESET}}$..... At the V_{CC} potentiall • TEST..... At the ground potential • R0, $R3_0$ to $R7_2$..... At the V_{CC} potential • D_0 to D_{13}, R1, R2, R8, R9, and RA_1..... At the V_{disp} potential

4. The power supply current with no I/O currents flowing.

Test conditions	Pin states	• R0, $R3_0$ to $R7_2$..... At the V_{CC} potential • D_0 to D_{13}, R1, R2, R8, R9, and RA_1..... At the ground potential

5. The current drain during operation and in standby mode is proportional to f_{OSC}. Therefore, the current ratings when f_{OSC} is x MHz can be calculated roughly as follows.
   maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)
6. Applies to the HD404334, HD404336, HD404338, HD4043312, and HD404339.
7. Applies to the HD4074339.

Table 25-30 Standard Pin I/O Characteristics (HD404339 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	R0, $R3_0$ to $R7_2$	0.7 V_{CC}	—	V_{CC} + 0.3 V	V		
Input low level voltage	V_{IL}	R0, $R3_0$ to $R7_2$	–0.3	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	R0, $R3_0$ to $R7_2$	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	R3 to R5	—	—	0.4	V	I_{OL} = 1.6 mA	
		R0, $R6_0$ to $R7_2$	—	—	2.0		I_{OL} = 10 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	R0, $R3_0$ to $R7_2$	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS transistor current	$–I_{PU}$	R0, $R3_0$ to $R7_2$	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	2
			30	80	180			3

Notes: 1. Except for the current flowing in the output buffers.
2. Applies to the HD404334, HD404336, HD404338, HD4043312, and HD404339.
3. Applies to the HD4074339.

Table 25-31 High Voltage Pin I/O Characteristics (HD404339 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	D_0 to D_{13}, R1, R2, R8, R9, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low level voltage	V_{IL}	D_0 to D_{13}, R1, R2, R8, R9, RA_1	V_{CC} – 40	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	D_0 to D_{13}, R1, R2, R8, R9, BUZZ	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA	
			V_{CC} – 2.0	—	—		$-I_{OH}$ = 10 mA	
			V_{CC} – 1.0	—	—		$-I_{OH}$ = 4 mA	
Output low level voltage	V_{OL}	D_0 to D_{13}, R1, R2, R8, R9, BUZZ	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
			—	—	V_{CC} – 37		150 kΩ at V_{CC} – 40 V	2
I/O leakage current	$\|I_{IL}\|$	D_0 to D_{13}, R1, R2, R8, R9, RA_1, BUZZ	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down resistor current	I_{PD}	D_0 to D_{13}, R1, R2, R8, R9, BUZZ	200	600	1000	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applies to pins for which the pull-down resistor mask option was selected.
2. Applies to pins for which the no pull-down resistor mask option was selected.
3. Except for the current flow in the output buffers.

(2) AC Characteristics

Tables 25-32 and 25-33 list the AC characteristics of the HD404339 Series microcomputers.

Table 25-32 AC Characteristics (HD404339 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Clock oscillator frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	4.5	MHz	Clock divisor = 4	1
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.89	1	10	µs		
	t_{subcyc}		—	244.14	—		Using a 32 kHz oscillator, clock divisor = 8	
			—	122.07	—		Using a 32 kHz oscillator, clock divisor = 4	
Oscillator stabilization period (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		2
Oscillator stabilization period (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		2
		X1, X2	—	—	2	s		2
External clock high level width	t_{CPH}	OSC_1	92	—	—	ns		3
External clock low level width	t_{CPL}	OSC_1	92	—	—	ns		3
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		3

Table 25-32 AC Characteristics (HD404339 Series) (cont)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB high level width	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB low level width	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4
$\overline{RESET}$ low level width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		5
$\overline{STOPC}$ low level width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		6
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		5
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		6
Input capacitance	C_{in}	All input pins other than TEST	—	—	30	pF	f = 1 Mhz, V_{in} = 0 V	
		TEST	—	—	30		f = 1 MHz, V_{in} = 0 V	7
			—	—	180			8

Notes: 1. When a sub-system oscillator (a 32.768 kHz crystal oscillator) is used, f_{OSC} must either be in the range 0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or be in the range 1.6 MHz ≤ f_{OSC} ≤ 4.5 MHz. Furthermore, the SSR11 bit in the system clock selection register 1 (SSR1: $027) must be set to indicate which of those ranges f_{OSC} falls in.

2. There are three cases where the oscillator stabilization period applies:
   - When power is first applied, the time between the point when V_{CC} reaches 4.0 V and the point the oscillator is stable.
   - When stop mode is cleared, the time between the point when the $\overline{RESET}$ input reaches the low level and the point the oscillator is stable.
   - When stop mode is cleared, the time between the point when the $\overline{STOPC}$ input reaches the low level and the point the oscillator is stable.

   To assure the time necessary to achieve stable oscillation at power on and when clearing stop mode, apply a low level to the $\overline{RESET}$ or $\overline{STOPC}$ input for at least t_{RC}.

   Since the oscillator stabilization period varies with the details of the mounted circuit, stray capacitances, and other factors, this value should be determined based on thorough consultations with the manufacturer of the ceramic oscillator used.
3. See figure 25-25.
4. See figure 26-26.
5. See figure 25-27.
6. See figure 25-28.

7. Applies to the HD404334, HD404336, HD404338, HD4043312, and HD404339.
8. Applies to the HD4074339.

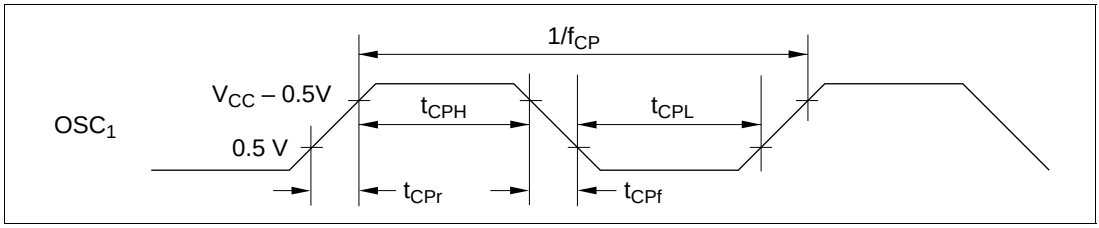


Figure 25-25 External Clock Timing (HD404339 Series)

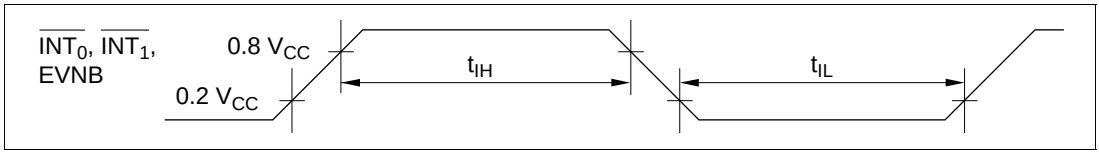


Figure 25-26 Interrupt Timing (HD404339 Series)

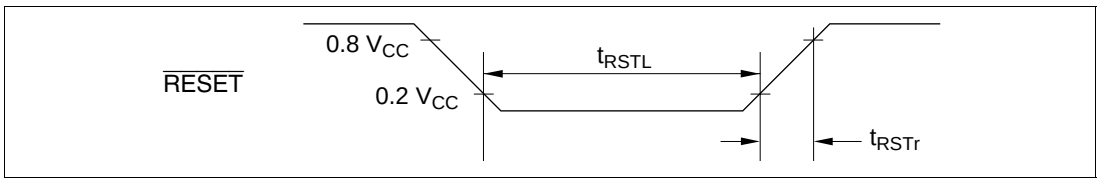


Figure 25-27 Reset Timing (HD404339 Series)

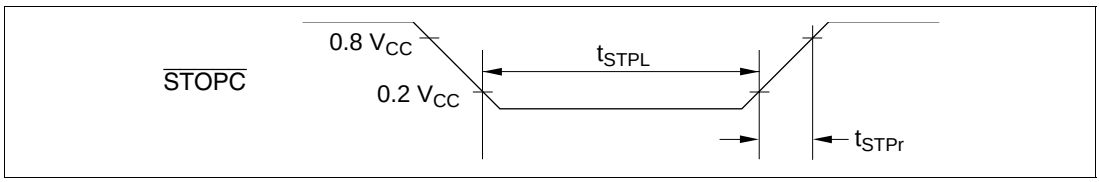


Figure 25-28 $\overline{\text{STOPC}}$ Timing (HD404339 Series)

Table 25-33 Serial Interface Timing Characteristics (HD404339 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	With the load shown in figure 25-30	1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-30	1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-30	1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-30	1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-30	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-30	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: See figure 25-29.

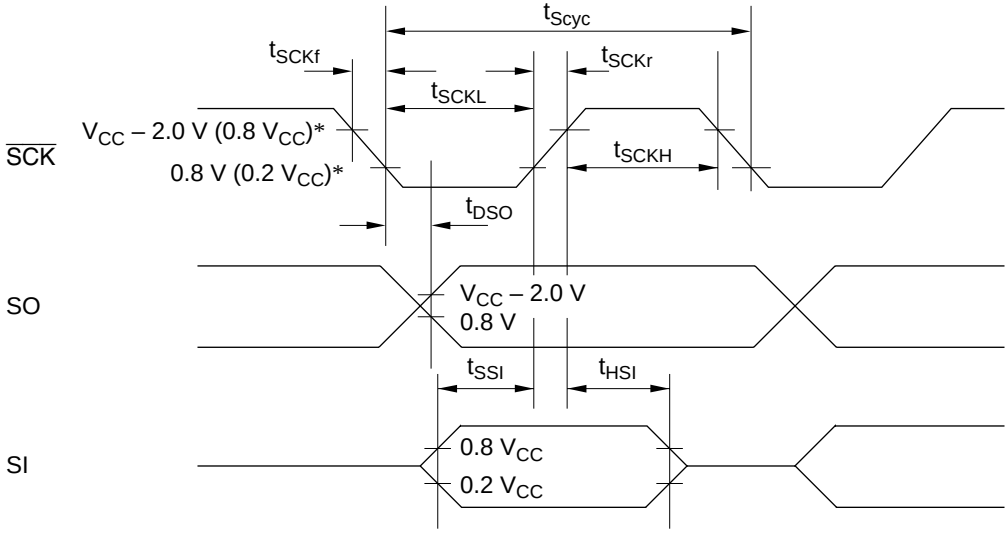
Table 25-33 Serial Interface Timing Characteristics (HD404339 Series) (cont)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

When the Transfer Clock is Input:

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-30	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: See figure 25-29.



Note: * The values V_{CC} – 2.0 V and 0.8 V are the voltages for transfer clock output.
The values 0.8 V_{CC} and 0.2 V_{CC} are the voltages for transfer clock input.

Figure 25-29 Serial Interface Timing (HD404339 Series)

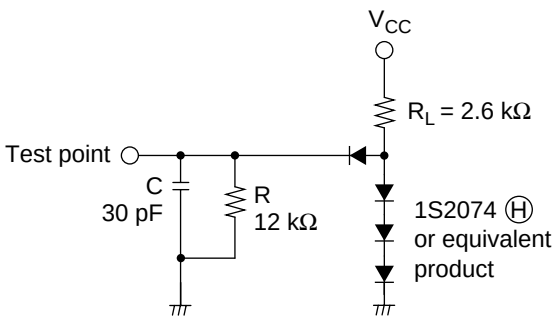


Figure 25-30 Timing Load Circuit

(3) A/D Converter Characteristics

Table 25-34 lists the characteristics of the HD404339 Series A/D converter.

Table 25-34 A/D Converter Characteristics (HD404339 Series)

V_{CC} = 4.0 to 5.5 V, GND = 0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0 to AN_{11}	AV_{SS}	—	AV_{CC}	V		
Current from AV_{CC} to AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0 to AN_{11}	—	—	30	pF		
Resolution			8	8	8	Bits		
Number of inputs			0	—	12	Channels		
Absolute precision			—	—	±2.0	LSB		
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0 to AN_{11}	1	—	—	MΩ		

Note: Connect to the V_{CC} pin if the A/D converter is not used in the application.

25.6 HD404369 Series

25.6.1 Absolute Maximum Ratings

Table 25-35 lists the absolute maximum ratings of the HD404369 Series microcomputers.

Table 25-35 Absolute Maximum Ratings (HD404369 Series)

Item	Symbol	Rated Value	Unit	Notes
Power supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		–0.3 to +15.0	V	3
Allowable total input current (current flowing in to the LSI)	$\sum I_0$	105	mA	4
Allowable total output current (current flowing out from the LSI)	$-\sum I_0$	50	mA	5
Allowable input current (current flowing in to the LSI)	I_0	4	mA	6, 7
		30	mA	6, 8
Allowable output current (current flowing out from the LSI)	$-I_0$	4	mA	7, 9
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes:
1. Applies to the HD407A4369 TEST (V_{PP}) pin.
2. Applies to all standard pins.
3. Applies to the medium voltage pins.
4. The allowable total input current is the sum of the currents flowing from all the I/O pins to ground at the same time.
5. The allowable total output current is the sum of the currents flowing from V_{CC} to all the I/O pins at the same time.
6. The allowable input current is the maximum value of the currents flowing from each I/O pin to ground.
7. Applies to D_0 to D_{13}, R0, and R3 to R9.
8. Applies to R1 and R2.
9. The allowable output current is the maximum value of the currents flowing from V_{CC} to each I/O pin.

Use of this LSI at levels that exceed the absolute maximum ratings can permanently damage the LSI. Also note that it is desirable to use this LSI within the conditions specified in the “Electrical Characteristics” section during normal operation. Exceeding those conditions can cause the LSI to operate incorrectly and may adversely affect LSI reliability.

All voltage values are referenced to ground.

25.6.2 Electrical Characteristics

(1) DC Characteristics

Tables 25-36 to 25-38 list the DC characteristics of the HD404369 Series microcomputers.

Table 25-36 DC Characteristics (HD404369 Series)

HD404364, HD404368, HD4043612, HD404369, HD40A4364, HD40A4368, HD40A43612, HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C,
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, EVNB	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7 V_{CC}		V_{CC} + 0.3			
		OSC1	V_{CC} – 0.5	—	V_{CC} + 0.3			
Input low level voltage	V_{IL}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, EVNB	–0.3	—	0.2 V_{CC}	V		
		SI	–0.3	—	0.3 V_{CC}			
		OSC_1	–0.3	—	0.5			
Output high level voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	SCK, SO, TOC	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK}$, SI, SO, EVNB, TOC, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1

Table 25-36 DC Characteristics (HD404369 Series) (cont)

HD404364, HD404368, HD4043612, HD404369, HD40A4364, HD40A4368, HD40A43612, HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C,
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Active mode current drain	I_{CC}	V_{CC}	—	—	5.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 5
Standby mode current drain	I_{SBY}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3, 5
Subactive mode current drain	I_{SUB}	V_{CC}	—	—	100	µA	V_{CC} = 5 V, using a 32 kHz oscillator	4
Watch mode current drain	I_{WTC}	V_{CC}	—	—	20	µA	V_{CC} = 5 V, using a 32 kHz oscillator	4
Stop mode current drain	I_{STOP}	V_{CC}	—	—	10	µA	V_{CC} = 5 V, X1 = GND, X2 = OPEN	4
Stop mode data retention voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes: 1. Except for the current flowing in the pull-up MOS transistors and output buffers.

2. The power supply current with the system in the reset state and no I/O currents flowing.

Test conditions	System state	Reset state
	Pin states	• $\overline{\text{RESET}}$, TEST..... At the ground potential

3. The power supply current with the system timers operating and no I/O currents flowing.

Test conditions	System state	• I/O: The same as in the reset state • Standby mode
	Pin states	• $\overline{\text{RESET}}$..... At the V_{CC} potential • TEST..... At the ground potential • D_0 to D_{13}, R0 to R9, and RA_1..... At the V_{CC} potential

4. The power supply current with no I/O currents flowing.

Test conditions	Pin states		
		• $\overline{\text{RESET}}$	At the V_{CC} potential
		• TEST	At the ground potential
		• D_0 to D_{13}, R0 to R9, and RA_1	At the V_{CC} potential

5. The current drain during operation and in standby mode is proportional to f_{OSC}. Therefore, the current ratings when f_{OSC} is x MHz can be calculated roughly as follows.
   maximum value (f_{OSC} = x MHz) = x/4 × maximum value (f_{OSC} = 4 MHz)

Table 25-37 Standard Pin I/O Characteristics (HD404369 Series)

HD404364, HD404368, HD4043612, HD404369, HD40A4364, HD40A4368, HD40A43612, HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C,
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	D_0 to D_{13}, R0, R3 to R9, RA_1	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low level voltage	V_{IL}	D_0 to D_{13}, R0, R3 to R9, RA_1	–0.3	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	D_0 to D_{13}, R0, R3 to R9	V_{CC} – 0.5	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low level voltage	V_{OL}	D_0 to D_{13}, R0, R3 to R9	—	—	0.4	V	I_{OL} = 1.6 mA	
I/O leakage current	$\|I_{IL}\|$	D_0 to D_{13}, R0, R3 to R9, RA_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS transistor current	$–I_{PU}$	D_0 to D_{13}, R0, R3 to R9	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	

Note: Except for the current flowing in the output buffers.

Table 25-38 Medium Voltage NMOS Open Drain Pin I/O Characteristics (HD404369 Series)

HD404364, HD404368, HD4043612, HD404369, HD40A4364, HD40A4368, HD40A43612, HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C,
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Input high level voltage	V_{IH}	R1, R2	0.7 V_{CC}	—	12.0	V		
Input low level voltage	V_{IL}	R1, R2	–0.3	—	0.3 V_{CC}	V		
Output high level voltage	V_{OH}	R1, R2	11.5	—	—	V	500 kΩ at 12 V	
Output low level voltage	V_{OL}	R1, R2	—	—	0.4	V	I_{OL} = 0.4 mA	
			—	—	2.0		I_{OL} = 15 mA, V_{CC} = 4.5 V to 5.5 V	
I/O leakage current	$\lvert I_{IL} \rvert$	R1, R2	—	—	20	µA	V_{in} = 0 V to V_{CC}	1

Note: Except for the current flow in the output buffers.

(2) AC Characteristics

Tables 25-39 (1), 25-39 (2), and 25-40 list the AC characteristics of the HD404369 Series microcomputers.

Table 25-39 (1) AC Characteristics (HD404364, HD404368, HD4043612, and HD404369)

V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Clock oscillator frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	5.0	MHz	Clock divisor = 4	1
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.8	1	10	µs		1
	t_{subcyc}		—	244.14	—		Using a 32 kHz oscillator, clock divisor = 8	
			—	122.07	—		Using a 32 kHz oscillator, clock divisor = 4	
Oscillator stabilization period (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		2
Oscillator stabilization period (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		2
		X1, X2	—	—	2	s		2
External clock high level width	t_{CPH}	OSC_1	80	—	—	ns		3
External clock low level width	t_{CPL}	OSC_1	80	—	—	ns		3
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		3
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB high level width	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4

Table 25-39 (1) AC Characteristics (HD404364, HD404368, HD4043612, and HD404369) (cont)

V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB low level width	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		4
$\overline{RESET}$ low level width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		5
$\overline{STOPC}$ low level width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		6
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		5
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		6
Input capacitance	C_{in}	All I/O pins other than R1 and R2	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		R1, R2	—	—	30		f = 1 MHz, V_{in} = 0 V	

Notes: 1. When a sub-system oscillator (a 32.768 kHz crystal oscillator) is used, f_{OSC} must either be in the range 0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or be in the range 1.6 MHz ≤ f_{OSC} ≤ 5.0 MHz. Furthermore, the SSR11 bit in the system clock selection register 1 (SSR1: $027) must be set to indicate which of those ranges f_{OSC} falls in.

2. There are three cases where the oscillator stabilization period applies:
   - When power is first applied, the time between the point when V_{CC} reaches 2.7 V and the point the oscillator is stable.
   - When stop mode is cleared, the time between the point when the $\overline{RESET}$ input reaches the low level and the point the oscillator is stable.
   - When stop mode is cleared, the time between the point when the $\overline{STOPC}$ input reaches the low level and the point the oscillator is stable.

   To assure the time necessary to achieve stable oscillation at power on and when clearing stop mode, apply a low level to the $\overline{RESET}$ or $\overline{STOPC}$ input for at least t_{RC}.

   Since the oscillator stabilization period varies with the details of the mounted circuit, stray capacitances, and other factors, this value should be determined based on thorough consultations with the manufacturer of the ceramic oscillator used.
3. See figure 25-31.
4. See figure 25-32.
5. See figure 25-33.
6. See figure 25-34.

Table 25-39 (2) AC Characteristics (HD40A4364, HD40A4368, HD40A43612, HD40A4369, and HD407A4369)

HD40A4364, HD40A4368, HD40A43612, HD40A4369:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C,
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Clock oscillator frequency	f_{OSC}	OSC_1, OSC_2	0.4	4	5.0	MHz	Clock divisor = 4	1
			0.4	4	8.5		Clock divisor = 4, V_{CC} = 4.5 to 5.5 V	2
		X1, X2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.8	1	10	µs		1
			0.47	1	10		V_{CC} = 4.5 to 5.5 V	2
	t_{subcyc}		—	244.14	—		Using a 32 kHz oscillator, clock divisor = 8	
			—	122.07	—		Using a 32 kHz oscillator, clock divisor = 4	
Oscillator stabilization period (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms		3
Oscillator stabilization period (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms		3
		X1, X2	—	—	2	s		3
External clock high level width	t_{CPH}	OSC_1	80	—	—	ns		4
			47	—	—		V_{CC} = 4.5 to 5.5 V	4
External clock low level width	t_{CPL}	OSC_1	80	—	—	ns		4
			47	—	—		V_{CC} = 4.5 to 5.5 V	4

Table 25-39 (2) AC Characteristics (HD40A4364, HD40A4368, HD40A43612, HD40A4369, and HD407A4369) (cont)

HD40A4364, HD40A4368, HD40A43612, HD40A4369:
V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C,
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		4
			—	—	15		V_{CC} = 4.5 to 5.5 V	4
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		4
			—	—	15		V_{CC} = 4.5 to 5.5 V	4
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB high level width	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		5
$\overline{INT_0}$, $\overline{INT_1}$, and EVNB low level width	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVNB	2	—	—	t_{cyc}/ t_{subcyc}		5
$\overline{RESET}$ low level width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		6
$\overline{STOPC}$ low level width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		7
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		6
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		7
Input capacitance	C_{in}	All I/O pins other than TEST, R1 and R2	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	15		f = 1 MHz, V_{in} = 0 V	8
			—	—	180			9
		R1, R2	—	—	30		f = 1 MHz, V_{in} = 0 V	

Notes: 1. When a sub-system oscillator (a 32.768 kHz crystal oscillator) is used, f_{OSC} must either be in the range 0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or be in the range 1.6 MHz ≤ f_{OSC} ≤ 5.0 MHz. Furthermore, the SSR11 bit in the system clock selection register 1 (SSR1: $027) must be set to indicate which of those ranges f_{OSC} falls in.

2. When a sub-system oscillator (a 32.768 kHz crystal oscillator) is used, f_{OSC} must either be in the range 0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz or be in the range 1.6 MHz ≤ f_{OSC} ≤ 8.5 MHz. Furthermore, the SSR11 bit in the system clock selection register 1 (SSR1: $027) must be set to indicate which of those ranges f_{OSC} falls in.
3. There are three cases where the oscillator stabilization period applies:
   - When power is first applied, the time between the point when V_{CC} reaches 2.7 V and the point the oscillator is stable.
   - When stop mode is cleared, the time between the point when the $\overline{\text{RESET}}$ input reaches the low level and the point the oscillator is stable.
   - When stop mode is cleared, the time between the point when the $\overline{\text{STOPC}}$ input reaches the low level and the point the oscillator is stable.

   To assure the time necessary to achieve stable oscillation at power on and when clearing stop mode, apply a low level to the $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input for at least tRC.

   Since the oscillator stabilization period varies with the details of the mounted circuit, stray capacitances, and other factors, this value should be determined based on thorough consultations with the manufacturer of the ceramic oscillator used.
4. See figure 25-31.
5. See figure 25-32.
6. See figure 25-33.
7. See figure 25-34.
8. Applies to the HD40A4364, HD40A4368, HD40A43612, and HD40A4369.
9. Applies to the HD407A4369.

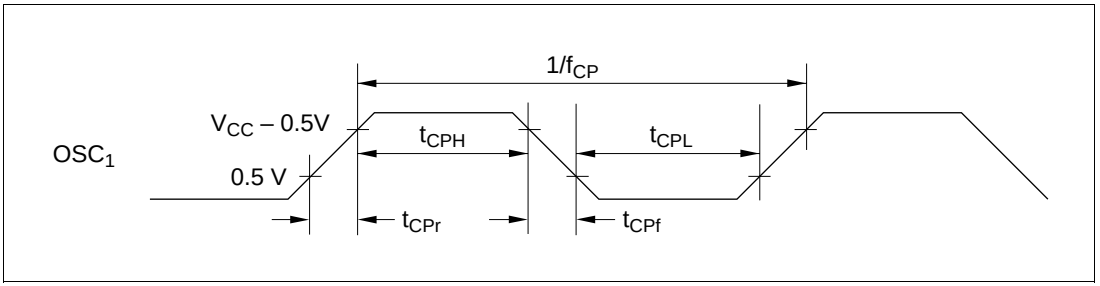


Figure 25-31 External Clock Timing (HD404369 Series)

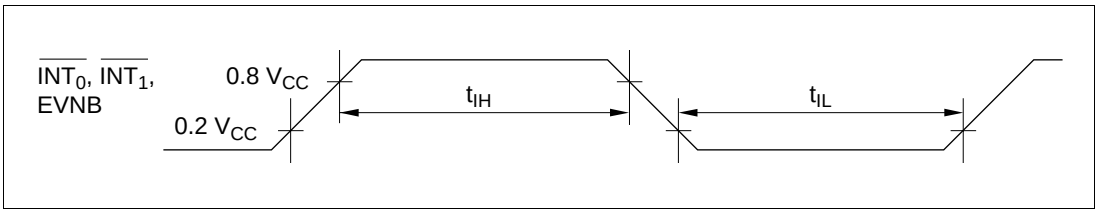


Figure 25-32 Interrupt Timing (HD404369 Series)

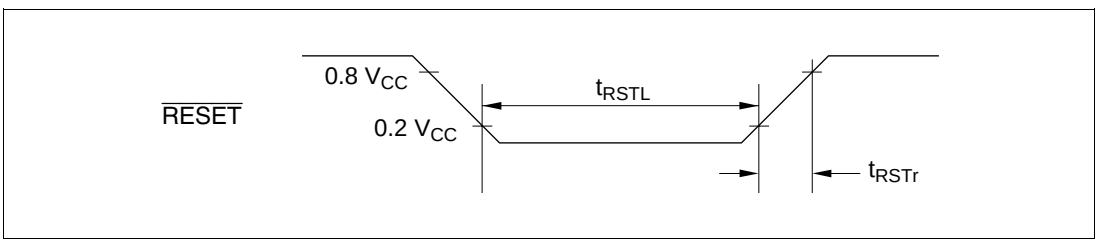


Figure 25-33 Reset Timing (HD404369 Series)

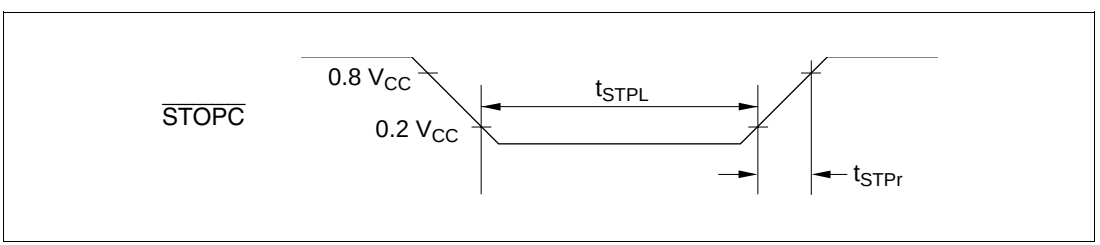


Figure 25-34 $\overline{\text{STOPC}}$ Timing (HD404369 Series)

Table 25-40 Serial Interface Timing Characteristics (HD404369 Series)

HD404364, HD404368, HD4043612, HD404369, HD40A4364, HD40A4368, HD40A43612, HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C,
unless specified otherwise.

When the Transfer Clock is Output:

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	With the load shown in figure 25-36	1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-36	1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}	With the load shown in figure 25-36	1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-36	1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns	With the load shown in figure 25-36	1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-36	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: See figure 25-35.

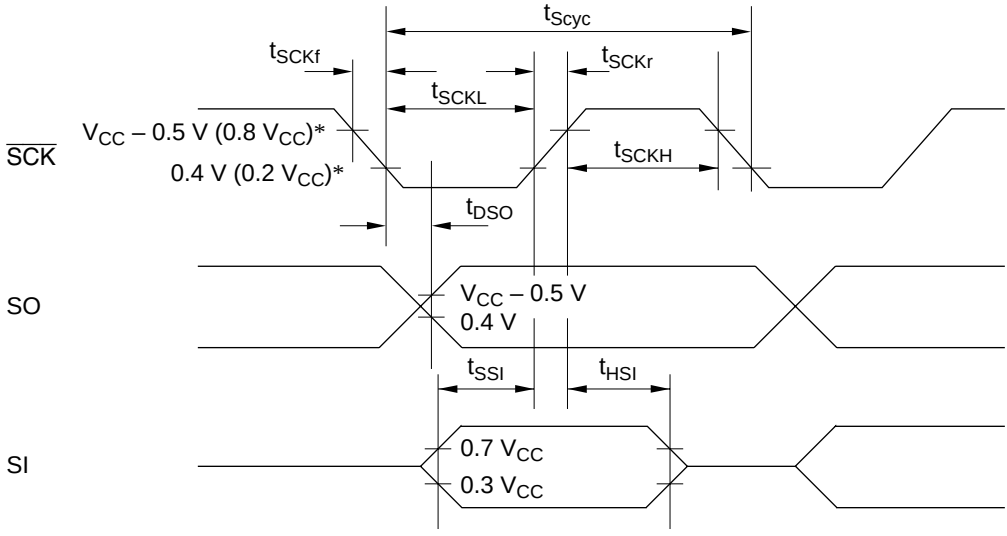
Table 25-40 Serial Interface Timing Characteristics (HD404369 Series) (cont)

HD404364, HD404368, HD4043612, HD404369, HD40A4364, HD40A4368, HD40A43612, HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C,
unless specified otherwise.

When the Transfer Clock is Input:

Item	Symbol	Applicable Pins	Rated Value Min	Typ	Max	Unit	Test Conditions	Notes
Transfer clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transfer clock high level width	t_{SCKH}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock low level width	t_{SCKL}	$\overline{SCK}$	0.4	—	—	t_{Scyc}		1
Transfer clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	80	ns		1
Transfer clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	300	ns	With the load shown in figure 25-36	1
Serial input data setup time	t_{SSI}	SI	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	200	—	—	ns		1

Note: See figure 25-35.



Note: * The values V_{CC} – 0.5 V and 0.4 V are the voltages for transfer clock output.
The values 0.8 V_{CC} and 0.2 V_{CC} are the voltages for transfer clock input.

Figure 25-35 Serial Interface Timing (HD404369 Series)

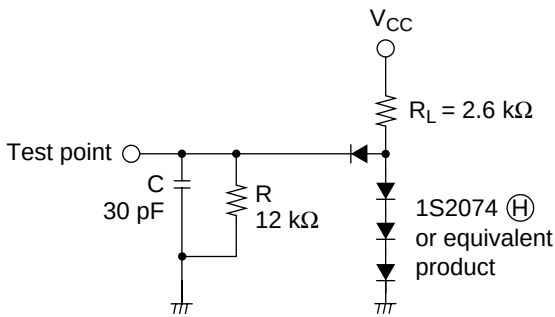


Figure 25-36 Timing Load Circuit

(3) A/D Converter Characteristics

Table 25-41 lists the characteristics of the HD404369 Series A/D converter.

Table 25-41 A/D Converter Characteristics (HD404369 Series)

HD404364, HD404368, HD4043612, HD404369, HD40A4364, HD40A4368, HD40A43612, HD40A4369: V_{CC} = 2.7 to 6.0 V, GND = 0 V, T_a = –20 to 75°C
HD407A4369: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to 75°C,
unless specified otherwise.

Item	Symbol	Applicable Pins	Rated Value			Unit	Test Conditions	Notes
			Min	Typ	Max			
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		1
Analog input voltage	AV_{in}	AN_0 to AN_{11}	AV_{SS}	—	AV_{CC}	V		
Current from AV_{CC} to AV_{SS}	I_{AD}		—	—	200	µA	V_{CC} = AV_{CC} = 5.0 V	
Analog input capacitance	CA_{in}	AN_0 to AN_{11}	—	—	30	pF		
Resolution			8	8	8	Bits		
Number of inputs			0	—	12	Channels		
Absolute precision			—	—	±2.0	LSB		
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0 to AN_{11}	1	—	—	MΩ		

Note: Connect to the V_{CC} pin if the A/D converter is not used in the application.

Appendix A Instruction Set

A.1 Instruction Set Overview

The HMCS400 CPU supports 101 instructions, which can be classified into the following ten classes.

- Immediate instructions
- Register to register instructions
- RAM addressing instructions
- RAM to register instructions
- Arithmetic and logic instructions
- Comparison instructions
- RAM bit manipulation instructions
- ROM addressing instructions
- I/O instructions
- Control instructions

Tables A-1 (1) to A-1 (10) describe the functions of these instructions. The table below describes the operation symbols used in the instruction descriptions.

Operation Symbols

A → B	Move A to B
A ↔ B	Exchange A and B
$\overline{X}$	Logical negation (not) symbol
1	High level
0	Low level
LSB	Low order bit
MSB	High order bit
NZ	A value other than 0 (not zero)
NB	No borrow occurred due to the operation
OVF	Overflow due to an addition
∩	Logical and symbol
∪	Logical or symbol
⊕	Logical exclusive or
≠	Inequality (not equal)
	Comparison symbol (less than or equal)
i, m, p	Expresses a single digit hexadecimal value ($0 to $F).
d	Expresses a three digit hexadecimal value ($000 to $3FF).
n	Expresses a two bit binary number.
a	Expresses a six bit binary number.
b	Expresses an eight bit binary number.
u	Means p and d.
y, x	Expresses either 0 or 1.

Table A-1 (1) Immediate Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Load A from immediate	LAI i	1	0	0	0	1	1	i_3	i_2	i_1	i_0	i → A		1/1
Load B from immediate	LBI i	1	0	0	0	0	0	i_3	i_2	i_1	i_0	i → B		1/1
Load memory from immediate	LMID i, d	0 d_9	1 d_8	1 d_7	0 d_6	1 d_5	0 d_4	i_3 d_3	i_2 d_2	i_1 d_1	i_0 d_0	i → M		2/2
Load memory from immediate, increment Y	LMIIY i	1	0	1	0	0	1	i3	i2	i1	i0	i → M, Y + 1 → Y	NZ	1/1

Table A-1 (2) Register to Register Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Load A from B	LAB	0	0	0	1	0	0	1	0	0	0	B → A		1/1
Load B from A	LBA	0	0	1	1	0	0	1	0	0	0	A → B		1/1
Load A from W	LAW	0 0	1 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	W → A		2/2*
Load A from Y	LAY	0	0	1	0	1	0	1	1	1	1	Y → A		1/1
Load A from SPX	LASPX	0	0	0	1	1	0	1	0	0	0	SPX → A		1/1
Load A from SPY	LASPY	0	0	0	1	0	1	1	0	0	0	SPY → A		1/1
Load A from MR	LAMR m	1	0	0	1	1	1	m_3	m_2	m_1	m_0	MR (m) → A		1/1
Exchange MR and A	XMRA m	1	0	1	1	1	1	m_3	m_2	m_1	m_0	MR (m) ↔ A		1/1

Note: * The LAW and LWA instructions require an operand ($000) in the second word. However, there is no need to explicitly code this word since the assembler will provide it automatically.

Table A-1 (3) RAM Addressing Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Load W from immediate	LWI i	0	0	1	1	1	1	0	0	i1	i0	i → W		1/1
Load X from immediate	LXI i	1	0	0	0	1	0	i3	i2	i1	i0	i → X		1/1
Load Y from immediate	LYI i	1	0	0	0	0	1	i3	i2	i1	i0	i → Y		1/1
Load W from A	LWA	0 0	1 0	0 0	0 0	0 0	1 0	0 0	0 0	0 0	0 0	A → W		2/2*
Load X from A	LXA	0	0	1	1	1	0	1	0	0	0	A → X		1/1
Load Y from A	LYA	0	0	1	1	0	1	1	0	0	0	A → Y		1/1
Increment Y	IY	0	0	0	1	0	1	1	1	0	0	Y + 1 → Y	NZ	1/1
Decrement Y	DY	0	0	1	1	0	1	1	1	1	1	Y Ð 1 → Y	NB	1/1
Add A to Y	AYY	0	0	0	1	0	1	0	1	0	0	Y + A → Y	OVF	1/1
Subtract A from Y	SYY	0	0	1	1	0	1	0	1	0	0	Y Ð A → Y	NB	1/1
Exchange X and SPX	XSPX	0	0	0	0	0	0	0	0	0	1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0	0	0	0	0	0	0	0	1	0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0	0	0	0	0	0	0	0	1	1	X ↔ SPX, Y ↔ SPY		1/1

Note: * The LAW and LWA instructions require an operand ($000) in the second word. However, there is no need to explicitly code this word since the assembler will provide it automatically.

Table A-1 (4) RAM to Register Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Load A from memory	LAM(XY)	0	0	1	0	0	1	0	0	y	x	M → A (X ⊕ SPX, Y ⊕ SPY)		1/1
Load A from memory	LAMD d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	0 d_1	0 d_0	M → A		2/2
Load B from memory	LBM(XY)	0	0	0	1	0	0	0	0	y	x	M → B (X ⊕ SPX, Y ⊕ SPY)		1/1
Load memory from A	LMA(XY)	0	0	1	0	0	1	0	1	y	x	A → M (X ⊕ SPX, Y ⊕ SPY)		1/1
Load memory from A	LMAD d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	1 d_4	0 d_3	1 d_2	0 d_1	0 d_0	A → M		2/2
Load memory from A, increment Y	LMAIY(X)	0	0	0	1	0	1	0	0	0	x	A → M Y + 1 → Y (X ⊕ SPX)	NZ	1/1
Load memory from A, decrement Y	LMADY(X)	0	0	1	1	0	1	0	0	0	x	A → M Y Ð 1 → Y (X ⊕ SPX)	NB	1/1
Exchange memory and A	XMA(XY)	0	0	1	0	0	0	0	0	y	x	M → A (X ⊕ SPX, Y ⊕ SPY)		1/1
Exchange memory and A	XMAD d	0 d9	1 d8	1 d7	0 d6	0 d5	0 d4	0 d3	0 d2	0 d1	0 d0	M ⊕ A		2/2
Exchange memory and B	XMB(XY)	0	0	1	1	0	0	0	0	y	x	M ⊕ B (X ⊕ SPX, Y ⊕ SPY)		1/1

Note: The terms (XY) and (X) in the mnemonics are interpreted as follows.

¥ Mnemonics with (XY) represent four mnemonics. The table below uses LAM(XY) as an example. The assembler generates the bits y and x shown in the table below for these instructions.

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X ↔ SPX, Y ↔ SPY

¥ Mnemonics with (X) represent two mnemonics. The table below uses LMAIY(X) as an example. The assembler generates the bit x shown in the table below for these instructions.

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table A-1 (5) Arithmetic and Logic Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Add immediate to A	AI i	1	0	1	0	0	0	i_3	i_2	i_1	i_0	A + i → A	OVF	1/1
Increment B	IB	0	0	0	1	0	0	1	1	0	0	B + 1 → B	NZ	1/1
Decrement B	DB	0	0	1	1	0	0	1	1	1	1	B Ð 1 → B	NB	1/1
Decimal adjust for addition	DAA	0	0	1	0	1	0	0	1	1	0			1/1
Decimal adjust for subtraction	DAS	0	0	1	0	1	0	1	0	1	0			1/1
Negate A	NEGA	0	0	0	1	1	0	0	0	0	0	$\overline{A}$ + 1 → A		1/1
Complement B	COMB	0	1	0	1	0	0	0	0	0	0	$\overline{B}$ → B		1/1
Rotate right A with carry	ROTR	0	0	1	0	1	0	0	0	0	0			1/1
Rotate left A with carry	ROTL	0	0	1	0	1	0	0	0	0	1			1/1
Set carry	SEC	0	0	1	1	1	0	1	1	1	1	1 → CA		1/1
Reset carry	REC	0	0	1	1	1	0	1	1	0	0	0 → CA		1/1
Test carry	TC	0	0	0	1	1	0	1	1	1	1		CA	1/1
Add A to memory	AM	0	0	0	0	0	0	1	0	0	0	M + A → A	OVF	1/1
Add A to memory	AMD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	M + A → A	OVF	2/2
Add A to memory with carry	AMC	0	0	0	0	0	1	1	0	0	0	M + A + CA → A OVF → CA	OVF	1/1
Add A to memory with carry	AMCD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	M + A + CA → A OVF → CA	OVF	2/2
Subtract A from memory with carry	SMC	0	0	1	0	0	1	1	0	0	0	M Ð A Ð $\overline{CA}$ → A NB → CA	NB	1/1
Subtract A from memory with carry	SMCD d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	M Ð A Ð $\overline{CA}$ → A NB → CA	NB	2/2
OR A and B	OR	0	1	0	1	0	0	0	1	0	0	A ∪ B → A		1/1
AND memory with A	ANM	0	0	1	0	0	1	1	1	0	0	A ∩ M → A	NZ	1/1
AND memory with A	ANMD d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	1 d_2	0 d_1	0 d_0	A ∩ M → A	NZ	2/2
OR memory with A	ORM	0	0	0	0	0	0	1	1	0	0	A ∪ M → A	NZ	1/1
OR memory with A	ORMD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	0 d_4	1 d_3	1 d_2	0 d_1	0 d_0	A ∪ M → A	NZ	2/2
EOR memory with A	EORM	0	0	0	0	0	1	1	1	0	0	A ⊕ M → A	NZ	1/1
EOR memory with A	EORMD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	1 d_4	1 d_3	1 d_2	0 d_1	0 d_0	A ⊕ M → A	NZ	2/2

Table A-1 (6) Comparison Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Immediate not equal to memory	INEM i	0	0	0	0	1	0	i3	i2	i1	i0	i ≠ M	NZ	1/1
Immediate not equal to memory	INEMD i, d	0 d_9	1 d_8	0 d_7	0 d_6	1 d_5	0 d_4	I_3 d_3	I_2 d_2	I_1 d_1	I_0 d_0	i ≠ M	NZ	2/2
A not equal to memory	ANEM	0	0	0	0	0	0	0	1	0	0	A ≠ M	NZ	1/1
A not equal to memory	ANEMD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	1 d_2	0 d_1	0 d_0	A ≠ M	NZ	2/2
B not equal to memory	BNEM	0	0	0	1	0	0	0	1	0	0	B ≠ M	NZ	1/1
Y not equal to immediate	YNEI i	0	0	0	1	1	1	i_3	i_2	i_1	i_0	Y ≠ i	NZ	1/1
Immediate less than or equal to memory	ILEM i	0	0	0	0	1	1	i_3	i_2	i_1	i_0	i M	NB	1/1
Immediate less than or equal to memory	ILEMD i, d	0 d_9	1 d_8	0 d_7	0 d_6	1 d_5	1 d_4	I_3 d_3	I_2 d_2	I_1 d_1	I_0 d_0	i M	NB	2/2
A less than or equal to memory	ALEM	0	0	0	0	0	1	0	1	0	0	A M	NB	1/1
A less than or equal to memory	ALEMD d	0 d_9	1 d_8	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	1 d_2	0 d_1	0 d_0	A M	NB	2/2
B less than or equal to memory	BLEM	0	0	1	1	0	0	0	1	0	0	B M	NB	1/1
A less than or equal to immediate	ALEI i	1	0	1	0	1	1	i_3	i_2	i_1	i_0	A i	NB	1/1

Table A-1 (7) RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Set memory bit	SEM n	0	0	1	0	0	0	0	1	n_1	n_0	1 → M (n)		1/1
Set memory bit	SEMD n, d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	0 d_4	0 d_3	1 d_2	n_1 d_1	n_0 d_0	1 → M (n)		2/2
Reset memory bit	REM n	0	0	1	0	0	0	1	0	n_1	n_0	0 → M (n)		1/1
Reset memory bit	REMD n, d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	n_1 d_1	n_0 d_0	0 → M (n)		2/2
Test memory bit	TM n	0	0	1	0	0	0	1	1	n_1	n_0		M (n)	1/1
Test memory bit	TMD n, d	0 d_9	1 d_8	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	1 d_2	n_1 d_1	n_0 d_0		M (n)	2/2

Table A-1 (8) ROM Addressing Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Branch on status 1	BR b	1	1	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0		1	1/1
Long branch on status 1	BRL u	0 d_9	1 d_8	0 d_7	1 d_6	1 d_5	1 d_4	p_3 d_3	p_2 d_2	p_1 d_1	p_0 d_0		1	2/2
Long jump unconditionally	JMPL u	0 d_9	1 d_8	0 d_7	1 d_6	0 d_5	1 d_4	p_3 d_3	p_2 d_2	p_1 d_1	p_0 d_0			2/2
Subroutine jump on status 1	CAL a	0	1	1	1	a_5	a_4	a_3	a_2	a_1	a_0		1	1/2
Long subroutine jump on status 1	CALL u	0 d_9	1 d_8	0 d_7	1 d_6	1 d_5	0 d_4	p_3 d_3	p_2 d_2	p_1 d_1	p_0 d_0		1	2/2
Table branch	TBR p	0	0	1	0	1	1	p_3	p_2	p_1	p_0			1/1
Return from subroutine	RTN	0	0	0	0	0	1	0	0	0	0			1/3
Return from interrupt	RTNI	0	0	0	0	0	1	0	0	0	1	$1 \rightarrow$ IE, CA restored	ST	1/3

Table A-1 (9) I/O Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
Set discrete I/O latch	SED	0	0	1	1	1	0	0	1	0	0	$1 \rightarrow$ D (Y)		1/1
Set discrete I/O latch direct	SEDD m	1	0	1	1	1	0	m_3	m_2	m_1	m_0	$1 \rightarrow$ D (m)		1/1
Reset discrete I/O latch	RED	0	0	0	1	1	0	0	1	0	0	$0 \rightarrow$ D (Y)		1/1
Reset discrete I/O latch direct	REDD m	1	0	0	1	1	0	m_3	m_2	m_1	m_0	$0 \rightarrow$ D (m)		1/1
Test discrete I/O latch	TD	0	0	1	1	1	0	0	0	0	0		D (Y)	1/1
Test discrete I/O latch direct	TDD m	1	0	1	0	1	0	m_3	m_2	m_1	m_0		D (m)	1/1
Load A from R-port register	LAR m	1	0	0	1	0	1	m_3	m_2	m_1	m_0	R (m) $\rightarrow$ A		1/1
Load B from R-port register	LBR m	1	0	0	1	0	0	m_3	m_2	m_1	m_0	R (m) $\rightarrow$ B		1/1
Load R-port register from A	LRA m	1	0	1	1	0	1	m_3	m_2	m_1	m_0	A $\rightarrow$ R (m)		1/1
Load R-port register from B	LRB m	1	0	1	1	0	0	m_3	m_2	m_1	m_0	B $\rightarrow$ R (m)		1/1
Pattern generation	P p	0	1	1	0	1	1	p_3	p_2	p_1	p_0			1/2

Table A-1 (10) Control Instructions

Operation	Mnemonic	Operation Code										Function	Status	Words/ Cycles
No operation	NOP	0	0	0	0	0	0	0	0	0	0			1/1
Start serial	STS	0	1	0	1	0	0	1	0	0	0			1/1
Standby mode/watch mode*	SBY	0	1	0	1	0	0	1	1	0	0			1/1
Stop mode/watch mode	STOP	0	1	0	1	0	0	1	1	0	1			1/1

Note: * Only on the transition from subactive mode.

A.2 Operation Code Map

Table A-2 Opcode Map

R8		0															
R9	H / L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	XSPX	XSPY	XSPXY	ANEM				AM				ORM			
	1	RTN	RTNI			ALEM				AMC				EORM			
	2	INEM i(4)															
	3	INEM i(4)															
	4	LBM(XY)				BNEM				LAB				IB			
	5	LMAIY(X)				AYY				LASPY				IY			
	6	NEGA				RED				LASPX							TC
	7	YNEI i(4)															
	8	LMA(XY)				SEM n(2)				REM n(2)				TM n(2)			
	9	LAM(XY)				LMA(XY)				SMC				ANM			
	A	ROTR	ROTL					DAA				DAS					LAY
	B	TBR p(4)															
	C	XMB(XY)				BLEM				LBA							DB
	D	LMADY(X)				SYY				LYA							DY
	E	TD				SED				LXA				REC			SEC
	F	LWI i(2)															
1	0	LBI i(4)															
	1	LYI i(4)															
	2	LXI i(4)															
	3	LAI i(4)															
	4	LBR m(4)															
	5	LAR m(4)															
	6	REDD m(4)															
	7	LAMR m(4)															
	8	AI i(4)															
	9	LMIY i(4)															
	A	TDD m(4)															
	B	ALEI i(4)															
	C	LRB m(4)															
	D	LRA m(4)															
	E	SEDD m(4)															
	F	XMRA m(4)															

One word/two cycle instructions

One word/three cycle instructions

RAM direct addressing instructions (two word/ two cycles)

Two word/two cycle instructions

Table A-2 Opcode Map (cont)

R9	H \ R8 L	1															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	LAW				ANEMD				AMD				ORMD			
	1	LWA				ALEMD				AMCD				EORMD			
	2	INEMD i(4)															
	3	INEMD i(4)															
	4	COMB				OR				STS				SBY	STOP		
	5	JMPL p(4)															
	6	CALL p(4)															
	7	BRL p(4)															
	8	XMAD				SEMD n(2)				REMD n(2)				TMD n(2)			
	9	LAMD				LMAD				SMCD				ANMD			
	A	LMID i(4)															
	B	P p(4)															
	C	CAL a(6)															
	D																
	E																
	F																
1	0	BR b(8)															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																

One word/two cycle instructions

One word/three cycle instructions

RAM direct addressing instructions (two word/ two cycles)

Two word/two cycle instructions

B.1 I/O Registers (1)

No indication: Registers and bits common to all products in the HMCS43XX family.
△: Registers and bits supported by the HD404318, HD404358, and HD404358R Series.
▲: Registers and bits supported by the HD404339 and HD404369 Series.
▒: Registers and bits that are unused in all products in the HMCS43xx family.

RAM Address	Register	Symbol	Bit				Module/Function
			Bit 3	Bit 2	Bit 1	Bit 0	
$000	Interrupt control bit area		IM0	IF0	RSP	IE	Interrupt control
$001			IMTA△▲	IFTA△▲	IM1△▲	IF1△▲	
$002			IMTC	IFTC	IMTB	IFTB	
$003			IMS	IFS	IMAD	IFAD	
$004	Port mode register A	PMRA	PMRA3△▲	PMRA2	PMRA1	PMRA0	D_3 and R_0 port pin function switching
$005	Serial mode register	SMR	SMR3	SMR2	SMR1	SMR0	Serial interface
$006	Serial data register L	SRL	SR3	SR2	SR1	SR0	
$007	Serial data register U	SRU	SR7	SR6	SR5	SR4	
$008	Timer mode register A	TMA△▲	TMA3▲	TMA2△▲	TMA1△▲	TMA0△▲	Timer A
$009	Timer mode register B1	TMB1	TMB13	TMB12	TMB11	TMB10	Timer B
$00A	Timer read register BL/	TRBL	TRBL3	TRBL2	TRBL1	TRBL0	
	Timer write register BL	TWBL	TWBL3	TWBL2	TWBL1	TWBL0	
$00B	Timer read register BU/	TRBU	TRBU3	TRBU2	TRBU1	TRBU0	
	Timer write register BU	TWBU	TWBU3	TWBU2	TWBU1	TWBU0	
$00C	Miscellaneous register	MIS	MIS3	MIS2	MIS1▲	MIS0▲	System control and other functions
$00D	Timer mode register C	TMC	TMC3	TMC2	TMC1	TMC0	Timer C
$00E	Timer read register CL/	TRCL	TRCL3	TRCL2	TRCL1	TRCL0	
	Timer write register CL	TWCL	TWCL3	TWCL2	TWCL1	TWCL0	
$00F	Timer read register CU/	TRCU	TRCU3	TRCU2	TRCU1	TRCU0	
	Timer write register CU	TWCU	TWCU3	TWCU2	TWCU1	TWCU0	
$010 to $015	—	—	▒	▒	▒	▒	—
$016	A/D channel register	ACR	ACR3*1	ACR2*1	ACR1*1	ACR0*1	A/D converter
$017	A/D data register L	ADRL	ADRL3	ADRL2	ADRL1	ADRL0	
$018	A/D data register U	ADRU	ADRU3	ADRU2	ADRU1	ADRU0	
$019	A/D mode register 1	AMR1	AMR13	AMR12	AMR11	AMR10*2	
$01A	A/D mode register 2	AMR2	▒	AMR22△	AMR21△▲	AMR20	

Notes: 1. Specification of a channel number not supported by the particular product is illegal.
2. AMR10 is unused only in the HD404394 Series.

B.1 I/O Registers (1) (cont)

No indication: Registers and bits common to all products in the HMCS43XX family.
△: Registers and bits supported by the HD404318, HD404358, and HD404358R Series.
▲: Registers and bits supported by the HD404339 and HD404369 Series.
: Registers and bits that are unused in all products in the HMCS43xx family.

RAM Address	Register	Symbol	Bit				Module/Function
			Bit 3	Bit 2	Bit 1	Bit 0	
$01B to $01F	—	—					—
$020	Register flag area		DTON▲	ADSF	WDON	LSON▲	Flags used by peripheral modules and other functions
$021			RAME	IAOF	ICEF△▲	ICSF△▲	
$022							
$023							
$024	Port mode register B	PMRB	PMRB3	PMRB2△▲	PMRB1△▲	PMRB0	D port pin function switching
$025	Port mode register C	PMRC	PMRC3△▲	PMRC2△▲	PMRC1	PMRC0	Serial interface
$026	Timer mode register B2	TMB2		TMB22△▲	TMB21	TMB20	Timer B
$027	System clock selection register 1	SSR1▲	SSR13▲	SSR12▲	SSR11▲		Clock oscillator
$028	System clock selection register 2	SSR2▲			SSR21▲	SSR20▲	
$029 to $02B	—	—					—
$02C to $039	Data control register	DCD0 to DCD3, DCR0 to DCR9	The set of valid bits differs between products. See sections 7 to 12, “I/O Ports”, for details.				Port I/O control
$03A to $03F	—	—					—

B.2 I/O Registers (2)

$004—Port Mode Register A **PMRA** **D0 and R0 ports**

Bit	3	2	1	0
	PMRA3*	PMRA2	PMRA1	PMRA0
Initial value	0	0	0	0
Read/Write	W	W	W	W

$R0_2$/SO pin function switch

0	$R0_2$ I/O pin
1	SO output pin

$R0_1$/SI pin function switch

0	$R0_1$ I/O pin
1	SI input pin

$R0_3$/TOC pin function switch

0	$R0_3$ I/O pin
1	TOC output pin

D_3/BUZZ pin function switch*

0	D_3 I/O pin
1	BUZZ output pin

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The PMRA3 bit is unused in the HD404344R and HD404394 Series.

Bit	3	2	1	0
	SMR3	SMR2	SMR1	SMR0
Initial value	0	0	0	0
Read/Write	W	W	W	W

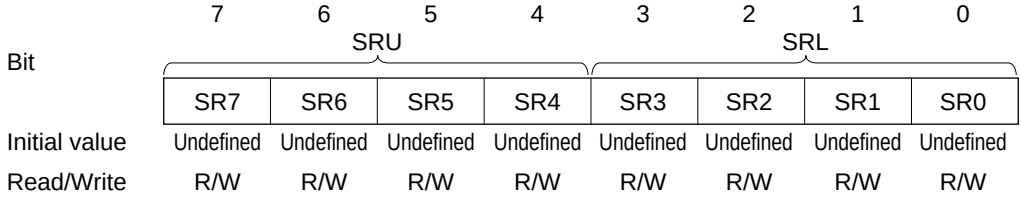
Transfer clock selection

SMR2	SMR1	SMR0	$\overline{\text{SCK}}$ pin	Clock source	Prescaler divisor*
0	0	0	Output	PSS	$ø_{PER}/2048$
		1	Output	PSS	$ø_{PER}/512$
	1	0	Output	PSS	$ø_{PER}/128$
		1	Output	PSS	$ø_{PER}/32$
1	0	0	Output	PSS	$ø_{PER}/8$
		1	Output	PSS	$ø_{PER}/2$
	1	0	Output	System clock	$ø_{PER}$
		1	Input	External clock	—

$R0_0/\overline{\text{SCK}}$ pin function switch

0	$R0_0$ I/O pin
1	$\overline{\text{SCK}}$ I/O pin

Note: * The transfer clock divisor is determined by the combination of the prescaler divisor specified by the SMR2 to SMR0 bits and the prescaler output divisor (2 or 4) specified by the PMRC PMRC0 bit.


Bit
7
6
5
4
3
2
1
0
SRU
SRL
SR7
SR6
SR5
SR4
SR3
SR2
SR1
SR0
Initial value
Undefined
Undefined
Undefined
Undefined
Undefined
Undefined
Undefined
Undefined
Read/Write
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W

HD404318/HD404358/HD404358R Series

Bit	3	2	1	0
	—	TMA2	TMA1	TMA0
Initial value	—	0	0	0
Read/Write	—	W	W	W

Unused

Timer A clock selection

TMA2	TMA1	TMA0	Input clock period
0	0	0	2048 t_{cyc}
		1	1024 t_{cyc}
	1	0	512 t_{cyc}
		1	128 t_{cyc}
1	0	0	32 t_{cyc}
		1	8 t_{cyc}
	1	0	4 t_{cyc}
		1	2 t_{cyc}

Note: $t_{cyc} = f_{OSC}/4$

HD404339/HD404369 Series

Bit	3	2	1	0
	TMA3	TMA2	TMA1	TMA0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Timer A clock selection

TMA3	TMA2	TMA1	TMA0	Prescaler	Input clock period	Mode
0	0	0	0	PSS	2048 t_{cyc} *1	Free-running timer mode
			1	PSS	1024 t_{cyc}	
		1	0	PSS	512 t_{cyc}	
			1	PSS	128 t_{cyc}	
	1	0	0	PSS	32 t_{cyc}	
			1	PSS	8 t_{cyc}	
		1	0	PSS	4 t_{cyc}	
			1	PSS	2 t_{cyc}	
1	0	0	0	PSW	32 t_{wcyc} *2	Clock time base mode
			1	PSW	16 t_{wcyc}	
		1	0	PSW	8 t_{wcyc}	
			1	PSW	2 t_{wcyc}	
	1	0	0	—	1/2 t_{wcyc}	
			1	—	Unused	
		1	*	—	PSW and TCA clear	

Notes: 1. $t_{cyc} = f_{OSC}/4$, $f_{OSC}/8$, $f_{OSC}/16$ or $f_{OSC}/32$
2. $t_{Wcyc} = f_X/8$

* Don't care

Bit	3	2	1	0
	TMB13	TMB12	TMB11	TMB10
Initial value	0	0	0	0
Read/Write	W	W	W	W

Timer B clock selection

TMB12	TMB11	TMB10	Input clock source
0	0	0	2048 t_{cyc}
		1	512 t_{cyc}
	1	0	128 t_{cyc}
		1	32 t_{cyc}
1	0	0	8 t_{cyc}
		1	4 t_{cyc}
	1	0	2 t_{cyc}
		1	EVNB (external event input pin)

Note: Set port mode register B as shown below when either t_{cyc} = f_{OSC}/4 or external event input is used as the timer B clock.

HD404344R/HD404394 Series: Set the PMRB0 bit to 1.
HD404318/HD404358/HD404358R/HD404339/HD404369 Series: Set the PMRB2 bit to 1.

Timer B function selection

0	Free-running timer
1	Reload timer

$00A—Timer Read Register BL **TRBL** **Timer B**
$00B—Timer Read Register BU **TRBU**

	Bit	3	2	1	0
TRBU		TRBU3	TRBU2	TRBU1	TRBU0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	R	R	R	R

	Bit	3	2	1	0
TRBL		TRBL3	TRBL2	TRBL1	TRBL0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	R	R	R	R

$00A—Timer Write Register BL **TWBL** **Timer B**
$00B—Timer Write Register BU **TWBU**

	Bit	3	2	1	0
TWBU		TWBU3	TWBU2	TWBU1	TWBU0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	W	W	W	W

	Bit	3	2	1	0
TWBL		TWBL3	TWBL2	TWBL1	TWBL0
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

Bit	3	2	1	0
	MIS3	MIS2	MIS1[*1]	MIS0[*1]
Initial value	0	0	0	0
Read/Write	W	W	W	W

Interrupt frame period and oscillator stabilization period[*1]

MIS1	MIS0	Interrupt frame period	Oscillator stabilization period	Oscillator circuit conditions
0	0	0.24414 ms	0.12207 (0.24414) ms[*2]	External clock
	1	15.625 ms	7.8125 ms	Ceramic oscillator
1	0	125 ms	62.5 ms	Crystal oscillator
	1	Unused		—

$R0_2$/SO pin output buffer control

0	PMOS transistor active (CMOS output)
1	PMOS transistor off (NMOS open drain output)

Pull-up MOS transistor control

0	All pull-up MOS transistors off
1	Pull-up MOS transistors active

Notes: 1. Applies to the HD404339 and HD404369 Series. Unused in the HD404318, HD404358, HD404358R, HD404344R, and HD404394 Series.
2. Values in parentheses are direct transition times.

Bit	3	2	1	0
	TMC3	TMC2	TMC1	TMC0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Timer C clock selection

TMC2	TMC1	TMC0	Input clock cource
0	0	0	2048 t_{cyc}
		1	1024 t_{cyc}
	1	0	512 t_{cyc}
		1	128 t_{cyc}
1	0	0	32 t_{cyc}
		1	8 t_{cyc}
	1	0	4 t_{cyc}
		1	2 t_{cyc}

Timer C function selection

0	Free-running timer
1	Reload timer

	Bit	3	2	1	0
TRCU		TRCU3	TRCU2	TRCU1	TRCU0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	R	R	R	R

	Bit	3	2	1	0
TRCL		TRCL3	TRCL2	TRCL1	TRCL0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	R	R	R	R

$00E—Timer Write Register CL **TWCL** **Timer C**
$00F—Timer Write Register CU **TWCU**

	Bit	3	2	1	0
TWCU		TWCU3	TWCU2	TWCU1	TWCU0
	Initial value	Undefined	Undefined	Undefined	Undefined
	Read/Write	W	W	W	W

	Bit	3	2	1	0
TWCL		TWCL3	TWCL2	TWCL1	TWCL0
	Initial value	0	0	0	0
	Read/Write	W	W	W	W

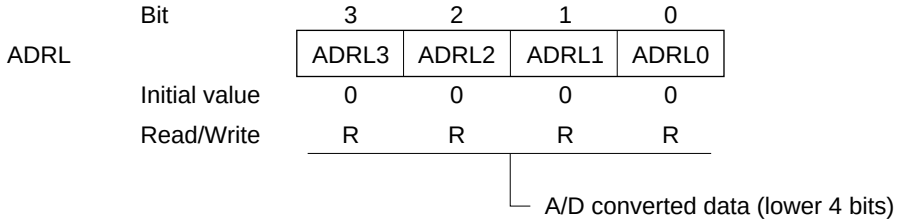
Bit	3	2	1	0
	ACR3	ACR2	ACR1	ACR0
Initial value	0	0	0	0
Read/Write	W	W	W	W

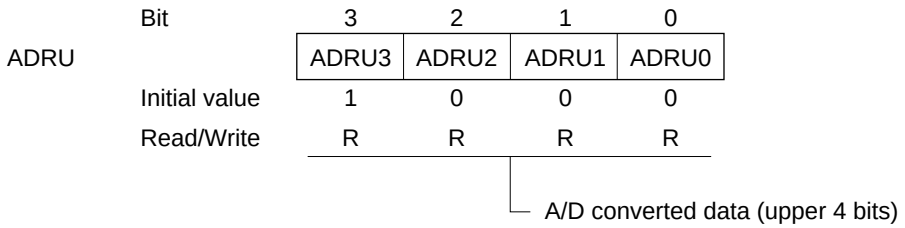
Analog input channel selection

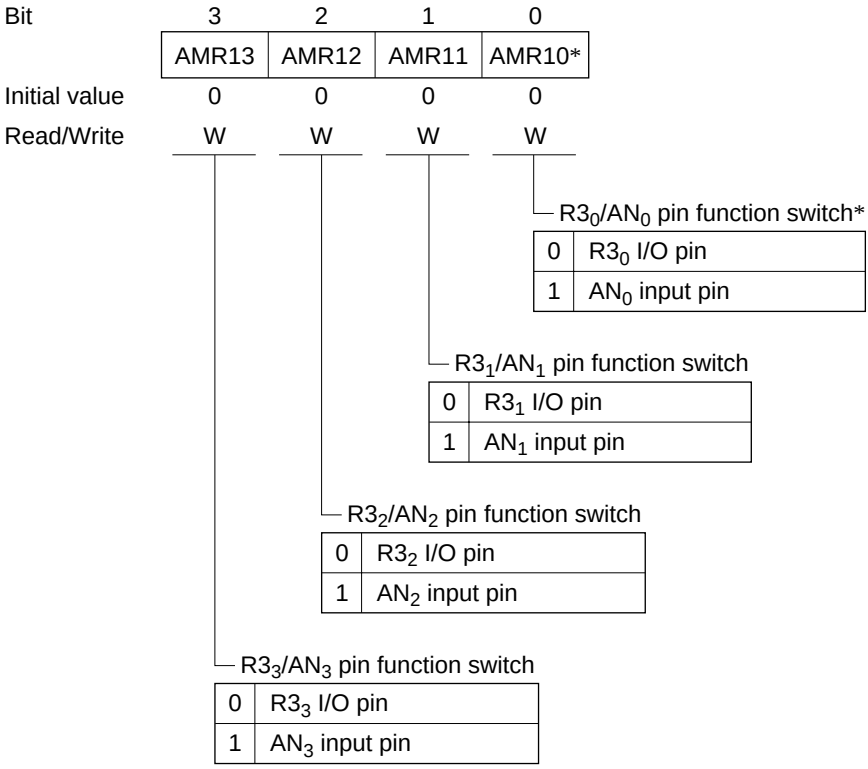
ACR3	ACR2	ACR1	ACR0	Input channel			
				HD404344R	HD404394	HD404318/ HD404358/ HD404358R	HD404339/ HD404369
0	0	0	0	AN_0		AN_0	AN_0
			1	AN_1	AN_1	AN_1	AN_1
		1	0	AN_2	AN_2	AN_2	AN_2
			1	AN_3	AN_3	AN_3	AN_3
	1	0	0			AN_4	AN_4
			1			AN_5	AN_5
		1	0			AN_6	AN_6
			1			AN_7	AN_7
1	0	0	0				AN_8
			1				AN_9
		1	0				AN_{10}
			1				AN_{11}
	1	*	*				

Note: * Don't care

: Unused


Bit
3
2
1
0
ADRL
ADRL3
ADRL2
ADRL1
ADRL0
Initial value
0
0
0
0
Read/Write
R
R
R
R
A/D converted data (lower 4 bits)


Bit
3
2
1
0
ADRU
ADRU3
ADRU2
ADRU1
ADRU0
Initial value
1
0
0
0
Read/Write
R
R
R
R
A/D converted data (upper 4 bits)



Note: * Applies to the HD404344R, HD404318, HD404358, HD404358R, HD404339, and HD404369 Series.
The AMR10 bit is unused in the HD404394 Series.

Bit	3	2	1	0
	—	AMR22*2	AMR21*1	AMR20
Initial value	—	0	0	0
Read/Write	—	W	W	W

Unused

A/D conversion time

0	34 t_{cyc}
1	67 t_{cyc}

$R4_0/AN_4$ to $R4_3/AN_7$ pin function switch*1

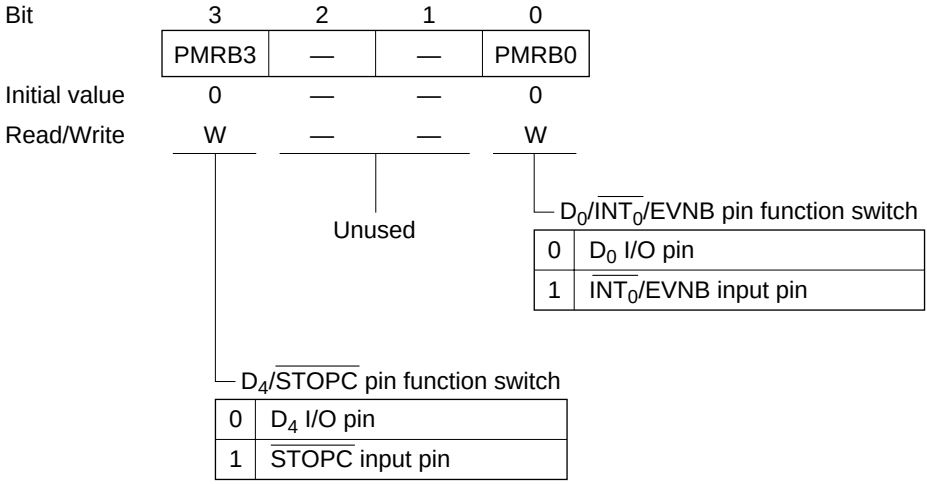
0	$R4_0$ to $R4_3$ I/O pins
1	AN_4 to AN_7 input pins

$R5_0/AN_8$ to $R5_3/AN_{11}$ pin function switch*2

0	$R5_0$ to $R5_3$ I/O pins
1	AN_8 to AN_{11} input pins

Notes: 1. Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The AMR21 bit is unused in the HD404344R and HD404394 Series.
2. Applies to the HD404339 and HD404369 Series. The AMR22 bit is unused in the HD404344R, HD404394, HD404318, HD404358, and HD404358R Series.

HD404344R/HD404394 Series



HD404318/HD404358/HD404358R/HD404339/HD404369 Series

Bit	3	2	1	0
	PMRB3	PMRB2	PMRB1	PMRB0
Initial value	0	0	0	0
Read/Write	W	W	W	W

$D_0/\overline{INT_0}$ pin function switch

0	D_0 I/O pin
1	$\overline{INT_0}$ input pin

$D_1/\overline{INT_1}$ pin function switch

0	D_1 I/O pin
1	$\overline{INT_1}$ input pin

D_2/EVNB pin function switch

0	D_2 I/O pin
1	EVNB input pin

$D_4/\overline{STOPC}$ pin function switch

0	D_4 I/O pin
1	$\overline{STOPC}$ input pin

Bit	3	2	1	0
	PMRC3*	PMRC2*	PMRC1	PMRC0
Initial value	0	0	0	0
Read/Write	W	W	W	W

Transfer clock divisor selection

0	PSS output divided by 2
1	PSS output divided by 4

Idle time high/low output control

0	The SO pin outputs a low level during idle
1	The SO pin outputs a high level during idle

Alarm frequency selection

PMRC3	PMRC2	Alarm frequency
0	0	$ø_{PER}/2048$
	1	$ø_{PER}/1024$
1	0	$ø_{PER}/512$
	1	$ø_{PER}/256$

$ø_{PER}$: The built-in peripheral module operating clock

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The PMRC3 and PMRC2 bits are unused in the HD404344R and HD404394 Series.

Bit	3	2	1	0
	—	TMB22*	TMB21	TMB20
Initial value		0	0	0
Read/Write	—	R/W	R/W	R/W

EVNB pin edge detection selection

TMB21	TMB20	EVNB pin edge detection
0	0	No detection
	1	Falling edge detection
1	0	Rising edge detection
	1	Falling/rising edge pair detection

Input capture setting*

0	Free-running/reload timer
1	Input capture timer

Note: * Applies to the HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The TMB22 bit is unused in the HD404344R and HD404394 Series.

HD404339/HD404369 Series

Bit	3	2	1	0
	SSR13	SSR12	SSR11	—
Initial value	0	0	0	—
Read/Write	W	W	W	—

Unused

System clock selection*1

0	0.4 to 1.0MHz
1	1.6 to 4.5 MHz (HD404339 Series)
	1.6 to 5.0 MHz (HD404369 Series)*2
	1.6 to 8.5 MHz (HD404369 Series)*3

Subsystem clock divisor switch

0	$f_{SUB} = f_X/8$
1	$f_{SUB} = f_X/4$

Subsystem clock stop setting

0	The subsystem clock operates in stop mode
1	The subsystem clock stops in stop mode

Notes: 1. When the subsystem clock (32.768 kHz crystal oscillator) is used, use the ranges 0.4 MHz ≤ f_{OSC} ≤ 1.0 MHz and 1.6 MHz ≤ f_{OSC} ≤ 4.5 MHz (8.5 MHz: HD404369 Series).
2. Applies to the HD404364, HD404368, HD4043612, and HD404369.
3. Applies to the HD40A4364, HD40A4368, HD40A43612, HD40A4369, and HD407A4369.

$028—System Clock Selection Register 2 **SSR2** **Clock oscillator**

HD404339/HD404369 Series

Bit	3	2	1	0
	—	—	SSR21	SSR20
Initial value	—	—	0	0
Read/Write	—	—	W	W

Unused

System clock divisor selection

0	0	Division by 4 ($f_{cyc} = f_{OSC}/4$)
	1	Division by 8 ($f_{cyc} = f_{OSC}/8$)
1	0	Division by 16 ($f_{cyc} = f_{OSC}/16$)
	1	Division by 32 ($f_{cyc} = f_{OSC}/32$)

$02C—Data Control Register D0 **DCD0** **D port**

HD404344R/HD404394/HD404358/HD404358R/HD404369 Series

Bit	3	2	1	0
	DCD03	DCD02	DCD01	DCD00
Initial value	0	0	0	0
Read/Write	W	W	W	W

$02D—Data Control Register D1 **DCD1** **D port**

HD404344R/HD404394/HD404358/HD404358R/HD404369 Series

Bit	3	2	1	0
	DCD13*	DCD12*	DCD11	DCD10
Initial value	0	0	0	0
Read/Write	W	W	W	W

Note: * Applies to the HD404358, HD404358R, and HD404369 Series. The DCD13 and DCD12 bits are unused in the HD404344R and HD404394 Series.

$02E—Data Control Register D2 **DCD2** **D port**

HD404358/HD404358R/HD404369 Series

Bit	3	2	1	0
	DCD23*	DCD22*	DCD21*	DCD20
Initial value	0	0	0	0
Read/Write	W	W	W	W

Note: * Applies to the HD404369 Series. The DCD23 to DCD21 bits are unused in the HD404358 and HD404358R Series.

$02F—Data Control Register D3 **DCD3** **D port**

HD404369 Series

Bit	3	2	1	0
	—	—	DCD31	DCD30
Initial value	—	—	0	0
Read/Write	—	—	W	W

$030—Data Control Register R0 **DCR0** **R0 Port**

HD404344R/HD404394/HD404318/HD404358/HD404358R/HD404339/HD404369 Series

Bit	3	2	1	0
	DCR03	DCR02	DCR01	DCR00
Initial value	0	0	0	0
Read/Write	W	W	W	W

$031—Data Control Register R1 **DCR1** **R1 Port**

HD404344R/HD404394/HD404358/HD404358R/HD404369 Series

Bit	3	2	1	0
	DCR13	DCR12	DCR11	DCR10
Initial value	0	0	0	0
Read/Write	W	W	W	W

$032—Data Control Register R2 **DCR2** **R2 Port**

HD404344R/HD404394/HD404358/HD404358R/HD404369 Series

Bit	3	2	1	0
	DCR23	DCR22	DCR21	DCR20
Initial value	0	0	0	0
Read/Write	W	W	W	W

$033—Data Control Register R3 **DCR3** **R3 Port**

HD404344R/HD404394/HD404318/HD404358/HD404358R/HD404339/HD404369 Series

Bit	3	2	1	0
	DCR33	DCR32	DCR31	DCR30*
Initial value	0	0	0	0
Read/Write	W	W	W	W

Note: * Applies to the HD404344R, HD404318, HD404358, HD404358R, HD404339, and HD404369 Series. The DCR30 bit is unused in the HD404394 Series.

$034—Data Control Register R4 **DCR4** **R4 port**

HD404318/HD404358/HD404358R/HD404339/HD404369 Series

Bit	3	2	1	0
	DCR43	DCR42	DCR41	DCR40
Initial value	0	0	0	0
Read/Write	W	W	W	W

$035—Data Control Register R5 **DCR5** **R5 port**

HD404339/HD404369 Series

Bit	3	2	1	0
	DCR53	DCR52	DCR51	DCR50
Initial value	0	0	0	0
Read/Write	W	W	W	W

$036—Data Control Register R6 **DCR6** **R6 port**

HD404339/HD404369 Series

Bit	3	2	1	0
	DCR63	DCR62	DCR61	DCR60
Initial value	0	0	0	0
Read/Write	W	W	W	W

$037—Data Control Register R7 **DCR7** **R7 port**

HD404339/HD404369 Series

Bit	3	2	1	0
	—	DCR72	DCR71	DCR70
Initial value	—	0	0	0
Read/Write	—	W	W	W

$038—Data Control Register R8 **DCR8** **R8 port**

HD404358/HD404358R/HD404369 Series

Bit	3	2	1	0
	DCR83	DCR82	DCR81	DCR80
Initial value	0	0	0	0
Read/Write	W	W	W	W

$039—Data Control Register R9 **DCR9** **R9 port**

HD404369 Series

Bit	3	2	1	0
	DCR93	DCR92	DCR91	DCR90
Initial value	0	0	0	0
Read/Write	W	W	W	W

Appendix C Option Lists

C.1 HD404344R Series Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number (Hitachi entry)	

1 ROM Size

☐ HD404341R: 1-kword	Ceramic oscillator
☐ HD404342R: 2-kword	External clock
☐ HD404344R: 4-kword	
☐ HD40C4341R: 1-kword	Resister oscillator
☐ HD40C4342R: 2-kword	
☐ HD40C4344R: 4-kword	

2 ROM Code Data Type

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU…).
☐ The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMs.

3 System Oscillator (OSC_1 and OSC_2)

	HD404341R/HD404342R/ HD404344R	HD40C4341R/HD40C4342R/ HD40C4344R
☐ Ceramic oscillator	f = MHz	
☐ External clock	f = MHz	
☐ Resistor oscillator		

The shaded portion ▒ indicates unavailable selections.

4 Stop Mode

☐ Used
☐ Not used

5 Package

☐ DP-28S
☐ FP-28DA
☐ FP-30D

C.2 HD404394 Series Option List

Please check off the appropriate applications and enter the necessary information .

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number (Hitachi entry)	

1 ROM Size

☐ HD404391: 1-kword
☐ HD404392: 2-kword
☐ HD404394: 4-kword

2 ROM Code Data Type

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU…).
☐ The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMs.

3 System Oscillator (OSC_1 and OSC_2)

☐ Ceramic oscillator	f =	MHz
☐ External clock	f =	MHz

4 Stop Mode

☐ Used
☐ Not used

5 Package

☐ DP-28S
☐ FP-28DA
☐ FP-30D

C.3 HD404318 Series Option List

Please check off the appropriate applications and enter the necessary information .

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number (Hitachi entry)	

1 ROM Size

☐ HD404314: 4-kword
☐ HD404316: 6-kword
☐ HD404318: 8-kword

2 I/O Option

Pin	I/O	I/O Option	
		D	E
$D_0/\overline{INT}_0$	I/O		
$D_1/\overline{INT}_1$	I/O		
D_2/EVNB	I/O		
D_3/BUZZ	I/O		
$D_4/\overline{STOPC}$	I/O		
D_5	I/O		
D_6	I/O		
D_7	I/O		
D_8	I/O		

D: Without pull-down resistance

E: With pull-down resistance

Pin		I/O	I/O Option	
			D	E
R1	$R1_0$	I/O		
	$R1_1$	I/O		
	$R1_2$	I/O		
	$R1_3$	I/O		
R2	$R2_0$	I/O		
	$R2_1$	I/O		
	$R2_2$	I/O		
	$R2_3$	I/O		
R8	$R8_0$	I/O		
	$R8_1$	I/O		
	$R8_2$	I/O		
	$R8_3$	I/O		
RA	RA_1	I	Selected in option 3	

3 RA_1/V_{disp}

☐ RA_1: Without pull-down resistance (D)
☐ V_{disp}

Note: If even one pin is selected with I/O option E, pin RA_1/V_{disp} must be selected to function as V_{disp}.

Continued on the following page.

Continued from the preceding page.

ROM code name	
LSI number (Hitachi entry)	

4 ROM Code Data Type

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ versions).

☐ The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU…).
☐ The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMs.

5 System Oscillator (OSC_1 and OSC_2)

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

6 Stop Mode

☐ Used
☐ Not used

7 Package

☐ DP-42S
☐ FP-44A

C.4 HD404358 Series Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number (Hitachi entry)	

1 ROM Size

☐ 5 MHz operation: HD404354	4-kword
☐ 8.5 MHz operation: HD40A4354	
☐ 5 MHz operation: HD404356	6-kword
☐ 8.5 MHz operation: HD40A4356	
☐ 5 MHz operation: HD404358	8-kword
☐ 8.5 MHz operation: HD40A4358	

2 ROM Code Data Type

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMs.

3 System Oscillator (OSC_1 and OSC_2)

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

4 Stop Mode

☐ Used
☐ Not used

5 Package

☐ DP-42S
☐ FP-44A

C.5 HD404358R Series Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number (Hitachi entry)	

1 ROM Size

☐ 5 MHz operation: HD404354R	4-kword
☐ 8.5 MHz operation: HD40A4354R	
☐ CR oscillator version: HD40C4354R	
☐ 5 MHz operation: HD404356R	6-kword
☐ 8.5 MHz operation: HD40A4356R	
☐ CR oscillator version: HD40C4356R	
☐ 5 MHz operation: HD404358R	8-kword
☐ 8.5 MHz operation: HD40A4358R	
☐ CR oscillator version: HD40C4358R	

2 ROM Code Data Type

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU…).
☐ The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMs.

3 System Oscillator (OSC_1 and OSC_2)

	HD404354R/6R/8R, HD40A4354R/6R/8R	HD40C4354R/6R/8R
☐ Ceramic oscillator	f = MHz	
☐ Crystal oscillator	f = MHz	
☐ External clock	f = MHz	
☐ Resistor oscillator		

The shaded portion ▒ indicates unavailable selections.

Continued on the following page.

Continued from the preceding page.

ROM code name	
LSI number (Hitachi entry)	

4 Stop Mode

☐ Used
☐ Not used

5 Package

☐ DP-42S
☐ FP-44A

C.6 HD404339 Series Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number (Hitachi entry)	

1 ROM Size

☐ HD404334: 4-kword
☐ HD404336: 6-kword
☐ HD404338: 8-kword
☐ HD4043312: 12-kword
☐ HD404339: 16-kword

2 Optional Function

* ☐ With 32-kHz CPU operation, with time-base for clock
* ☐ Without 32-kHz CPU operation, with time-base for clock
☐ Without 32-kHz CPU operation, without time-base for clock

Note: * Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

Continued on the following page.

Continued from the preceding page.

ROM code name	
LSI number (Hitachi entry)	

3 I/O Option

Pin	I/O	I/O Option	
		D	E
$D_0/\overline{INT}_0$	I/O		
$D_1/\overline{INT}_1$	I/O		
D_2/EVNB	I/O		
D_3/BUZZ	I/O		
$D_4/\overline{STOPC}$	I/O		
D_5	I/O		
D_6	I/O		
D_7	I/O		
D_8	I/O		
D_9	I/O		
D_{10}	I/O		
D_{11}	I/O		
D_{12}	I/O		
D_{13}	I/O		

D: Without pull-down resistance

E: With pull-down resistance

Pin		I/O	I/O Option	
			D	E
R1	$R1_0$	I/O		
	$R1_1$	I/O		
	$R1_2$	I/O		
	$R1_3$	I/O		
R2	$R2_0$	I/O		
	$R2_1$	I/O		
	$R2_2$	I/O		
	$R2_3$	I/O		
R8	$R8_0$	I/O		
	$R8_1$	I/O		
	$R8_2$	I/O		
	$R8_3$	I/O		
R9	$R9_0$	I/O		
	$R9_1$	I/O		
	$R9_2$	I/O		
	$R9_3$	I/O		
RA	RA_1	I	Selected in item 4	

4 RA_1/V_{disp}

☐ RA_1: Without pull-down resistance (D)
☐ V_{disp}

Note: If even one pin is selected with I/O option E, pin RA_1/V_{disp} must be selected to function as Vdisp.

Continued on the following page.

Continued from the preceding page.

ROM code name	
LSI number (Hitachi entry)	

5 ROM Code Data Type

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version)

☐ The upper bits and ower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMs.

6 System Oscillator (OSC_1 and OSC_2)

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

7 Stop Mode

☐ Used
☐ Not used

8 Package

☐ FP-64B
☐ DP-64S

C.7 HD404369 Series Option List

Please check off the appropriate applications and enter the necessary information .

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number (Hitachi entry)	

1 ROM Size

☐ 5 MHz operation: HD404364	4-kword
☐ 8.5 MHz operation: HD40A4364	
☐ 5 MHz operation: HD404368	8-kword
☐ 8.5 MHz operation: HD40A4368	
☐ 5 MHz operation: HD4043612	12-kword
☐ 8.5 MHz operation: HD40A43612	
☐ 5 MHz operation: HD404369	16-kword
☐ 8.5 MHz operation: HD40A439	

2 Function Options

* ☐ With 32-kHz CPU operation, with time-base for clock
* ☐ Without 32-kHz CPU operation: with time-base for clock
☐ Without 32-kHz CPU operation: without time-base for clock

Note: * Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

3 ROM Code Data Type

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMs.

4 System Oscillator (OSC_1 and OSC_2)

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

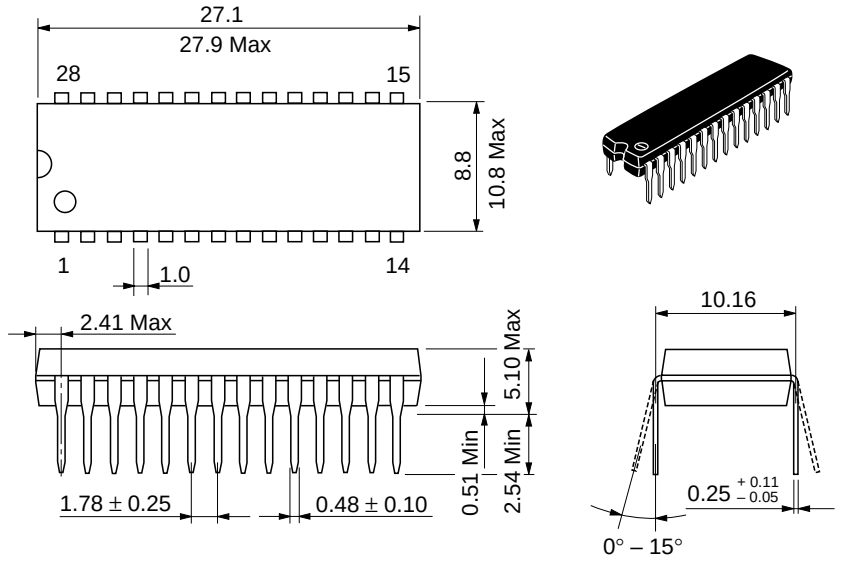
5 Stop Mode

☐ Used
☐ Not used

☐ DP-64S
☐ FP-64B

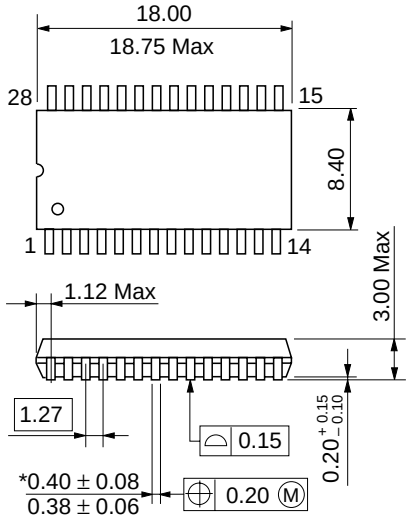
Appendix D Package Dimensions

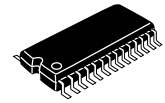
Unit: mm

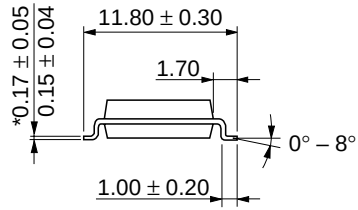


Hitachi Code	DP-28S
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.9 g

Unit: mm



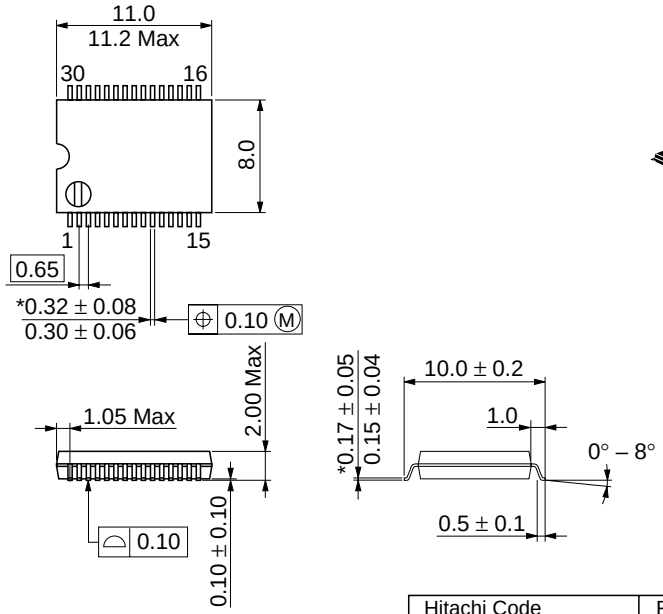




*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-28DA
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.82 g

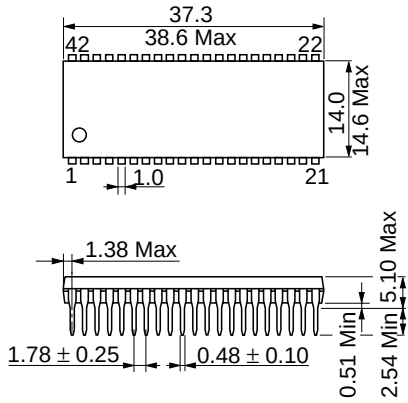
Unit: mm

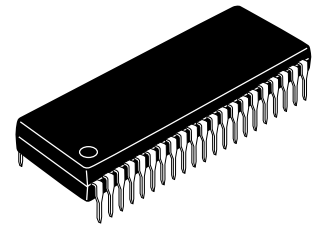


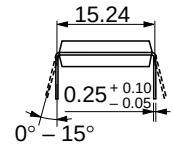
Hitachi Code	FP-30D
JEDEC	—
EIAJ	—
Weight (reference value)	—

*Dimension including the plating thickness
Base material dimension

Unit: mm

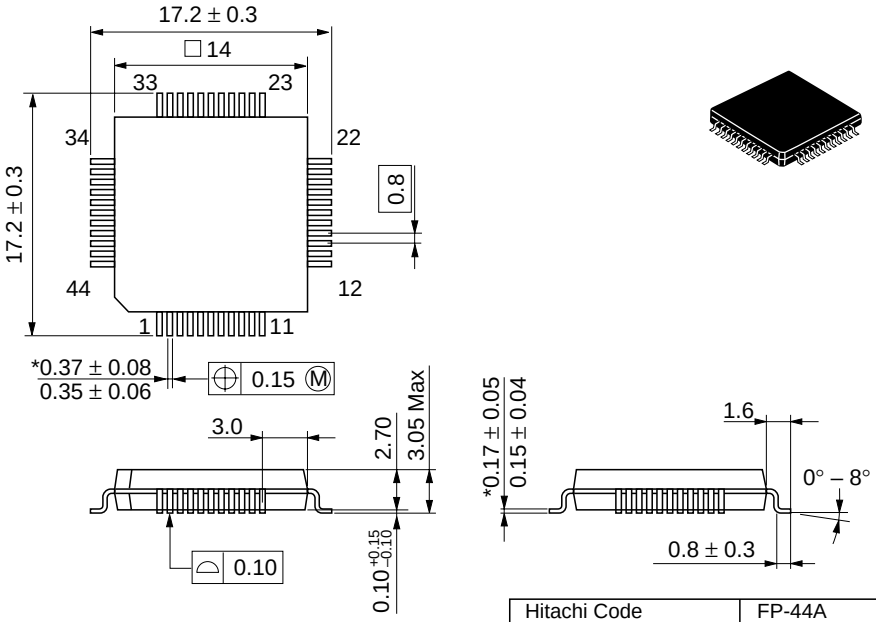






Hitachi Code	DP-42S
JEDEC	—
EIAJ	Conforms
Weight (reference value)	4.8 g

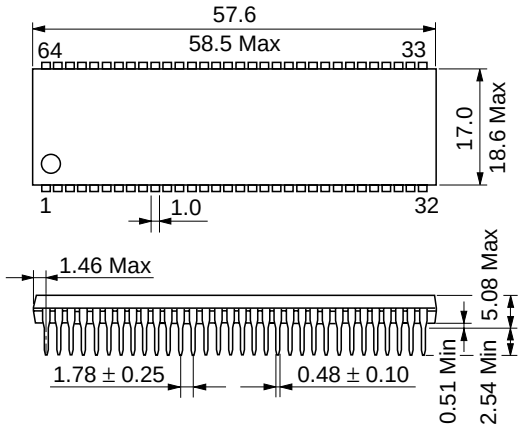
Unit: mm

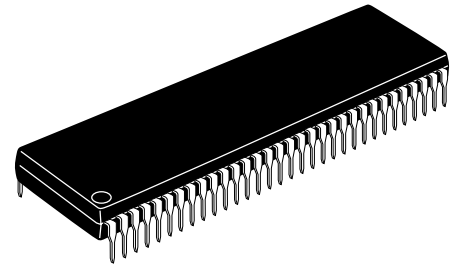


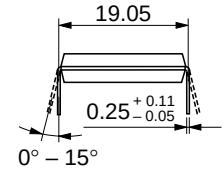
Hitachi Code	FP-44A
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.2 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



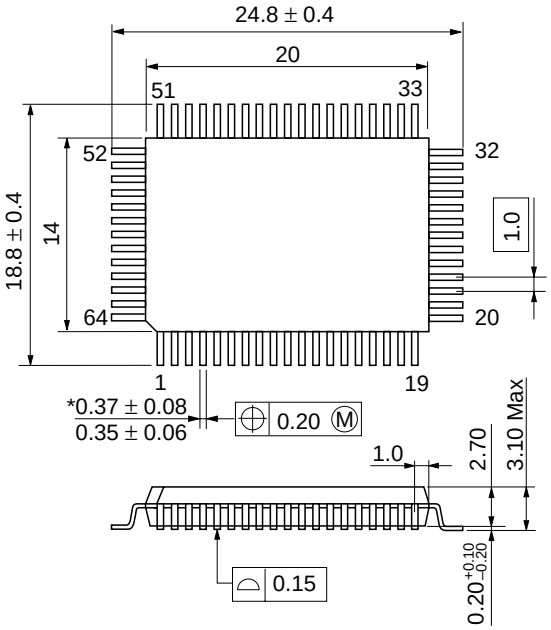


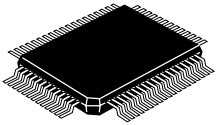


Hitachi Code	DP-64S
JEDEC	—
EIAJ	Conforms
Weight (reference value)	8.8 g

*Dimension including the plating thickness
Base material dimension

Unit: mm





Hitachi Code	FP-64B
JEDEC	—
EIAJ	—
Weight (reference value)	1.7 g

*Dimension including the plating thickness
Base material dimension

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