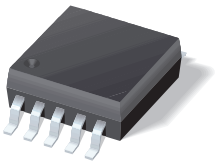


SLVS391B − OCTOBER 2001 − REVISED FEBRUARY 2002

HIGH EFFICIENCY, 250-mA STEP-DOWN CHARGE PUMP

FEATURES

- Regulated 3.3-V, 1.8-V, 1.5-V, or Adjustable Output Voltage
- Up to 250-mA Output Current
- 1.8-V to 6.5-V Input Voltage
- Up to 90% Efficiency
- Output Voltage Tolerance 3% Over Line, Load, and Temperature Variation
- Device Quiescent Current Less Than 40 μA
- Output Voltage Supervisor Included (Power Good)
- Internal Soft Start
- Load Isolated From Battery During Shutdown
- Overtemperature and Overcurrent Protected
- Micro-Small 10-Pin MSOP Package
- EVM Available, TPS60500EVM-193

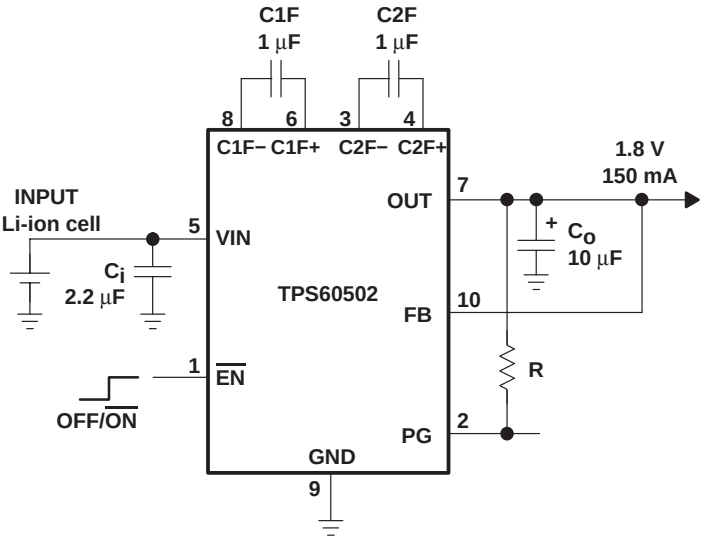
APPLICATIONS

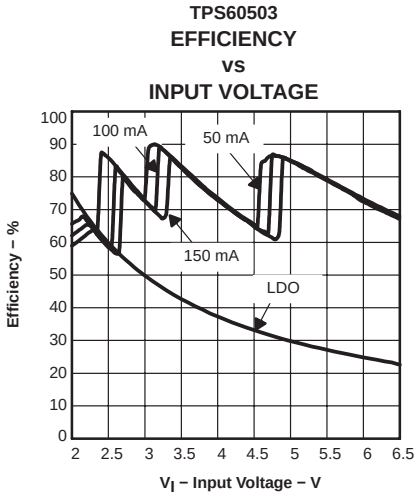
- Personal Digital Assistants
- DSP Core Supply
- Cellular Phones
- Portable Instruments
- Internet Audio Player
- PC Peripherals
- USB Powered Applications

DESCRIPTION

The TPS6050x devices are a family of step-down charge pumps that generate a regulated, fixed 3.3-V, 1.8-V, 1.5-V, or adjustable output voltage. Only four small ceramic capacitors are required to build a complete high efficiency dc/dc charge pump converter. To achieve the high efficiency over a wide input voltage range, the charge pump automatically selects between three different conversion modes. The output can deliver a maximum of 250-mA output current. The power good function supervises the output voltage and goes high when the output voltage rises to 97% of its nominal value.

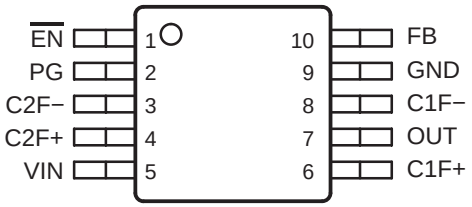
Typical Application Circuit





pin assignments

DGS PACKAGES
(TOP VIEW)



ACTUAL SIZE
3,05 mm x 4,98 mm

AVAILABLE OPTIONS

PART NUMBER†	MARKING DGS PACKAGE	OUTPUT VOLTAGE [V]	MINIMUM INPUT VOLTAGE FOR I_O = 150 mA
TPS60500DGS	AVB	Adjustable (0.8 V to 3.3 V)	$V_I > V_O + 1$
TPS60501DGS	AVC	3.3	$V_I > 4.3$ V
TPS60502DGS	AVD	1.8	$V_I > 2.8$ V
TPS60503DGS	AVE	1.5	$V_I > 2.5$ V

† The DGS package is available taped and reeled. Add R suffix to device type (e.g. TPS60500DGSR) to order quantities of 2500 devices per reel.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
C1F+	6		Positive terminal of the flying capacitor C1F
C1F−	8		Negative terminal of the flying capacitor C1F
C2F+	4		Positive terminal of the flying capacitor C2F
C2F−	3		Negative terminal of the flying capacitor C2F
$\overline{EN}$	1	I	Device-enable Input. − $\overline{EN}$ = High disables the device. Output and input are isolated in shutdown mode. − $\overline{EN}$ = Low enables the device.
GND	9		Ground
FB	10	O	TPS60500: connect via voltage divider to V_O TPS60501 to TPS60503: connect directly to V_O
OUT	7	O	Regulated 3.3 V, 1.8 V, 1.5 V, or adjustable power output Bypass OUT to GND with the output filter capacitor C_o.
PG	2	O	Open drain power good detector output. As soon as the voltage on OUT reaches about 97% of its nominal value this pin goes high.
VIN	5	I	Supply Input. Connect to an input supply in the 1.8-V to 6.5-V range.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage range at VIN, $\overline{EN}$, PG to GND (see Note 1) . . . . . −0.3 V to 7 V
Voltage range at OUT, FB to GND . . . . . −0.3 V to 3.6 V
Voltage range at C1F+, C1F−, C2F+, C2F− to GND . . . . . −0.3 V to 7 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Output current at OUT . . . . . 300 mA
Storage temperature range, T_{stg} . . . . . −55°C to 150°C
Maximum junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The voltage at EN, and PG can exceed VIN up to the maximum rated voltage without increasing the leakage current drawn by these mode select inputs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGS	555 mW	5.56 mW/°C	305 mW	221 mW

NOTE: The thermal resistance junction to ambient of the DGS package when soldered on a PCB is $R_{\theta JA} \approx 180°C/W$.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage range at VIN, V_I	1.8		6.5	V
Output current range at OUT, I_O			250	mA
Input capacitor, C_i	2.2			µF
Flying capacitors, C1F, C2F		1		µF
Output capacitor, C_o for $I_O \le 150$ mA	4.7			µF
Output capacitor, C_o for 150 mA < I_O < 250 mA	22			µF
Operating junction temperature, T_J	−40		125	°C

RECOMMENDED CAPACITOR VALUES

$I_{O, max}$ [mA]	C_i [µF]	$C_{(xF)}$ [µF]	C_o [µF]
50	2.2	0.22	4.7
150	4.7	1	10
250	4.7	1	22

electrical characteristics at C_i = 4.7 µF, C1F = C2F = 1 µF, C_o = 10 µF, T_A = −40°C to 85°C, V_I = 5 V, $V_{(EN)}$ = GND (unless otherwise noted)

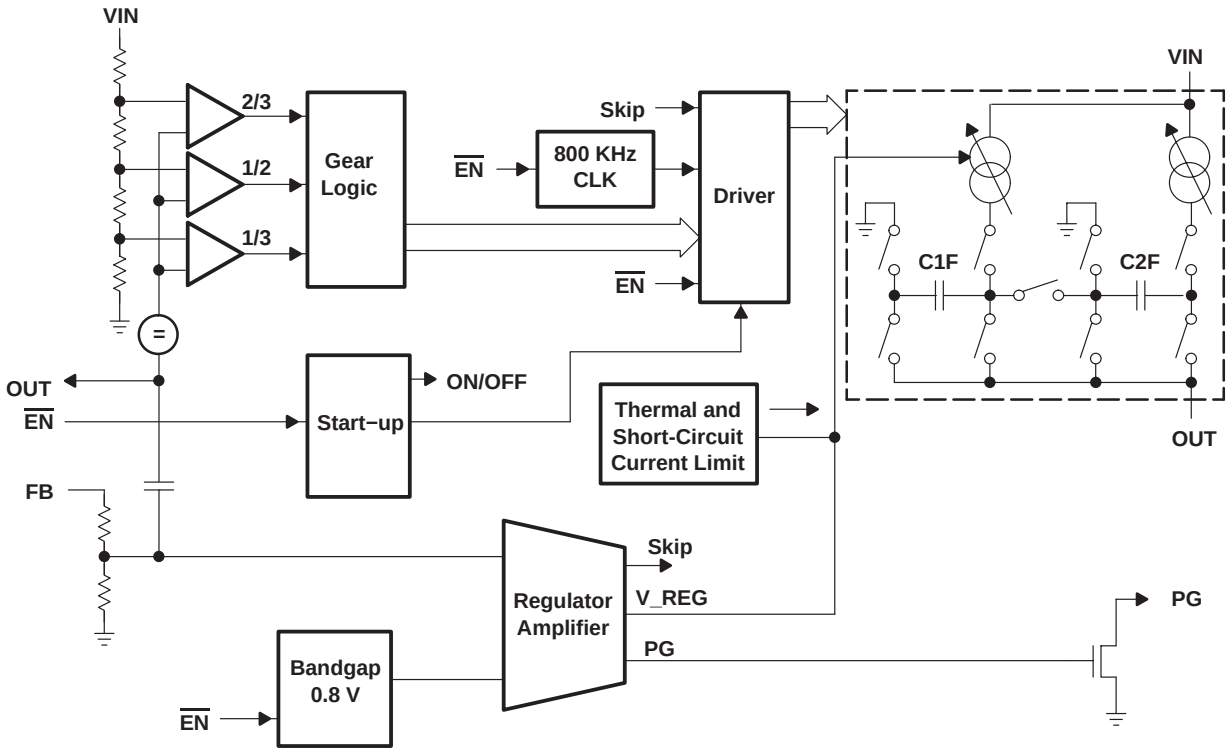
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Supply voltage range			1.8		6.5	V
I_O	Maximum output current		V_I = 1.8 V to 2.7 V, V_I−V_O > 1 V	50			mA
			V_I ≥ 2.7 V, V_I−V_O > 1 V	150			
			V_O = 1.5 V, V_I ≥ 3.1 V	250			
			V_I ≥ 3.7 V, 1.8 V ≤ V_O ≤ 2.5 V	250			
			V_O > 2.5 V, V_I > V_O + 1.2 V	250			
V_O	Output voltage	TPS60500	V_I > 2.7V; V_I−V_O > 1 V at I_{OUT} ≤ 150 mA V_I > 1.8 V; V_I−V_O > 1 V at I_{OUT} ≤ 50mA	0.8		3.3	V
		TPS60501			3.30		
		TPS60502			1.80		
		TPS60503			1.50		
$V_{(FB)}$	Feedback voltage	TPS60500			0.8		V
	Tolerance of output voltage	TPS60501	I_O = 0 mA to 150 mA, C_O = 47 µF	−4%		3%	
		TPS60500	I_O = 0 mA to 150 mA, C_O = 47 µF			3%	
		TPS60502	I_O = 0 mA to 150 mA, C_O = 10 µF			4%	
		TPS60503	I_O = 0 mA to 250 mA, C_O = 47 µF			4%	
V_{pp}	Output voltage ripple at OUT		I_O = 150 mA, V_O = 1.5 V		30		mV_{PP}
I_Q	Quiescent current (no-load input current)		I_O = 0 mA		40	75	µA
$T_{(SD)}$	Thermal shutdown temperature				150		°C
$I_{O(SD)}$	Shutdown supply current		$V_{(EN)}$ = V_I		0.05	0.5	µA
$f_{(OSC)}$	Internal switching frequency			600	800	1200	kHz
V_{IL}	$\overline{EN}$ input low voltage					0.3 x V_I	V
V_{IH}	$\overline{EN}$ input high voltage			0.7 x V_I			V
$I_{lkg(SD)}$	$\overline{EN}$ input leakage current		$V_{(EN)}$ = 0 V or V_I		0.01	0.1	µA
$I_{lkg(FB)}$	FB input leakage current	TPS60500				0.1	µA
$R_{(max)}$	Maximum resistance of the external voltage divider	TPS60500	R1 + R2 at FB pin			1	MΩ
	Short circuit current (start-up current)		V_I = 6.5V, V_O = 0 V	100	300		mA
	Output current limit		V_O > 0.6 V		500		mA
	No load start-up time				80		µs

electrical characteristics for power good comparator of devices TPS6050x at T_A = −40°C to 85°C, V_I = 5 V and $V_{(EN)}$ = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PG)}$	Power good trip voltage	See Note 2		V_{ml} – 2%		V
$t_{d,r}$	Power good delay time	V_O ramping positive		100	200	µs
$t_{d,f}$		V_O ramping negative		50	100	µs
V_{OL}	Power good output voltage low	V_O = 0 V, $I_{(PG)}$ = 1 mA			0.3	V
I_{lkg}	Power good leakage current	V_O = 3.3 V, $V_{(PG)}$ = 3.3 V		0.01	0.1	µA

NOTE 2: V_{ml} is the output voltage at the maximum load current. V_{ml} is not a JEDEC symbol.

functional block diagram TPS6050x



TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_I	Minimum input voltage	vs Output current	1−4
	Efficiency	vs Input voltage	5−8
V_O	Output voltage	vs Output current	9−12
	Quiescent current	vs Input voltage	13
	Efficiency	vs Output current	14−17
V_O	Output voltage (ripple)	vs Time	18
	Line transient response		19
	Load transient response		20

TYPICAL CHARACTERISTICS

TPS60503
MINIMUM INPUT VOLTAGE vs OUTPUT CURRENT

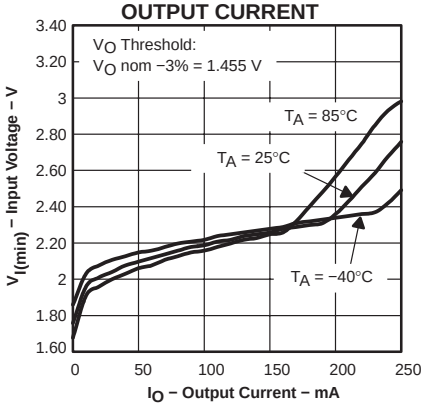


Figure 1

TPS60502
MINIMUM INPUT VOLTAGE vs OUTPUT CURRENT

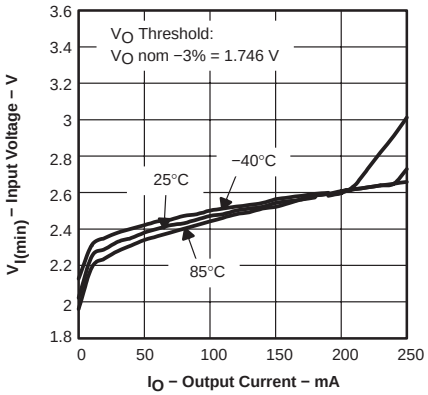


Figure 2

TPS60501
MINIMUM INPUT VOLTAGE vs OUTPUT CURRENT

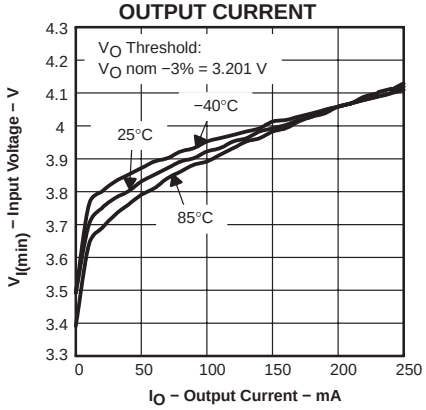


Figure 3

TPS60500
MINIMUM INPUT VOLTAGE vs OUTPUT CURRENT

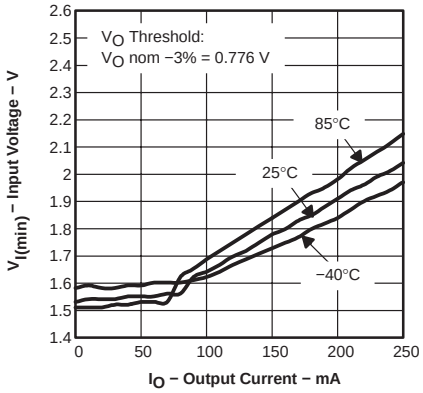


Figure 4

TPS60503
EFFICIENCY vs INPUT VOLTAGE

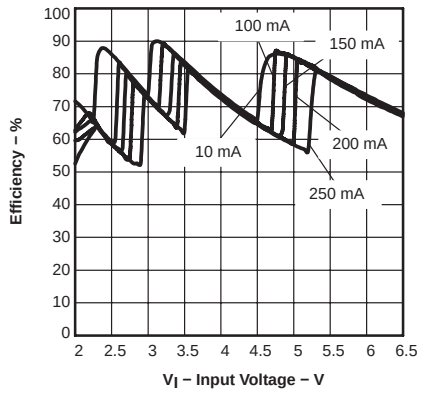


Figure 5

TPS60502
EFFICIENCY vs INPUT VOLTAGE

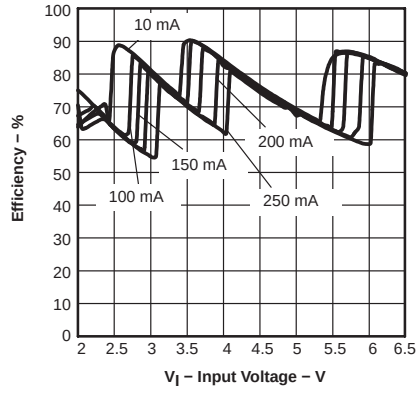


Figure 6

TPS60501
EFFICIENCY vs INPUT VOLTAGE

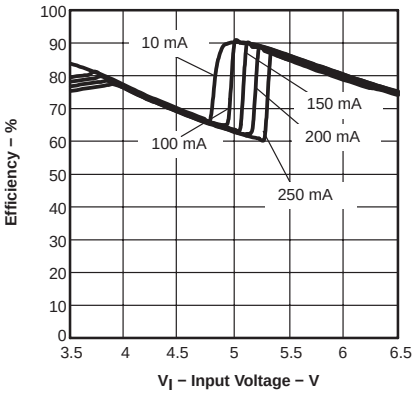


Figure 7

TPS60500
EFFICIENCY vs INPUT VOLTAGE

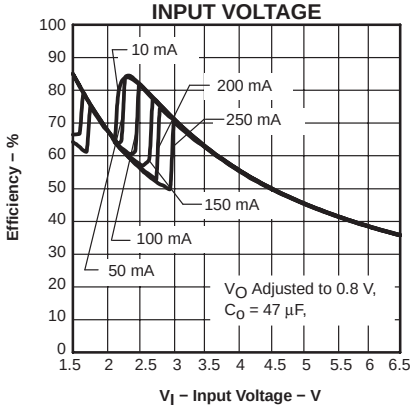


Figure 8

TPS60503
OUTPUT VOLTAGE vs OUTPUT CURRENT

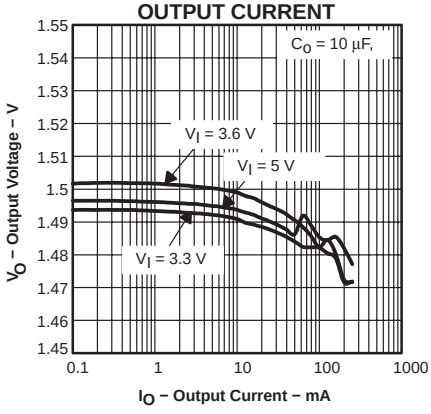


Figure 9

TYPICAL CHARACTERISTICS

TPS60502
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

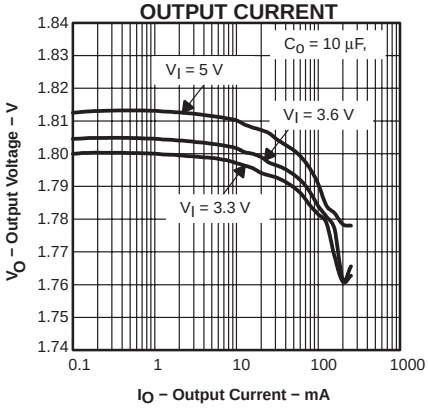


Figure 10

TPS60500
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

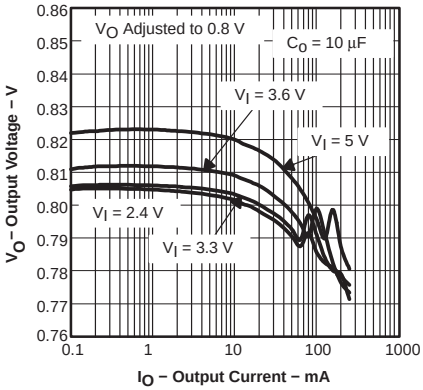


Figure 11

TPS60501
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

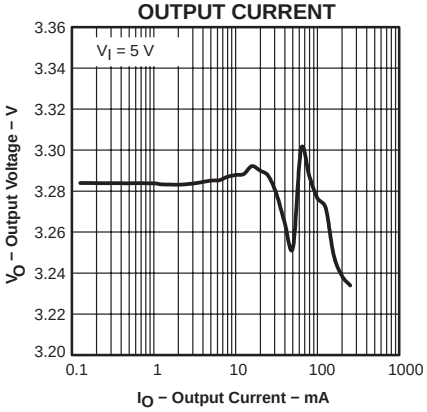


Figure 12

QUIESCENT CURRENT
vs
INPUT VOLTAGE

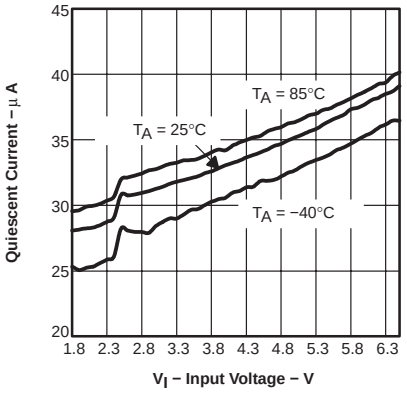


Figure 13

TPS60503
EFFICIENCY
vs
OUTPUT CURRENT

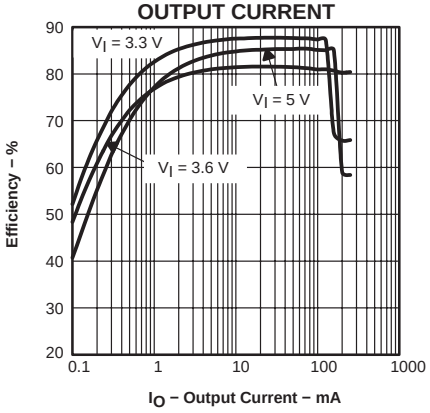


Figure 14

TPS60502
EFFICIENCY
vs
OUTPUT CURRENT

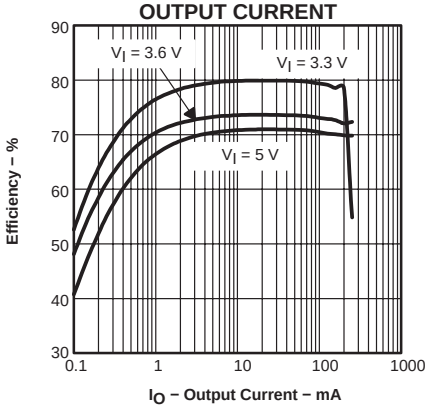


Figure 15

TPS60501
EFFICIENCY
vs
OUTPUT CURRENT

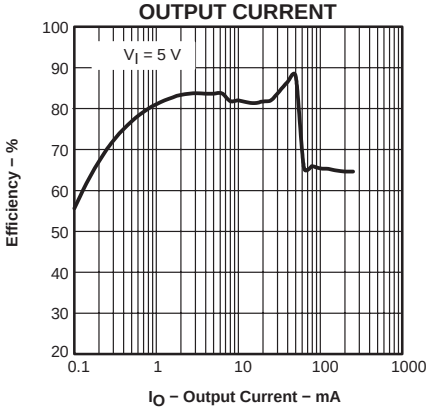


Figure 16

TPS60500
EFFICIENCY
vs
OUTPUT CURRENT

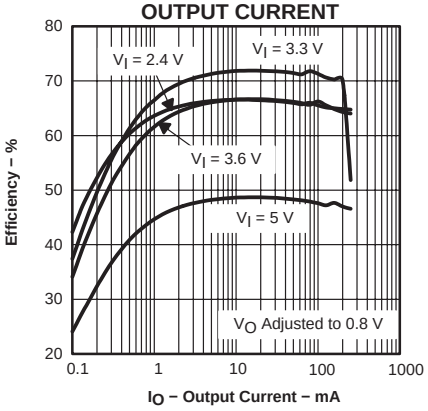


Figure 17

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE (RIPPLE)
vs
TIME

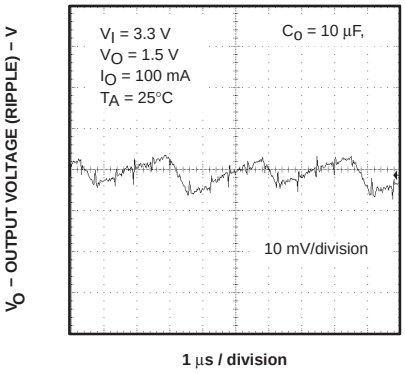


Figure 18

LINE TRANSIENT RESPONSE

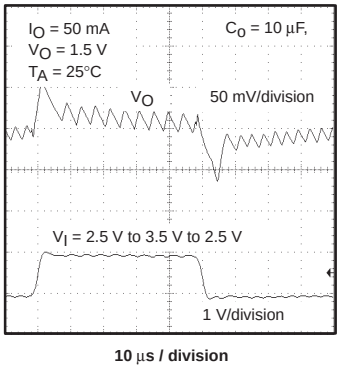


Figure 19

LOAD TRANSIENT RESPONSE

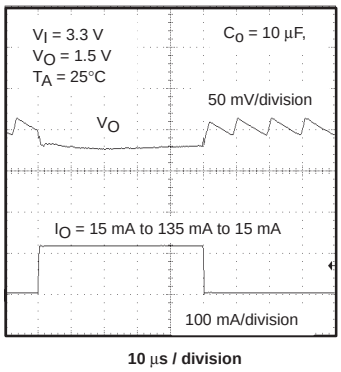


Figure 20

PRINCIPLES OF OPERATION

The TPS6050x charge pumps provide a regulated output voltage in the range of 0.8 V to 3.3 V from an input voltage of 1.8 V to 6.5 V. The devices use switched capacitor fractional conversion to achieve high efficiency over the entire input and output voltage range. Regulation is achieved by sensing the output voltage and enabling the internal switches as needed to maintain the selected output voltage. This skip-mode regulation is used over a load range from 0 mA to 150 mA. At a higher output current, the device works in a linear regulation mode.

The TPS6050x circuits consist of an oscillator, a voltage reference, an internal resistive feedback circuit (fixed voltage version only), an error amplifier, two charge pump stages with MOSFET switches, a shutdown/start-up circuit, and a control circuit.

short-circuit current limit and thermal protection

When the output voltage is lower than 0.6 V, the output current is limited to 300 mA typically. The device also has a thermal protection which reduces the output current when the temperature of the chip exceeds 150°C. The output current declines to 0 mA when the chip temperature rises to 160°C.

enable

Driving $\overline{EN}$ high disables the converter. This disables all internal circuits, reducing input current to only 0.05μA. Leakage current drawn from the output pin OUT is a maximum of 1 μA. The device exits shutdown once $\overline{EN}$ is set low (see start up procedure described below). The typical no-load start-up time is 80 μs. When the device is disabled, the load is isolated from the input, an important feature in battery-operated products because it extends the battery shelf life.

start-up procedure

The device is enabled when $\overline{EN}$ is set from logic high to logic low. The charge pump stages immediately start switching to transfer energy to the output. In start-up until the output voltage has reached 0.6 V, the input current is limited to 300 mA typically.

power good detector

The power good (PG) output is an open-drain output on all TPS6050x devices. The PG output pulls low when the output is out of regulation. When the output rises to within 97% of regulation, the power good output goes high. In shutdown, power good is pulled low. In normal operation, an external pullup resistor is typically used to connect the PG pin to V_O or V_I. If the PG output is not used, it should remain unconnected.

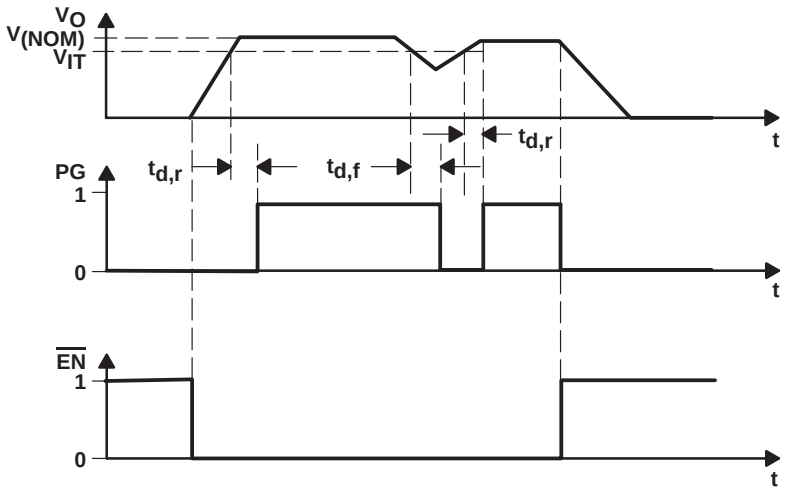


Figure 21. Power Good Timing Diagram

PRINCIPLES OF OPERATION

The TPS6050x devices use fractional conversion to achieve high efficiency over a wide input and output voltage range. Depending on the input to output voltage ratio and output current, internal circuitry switches between an LDO mode, a 2/3x mode, a 0.5x mode, and a 1/3x mode.

LDO conversion mode

In the LDO mode, the flying capacitors are no longer used for transferring energy. The switches 1, 2, 5, and 6 are closed and connect the input directly with the output. This mode is automatically selected if the input to output voltage ratio does not allow the use of another conversion mode with higher efficiency. In LDO mode, the regulation is done by switching off MOSFET 2 and 6 until the output current reaches the *linear-skip* current (150 mA typ). At a higher output current, the output voltage is regulated by controlling the resistance of the switch. The minimum input to output voltage difference required for regulation is 1 V.

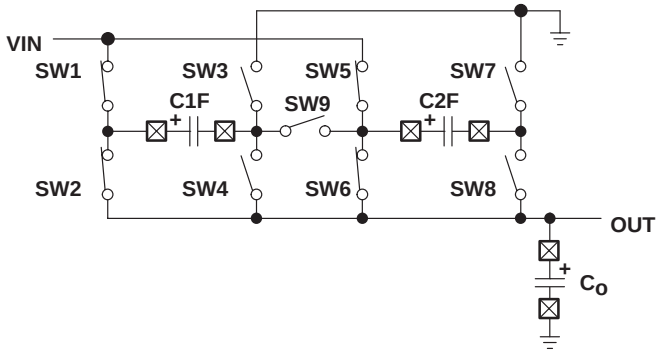


Figure 22. LDO Conversion Mode

2/3x conversion mode

In the first cycle, the two flying capacitors are connected in parallel and are charged up in series with the output capacitor. In the second cycle, the flying capacitors are connected in series. This mode provides higher efficiency than the LDO mode because the current into VIN is only 2/3 of the output current. The mode is automatically selected if the input voltage is higher than 3/2 of the selected output voltage.

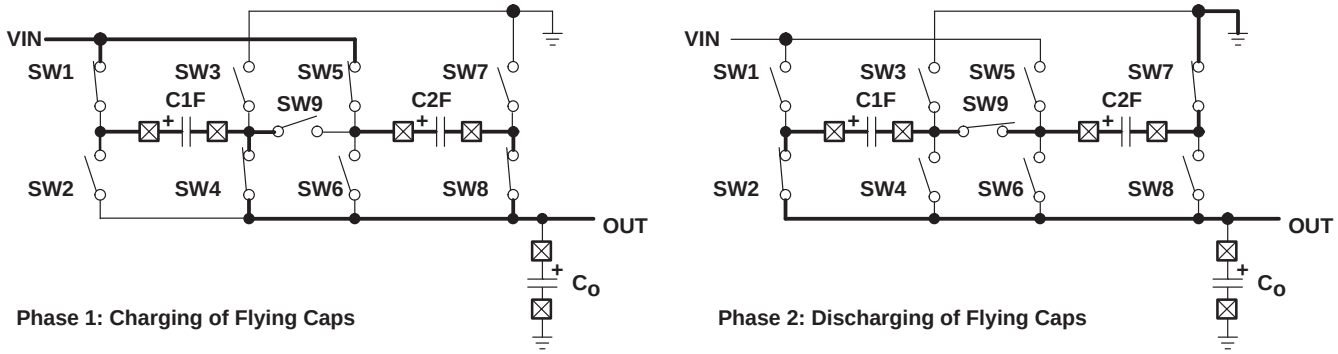


Figure 23. 2/3x Conversion Mode

PRINCIPLES OF OPERATION

0.5x conversion mode

This conversion mode is internally selected if the input to output voltage ratio is greater than two (e.g. 3.6 V to 1.5 V conversion). In the 0.5x mode, the flying capacitors and the switches always work in parallel, which reduces the resistance of the circuit compared to the other modes. In the first cycle, the flying capacitors are charged in series with the output capacitors. In the second cycle, the flying capacitors are connected in parallel with the output capacitor, which discharges the flying capacitors.

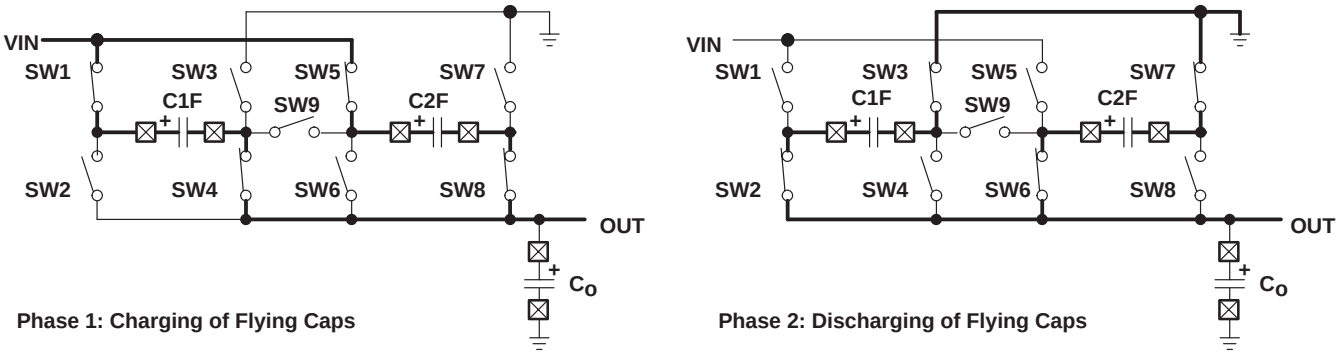


Figure 24. 0.5x Conversion Mode

1/3x conversion mode

This mode was implemented to provide high efficiency even with an input to output voltage ratio greater than three (e.g. 5 V to 1.5 V conversion). In the first cycle, the two flying capacitors are charged in series with the output capacitor. In the next step, the flying capacitors which are charged to VIN/3, are connected in parallel to the output capacitor.

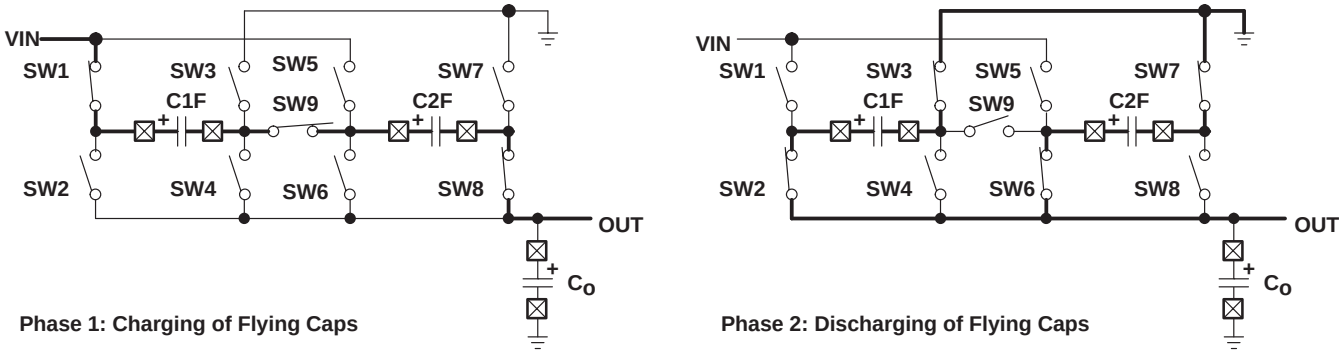


Figure 25. 1/3x Conversion Mode

DESIGN PROCEDURE

capacitor selection

Designed specifically for space-critical battery-powered applications, the complete converter requires only four external capacitors. The capacitor values are closely linked to the required output current, output noise, and ripple requirements. The input capacitor improves system efficiency by reducing the input impedance, and it also stabilizes the input current. The value of the output capacitor, C_O, influences the stability of the voltage regulator. The minimum required capacitance for C_O is 4.7 µF. Depending on the maximum allowed output ripple voltage and load current, larger values can be chosen. For an output current greater than 150 mA, a minimum output capacitor of 22 µF is required. Table 1 shows ceramic capacitor values recommended for low output voltage ripple.

Table 1. Recommended Capacitors

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	LMK212BJ105KG	0805	1 µF	Ceramic
	LMK212BJ225MG	0805	2.2 µF	Ceramic
	EMK316BJ225KL	1206	2.2 µF	Ceramic
	LMK316BJ475KL	1206	4.7 µF	Ceramic
	JMK316BJ106KL	1206	10 µF	Ceramic
TDK	C2012X5R1C105M	0805	1 µF	Ceramic
	C2012X5R1A225M	0805	2.2 µF	Ceramic
	C2012X5R0J106M	0805	10 µF/6.3 V	Ceramic

Table 2 contains a list of manufacturers of ceramic capacitors. Ceramic capacitors provide the lowest output voltage ripple because they typically have the lowest ESR-rating.

Table 2. Recommended Capacitor Manufacturers

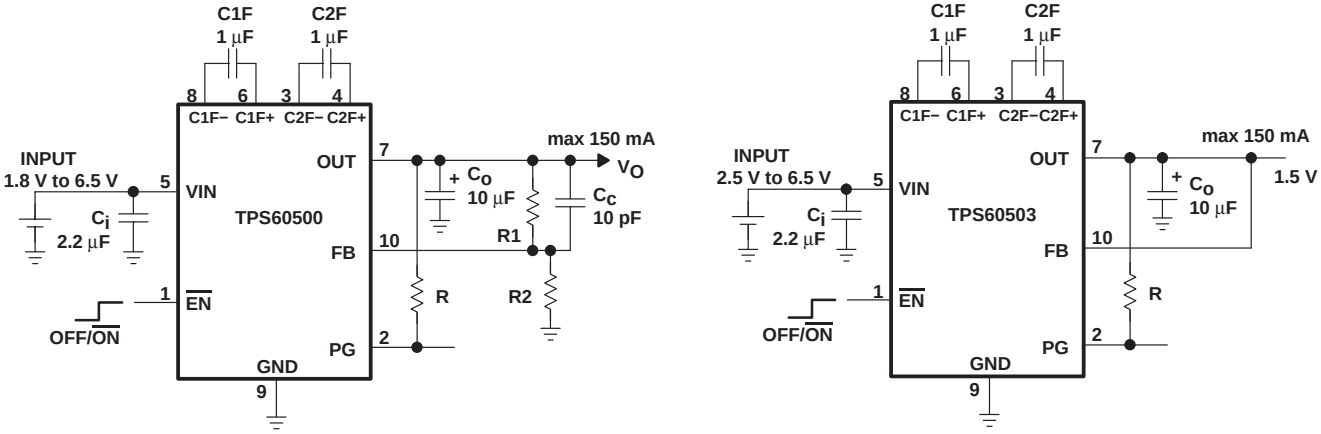
MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t−yuden.com
TDK	X7R/X5R ceramic	www.component.tdk.com
Vishay	X7R/X5R ceramic	www.vishay.com
Kemet	X7R/X5R ceramic	www.kemet.com

APPLICATION INFORMATION

typical application circuit for fixed voltage and adjustable voltage versions

Figure 26 shows the typical operation circuit. The TPS60501 to TPS60503 devices use an internal resistor divider for sensing the output voltage. The FB pin must be connected externally with the output. For maximum output current and best performance, 4 ceramic capacitors are recommended. For lower currents or higher allowed output voltage ripple, other capacitors can also be used. *It is recommended that the output capacitor has a minimum value of 4.7 µF.* This value is necessary to maintain a stable operation of the system. Flying capacitors lower than 1 µF can be used, but this decreases the maximum output power. This means that the device works in linear mode with lower output currents. The device works in the linear mode for an output current of greater than 150 mA. With an output current greater than 150 mA, an output capacitor of ≥22 µF must be used. Figure 26 shows that two 10-µF capacitors can also be used in parallel.

APPLICATION INFORMATION

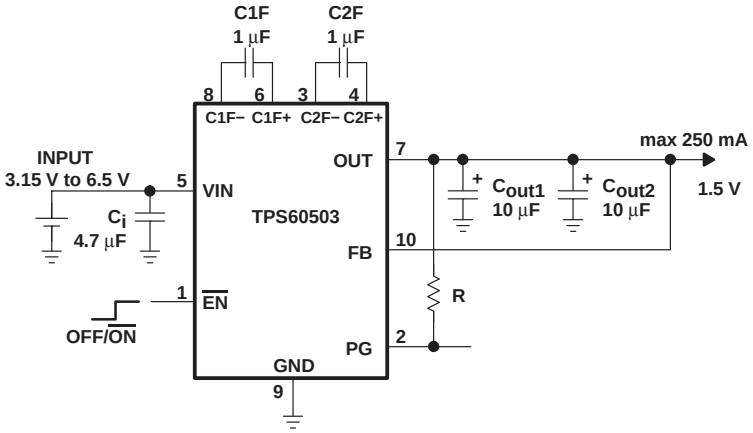


$$R1 = R2\left(\frac{V_O}{V_{FB}}\right) - R2$$

$$V_O = \frac{(R1 + R2)}{R2} \times VFB$$

VFB = 0.8 V

Nominal Output Voltage	Equation	Possible E24 Resistor Combination
1.2 V	R1 = 0.5R2	R1 = 100 kΩ, R2 = 200 kΩ (1.20 V)
1.5 V	R1 = 0.875R2	R1 = 160 kΩ, R2 = 180 kΩ (1.51 V)
1.6 V	R1 = R2	Any
1.8 V	R1 = 1.25R2	R1 = 150 kΩ, R2 = 120 kΩ (1.80 V)
2.5 V	R1 = 2.125R2	R1 = 510 kΩ, R2 = 240 kΩ (2.50 V) R1 = 470 kΩ, R2 = 220 kΩ (2.51 V)



Power supply with 1,4 mm maximum height for 250-mA output current

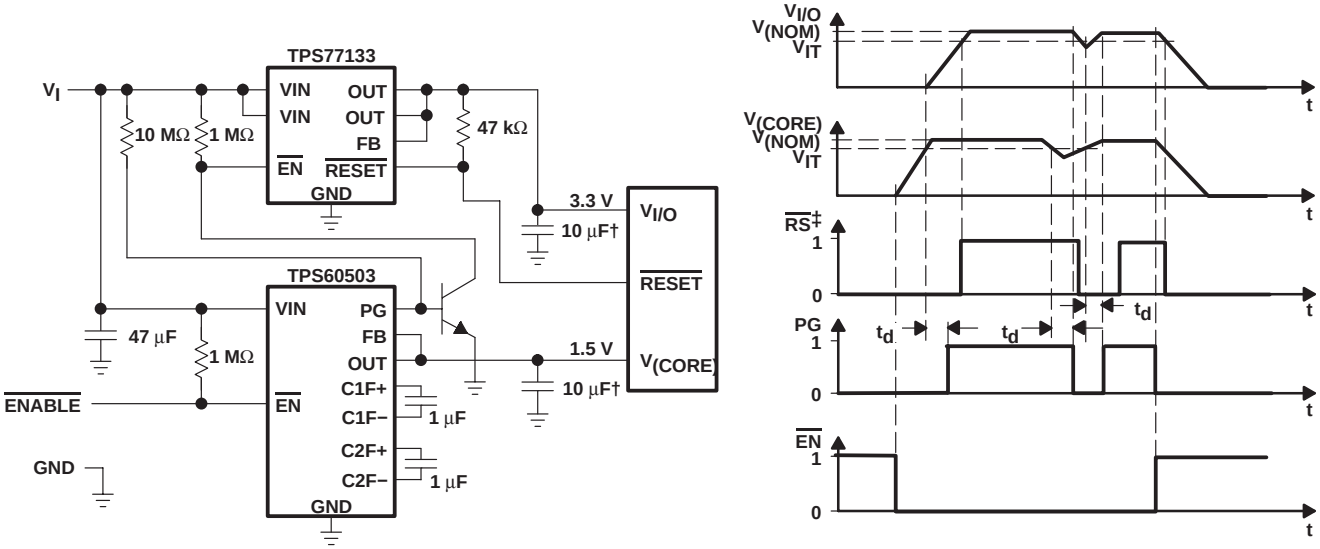
Figure 26. Typical Operating Circuit

APPLICATION INFORMATION

DSP supply with sequencing

This application shows a power supply for a typical DSP. DSPs usually have core voltages in the 1-V to 2.5-V range, whereas the voltage at the I/O-pins (I/O voltage) is typically 3.3 V to interface with external logic and converters. Therefore, a power supply with two output voltages is required. The application works with an input voltage in the range of 3.5 V to 6.5 V. The maximum output current is 150 mA on each output.

The supply is enabled by pulling the enable pin ($\overline{EN}$ of the TPS60503) to GND. The step-down charge pump starts and its power good (PG) output goes high. This enables the LDO which powers the I/O lines and generates a reset signal for the DSP. Figure 27 shows the timing diagram of the start-up/shutdown procedure.



† Recommended value for stability, DSP may require higher capacitance.
‡ $\overline{RS}$ is the $\overline{RESET}$ output of the TPS77133.

Figure 27. DSP Supply With Sequencing

APPLICATION INFORMATION

LC-post filter

If the output voltage ripple of the stepdown charge pump is to high, an LC post filter can be used.

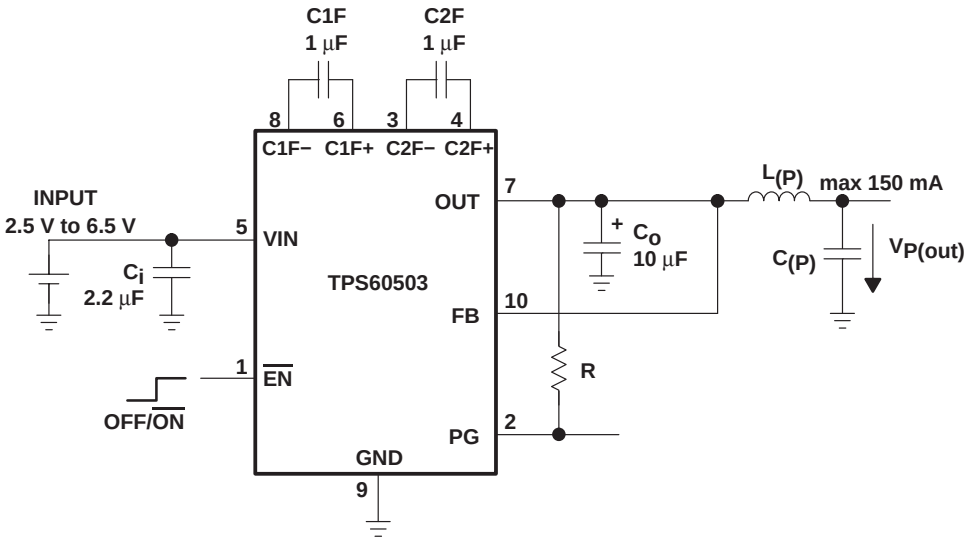


Figure 28. LC-Post Filter

Table 3. Measurement Results on Different $C_{(fly)}$, $C_{(P)}$, $L_{(P)}$ Combinations; BW = 500 MHz

V_I [V]	I_O [mA]	C_I [µF]	$C_{(XF)}$ [µF]	C_O [µF]	$L_{(P)}$ [µH]	$C_{(P)}$ [µF]	V_O [V]	TYPICAL $V_{P(Out)}$ V_{PP}[mV]	TYPICAL $V_{O(RMS)}$ [mV]
		CERAMIC	CERAMIC	CERAMIC		CERAMIC			
5	50	2.2	0.22	4.7	—	0.1 (X7R)	3.3	50	8
5	50	2.2	0.22	4.7	—	0.1 (X7R)	1.5	30	9
5	150	4.7	1	10	—	0.1 (X7R)	1.5	50	6
5	250	4.7	1	2 x 10	—	0.1 (X7R)	1.5	45	8
5	100	4.7	1	10	0.1	0.1 (X7R)	1.5	20	4

power supply with dynamic voltage scaling

Dynamic voltage scaling of the core can be used to reduce power consumption of a digital signal processor (DSP). During the periods, in which the maximum DSP performance is not required, the core voltage can be reduced when the DSP operates at a lower clock-rate. This idea is called runtime power control (RPC) and is supported by modern DSPs. RPC extends battery-life time in handheld applications, like MP3 players, digital cameras, PDA.

The supply of DSPs is separated into I/O interface and core supply. Interface is mostly powered by a 3.3-V system supply, whereas core supply achieves voltages far below 1.5 V. The TPS60500 is powered by the 3.3-V system supply. The DSP itself selects the applied core voltage.

The core voltage is switched between 1.5 V and 1.1 V by changing the feedback resistor network. A MOSFET modifies the voltage divider at the feedback (FB) pin by switching a resistor. In this application, a general purpose MOSFET BSS138 is used with a $V_{GS(th)}$ of 1.6 V. A DSP 3.3-V I/O port drives the gate. The feedback resistor network consists of R2, R3 and R4. $C_{(ff)}$ is the fast forward capacitor for improved line regulation.

APPLICATION INFORMATION

power supply with dynamic voltage scaling (continued)

General requirements for the application:

- Output voltage1 (DSP core): 1.5 V ±0.08 V
- Output voltage 2 (DSP core): 1.1 V +0.1 V –0.05 V
- Input voltage: 3 V to 3.3 V
- Output current: 150 mA (10R load)

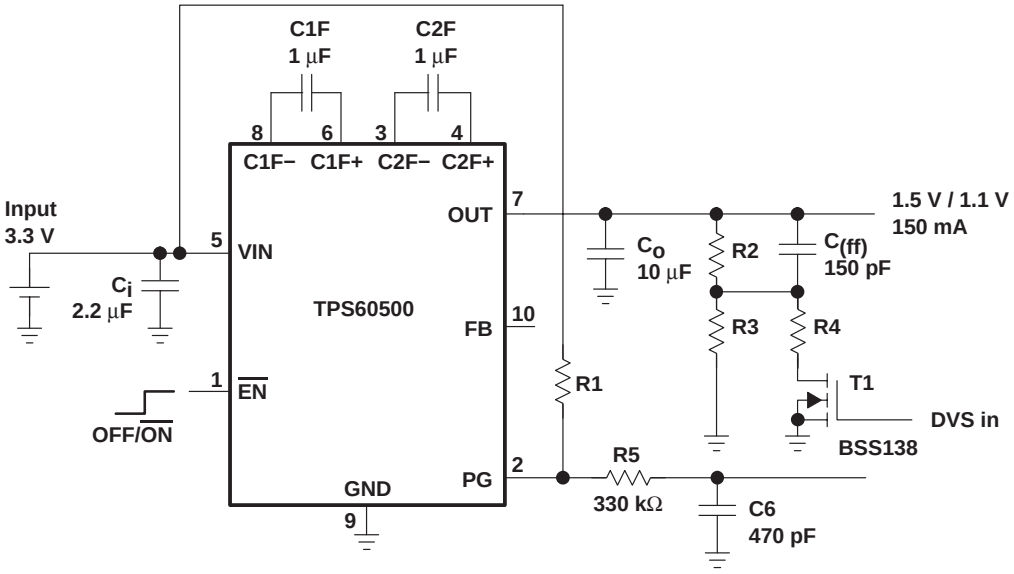


Figure 29. Dynamic Voltage Scaling Application

To keep current through the adjustment resistor network as low as possible, the resistors are calculated to:

V_{out1} adjusted by R2 and R3 (1)

$$R3 = \frac{V_{FB}}{\frac{V_{out1} - V_{FB}}{R2}}$$

V_{out1} = 1.1 V,
R2 = 180 kΩ,
V_{ref} = 0.80 V,
→R3 = 470 kΩ

V_{out2} adjusted by R2 and Rx = R3||R4 (2)

$$Rx = \frac{V_{FB} \times R2}{\left(V_{out2} - V_{FB}\right)}$$

V_{out2} = 1.5 V,
→Rx = 206 kΩ

$$\frac{1}{Rx} = \frac{1}{R3} + \frac{1}{R4} \qquad \rightarrow R4 = \frac{1}{\frac{1}{Rx} - \frac{1}{R3}}$$

→R4 = 360 kΩ (3)

APPLICATION INFORMATION

internet audio power supply

The input voltage from a single or dual NiCd, NiMH or alkaline cell is boosted to 3.3 V. This voltage is used as system supply for the application and as an input voltage for the step-down charge pump which is used to provide the core voltage for a DSP.

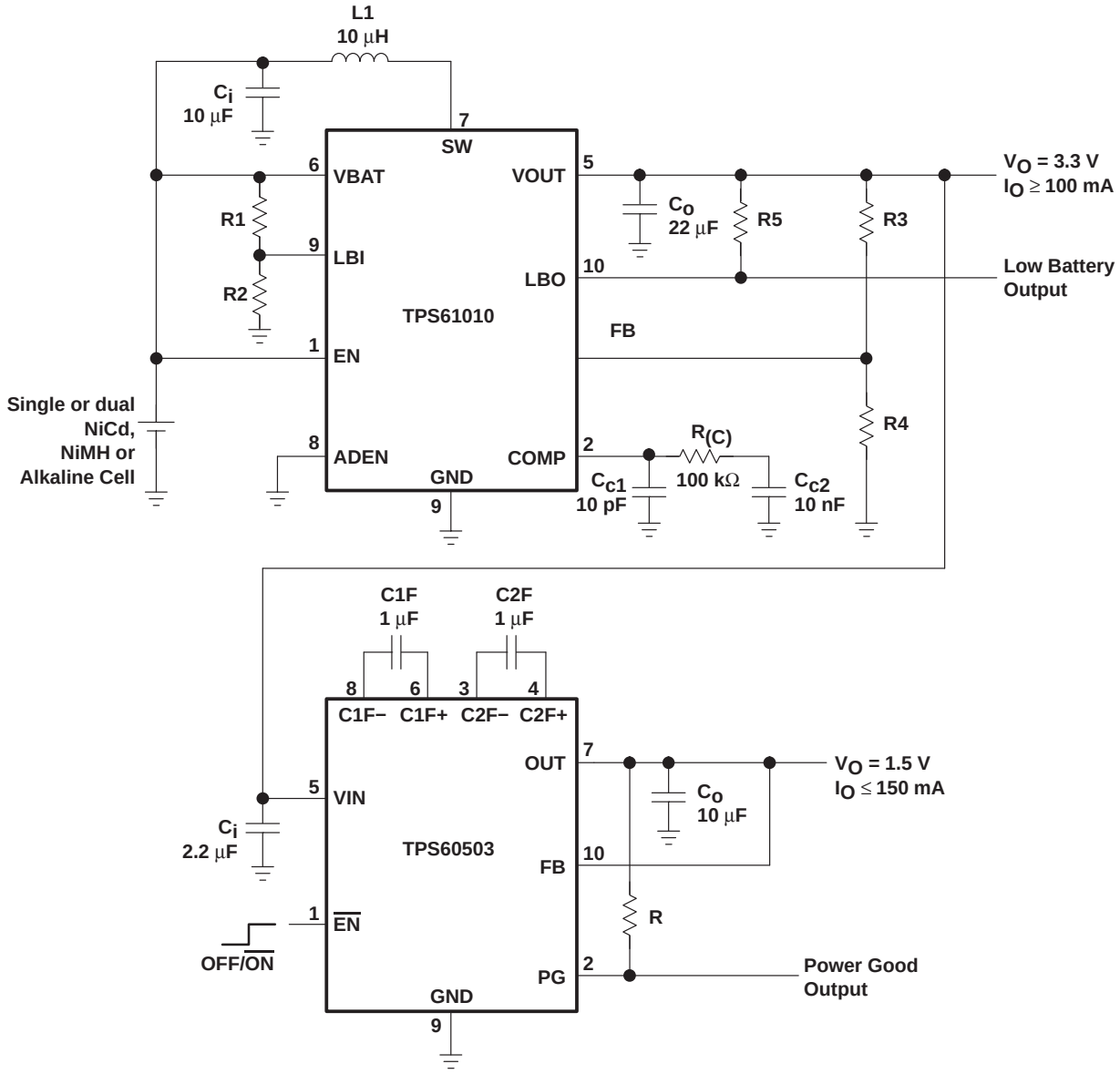


Figure 30. Internet Audio Power Supply

APPLICATION INFORMATION

layout and board space

All capacitors should be soldered as close as possible to the IC. A PCB layout proposal for a two-layer board is shown in Figure 31. Care has been taken to connect all capacitors as close as possible to the circuit to achieve optimized output voltage ripple performance.

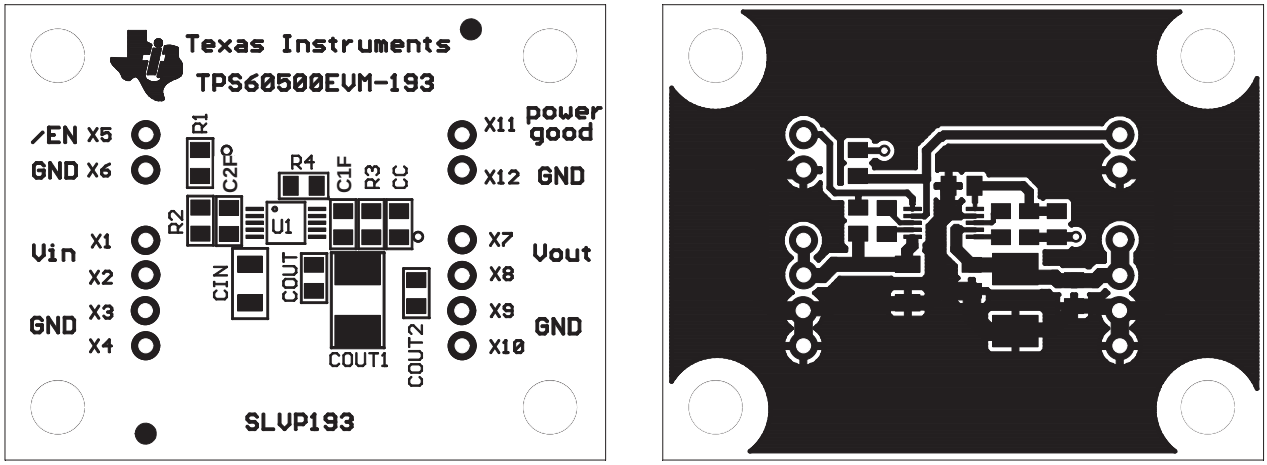


Figure 31. Recommended PCB Layout for TPS6050x (top layer)

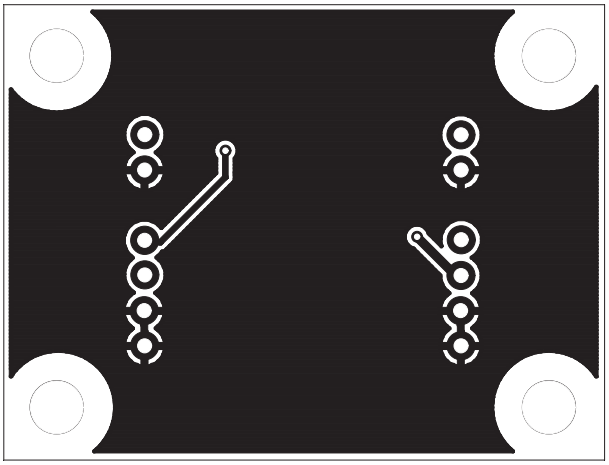


Figure 32. Recommended PCB Layout for TPS6050x (bottom layer)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60500DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AVB	Samples
TPS60500DGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVB	Samples
TPS60500DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AVB	Samples
TPS60500DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVB	Samples
TPS60501DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC	Samples
TPS60501DGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC	Samples
TPS60501DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC	Samples
TPS60501DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC	Samples
TPS60502DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVD	Samples
TPS60502DGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVD	Samples
TPS60502DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVD	Samples
TPS60502DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVD	Samples
TPS60503DGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVE	Samples
TPS60503DGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

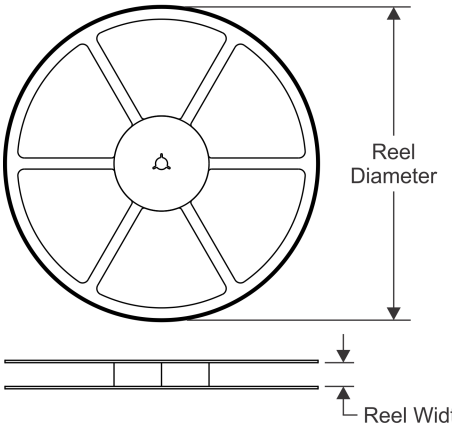
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

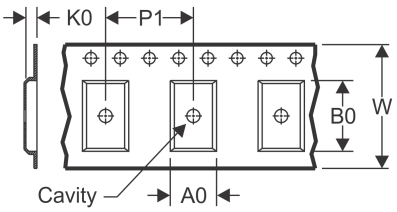
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

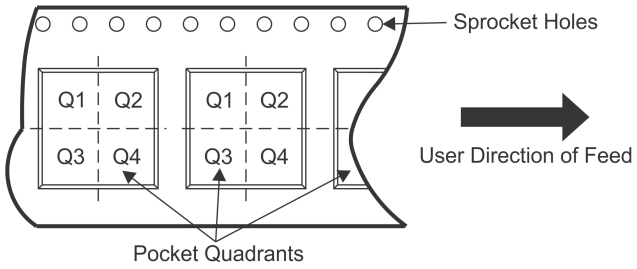


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

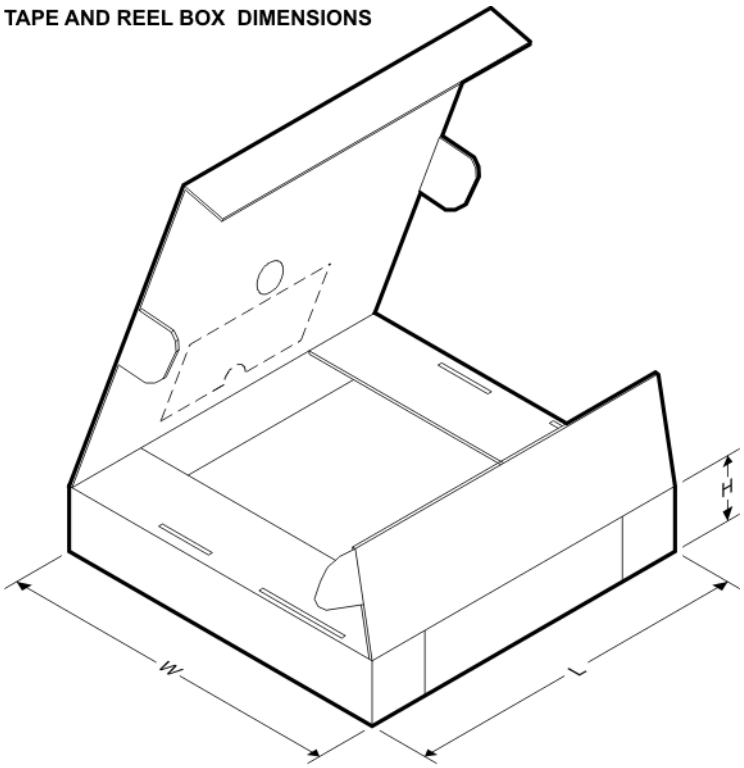
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60500DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60501DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60502DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

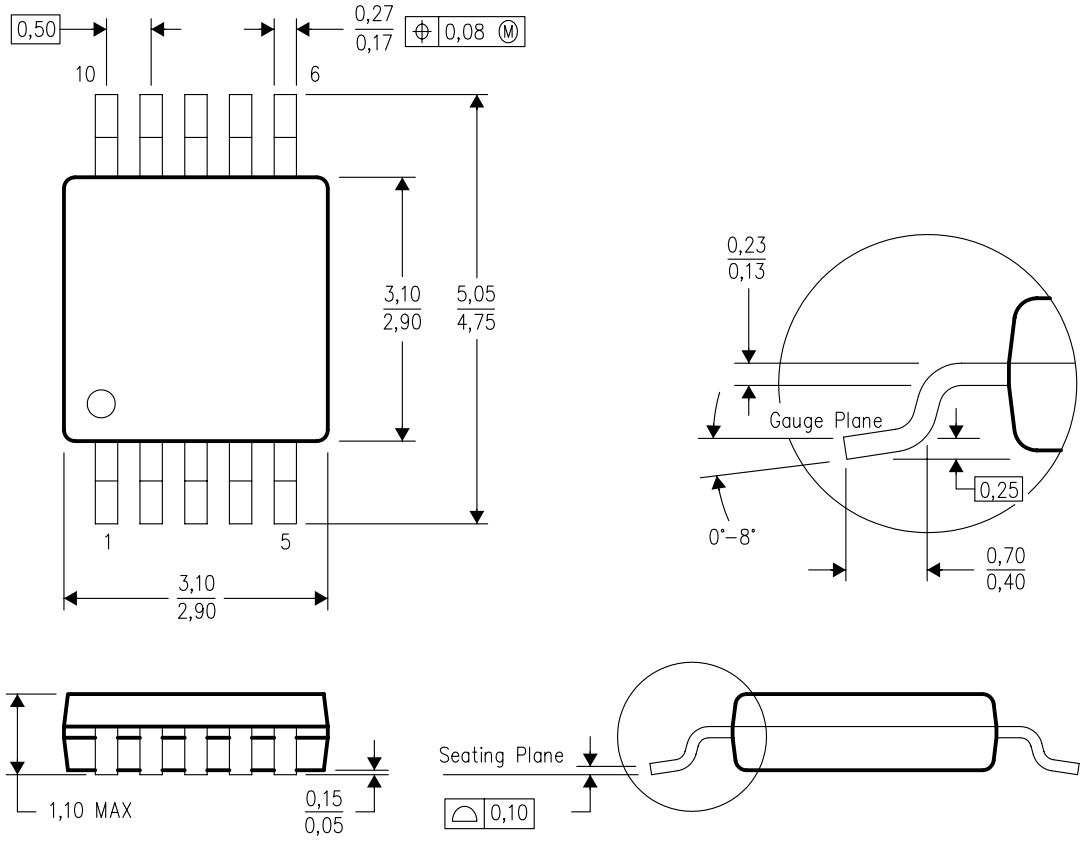
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60500DGSR	VSSOP	DGS	10	2500	340.5	338.1	20.6
TPS60501DGSR	VSSOP	DGS	10	2500	340.5	338.1	20.6
TPS60502DGSR	VSSOP	DGS	10	2500	340.5	338.1	20.6

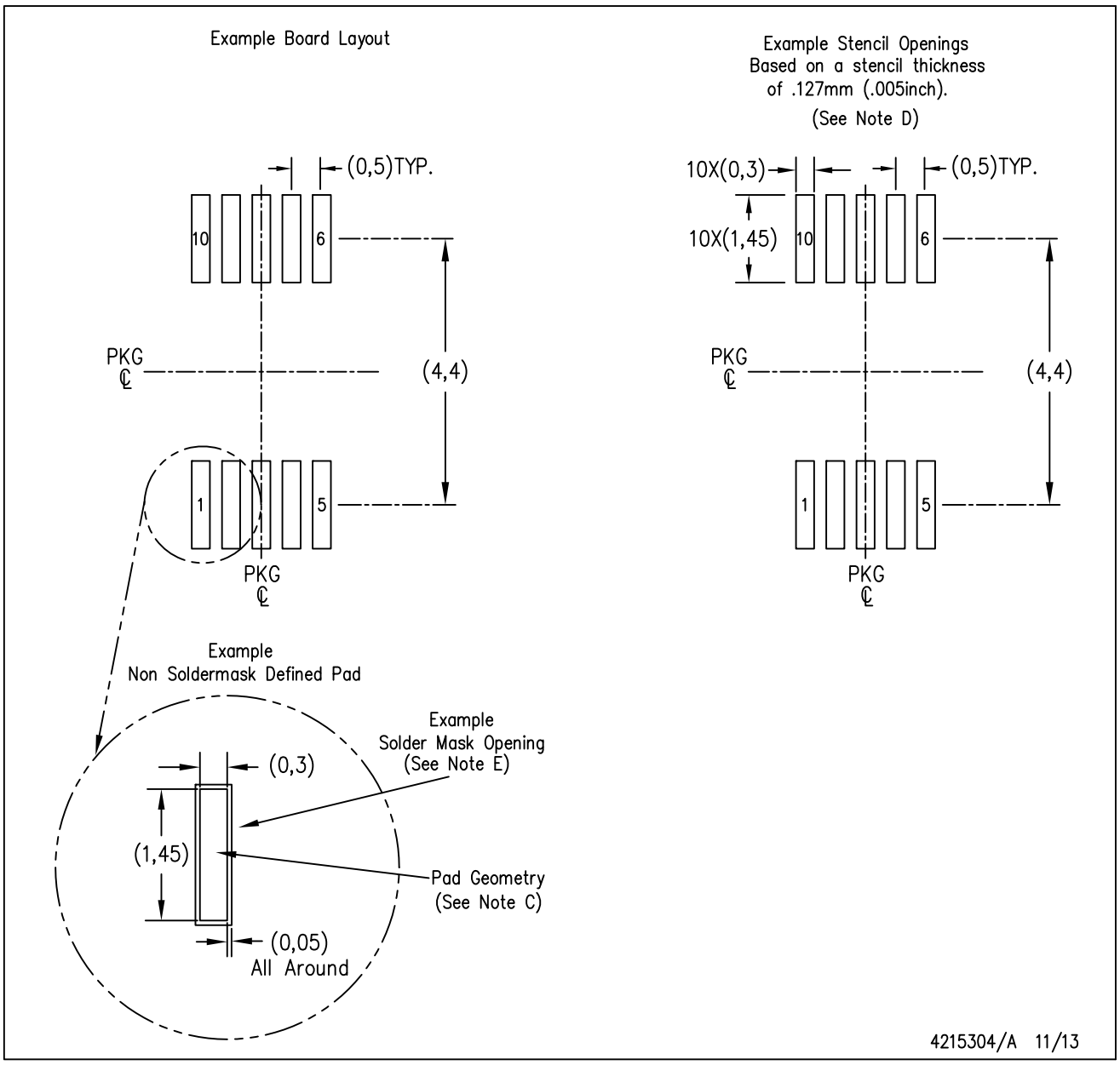
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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