

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

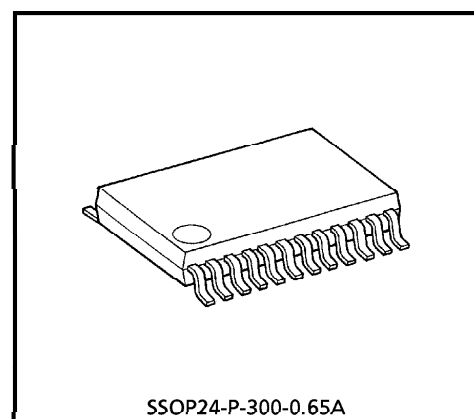
TA1243CFN

RF MODULATOR FOR VCR

The TA1243CFN is a PLL RF modulator for the UHF frequency range. The multi system can easily make the lineup development.

FEATURES

- Phase locked loop frequency synthesizer for RF carrier and sound subcarrier
- Programmable of no adjustment sound subcarriers (4.5MHz, 5.5MHz, 6.0MHz, 6.5MHz)
- Possible to use for L-SECAM
- Programmable picture to sound ratio
- Bus controlled Test pattern Signal Generator
- Bus controlled one logic output port
- Bus controlled power save mode
- Controlled by I²C bus
- The ripple rejection of power supply voltage is improved from TA1243BF.

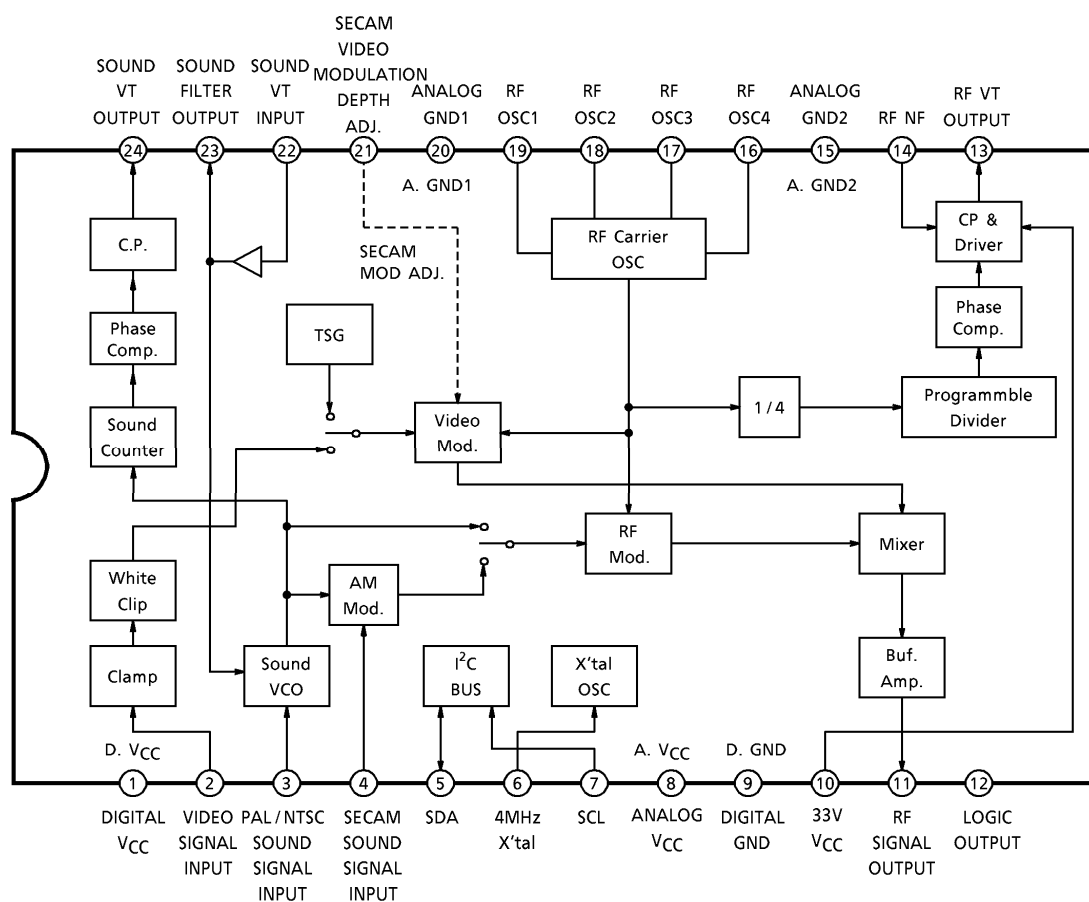


SSOP24-P-300-0.65A
Weight : 0.14g (Typ.)

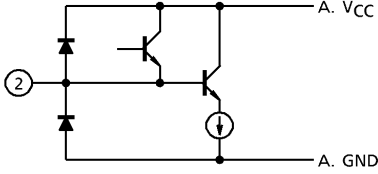
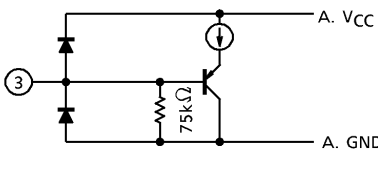
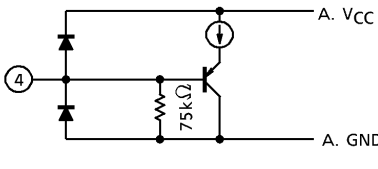
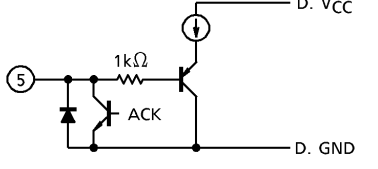
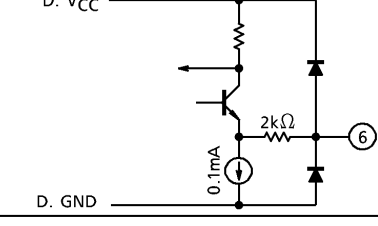
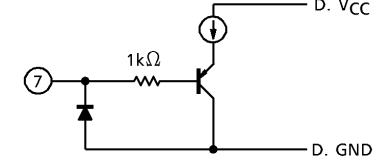
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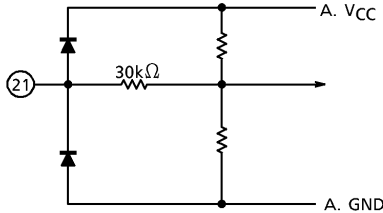
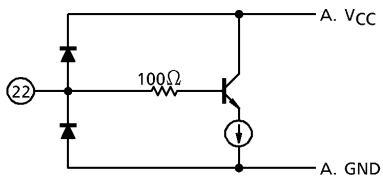
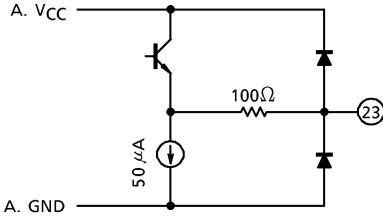
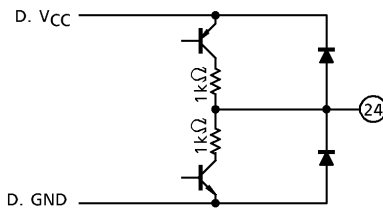
BLOCK DIAGRAM



TERMINAL CHARACTERISTICS ($V_{CC1} = 5.0V$, $V_{CC2} = 33V$, $T_a = 25^\circ C$)

PIN No.	FUNCTION	TYP. DC VOLTAGE	TYP. AC VOLTAGE	INTERFACE	NOTE
1	Digital V_{CC}	(5.0V)	—	—	—
2	Video Signal Input	2.4V (Sync TIP)	0.5V _{p-p}		Sync TIP clamp input
3	PAL / NTSC Sound Signal Input	0V	200mV _{p-p}		
4	SECAM Sound Signal Input	0V	200mV _{p-p}		
5	SDA	OPEN BASE	5V _{p-p}		I ² C BUS serial data
6	4MHz X'tal	2.7V	—		
7	SCL	OPEN BASE	5V _{p-p}		I ² C BUS serial clock

PIN No.	FUNCTION	TYP. DC VOLTAGE	TYP. AC VOLTAGE	INTERFACE	NOTE
8	Analog V _{CC}	(5.0V)	—	—	Analog power supply
9	Digital GND	(0V)	—	—	Digital ground
10	V _{CC33}	33V	—	—	Tuning voltage power supply
11	RF Signal Output	3.8V	80dB μ V (Picture)		
12	Logic Output	H : 4.3V L : 0V	—		BUS control I _{Max} = 10mA
13	RF V _T Output	—	—		Tuning voltage output
14	RF NF	—	—		
15	Analog GND2	(0V)	—	—	Analog ground
16	RF OSC4	3.4V	—		
17	RF OSC3	3.4V			
18	RF OSC2	3.4V			
19	RF OSC1	3.4V			

PIN No.	FUNCTION	TYP. DC VOLTAGE	TYP. AC VOLTAGE	INTERFACE	NOTE
20	Analog GND1	(0V)	—	—	Analog ground
21	SECAM Video Modulation depth Adj.	3.1V	—		Possible to adjustment by the outside resistance. Resistance is inserted between VCC and 21 pin : Modulation depth decreases Resistance is inserted between GND and 21 pin : Modulation depth increases
22	Sound VT Input	—	—		
23	Sound Filter Output	—	—		
24	Sound VT Output	—	—		

I²C-BUS DATA FORMAT

		MSB							LSB	ACK
Address Byte	ADR	1	1	0	0	1	0	1	0	ACK
Control Byte1	C1	1	(*)	(*)	(*)	PS2	PS1	PS0	LE	ACK
Control Byte2	C2	WO	PSA	LO	FA1	FA0	(*)	(*)	(*)	ACK
Prog. Data Byte1	PD1	0	TSG	N10	N9	N8	N7	N6	N5	ACK
Prog. Data Byte2	PD2	N4	N3	N2	N1	0	1	0	0	ACK

(*) Don't care

Bus data transmission : ADR + C1 + C2 + PD1 + PD2 or
 ADR + PD1 + PD2 + C1 + C2 or
 ADR + C1 + C2 or
 ADR + PD1 + PD2

1. PS2~PS0 : Picture to sound ratio setting (Video signal input : Stair case (B/W) 0.5V_{p-p}
 Sound signal input : 1kHz sin wave 0.2V_{p-p})

PS RATIO (SYSTEM L)	PS RATIO (OTHER THAN SYSTEM L)	PS2	PS1	PS0
- 6dB	- 10dB	0	0	0
- 7dB	- 11dB	0	0	1
- 8dB	- 12dB	0	1	0
- 9dB	- 13dB	0	1	1
- 10dB	- 14dB	1	0	0
- 11dB	- 15dB	1	0	1
- 12dB	- 16dB	1	1	0
- 13dB	- 17dB	1	1	1

2. LE : System L enable

1 ... This mode is SYSTEM L. Positive modulation for video and AM modulation for sound inter carrier at 6.5MHz.

In this case, FA1 and FA2 don't care.

0 ... Modes other than SYSTEM L. Negative modulation for video and FM modulation for sound inter carrier at 4.5MHz, 5.5MHz, 6.0MHz, 6.5MHz.

The system is selected by FA1 and FA2.

3. WO : Control of white clip

1 ... White clip off. The system L is used, and the characteristic of 100% modulations can be evaluated.

0 ... White clip on.

4. PSA : Control of power save

- 1 ... Power save off. (normal operation)
 0 ... Power save on. Becomes waiting for the bus data.
 And power supplies other than the bus decoder are turned off.

The data of the decoder is maintained while V_{CC} is added.

When V_{CC} is turned off, power on reset changes the data of the decoder by turning on V_{CC} again.

5. LO : Control of logic out

- 1 ... 12 pin become high voltage.
 0 ... 12 pin become low voltage.

6. FA1~FA0 : Sound Inter Carrier Frequencies setting

FA1	FA0	SOUND INTER CARRIER FREQUENCY	FREQUENCY DEVIATION
0	0	4.5MHz	$\pm 25\text{kHz}$
0	1	5.5MHz	$\pm 50\text{kHz}$
1	0	6.0MHz	$\pm 50\text{kHz}$
1	1	6.5MHz	$\pm 50\text{kHz}$

7. TPSG : Control of test pattern signal generator

- 1 ... ON
 0 ... OFF (normal operation)

8. N10~N1 : Programmable Divider Data setting

The frequency of VCO is calculated by the next expression.

$$f_{VCO} = 31.25\text{kHz} \times 32 \times N + 250\text{kHz}$$

$$N = 512 \times N_{10} + 256 \times N_9 + 128 \times N_8 + 64 \times N_7 + 32 \times N_6 + 16 \times N_5 + 8 \times N_4 + 4 \times N_3 + 2 \times N_2 + N_1$$

The frequency step is 1MHz, and 250kHz is given in the IC.

The divider data N is made frequency -250kHz of the set channel.

POWER ON RESET MODE

Power on reset functions when the power supply is turned on.

The decoder data is the data of power on reset until the bus data is received.

In this mode, because the power saving is turned on, the RF signal is not output.

- VCO Frequency Setting : 591.25MHz (CCIR 36ch)
- Television System : System G (Sound carrier frequency : 5.5MHz,
FM deviation : $\pm 50\text{kHz}$,
Video modulation polarity : negative modulation)
- P/S Ratio Set Up : -13dB
- White Clip : ON
- Power Save : ON
- Logic Output : LOW
- TPSG : OFF

		MSB							LSB	ACK
Address Byte	ADR	1	1	0	0	1	0	1	0	ACK
Control Byte1	C1	1	(*)	(*)	(*)	0	1	1	0	ACK
Control Byte2	C2	0	0	0	0	1	(*)	(*)	(*)	ACK
Prog. Data Byte1	PD1	0	0	1	0	0	1	0	0	ACK
Prog. Data Byte2	PD2	1	1	1	1	0	1	0	0	ACK

(*) Don't care

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage 5V System	V _{CC1}	8	V
Supply Voltage 33V System	V _{CC2}	35	V
Power Dissipation (Note)	P _D	850	mW
Input Terminal Voltage	V _{IN}	GND – 0.3~V _{CC} + 0.3	V
Operating Temperature	T _{opr}	– 20~75	°C
Storage Temperature	T _{stg}	– 55~150	°C

(Note) Derated linearly above Ta = 25°C in the proportion of 6.8mW/°C.

Please note the product design of the board because the calorific value is large.

- The copper area is widened.
- Hole for heat radiation of shield case.
- Other enough consideration.

RECOMMENDED OPERATING CONDITION

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage 5V System	V _{CC1}	4.5	5	5.5	V
Supply Voltage 33V System	V _{CC2}	27	33	35	V

ELECTRICAL CHARACTERISTICS ($V_{CC1} = 5.0V$, $V_{CC2} = 33V$, $T_a = 25^\circ C$, $f_p = 591.25MHz$)

	No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT	NOTE
Whole	1-1	Supply Current 1 (A. V_{CC} + D. V_{CC})	I_{CC1}	—	45	62	80	mA	Power supply of 5V part
	1-2	Supply Current 2 (A. V_{CC} + D. V_{CC})	I_{CC2}	—	4	6	8	mA	5V power supply of power save
	1-3	Supply Current 3 (V_{CC} 33V)	I_{CC3}	—	2.0	2.5	3.5	mA	Power supply of 33V part
	1-4	Operating Frequency Range	f_{op}	—	471.25	—	855.25	MHz	f_p frequency
Video Part	2-1-1	Video RF Output Level (Negative Modulation)	$V_{on}(fp)$	—	77	80	83	$dB_{\mu V}$	50 Ω Termination STAIR CASE (B / W) signal : 0.5V _{p-p} input
	2-1-2	Video RF Output Level (Positive Modulation)	$V_{op}(fp)$						
	2-2-1	Video modulation Depth (Negative Modulation)	mpn	—	75	79	83	%	WHITE signal : 0.5V _{p-p} input
	2-2-2	Video modulation Depth (Positive Modulation)	mpp	—	84	88	92		
	2-3-1	White Clipping Level (Negative Modulation)	$mpn(MAX)$	—	90	94	98	%	WHITE signal : 1.0V _{p-p} input
	2-3-2	White Clipping Level (Positive Modulation)	$mpp(MAX)$	—	210	240	—		DG / DP : 5% / 5%, WHITE CLIP : OFF
	2-4-1	Differential Gain (Negative Modulation)	DGn	—	—	± 3	± 5	%	STAIR CASE : 0.5V _{p-p} (chrominance signal 20IRE)
	2-4-2	Differential Gain (Positive Modulation)	DGp						

	No.	CHARACTERISTIC	SYMBOL	TEST CIRCUIT	MIN.	TYP.	MAX.	UNIT	NOTE
Video Part	2-5-1	Differential Phase (Negative Modulation)	DPn	—	—	± 3	± 5	°	STAIR CASE : 0.5V _{p-p} (Chrominance signal 20IRE)
	2-5-2	Differential Phase (Positive Modulation)	DPp						
	2-6-1	Video S / N Ratio (Negative Modulation)	mpn (S / N)	—	51	53	—	dB	0.1~5MHz, Unweighting, WHITE 50% signal input
	2-6-2	Video S / N Ratio (Positive Modulation)	mpp (S / N)						
	2-7-1	Video Frequency Response (Negative Modulation)	f _{pn}	—	—	± 1	± 2	dB	0.1~5MHz 1MHz Reference
	2-7-2	Video Frequency Response (Positive Modulation)	f _{pp}						
	2-8	Average Picture Level Drift	mp (APL)	—	—	± 0.5	± 3.0	%	APL 10-90%, 50% Reference
	2-9	Sync Crush Level	Δ sync	—	—	1	3	%	{1 - (V _{sync} / V _{white}) × (100 / 40)}
	2-10-1	Chroma Beat (Negative Modulation)	V _{cn}	—	—	-75	-70	dB	4.43MHz sin wave : 0.5V _{p-p} input, Video carrier level reference, P / S = -13dB
	2-10-2	Chroma Beat (Positive Modulation)	V _{cp}	—	—	-65	-60		
	2-11-1	RF Carrier 2'nd Harmonic Level	V _{2fp}	—	—	-28	-20	dB	Reference = Video carrier level
	2-11-2	RF Carrier 3'rd Harmonic Level	V _{3fp}	—	—	-22	-12		
	2-12	Video Signal 2nd Harmonic Level	V _{pH}	—	—	-55	-50	dB	1MHz sin wave : 0.5V _{p-p} input, f _p + 1MHz Reference, f _p + 2MHz measurement
	2-13-1	Prescaller Spurious (f _p × 1 / 2)	V _{PR1 / 2}	—	—	0	10	dB _{μV}	—
	2-13-2	Prescaller Spurious (f _p × 3 / 2)	V _{PR3 / 2}	—	—	10	20		
	2-14-1	Video Carrier Frequency Accuracy	Δ f _p	—	—	—	± 100	kHz	X'tal series capacitor : 7pF

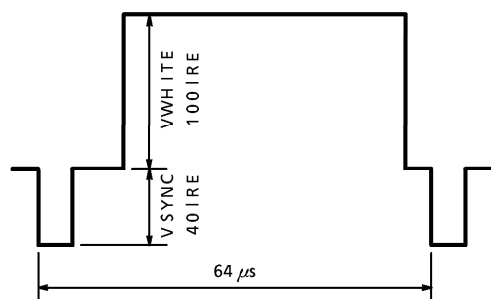
	No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN.	TYP.	MAX.	UNIT	NOTE
TPSG Part	3-1-1	TPSG Modulation Depth (Negative Modulation)	mpn (TPSG)	—	64	74	84	%	TPSG mode
	3-1-2	TPSG Modulation Depth (Positive Modulation)	mpp (TPSG)		82	92	97		
	3-2	TPSG V / S Ratio	V / S		2.0	2.4	2.8	—	
	3-3-1	TPSG Horizontal Sync Signal Cycle	Tsync	—	62	64	66	μs	
	3-3-2	TPSG Horizontal Sync Signal Width	Wsync		3.6	4.0	4.4		
	3-4-1	TPSG SYNC-1'st Signal Time	W1		22	24	26		
	3-4-2	TPSG SYNC-2'nd Signal Time	W2		38	40	42		
Sound Part	4-1-1	P / S Ratio FM	R _p / SFM	—	− 15	− 13	− 11	dB	Set in − 13dB by bus, STAIR CASE (B / W) signal : 0.5V _{p-p} input, 1kHz sin wave input : 0.2V _{p-p} (AM)
	4-1-2	P / S Ratio AM	R _p / SAM	—	− 11	− 9	− 7		
	4-2-1	Range of P / S Ratio FM	ΔR _p / SFM	—	− 17	—	− 10	dB	P / S ratio can be adjusted by 1dB. 1kHz sin wave input : 0.2V _{p-p} (AM)
	4-2-2	Range of P / S Ratio AM	ΔR _p / SAM	—	− 13	—	− 6		
	4-3-1	Sound Modulation Sensitivity FM1 (5.5MHz/ 6.0MHz / 6.5MHz)	β _{FM1}	—	0.531	0.59	0.649	kHz / mV	1kHz sin wave : 0.2V _{p-p} input, β _{FM} = Δf (kHz) / 200 (mV)
	4-3-2	Sound Modulation Sensitivity FM2 (4.5MHz)	β _{FM2}	—	0.265	0.295	0.325	kHz / mV	
	4-3-3	Sound Modulation Sensitivity AM	β _{AM}	—	58.1	64.4	71.1	%	1kHz sin wave : 0.2V _{p-p} input

	No.	CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	MIN.	TYP.	MAX.	UNIT	NOTE
Sound Part	4-4-1	Sound S / N Ratio FM1 (5.5MHz / 6.0MHz / 6.5MHz)	S / N (FM1)	—	50	55	—	dB	1kHz sin wave input : ± 50 kHz dev. = 0dB Inter Carrier demod., de-emph = 1N, Colorbar signal : 0.5V _{p-p} input
	4-4-2	Sound S / N Ratio FM2 (4.5MHz)	S / N (FM2)	—	47	52	—		1kHz sin wave input : ± 25 kHz dev. = 0dB Inter Carrier demod., de-emph = 1N, Colorbar signal : 0.5V _{p-p} input
	4-4-3	Sound S / N Ratio AM	S / N (AM)	—	50	55	—		1kHz sin wave input : 60% mod. = 0dB de-emph = 1N, Colorbar signal : 0.5V _{p-p} input
	4-5-1	Sound Distortion FM	THD (FM)	—	—	0.25	0.5	%	1kHz sin wave : ± 50 (25) kHz dev.
	4-5-2	Sound Distortion AM	THD (AM)	—					1kHz sin wave : 60% MOD.
	4-6-1	Sound Frequency Response FM	fs (FM)	—	—	± 1	± 2	dB	100Hz~20kHz, 1kHz reference
	4-6-2	Sound Frequency Response AM	fs (AM)	—	—	± 0.5	± 1		
	4-7-1	Sound 2'nd Harmonic Level	V _{SH1}	—	—	- 65	- 60	dB	P / S ratio = - 13dB, Video carrier level reference
	4-7-2	Sound 3'rd Harmonic Level	V _{SH2}	—	—	- 75	- 70		
	4-8	Sound Inter-Carrier Frequency Accuracy	Δf_s	—	—	—	± 750	Hz	X'tal series capacitor : 7pF

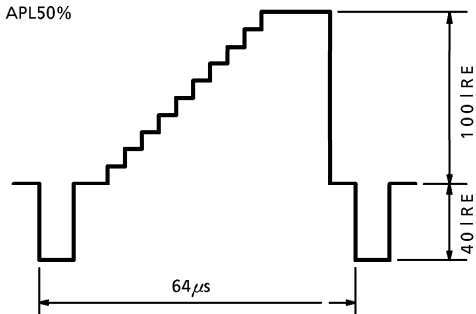
	No.	CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	MIN.	TYP.	MAX.	UNIT	NOTE
Logic part	5-1	LOW Level Input Voltage of Both SDA and SCL Lines	V_L	—	0	—	1.8	V	—
	5-2	HIGH Level Input Voltage of Both SDA and SCL Lines	V_H	—	2.8	—	V_{CC}	V	—
	5-3	LOW Level Output Voltage of SDA Line	V_{ACK}	—	0	—	0.4	V	at 3mA sink current During the acknowledge clock pulse
	5-4	Threshold Voltage of Power On Reset	V_{RESET}	—	2.0	2.8	3.6	V	—
	5-5	Logic Out Current	I_{LOGIC}	—	—	—	10	mA	Mounts on the board of power dissipation 830mW. T_a (MAX) = 75°C
—	6-1	Negative Resistance of X'tal Oscillator	R_{XO}	—	-1	—	—	k Ω	—

INPUT WAVE FORM

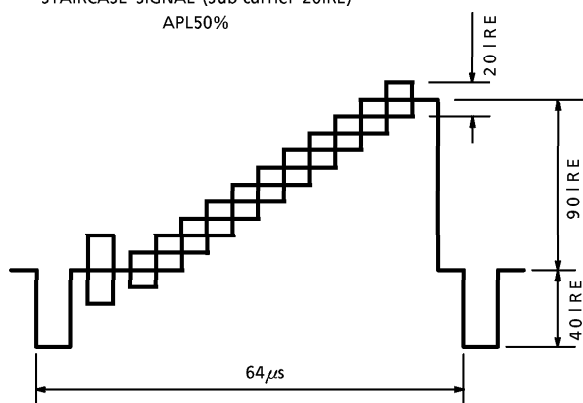
WHITE SIGNAL



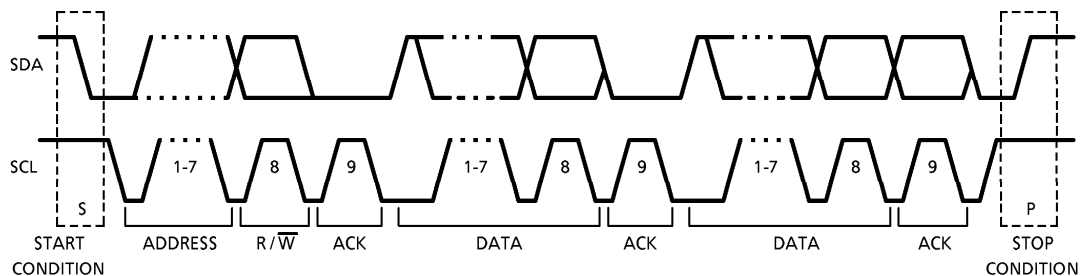
STAIRCASE (B/W) SIGNAL
APL50%



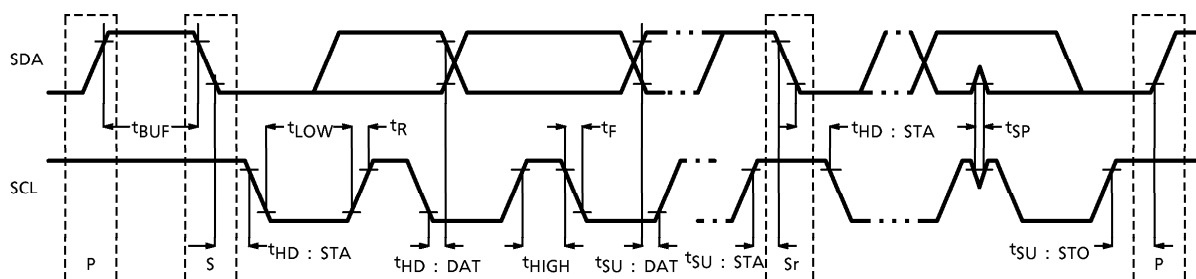
STAIRCASE SIGNAL (Sub-carrier 20IRE)
APL50%



DATA TRANSFER ON THE I²C-BUS



TIMING REQUIREMENTS FOR THE I²C-BUS



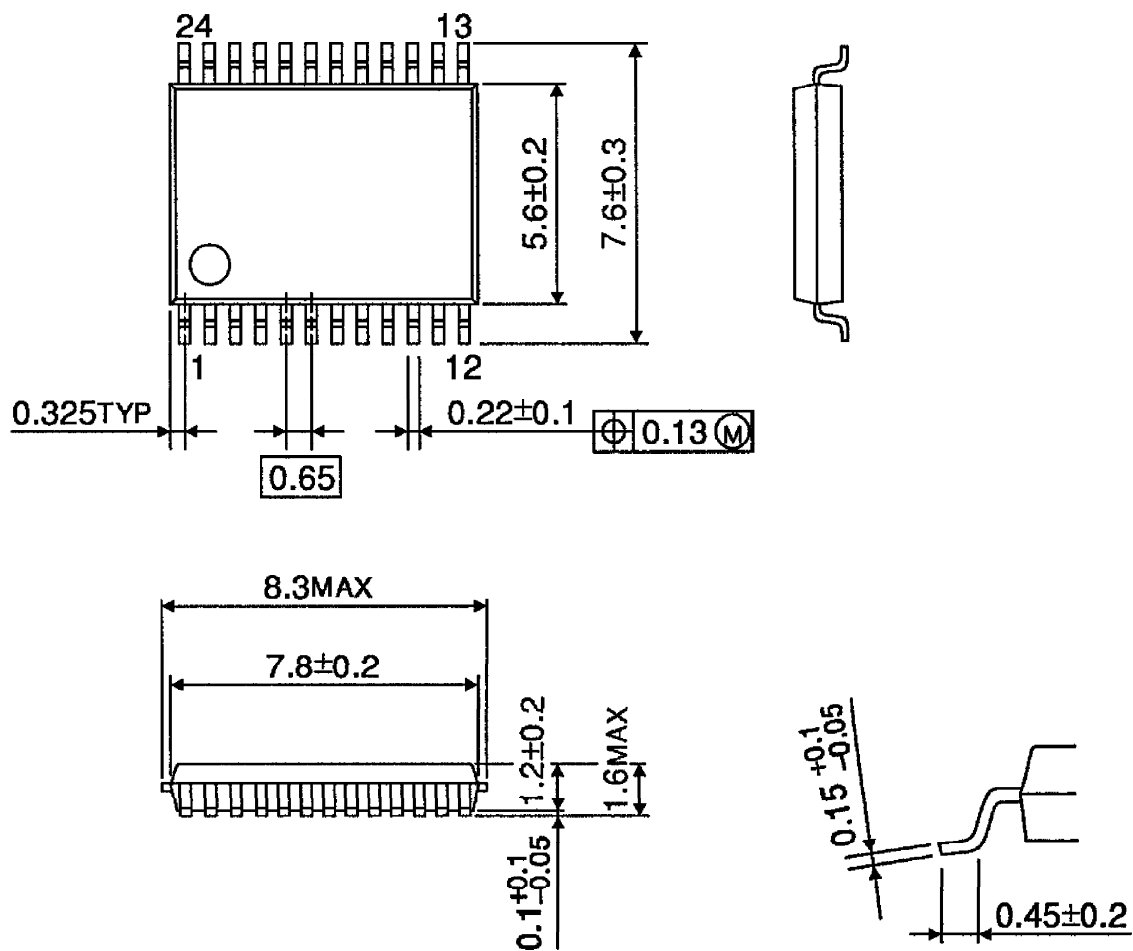
The diagram illustrates the internal architecture and pin configuration of the TDA9867 IC. The top section shows functional blocks such as the Color Processor (C.P.), Phase Comparator, Sound Counter, White Clip, Clamp, Sound VCO, AM Modulator, Video Modulator, RF Carrier Oscillator, RF Modulator, Mixer, Buffer Amplifier, Programmable Divider, Phase Comparator, and CP & Driver. The bottom section details the 12 pins, their electrical connections to various components (e.g., resistors, capacitors, crystals, diodes), and the power supply rails (D. VCC, D. GND, A. VCC, A. GND1, A. GND2).

1998-07-21 17/18

OUTLINE DRAWING

SSOP24-P-300-0.65A

Unit : mm



Weight : 0.14g (Typ.)