



22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipsets

General Description

The MAX9223/MAX9224 serializer/deserializer chipsets reduce wiring by serializing 22 bits onto a single differential pair. 22 bits are serialized in each cycle of the parallel input clock resulting in a 110Mbps to 220Mbps net serial-data rate ideal for cell phone QVGA and QCIF displays. The MAX9223 serializes the 18-bit RGB, VSYNC, HSYNC, and two control signals from the baseband processor to reduce wiring through the hinge to the LCD controller. The 2-wire serial interface uses low-current differential signaling (LCDS) for low EMI, high common-mode noise immunity, and ground-shift tolerance. The MAX9223/MAX9224 automatically identify the word boundary in serial data in case of signal interruption. The MAX9224 power-down is controlled by the MAX9223. The MAX9223 and MAX9224 consume 3.5μA or less in power-down mode.

The MAX9223 serializer operates from a single +2.375V to +3.465V supply and accepts +1.71V to +3.465V inputs. The MAX9224 deserializer operates from a +2.375V to +3.465V core supply and has a separate output buffer supply (VDDO), allowing +1.71V to +3.465V output high levels.

The MAX9223/MAX9224 are specified over the -40°C to +85°C extended temperature range and are available in 28-pin TQFN (4mm x 4mm x 0.8mm) packages with an exposed paddle.

Applications

Cell Phones
LCDs
Digital Cameras

Features

- ◆ Ideal for Serializing Cell Phone LCD or Imager Parallel Interface
- ◆ MAX9223 Serializes 18-Bit RGB, VSYNC, HSYNC, and Two Control Signals
- ◆ LCDS Rejects Common-Mode Noise
- ◆ Automatic Location of Word Boundary After Signal Interruption
- ◆ Power-Down Control Through the Serial Link
- ◆ Power-Down Supply Current
0.5μA (max)—MAX9223
3.0μA (max)—MAX9224
- ◆ +2.375V to +3.465V Core Supply Voltage
- ◆ Parallel I/O Interfaces Directly to 1.8V to 3.3V Logic
- ◆ ±15kV Human Body Model ESD Protection
- ◆ -40°C to +85°C Operating Temperature Range

Ordering Information

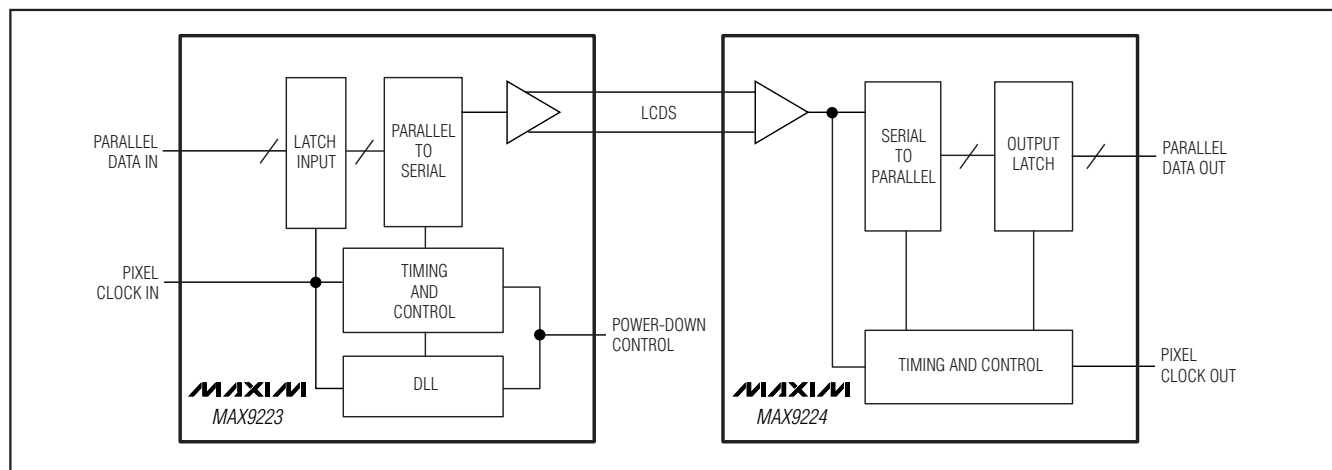
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9223ETI	-40°C to +85°C	28 TQFN-EP*	T2844-1
MAX9223ETI+	-40°C to +85°C	28 TQFN-EP*	T2844-1
MAX9224ETI	-40°C to +85°C	28 TQFN-EP*	T2844-1
MAX9224ETI+	-40°C to +85°C	28 TQFN-EP*	T2844-1

+Denotes lead-free package.

*EP = Exposed paddle.

Pin Configurations appear at end of data sheet.

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.5V to +4.0V	Single-Layer PCB (derate 20.8mW/°C above +70°C).....	1667mW
V _{DDO} to GND.....	-0.5V to +4.0V	Storage Temperature Range	-65°C to +150°C
Serial Interface (SDO+, SDO-, SDI+, SDI-) to GND	-0.5V to +4.0V	Junction Temperature	+150°C
Single-Ended Inputs (DIN_, PCLKIN, PWRDN) to GND	-0.5V to (V _{DD} + 0.5V)	Lead Temperature (soldering, 10s)	+300°C
Single-Ended Outputs (DOOUT_, PCLKOUT) to GND	-0.5V to (V _{DDO} + 0.5V)	ESD Protection (Human Body Model) SDO+, SDO-, SDI+, SDI- to GND	> ±15kV
Continuous Power Dissipation (T _A = +70°C) 28-Pin TQFN (4mm x 4mm x 0.8mm) Multilayer PCB (derate 28.6mW/°C above +70°C).....	2286mW	All Other Pins	> ±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—MAX9223

(V_{DD} = +2.375V to +3.465V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +2.5V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (PCLKIN, DIN_, PWRDN)							
High-Level Input Voltage	V _{IH}			1.19	V _{DD} + 0.3		V
Low-Level Input Voltage	V _{IL}			-0.3	+0.3		V
Input Current	I _{IN}	V _{IN} = 0V to V _{DD}		-20	+20		μA
		-0.3V ≤ V _{IN} < 0V		-100	+100		
		V _{DD} < V _{IN} ≤ (V _{DD} + 0.3V)					
LCDS OUTPUT (SDO+, SDO-)							
Differential Output Current (Note 3)	I _{ODH}	High level		600	643	880	μA
	I _{ODL}	Low level		200	229	300	
Output Short-Circuit Current	I _{OS}	Shorted to 0V or V _{DD}		880			μA
POWER SUPPLY							
Supply Current	I _{DD}	V _{DD} = 2.5V, DIN_ = all low or all high	PCLKIN = 5MHz (110Mbps)	4.4		8.2	mA
			PCLKIN = 10MHz (220Mbps)	5.6		8.2	
Worst-Case Pattern Supply Current	I _{DDW}	V _{DD} = 2.5V, Figure 1	PCLKIN = 5MHz (110Mbps)	4.1		10.6	mA
			PCLKIN = 10MHz (220Mbps)	5.4		10.6	
Power-Down Supply Current	I _{DDZ}	All inputs = low		0.5			μA

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DC ELECTRICAL CHARACTERISTICS—MAX9224

($V_{DD} = +2.375V$ to $+3.465V$, $V_{DDO} = +1.71V$ to $+3.465V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{DD} = V_{DDO} = +2.5V$, $T_A = +25^{\circ}C$.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED OUTPUTS (PCLKOUT, DOUT_)							
High-Level Output Voltage	VOH	VDDO = +2.375V to +3.465V, IOH = -1mA		0.8 x VDDO			V
Low-Level Output Voltage	VOL	VDDO = +2.375V to +3.465V, IOL = 1mA		0.2			V
Output Short-Circuit Current	IOS	Output shorted to ground	VDDO = 2.375V	-2			mA
			VDDO = 3.135V	-9			
			VDDO = 3.465V	-25			
LCDS INPUT (SDI+, SDI-)							
Differential Input-Current Threshold	IID			400			μA
Common-Mode Input Current	IIC			-300	±500	+300	μA
Differential Input Impedance	ZID	IIC = 0μA at VDD = 3.3V ±5%		69	90	109	Ω
		IIC = 0μA at VDD = 2.8V ±5%		82	108	132	
		IIC = 0μA at VDD = 2.5V ±5%		95	125	153	
		IIC = ±300μA at VDD = 3.3V ±5%		67	91	112	
		IIC = ±300μA at VDD = 2.8V ±5%		86	108	136	
Common-Mode Input Impedance	ZIC	IIC = ±300μA		90	167	375	Ω
Input Capacitance	CIN	SDI+ or SDI- to ground		2			pF
POWER SUPPLY							
Supply Current (Note 4)	ITOT	VDD = VDDO = 2.5V DOUT_ = all high or all low	PCLKOUT = 5MHz (110Mbps)	912			mA
			PCLKOUT = 10MHz (220Mbps)	912			
Worst-Case Pattern Supply Current (Note 4)	ITOTW	CL = 5pF, VDD = VDDO = 2.5V, Figure 2	PCLKOUT = 5MHz (110Mbps)	1012			mA
			PCLKOUT = 10MHz (220Mbps)	1012			
Power-Down Supply Current (Note 4)	ITOTZ			0.083			μA
Supply Difference	VSD	MAX9223 VDD to MAX9224 VDD		-5+5			%
GROUND POTENTIAL							
Ground Difference	VGD	MAX9223 to MAX9224 ground difference		-0.2+0.2			V

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AC ELECTRICAL CHARACTERISTICS—MAX9223

($V_{DD} = +2.375V$ to $+3.465V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{DD} = +2.5V$, $T_A = +25^{\circ}C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PCLKIN INPUT REQUIREMENTS (Figure 3)						
Input Rise Time	t_R				2	ns
Input Fall Time	t_F				2	ns
PCLKIN Period	t_P		100		200	ns
High-Level Pulse Width	t_{PWH}		$0.3 \times t_P$		$0.7 \times t_P$	ns
Low-Level Pulse Width	t_{PWL}		$0.3 \times t_P$		$0.7 \times t_P$	ns
Setup Time	t_S		3			ns
Hold Time	t_H		1			ns

AC ELECTRICAL CHARACTERISTICS—MAX9224

($V_{DD} = V_{DDO} = +2.375V$ to $+3.465V$, $C_L = 5pF$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{DD} = V_{DDO} = +2.5V$, $T_A = +25^{\circ}C$.) (Notes 3, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PCLKOUT Period	t_P	Figure 4	100		200	ns
High-Level Pulse Width	t_{PWH}	Figure 4	$0.4 \times t_P$		$0.6 \times t_P$	ns
Low-Level Pulse Width	t_{PWL}	Figure 4	$0.4 \times t_P$		$0.6 \times t_P$	ns
Data Valid Before PCLKOUT	t_{VB}	Figure 4	5			ns
Data Valid After PCLKOUT	t_{VA}	Figure 4	5			ns
SERIALIZER AND DESERIALIZER LINK						
Power-Up Time	t_{PU1}	From $V_{DD} = V_{DDO} = 2.375V$ when supplies are ramping up			$6144 \times t_P$	ns
	t_{PU2}	From $\overline{PWRDN}$ low to high			$4096 \times t_P$	
Power-Down Time	t_{PWRDN}	From $\overline{PWRDN}$ high to low		2.8	10	μs

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at $T_A = +85^{\circ}C$.

Note 3: Parameters are guaranteed by design and characterization, and are not production tested. Limits are set at ± 6 sigma.

Note 4: $I_{TOT} = I_{DD} + I_{DDO}$.

Note 5: C_L includes probe and test jig capacitance.

MAX9223/MAX9224

The timing diagram shows three digital signals over time. The horizontal axis represents time, and the vertical axis represents the signal level (high or low). The signals are labeled on the left: ODD DIN, EVEN DIN, and PCLKIN.

- ODD DIN:** This signal starts at a low level, transitions to high, remains high for a duration, transitions back to low, remains low for a duration, and then transitions back to high.
- EVEN DIN:** This signal starts at a high level, transitions to low, remains low for a duration, transitions back to high, remains high for a duration, and then transitions back to low.
- PCLKIN:** This signal starts at a high level, transitions to low, remains low for a duration, transitions back to high, remains high for a duration, transitions back to low, remains low for a duration, transitions back to high, remains high for a duration, and then transitions back to low.

The diagram illustrates the relationship between these signals, showing that ODD DIN and EVEN DIN are complementary signals, and PCLKIN is a periodic clock signal.

The timing diagram shows three digital signals over time. The top signal, ODD DOUT_, is high during the first and third clock cycles and low during the second and fourth. The middle signal, EVEN DOUT_, is low during the first and third clock cycles and high during the second and fourth. The bottom signal, PCLKOUT, is a periodic clock signal with a period of one clock cycle.

The diagram shows two signals: PCLKIN and DIN/PWRDN. PCLKIN is a clock signal with period t_p , high pulse width t_{pWH} , low pulse width t_{pWL} , rise time t_R , and fall time t_F . Its voltage levels are V_{IH} and V_{IL} . DIN/PWRDN is a data or power-down signal that transitions between V_{IH} and V_{IL} at the clock edges. The setup time t_S is the time from the signal crossing V_{IL} to the clock edge, and the hold time t_H is the time from the clock edge to the signal crossing V_{IH} .

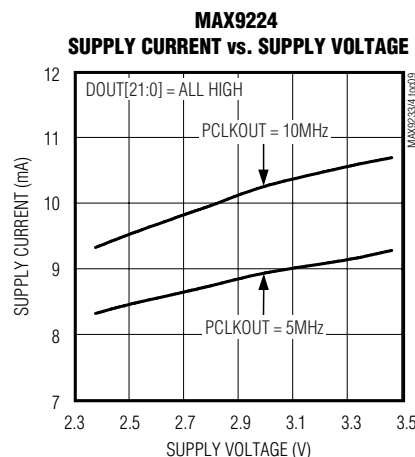
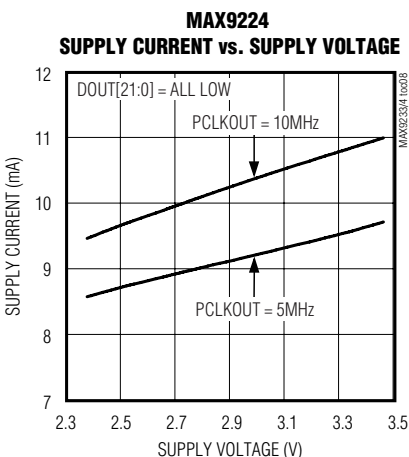
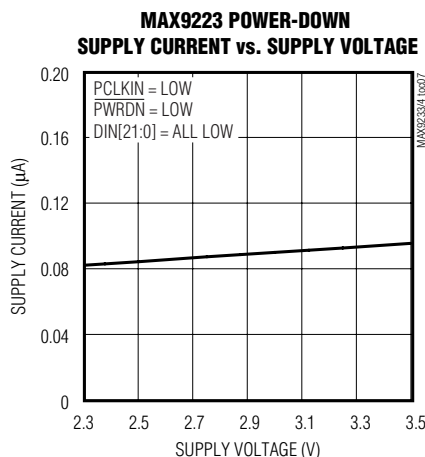
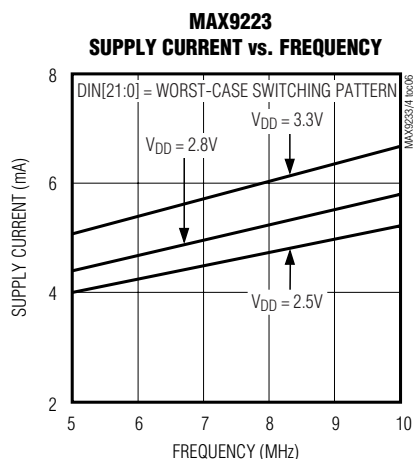
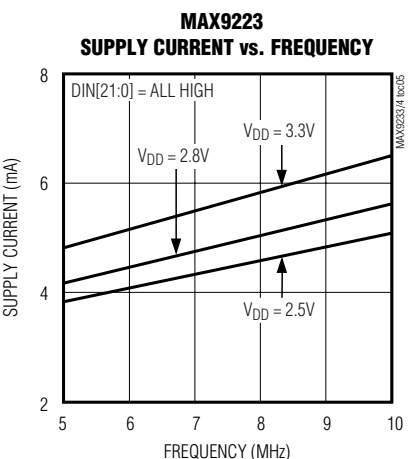
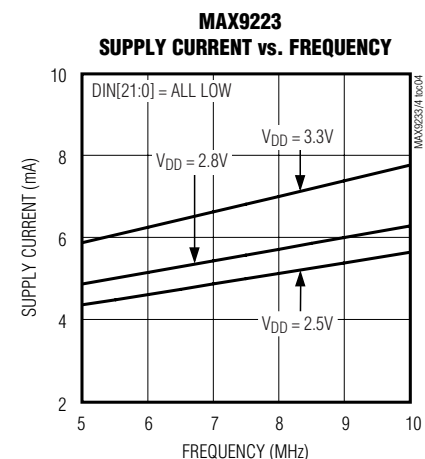
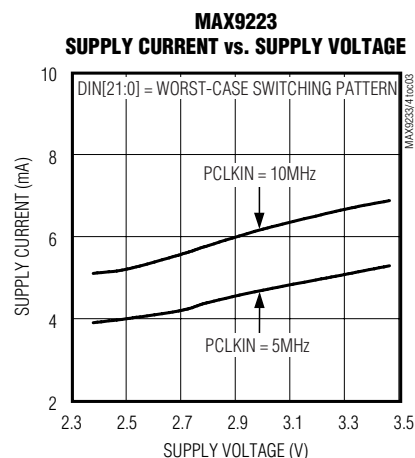
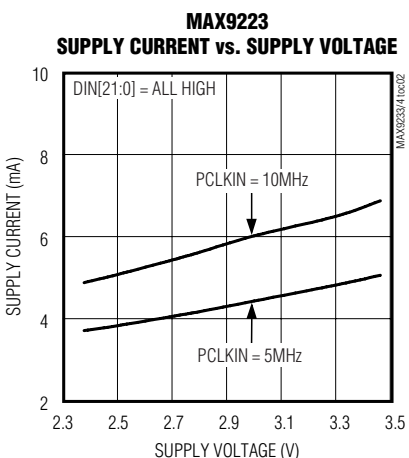
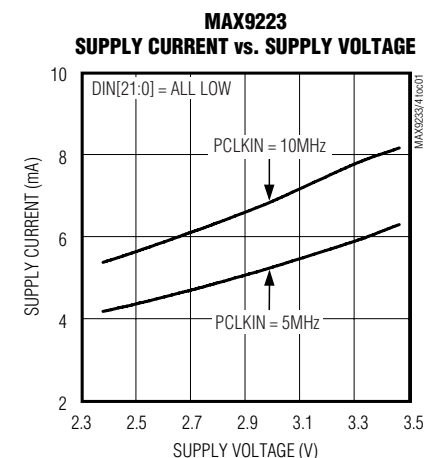
The diagram shows two digital signals over time. The top signal, PCLKOUT, is a periodic square wave. Its high-level output is labeled V_{OH} and its low-level output is labeled V_{OL} . The period of the signal is labeled t_P . The time from the rising edge to the 50% crossing is labeled t_{PWL} , and the time from the falling edge to the 50% crossing is labeled t_{PWH} . The bottom signal, DOUT_, is a square wave that is high during the low phase of PCLKOUT and low during the high phase of PCLKOUT. Its high-level output is labeled V_{OH} and its low-level output is labeled V_{OL} . The time from the rising edge of DOUT_ to the 50% crossing of PCLKOUT is labeled t_{VB} , and the time from the falling edge of DOUT_ to the 50% crossing of PCLKOUT is labeled t_{VA} .

MAXIM

22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipset

Typical Operating Characteristics

($V_{DD} = V_{DDO} = +2.8V$, logic input levels = 0 to +2.8V, logic output load $C_L = 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)

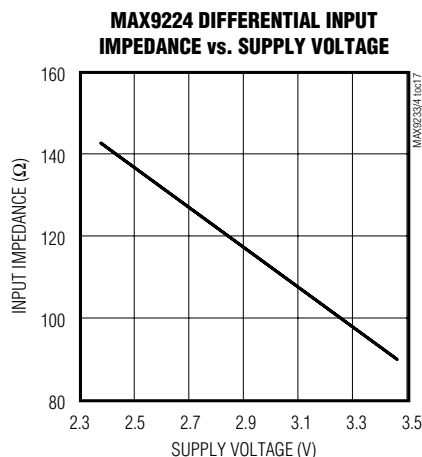
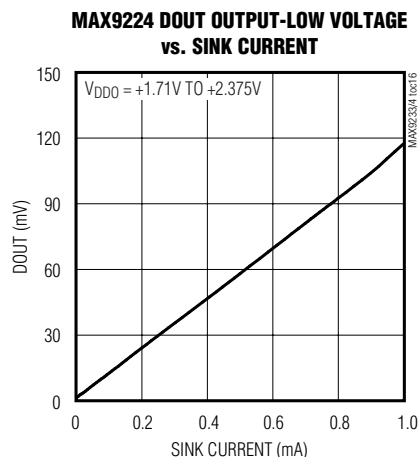
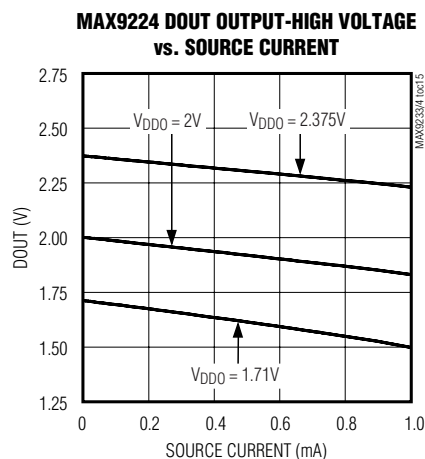
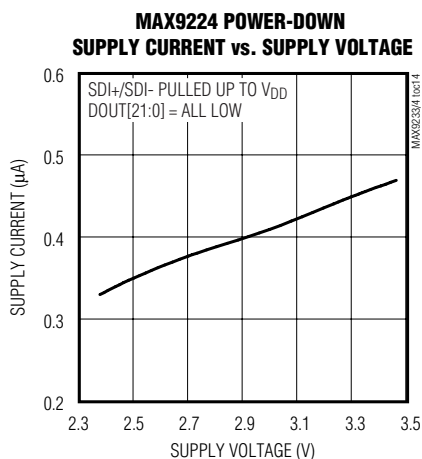
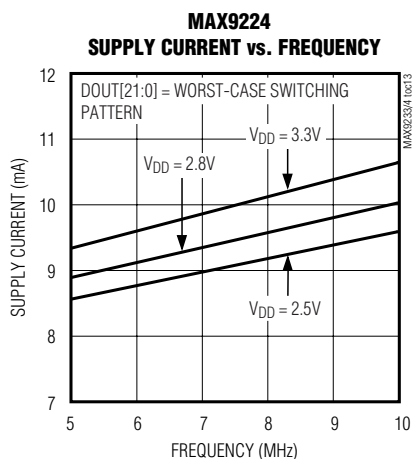
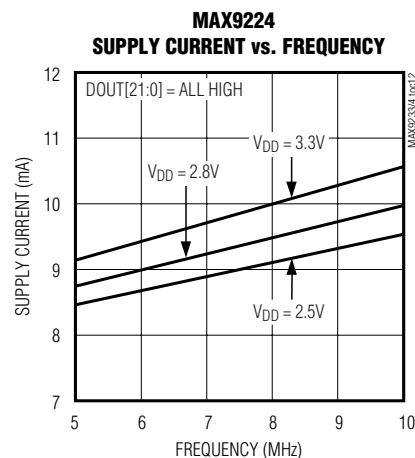
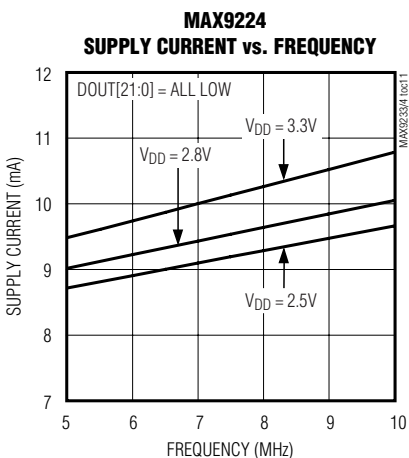
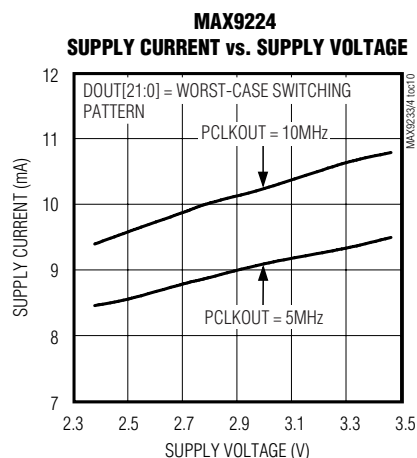


22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipset

Typical Operating Characteristics (continued)

($V_{DD} = V_{DDO} = +2.8V$, logic input levels = 0 to +2.8V, logic output load $C_L = 5pF$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX9223/MAX9224



22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipset

Pin Description (MAX9223)

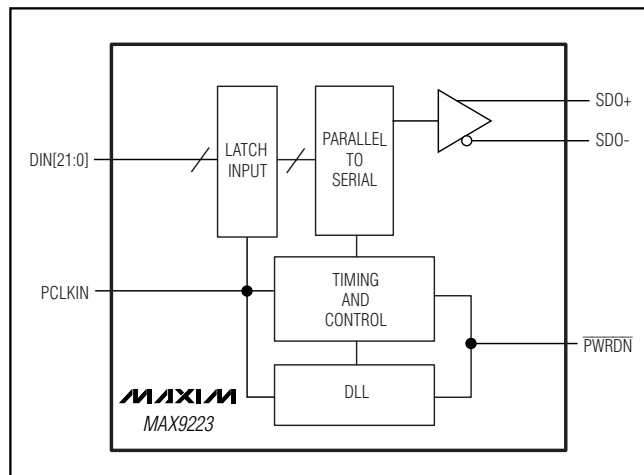
PIN	NAME	FUNCTION
1–12, 14, 15, 21–28	DIN13–DIN2, DIN1, DIN0, DIN21–DIN14	Single-Ended Parallel Data Inputs. The 22 data bits are loaded into the input latch on the rising edge of PCLKIN. DIN[21:0] are 1.71V to 3.465V tolerant. Internally pulled down to GND.
13	PCLKIN	Parallel Clock Input. The rising edge of PCLKIN (typically the pixel clock) latches the parallel data input. Internally pulled down to GND.
16	$\overline{\text{PWRDN}}$	Power-Down Input. Pull $\overline{\text{PWRDN}}$ low to place the MAX9223 and MAX9224 in power-down mode. Drive $\overline{\text{PWRDN}}$ high for normal operation. Internally pulled down to GND.
17	SDO-	Inverting LCDS Serial-Data Output
18	SDO+	Noninverting LCDS Serial-Data Output
19	GND	Ground
20	V _{DD}	Core Supply Voltage. Bypass to GND with 0.1 μ F and 0.01 μ F capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
—	EP	Exposed Paddle. Connect EP to ground.

Pin Description (MAX9224)

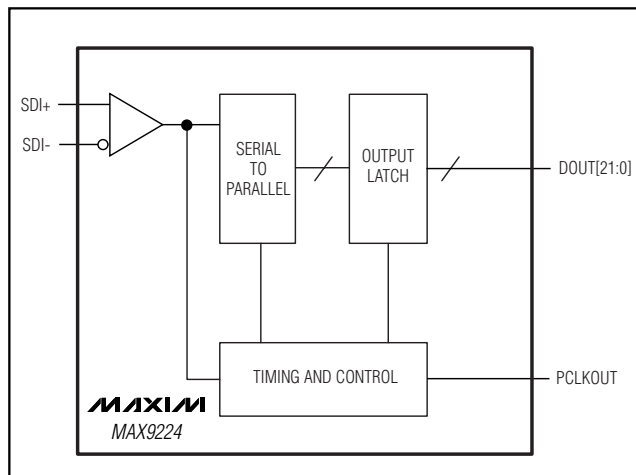
PIN	NAME	FUNCTION
1, 7, 8, 10–28	DOUT21, DOUT0, DOUT1, DOUT2–DOUT20	Single-Ended Parallel Data Outputs. DOUT[21:0] are valid on the rising edge of PCLKOUT.
2	V _{DDO}	Output Supply Voltage. Bypass to GND with 0.1 μ F and 0.01 μ F capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
3	GND	Ground
4	SDI+	Noninverting LCDS Serial-Data Input
5	SDI-	Inverting LCDS Serial-Data Input
6	V _{DD}	Core Supply Voltage. Bypass to GND with 0.1 μ F and 0.01 μ F capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
9	PCLKOUT	Parallel Clock Output. Parallel output data are valid on the rising edge of PCLKOUT (typically the pixel clock).
—	EP	Exposed Paddle. Connect EP to ground.

22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipset

MAX9223 Functional Diagram



MAX9224 Functional Diagram



MAX9223/MAX9224

Detailed Description

The MAX9223 serializer operates at a 5MHz to 10MHz parallel clock frequency, serializing 22 bits of parallel input data DIN[21:0] in each cycle of the parallel clock. DIN[21:0] are latched on the rising edge of PCLKIN. The data and internally generated serial clock are combined and transmitted through SDO+/SDO- using multilevel LCDS. The MAX9224 deserializer receives the LCDS signal on SDI+/SDI-. The deserialized data and recovered parallel clock are available at DOUT[21:0]

and PCLKOUT. Output data is valid on the rising edge of PCLKOUT.

The first bit (G) is internally grounded and transmitted first. Bit 0 (DIN[0]) is the first valid data bit. Boundary bits OH are used by the MAX9224 deserializer to identify the word boundary and are the inverse polarity of data bit 21 (DIN[21]). Therefore, at least one level transition is guaranteed in one word. The clock is recovered from the serial input.

Serial word format:

G	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	OH	OH
---	---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----	----	----	----

LCDS

The MAX9223/MAX9224 use a proprietary multilevel LCDS interface. Figure 5 provides a representation of the data and clock in the multilevel LCDS interface. This interface offers advantages over other chipsets, such as requiring only one differential pair as the transmission medium, the inherently aligned data and clock, and much smaller current levels than the 4mA typically found in traditional LVDS interfaces.

MAX9223/MAX9224 Handshaking

The handshaking function of the MAX9223/MAX9224 provides bidirectional communication between the two devices in case a word boundary error is detected. Prior

to data transmission, the MAX9223 serializer adds boundary bits (OH) to the end of the latched word. These boundary bits are the inverse of the last bit of the latched word. During data transmission, the MAX9224 deserializer continuously monitors the state of the boundary bits of each word. If a word boundary error is detected, the serial link is pulled up to V_{DD} and the MAX9224 powers down. The MAX9223 detects the pullup of the serial link and powers down for 1.0μs. After 1.0μs, the MAX9223 powers up, causing the power-up of the MAX9224. Then the word boundary is reestablished, and data transfer resumes. The handshaking function is disabled when PWRDN is pulled low.

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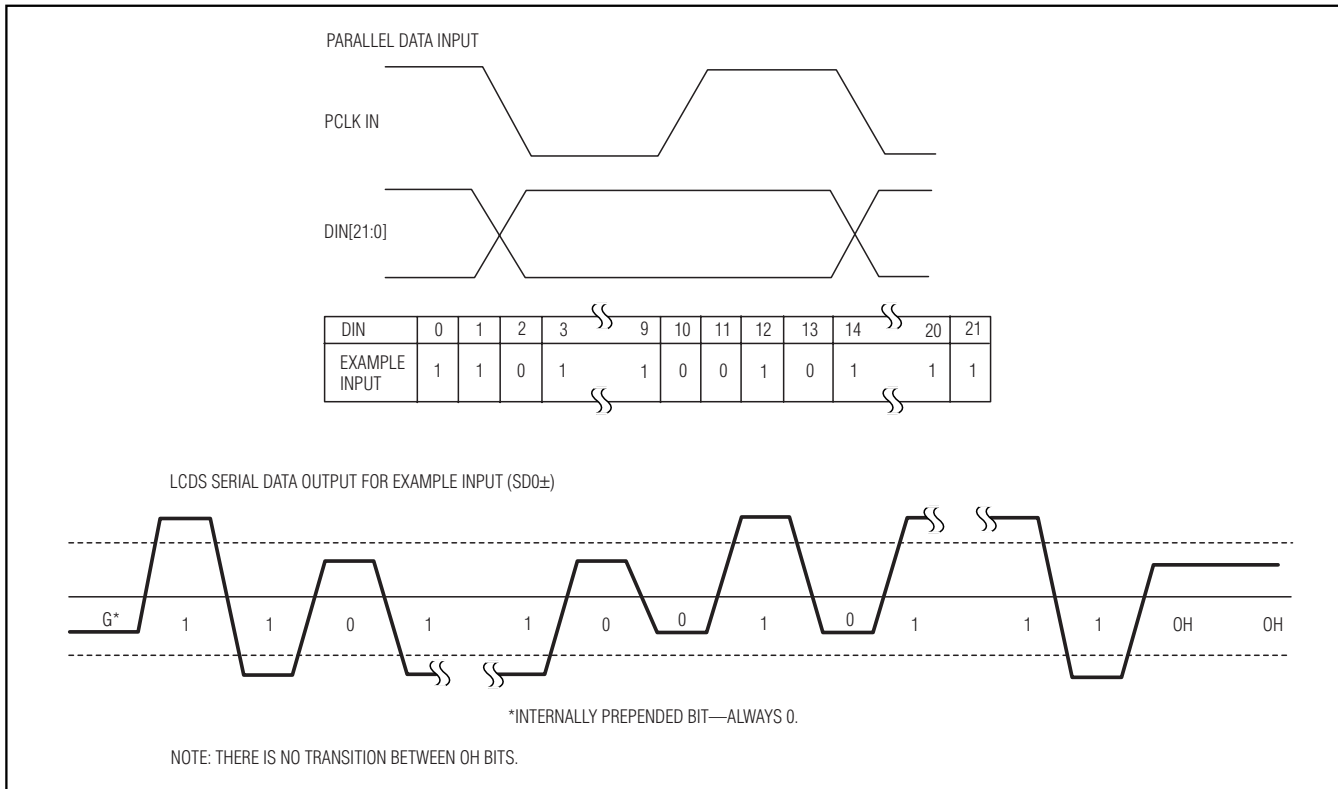


Figure 5. Multilevel LCDS Output Representation

Applications Information

PCLKIN Latch Edge

The parallel data input of the MAX9223 serializer is latched on the rising edge of PCLKIN. Figure 3 shows the serializer input timing.

PCLKOUT Strobe

The serial-data output of the MAX9224 deserializer is valid on the rising edge of PCLKOUT. Figure 4 shows the deserializer output timing.

Power-Down and Power-Up

Driving $\overline{\text{PWRDN}}$ low puts the MAX9223 in power-down mode and sends a pulse to power down the MAX9224. In power-down mode, the DLL is stopped, SDO+/SDO- are high impedance to ground and differential, and the LCDS link is weakly biased around $V_{DD} - 0.8V$. With $\overline{\text{PWRDN}}$ and all inputs low, the combined MAX9223/MAX9224 supply current is reduced to 3.5μA or less.

Driving $\overline{\text{PWRDN}}$ high starts DLL lock to PCLKIN and initiates a MAX9224 power-up sequence. The MAX9223

LCDS output is not driven until the DLL locks. 4096 clock cycles are required for the power-up and link synchronization, before valid DIN can be latched. See Figure 6 for an overall power-up and power-down timing diagram. For normal operation, PCLKIN must be running and settled before driving $\overline{\text{PWRDN}}$ high.

If $V_{DD} = 0$, the LCDS outputs are high impedance to ground and differential.

Ground-Shift Tolerance

The MAX9223/MAX9224 are designed to function normally in the event of a slight shift in ground potential. However, the MAX9224 deserializer ground must be within $\pm 0.2V$ relative to the MAX9223 serializer ground to maintain proper operation.

MAX9224 Output Buffer Supply (V_{DDO})

The MAX9224 parallel outputs are powered from V_{DDO} , which accepts a +1.71V to +3.465V supply, allowing direct interface to inputs with 1.8V to 3.3V logic levels.

22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipset

MAX9223/MAX9224

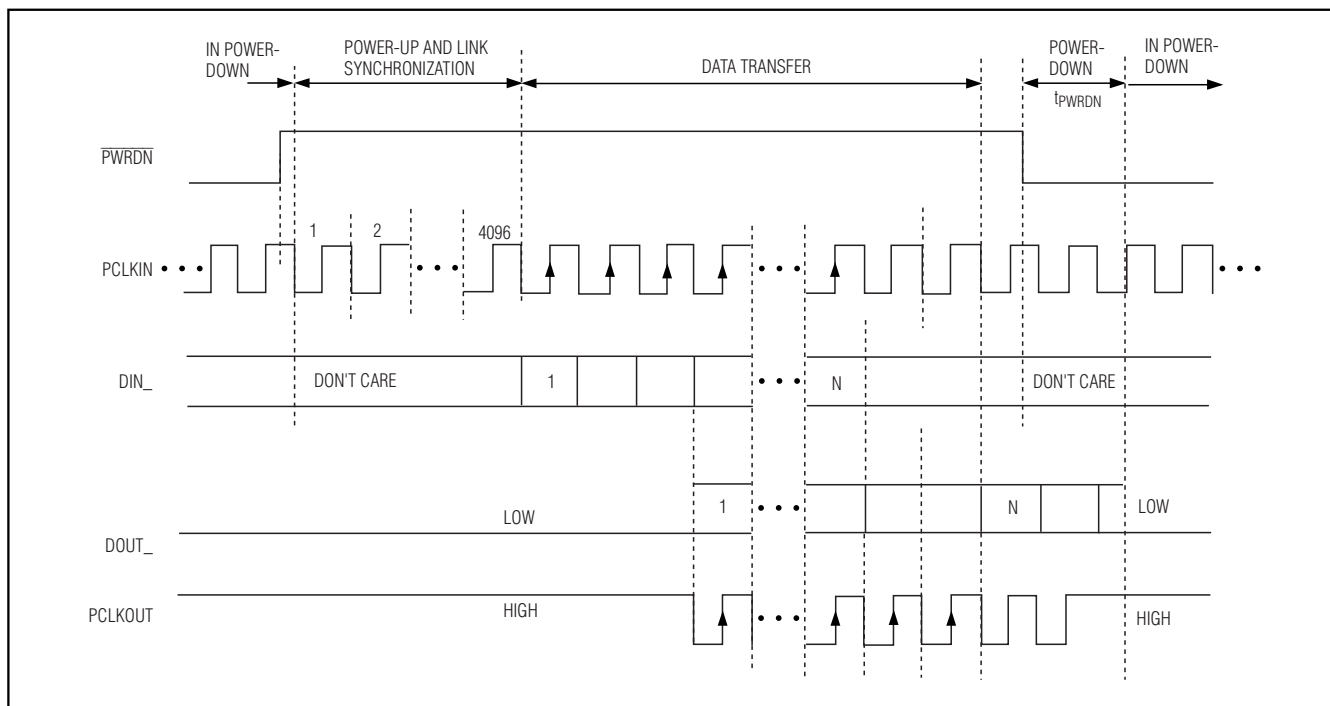


Figure 6. MAX9223/MAX9224 Power-Up/Power-Down Sequence

Flex Cable, PCB Interconnect, and Connectors

Interconnect for LCDS typically has a differential impedance of 110Ω . Use interconnect and connectors that have matched differential impedance to minimize impedance discontinuities.

Board Layout and Supply Bypassing

Separate the logic and LCDS signals to prevent crosstalk. A PCB or flex with separate layers for power, ground, and signals is recommended.

Bypass each V_{DD} and V_{DDO} pin with high-frequency, surface-mount ceramic $0.1\mu\text{F}$ and $0.01\mu\text{F}$ capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

ESD Protection

The MAX9223/MAX9224 LCDS inputs and outputs (SDO+/SDO-, SDI+/SDI-) are rated for $\pm 15\text{kV}$ ESD protection using the Human Body Model. The Human Body Model discharge components are $C_S = 100\text{pF}$ and $R_D = 1.5\text{k}\Omega$ (Figure 7).

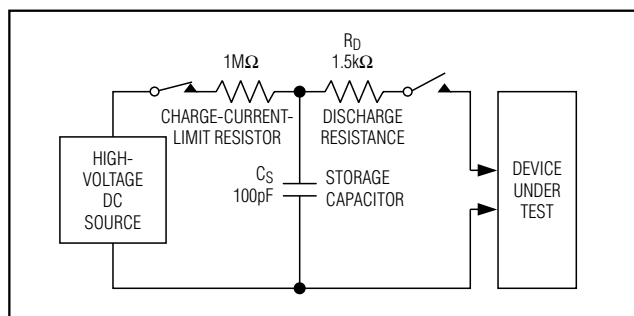


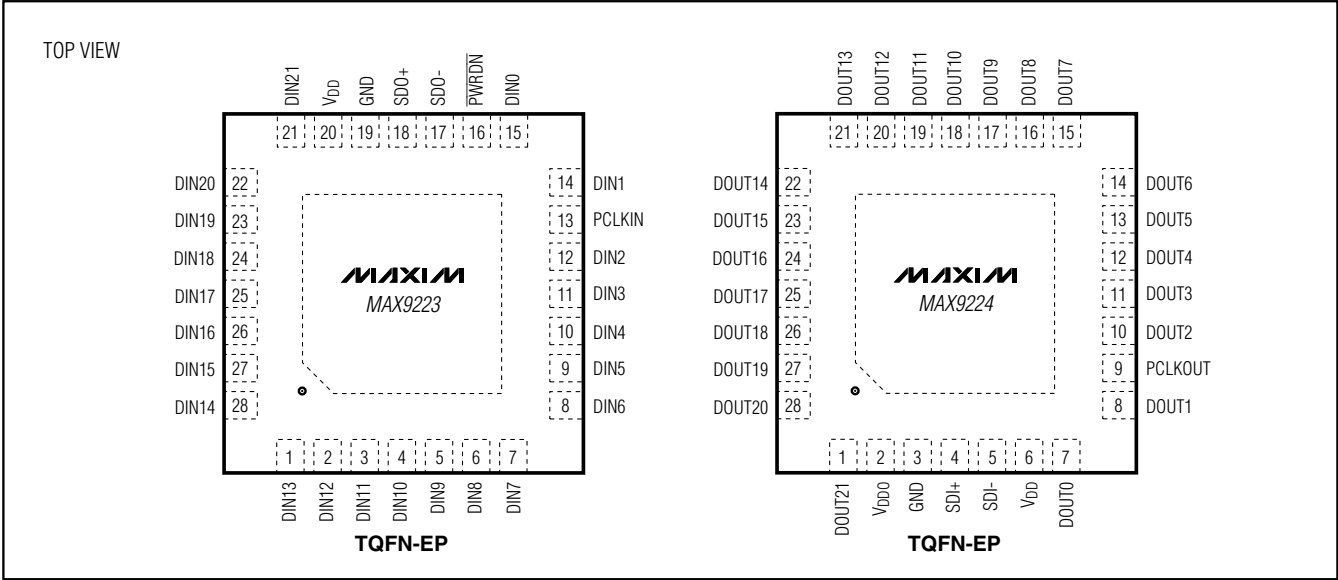
Figure 7. Human Body Model ESD Test Circuit

Chip Information

PROCESS: CMOS

22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipset

Pin Configurations



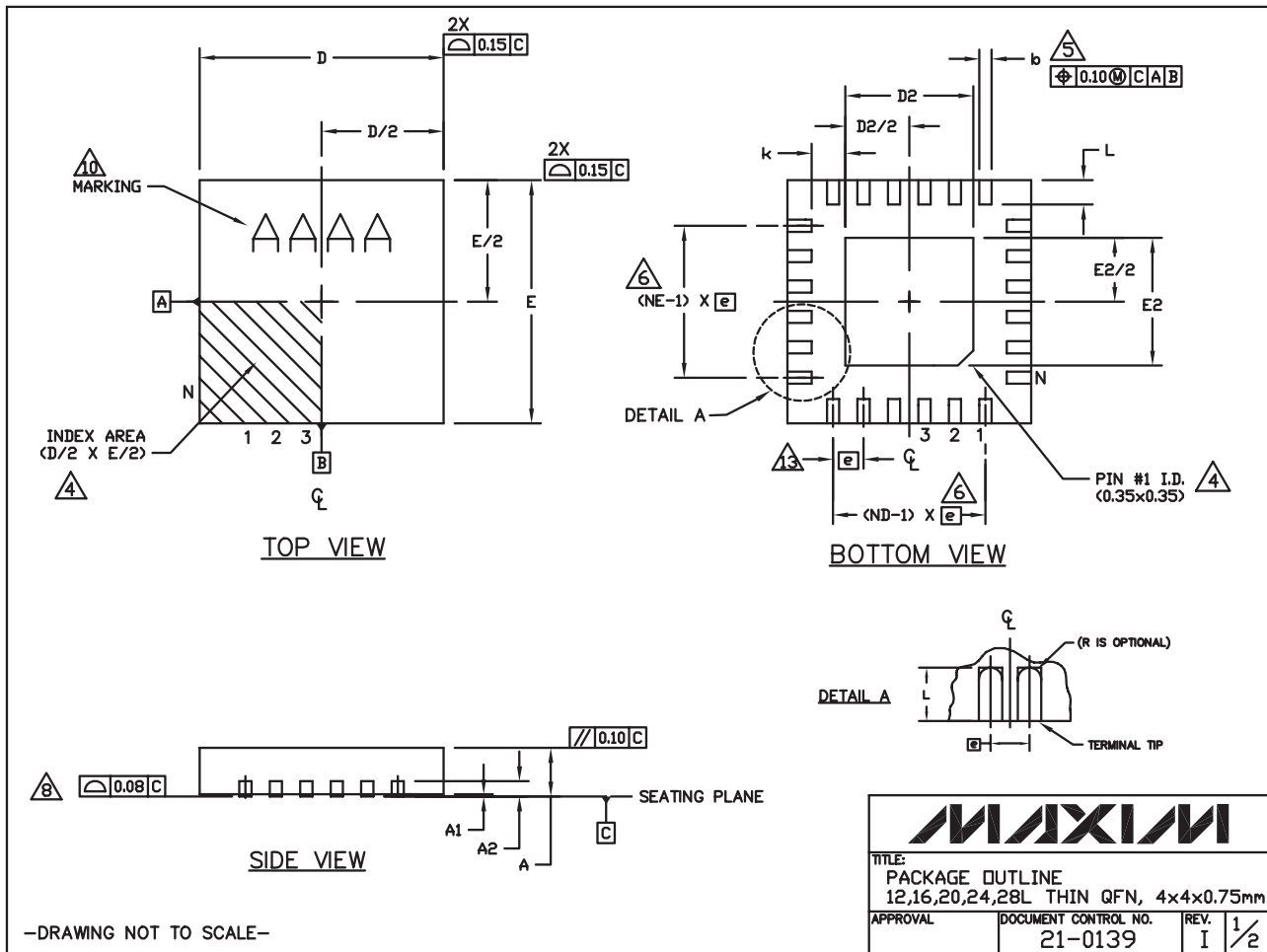
22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipset

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX9223/MAX9224

24L QFN THIN.EPS



22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipset

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
JeDEC	WGGB			WGGB			VGGG-1			VGGG-2			WGGE		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- COPLANARITY SHALL NOT EXCEED 0.08mm.
- WARPAGE SHALL NOT EXCEED 0.10mm.
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ± 0.05 .
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbfREE (+) PACKAGE CODES.

—DRAWING NOT TO SCALE—

MAXIM			
TITLE: PACKAGE OUTLINE 12,16,20,24,28L THIN QFN, 4x4x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0139	REV. I	2/2

22-Bit, Low-Power, 5MHz to 10MHz Serializer and Deserializer Chipset

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/05	Initial release	—
1	12/07	Changed min output short-circuit current from -20 to -25 and updated package outlines.	3, 13

MAX9223/MAX9224

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