

# 74HC164; 74HCT164

8-bit serial-in, parallel-out shift register

Rev. 7 — 13 June 2013

Product data sheet

## 1. General description

The 74HC164; 74HCT164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel data outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input (MR) clears the register and forces all outputs LOW, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Input levels:
  - ◆ For 74HC164: CMOS level
  - ◆ For 74HCT164: TTL level
- Gated serial data inputs
- Asynchronous master reset
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .



### 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74HC164N	−40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)		SOT27-1
74HCT164N					
74HC164D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm		SOT108-1
74HCT164D					
74HC164DB	−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm		SOT337-1
74HCT164DB					
74HC164PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm		SOT402-1
74HCT164PW					
74HC164BQ	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm		SOT762-1
74HCT164BQ					

### 4. Functional diagram

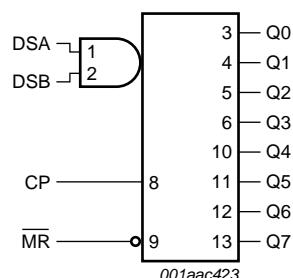


Fig 1. Logic symbol

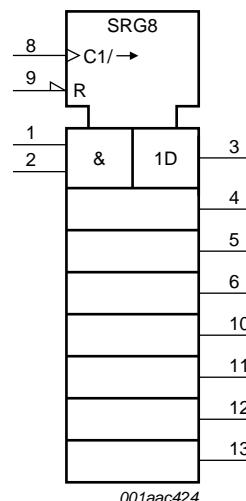


Fig 2. IEC logic symbol

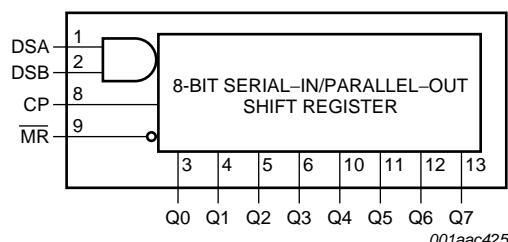


Fig 3. Logic diagram

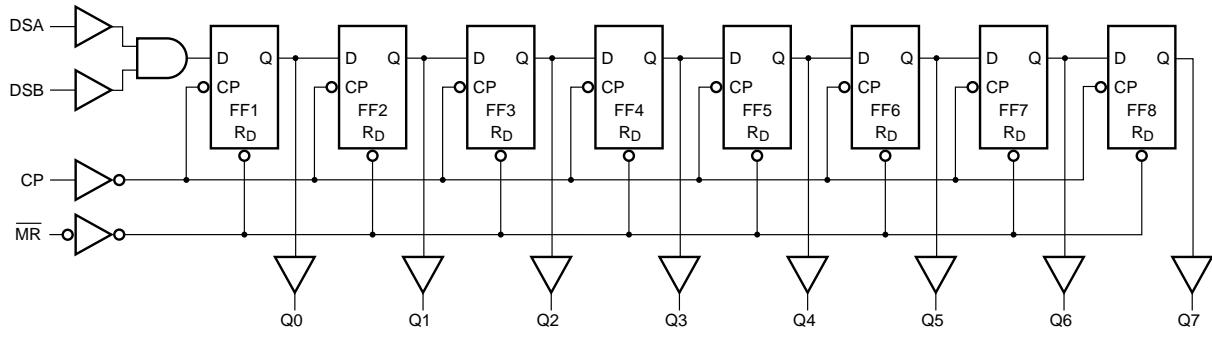


Fig 4. Functional diagram

## 5. Pinning information

### 5.1 Pinning

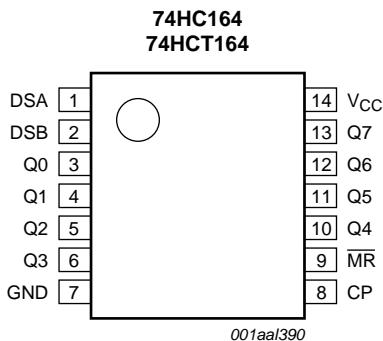


Fig 5. Pin configuration DIP14, SO14, (T)SSOP14

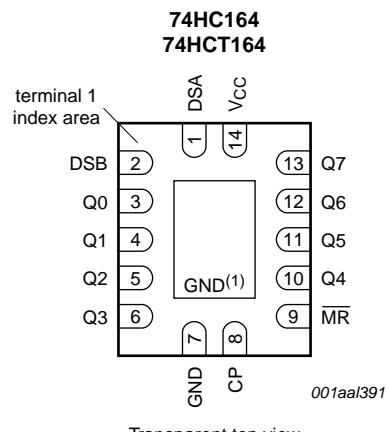


Fig 6. Pin configuration DHVQFN14

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	data input
DSB	2	data input
Q0 to Q7	3, 4, 5, 6, 10, 11, 12, 13	output
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH, edge-triggered)
MR	9	master reset input (active LOW)
V <sub>CC</sub>	14	positive supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating modes	Input				Output	
	MR	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	I	I	L	q0 to q6
	H	↑	I	h	L	q0 to q6
	H	↑	h	I	L	q0 to q6
	H	↑	h	h	H	q0 to q6

[1] H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	[1] -	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1] -	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C

**Table 4. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$P_{tot}$	total power dissipation		[2]		
	DIP14 package		-	750	mW
	SO14, (T)SSOP14 and DHVQFN14 packages		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP14 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.For SO14 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.For (T)SSOP14 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.For DHVQFN14 packages:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC164			74HCT164			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC164</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5$ V	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0$ V	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0$ V	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5$ V	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0$ V	-	2.8	1.8	-	1.8	-	1.8	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = −20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = −20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = −20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = −4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

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V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = −4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8	-	80	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> − 2.1 V; I <sub>O</sub> = 0 A; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V	-	100	360	-	450	-	490	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND = 0 V;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ ; test circuit see [Figure 10](#); unless otherwise specified*

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC164</b>										
$t_{pd}$	propagation delay	CP to Qn; see <a href="#">Figure 7</a> [1]								
		$V_{CC} = 2.0 \text{ V}$	-	41	170	-	215	-	255	ns
		$V_{CC} = 4.5 \text{ V}$	-	15	34	-	43	-	51	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	12	-	-	-	-	-	ns
$t_{PHL}$	HIGH to LOW propagation delay	MR to Qn; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	-	39	140	-	175	-	210	ns
		$V_{CC} = 4.5 \text{ V}$	-	14	28	-	35	-	42	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	11	-	-	-	-	-	ns
$t_t$	transition time	see <a href="#">Figure 7</a> [2]								
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	16	-	19	ns
$t_w$	pulse width	CP HIGH or LOW; see <a href="#">Figure 7</a>								
		$V_{CC} = 2.0 \text{ V}$	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	4	-	17	-	20	-	ns
$t_{rec}$	recovery time	MR LOW; see <a href="#">Figure 8</a>								
		$V_{CC} = 2.0 \text{ V}$	60	17	-	75	-	90	-	ns
		$V_{CC} = 4.5 \text{ V}$	12	6	-	15	-	18	-	ns
		$V_{CC} = 6.0 \text{ V}$	10	5	-	13	-	15	-	ns
$t_{su}$	set-up time	DSA, and DSB to CP; see <a href="#">Figure 9</a>								
		$V_{CC} = 2.0 \text{ V}$	60	8	-	75	-	90	-	ns
		$V_{CC} = 4.5 \text{ V}$	12	3	-	15	-	18	-	ns
		$V_{CC} = 6.0 \text{ V}$	10	2	-	13	-	15	-	ns
$t_h$	hold time	DSA, and DSB to CP; see <a href="#">Figure 9</a>								
		$V_{CC} = 2.0 \text{ V}$	+4	-6	-	4	-	4	-	ns
		$V_{CC} = 4.5 \text{ V}$	+4	-2	-	4	-	4	-	ns
		$V_{CC} = 6.0 \text{ V}$	+4	-2	-	4	-	4	-	ns

**Table 7. Dynamic characteristics ...continued**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; test circuit see [Figure 10](#); unless otherwise specified

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
$f_{max}$	maximum frequency	for $C_p$ , see <a href="#">Figure 7</a>									
			$V_{CC} = 2.0$ V	6	23	-	5	-	4	-	MHz
			$V_{CC} = 4.5$ V	30	71	-	24	-	20	-	MHz
			$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	78	-	-	-	-	-	MHz
$C_{PD}$	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC}$	[3]	-	40	-	-	-	-	-	pF
<b>74HCT164</b>											
$t_{pd}$	propagation delay	CP to $Q_n$ ; see <a href="#">Figure 7</a>	[1]								
		$V_{CC} = 4.5$ V	-	17	36	-	45	-	54	ns	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	14	-	-	-	-	-	ns	
$t_{PHL}$	HIGH to LOW propagation delay	MR to $Q_n$ ; see <a href="#">Figure 8</a>									
		$V_{CC} = 4.5$ V	-	19	38	-	48	-	57	ns	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	16	-	-	-	-	-	ns	
$t_t$	transition time	see <a href="#">Figure 7</a>	[2]								
			$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
$t_w$	pulse width	CP HIGH or LOW; see <a href="#">Figure 7</a>									
		$V_{CC} = 4.5$ V	18	7	-	23	-	27	-	ns	
		MR LOW; see <a href="#">Figure 8</a>									
$t_{rec}$	recovery time	MR to CP; see <a href="#">Figure 8</a>									
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns	
$t_{su}$	set-up time	DSA, and DSB to CP; see <a href="#">Figure 9</a>									
		$V_{CC} = 4.5$ V	12	6	-	15	-	18	-	ns	
$t_h$	hold time	DSA, and DSB to CP; see <a href="#">Figure 9</a>									
		$V_{CC} = 4.5$ V	+4	-2	-	4	-	4	-	ns	
$f_{max}$	maximum frequency	for $C_p$ , see <a href="#">Figure 7</a>									
			$V_{CC} = 4.5$ V	27	55	-	22	-	18	-	MHz
			$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	61	-	-	-	-	-	MHz

**Table 7. Dynamic characteristics ...continued**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; test circuit see [Figure 10](#); unless otherwise specified

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$C_{PD}$	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC} - 1.5$ V	[3]	-	40	-	-	-	-	pF

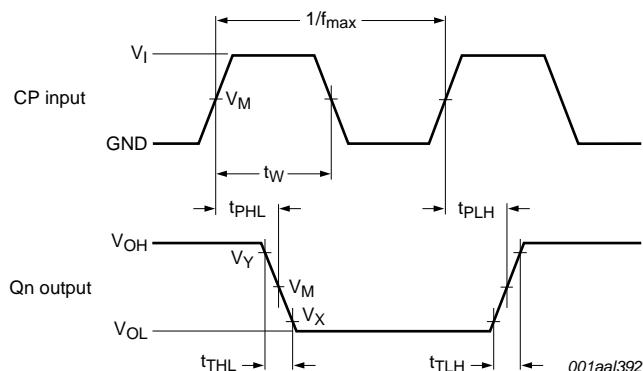
[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

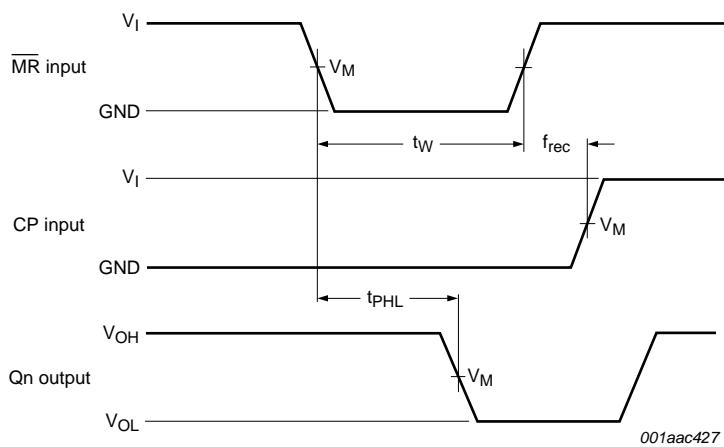
 $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = output load capacitance in pF; $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$$

(1) Measurement points are given in [Table 8](#). $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.**Fig 7. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency****Table 8. Measurement points**

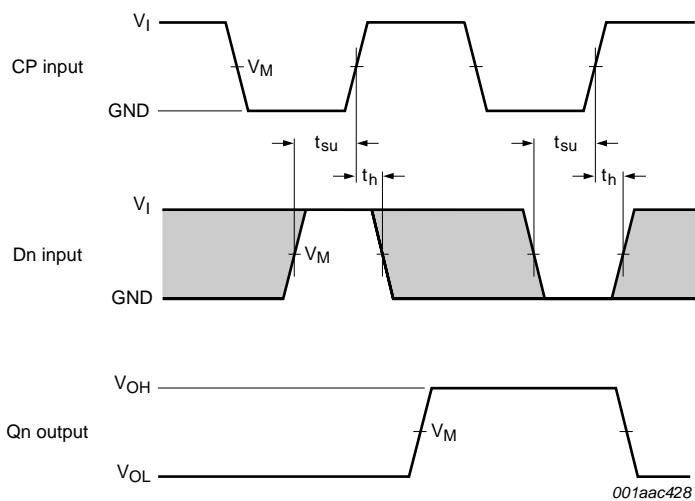
Type	Input	Output		
		$V_M$	$V_X$	$V_Y$
74HC164	0.5 $V_{CC}$	0.5 $V_{CC}$	0.1 $V_{CC}$	0.9 $V_{CC}$
74HCT164	1.3 V	1.3 V	0.1 $V_{CC}$	0.9 $V_{CC}$



(1) Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 8. Waveforms showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CP) removal time**

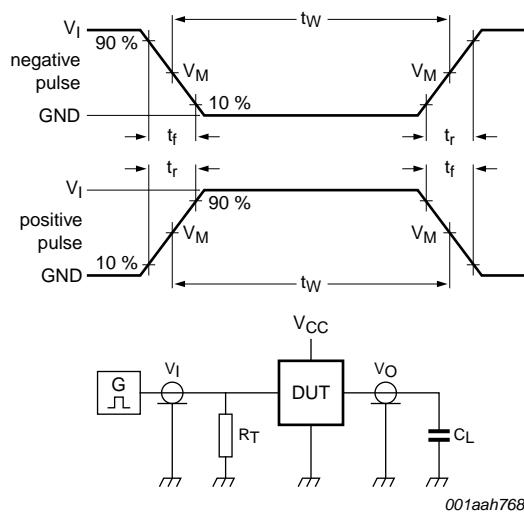


(1) Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 9. Waveforms showing the data set-up and hold times for Dn inputs**



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig 10. Test circuit for measuring switching times**

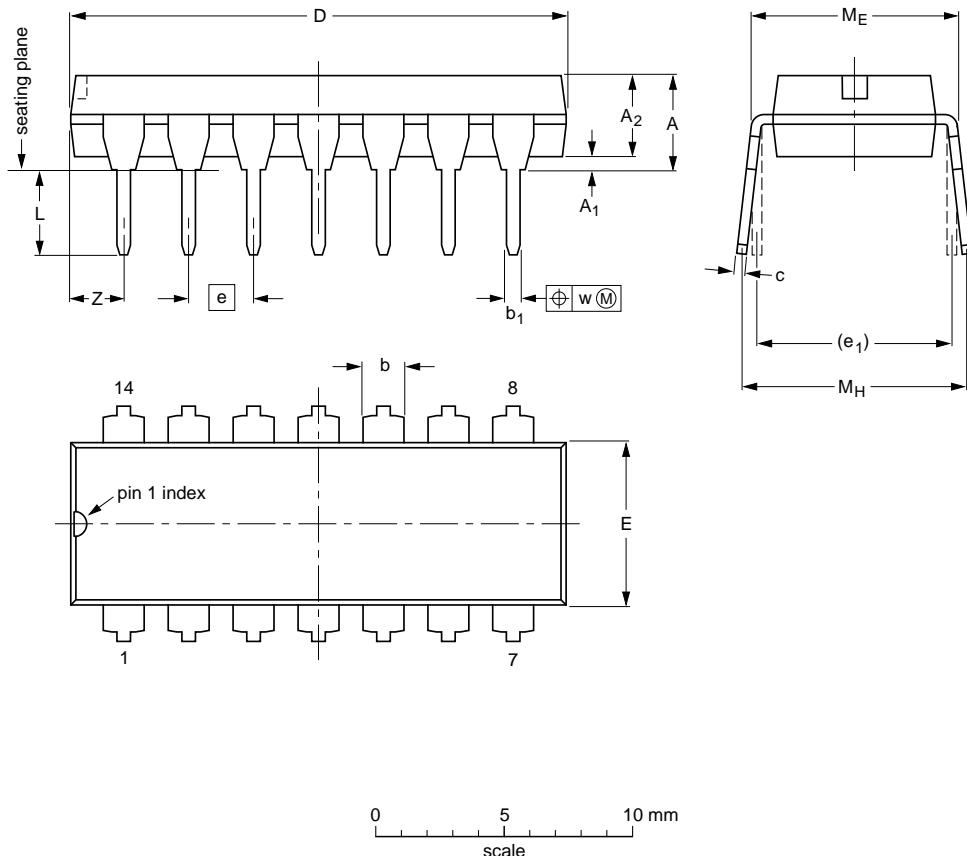
**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$		
74HC164	$V_{CC}$	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74HCT164	3.0 V	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

## 11. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

### Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			99-12-27 03-02-13

Fig 11. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

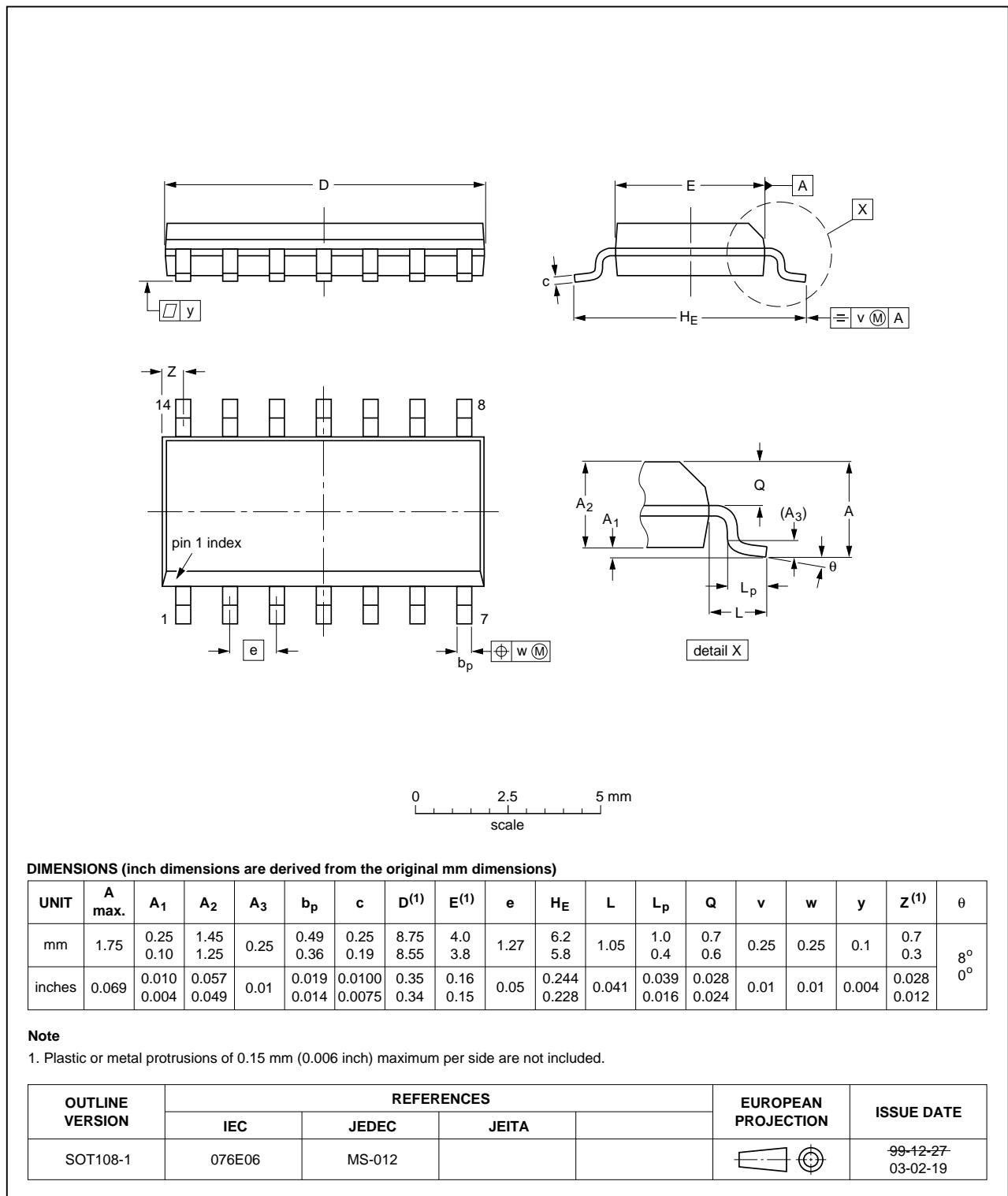


Fig 12. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

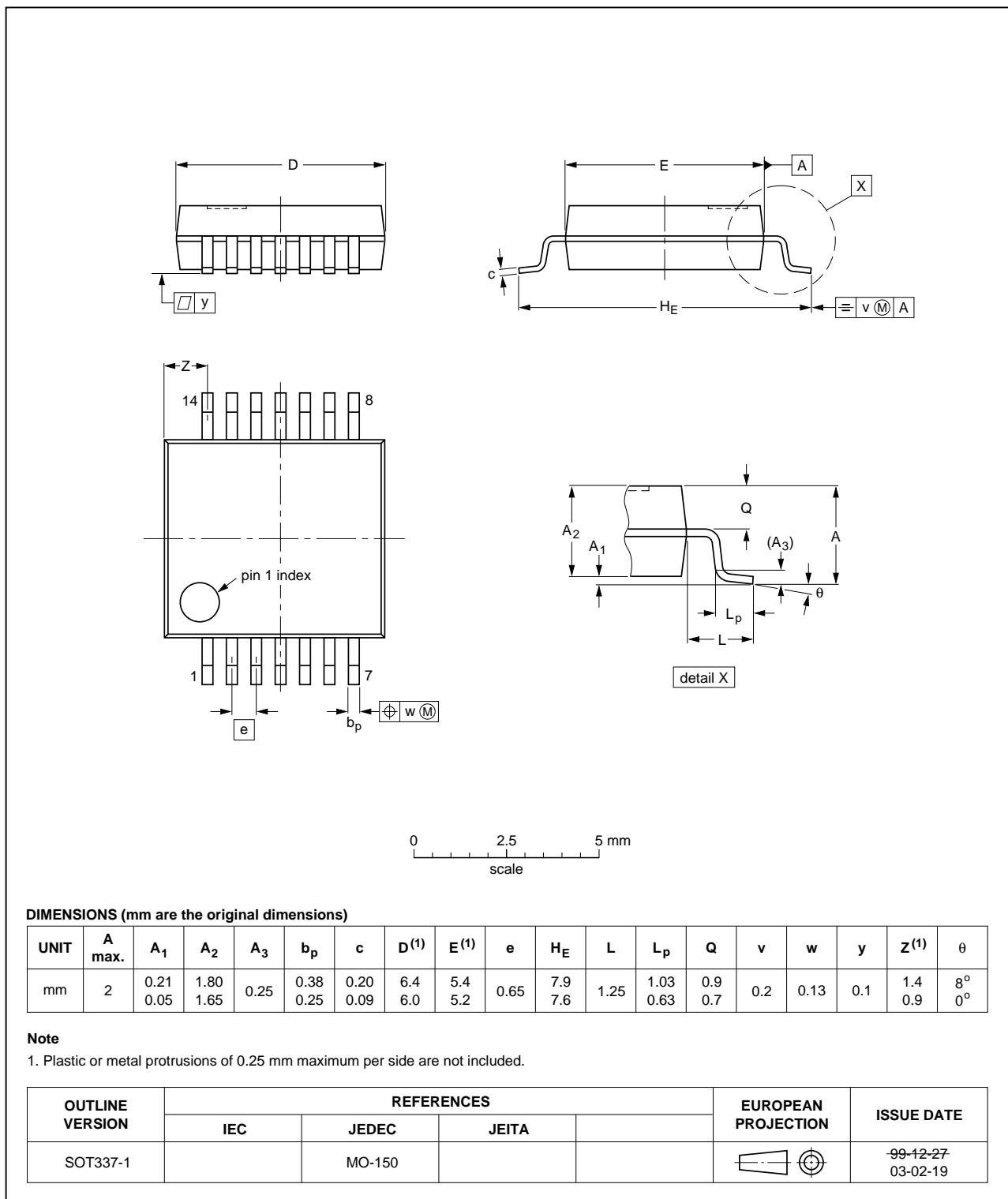


Fig 13. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

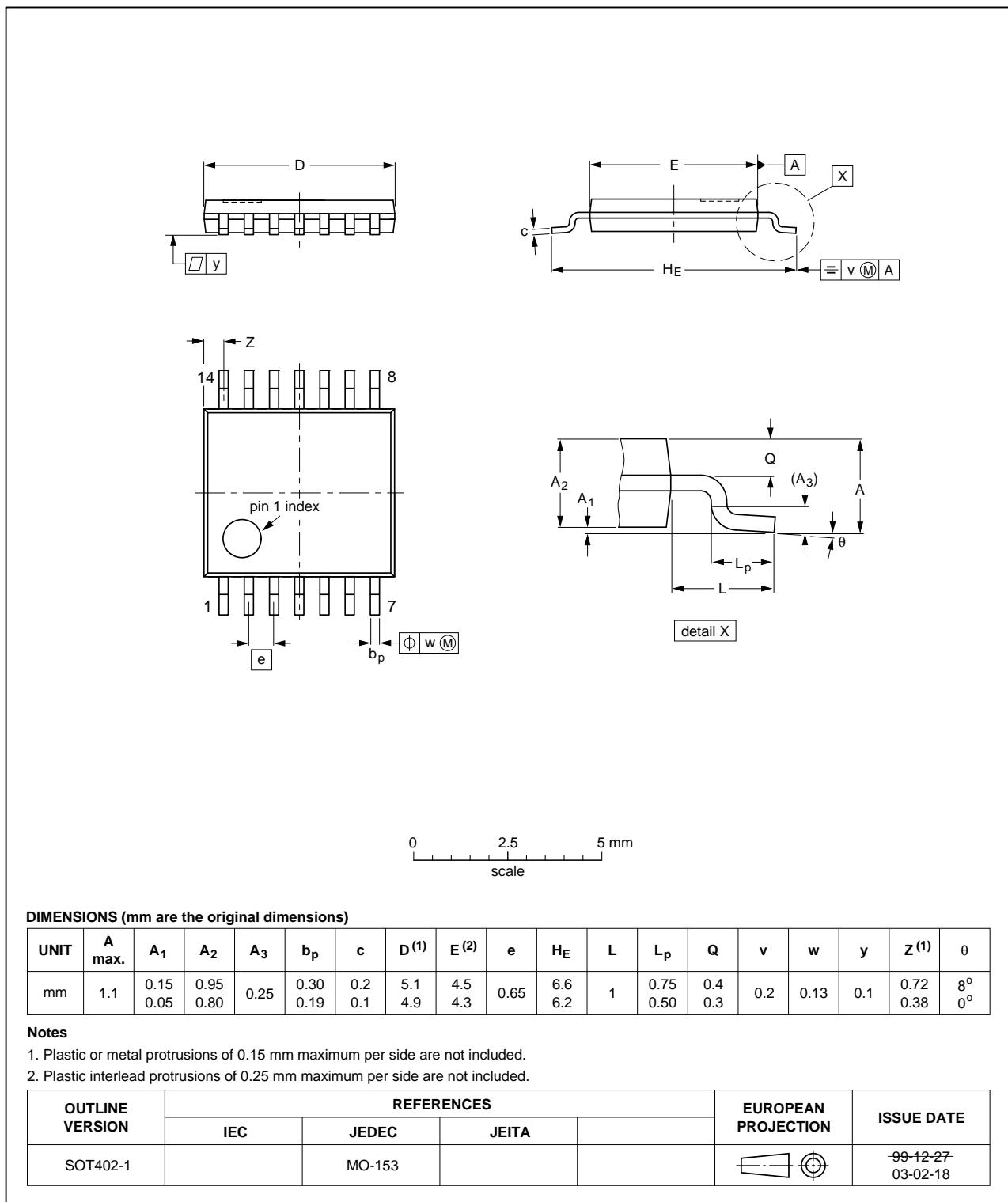


Fig 14. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

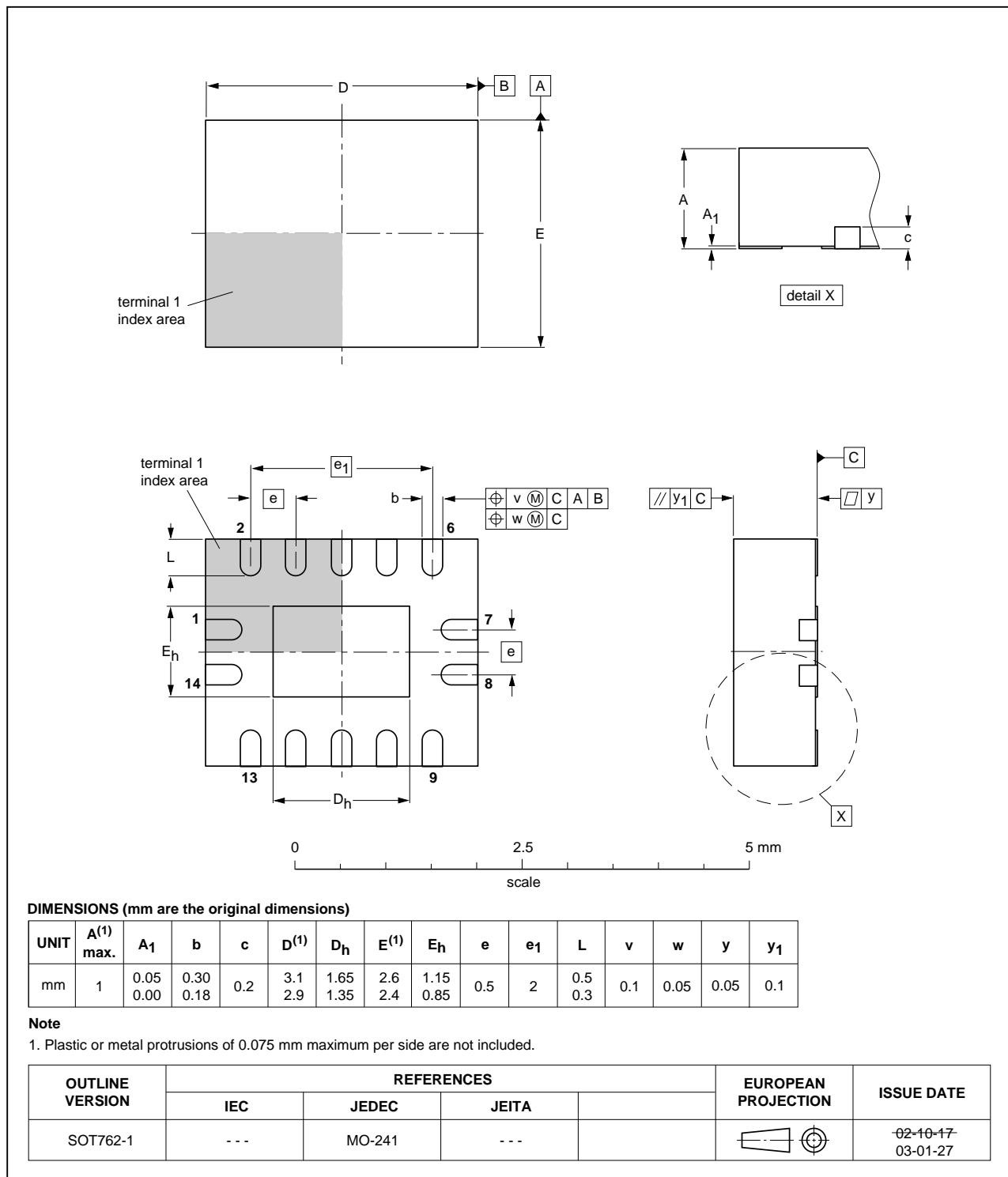


Fig 15. Package outline SOT762-1 (DHVQFN14)

## 12. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT164 v.7	20130613	Product data sheet	-	74HC_HCT164 v.6
Modifications:		• General description updated.		
74HC_HCT164 v.6	20111212	Product data sheet	-	74HC_HCT164 v.5
Modifications:		• Legal pages updated.		
74HC_HCT164 v.5	20101125	Product data sheet	-	74HC_HCT164 v.4
74HC_HCT164 v.4	20100202	Product data sheet	-	74HC_HCT164 v.3
74HC_HCT164 v.3	20050404	Product data sheet	-	74HC_HCT164_CNV v.2
74HC_HCT164_CNV v.2	19901201	Product specification	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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