



2.5V CMOS Static RAM 1 Meg (64K x 16-Bit)

IDT71T016SA

Features

- ◆ 64K x 16 advanced high-speed CMOS Static RAM
- ◆ Equal access and cycle times
 - Commercial: 10/12/15/20ns
 - Industrial: 12/15/20ns
- ◆ One Chip Select plus one Output Enable pin
- ◆ Bidirectional data inputs and outputs directly LVTTTL-compatible
- ◆ Low power consumption via chip deselect
- ◆ Upper and Lower Byte Enable Pins
- ◆ Single 2.5V power supply
- ◆ Available in 44-pin Plastic SOJ, 44-pin TSOP, and 48-Ball Plastic FBGA packages

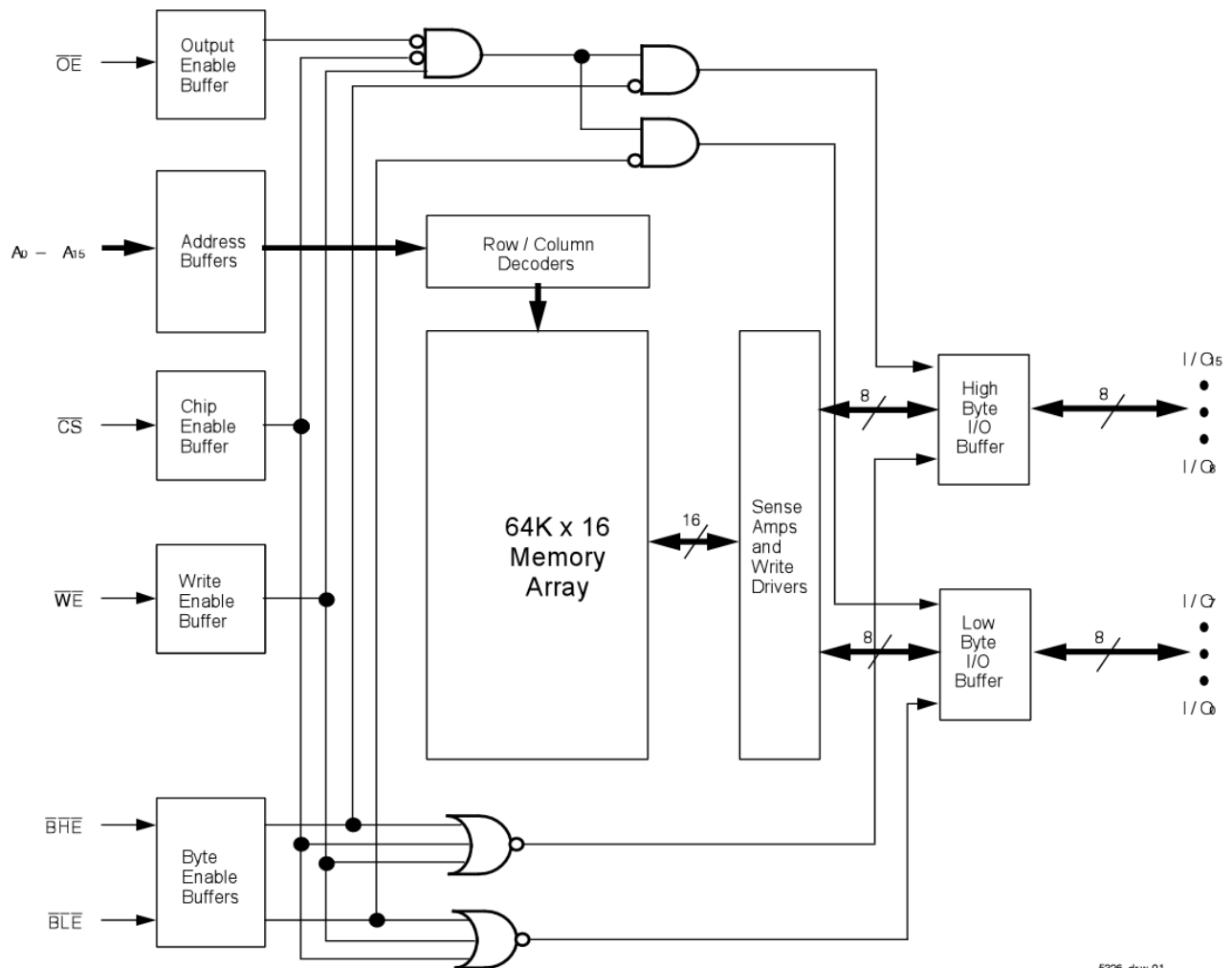
Description

The IDT71T016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71T016 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71T016 are LVTTTL-compatible and operation is from a single 2.5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71T016 is packaged in a JEDEC standard a 44-pin Plastic SOJ, 44-pin TSOP Type II, and a 48-ball plastic 7 x 7 mm FBGA.

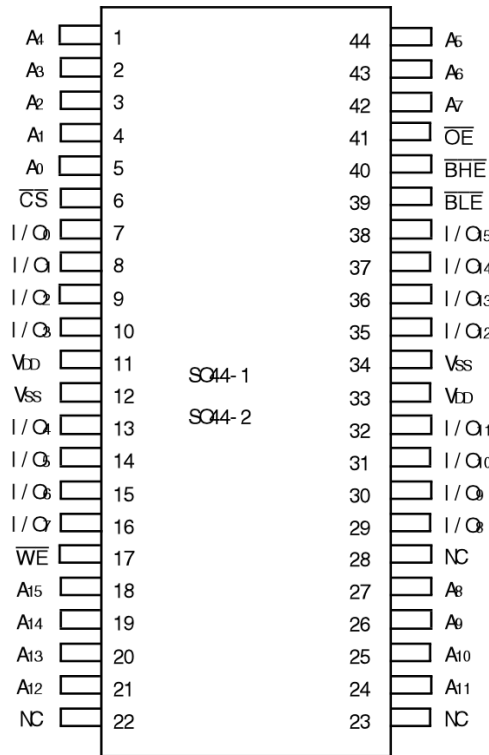
Functional Block Diagram



5326 drw 01

JULY 2008

Pin Configurations



5326 drw 02



5326 tbl 02a

Pin Description

A0 – A15	Address Inputs	Input
$\overline{CS}$	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
$\overline{BHE}$	High Byte Enable	Input
$\overline{BLE}$	Low Byte Enable	Input
I/O0 – I/O15	Data Input/Output	I/O
VDD	2.5V Power	Power
VSS	Ground	Gnd

5326 tbl 01

Truth Table⁽¹⁾

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O0-I/O7	I/O8-I/O15	Function
H	X	X	X	X	High-Z	High-Z	Deselected – Standby
L	L	H	L	H	DATA _{OUT}	High-Z	Low Byte Read
L	L	H	H	L	High-Z	DATA _{OUT}	High Byte Read
L	L	H	L	L	DATA _{OUT}	DATA _{OUT}	Word Read
L	X	L	L	L	DATA _{IN}	DATA _{IN}	Word Write
L	X	L	L	H	DATA _{IN}	High-Z	Low Byte Write
L	X	L	H	L	High-Z	DATA _{IN}	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

5326 tbl 02

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't care.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Value	Unit
V _{DD}	Supply Voltage Relative to V _{SS}	-0.3 to +3.6	V
V _{IN} , V _{OUT}	Terminal Voltage Relative to V _{SS}	-0.3 to V _{DD} +0.3	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	1.25	W
I _{OUT}	DC Output Current	50	mA

NOTE:

5326 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	6	pF
C _{IO}	I/O Capacitance	V _{OUT} = 3dV	7	pF

NOTE:

5326 tbl 06

- This parameter is guaranteed by device characterization, but not production tested.

DC Electrical Characteristics

(V_{DD} = Min. to Max., Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Condition	IDT71T016SA		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current	V _{DD} = Max., V _{IN} = V _{SS} to V _{DD}	—	5	μA
I _{LO}	Output Leakage Current	V _{DD} = Max., $\overline{CS}$ = V _{IH} , V _{OUT} = V _{SS} to V _{DD}	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = 2.0mA, V _{DD} = Min.	—	0.7	V
V _{OH}	Output High Voltage	I _{OH} = 2.0mA, V _{DD} = Min.	1.7	—	V

DC Electrical Characteristics^(1,2)

(V_{DD} = Min. to Max., V_{LC} = 0.2V, V_{HC} = V_{DD} - 0.2V)

Symbol	Parameter	71T016SA10		71T016SA12		71T016SA15		71T016SA20		Unit
		Com'l	Ind	Com'l	Ind	Com'l	Ind	Com'l	Ind	
I _{CC}	Dynamic Operating Current $\overline{CS} \leq V_{LC}$, Outputs Open, V _{DD} = Max., f = f _{MAX} ⁽³⁾	Max.	160	150	160	130	130	120	120	mA
		Typ. ⁽⁴⁾	90	85	—	80	—	80	—	
I _{SB}	Dynamic Standby Power Supply Current $\overline{CS} \geq V_{HC}$, Outputs Open, V _{DD} = Max., f = f _{MAX} ⁽³⁾	45	40	45	35	35	30	30	30	mA
I _{SB1}	Full Standby Power Supply Current (static) $\overline{CS} \geq V_{HC}$, Outputs Open, V _{DD} = Max., f = 0 ⁽³⁾	10	15	15	15	15	15	15	15	mA

NOTES:

- All values are maximum guaranteed values.
- All inputs switch between 0.2V (Low) and V_{DD} - 0.2V (High).
- f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
- Typical values are measured at 2.5V, 25°C and with equal read and write cycles. This parameter is guaranteed by device characterization but is not production tested.

5326 tbl 8

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	V _{SS}	V _{DD}
Commercial	0°C to +70°C	0V	See Below
Industrial	-40°C to +85°C	0V	See Below

5326 tbl 04

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	2.375	2.5	2.625	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	1.7	—	V _{DD} +0.3 ⁽¹⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽²⁾	—	0.7	V

NOTES:

5326 tbl 05

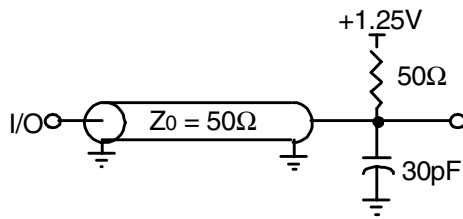
- V_{IH} (max) = V_{DD} + 1.0V a.c. (pulse width less than tc_{yc}/2) for I ≤ 20 mA, once per cycle.
- V_{IL} (min) = -1.0V a.c. (pulse width less than tc_{yc}/2) for I ≤ 20 mA, once per cycle.

AC Test Conditions

Input Pulse Levels	0V to 2.5V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	(V _{DD} /2)
Output Reference Levels	(V _{DD} /2)
AC Test Load	See Figure 1, 2 and 3

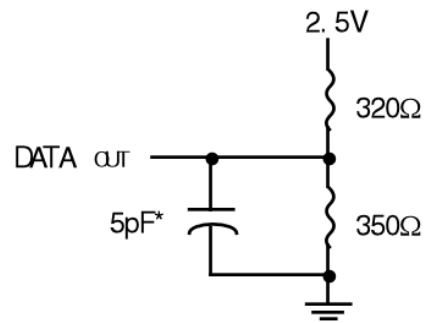
5326 tbl 09

AC Test Loads



5326 drw 03

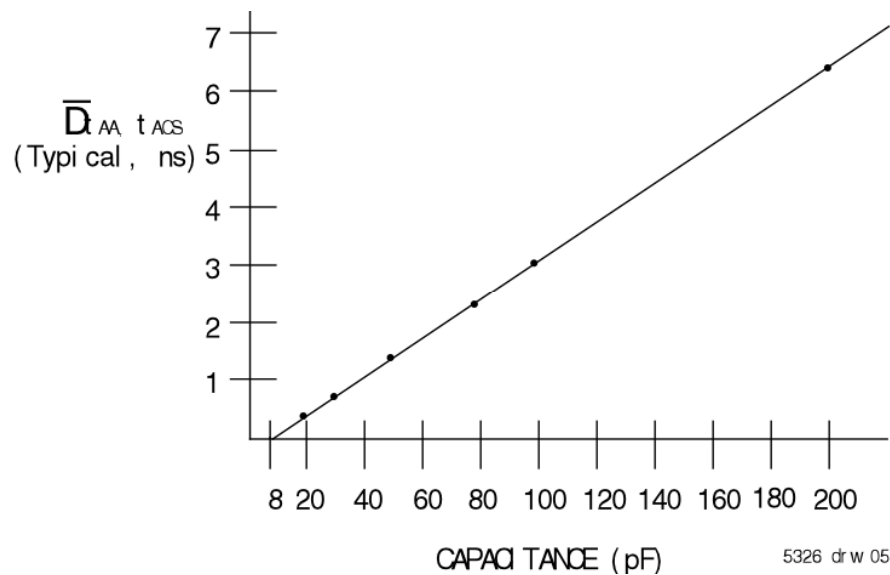
Figure 1. AC Test Load



5326 drw 04

*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})



5326 drw 05

Figure 3. Output Capacitive Derating

AC Electrical Characteristics (V_{DD} = Min. to Max., Commercial and Industrial Temperature Ranges)

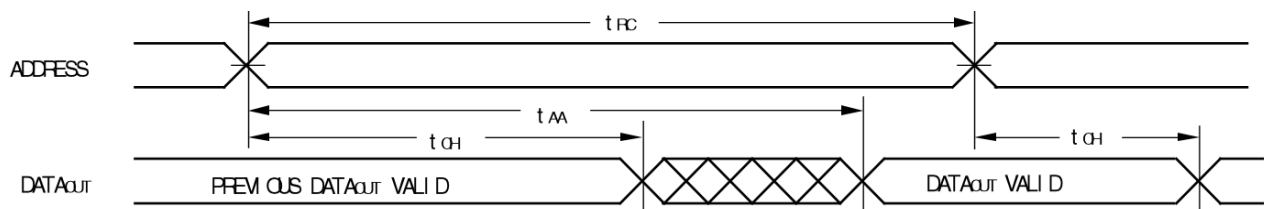
Symbol	Parameter	71T016SA10 ⁽²⁾		71T016SA12		71T016SA15		71T016SA20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t _{AA}	Address Access Time	—	10	—	12	—	15	—	20	ns
t _{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	20	ns
t _{CLZ} ⁽¹⁾	Chip Select Low to Output in Low-Z	4	—	4	—	5	—	5	—	ns
t _{CHZ} ⁽¹⁾	Chip Select High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t _{OE}	Output Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t _{OLZ} ⁽¹⁾	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t _{OHZ} ⁽¹⁾	Output Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
t _{OH}	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
t _{BE}	Byte Enable Low to Output Valid	—	5	—	6	—	7	—	8	ns
t _{BLZ} ⁽¹⁾	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t _{BHZ} ⁽¹⁾	Byte Enable High to Output in High-Z	—	5	—	6	—	6	—	8	ns
WRITE CYCLE										
t _{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t _{AW}	Address Valid to End of Write	7	—	8	—	10	—	12	—	ns
t _{CW}	Chip Select Low to End of Write	7	—	8	—	10	—	12	—	ns
t _{BW}	Byte Enable Low to End of Write	7	—	8	—	10	—	12	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t _{WR}	Address Hold from End of Write	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	7	—	8	—	10	—	12	—	ns
t _{DW}	Data Valid to End of Write	5	—	6	—	7	—	9	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t _{OW} ⁽¹⁾	Write Enable High to Output in Low-Z	3	—	3	—	3	—	3	—	ns
t _{WHZ} ⁽¹⁾	Write Enable Low to Output in High-Z	—	5	—	6	—	6	—	8	ns

NOTES:

5326 tbl 10

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. 0°C to +70°C temperature range only.

Timing Waveform of Read Cycle No. 1^(1,2,3)

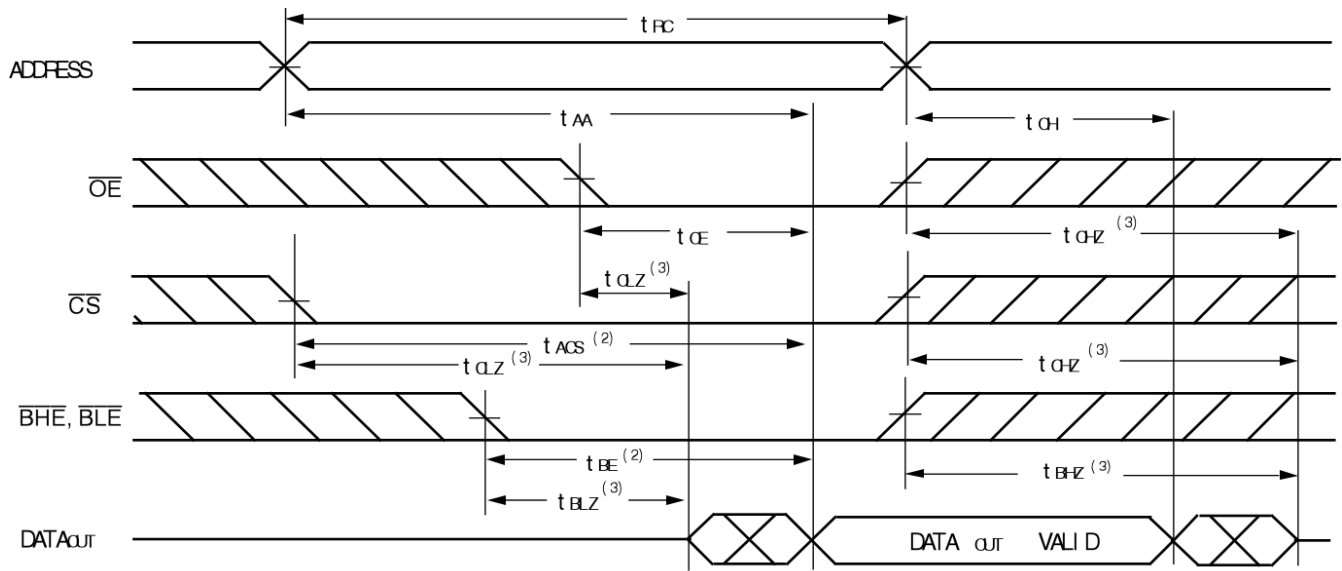


NOTES:

5326 dr w 06

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ are LOW.

Timing Waveform of Read Cycle No. 2⁽¹⁾

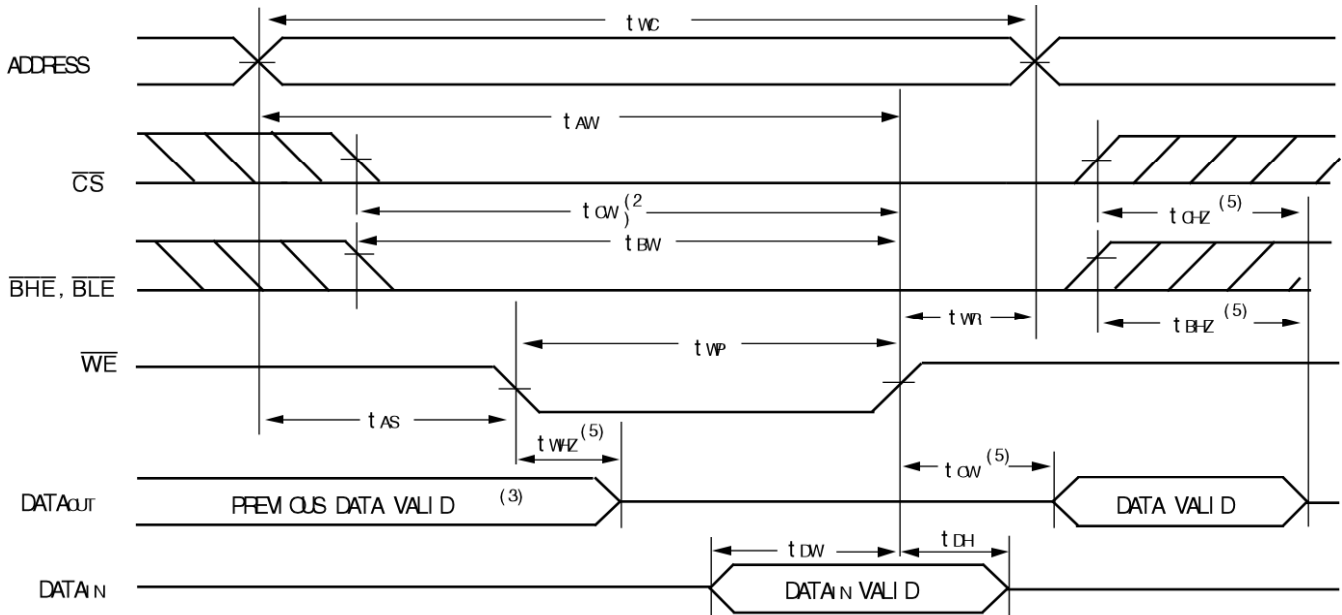


5326 drw 07

NOTES:

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of $\overline{CS}$, $\overline{BHE}$, or $\overline{BLE}$ transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)^(1,2,4)

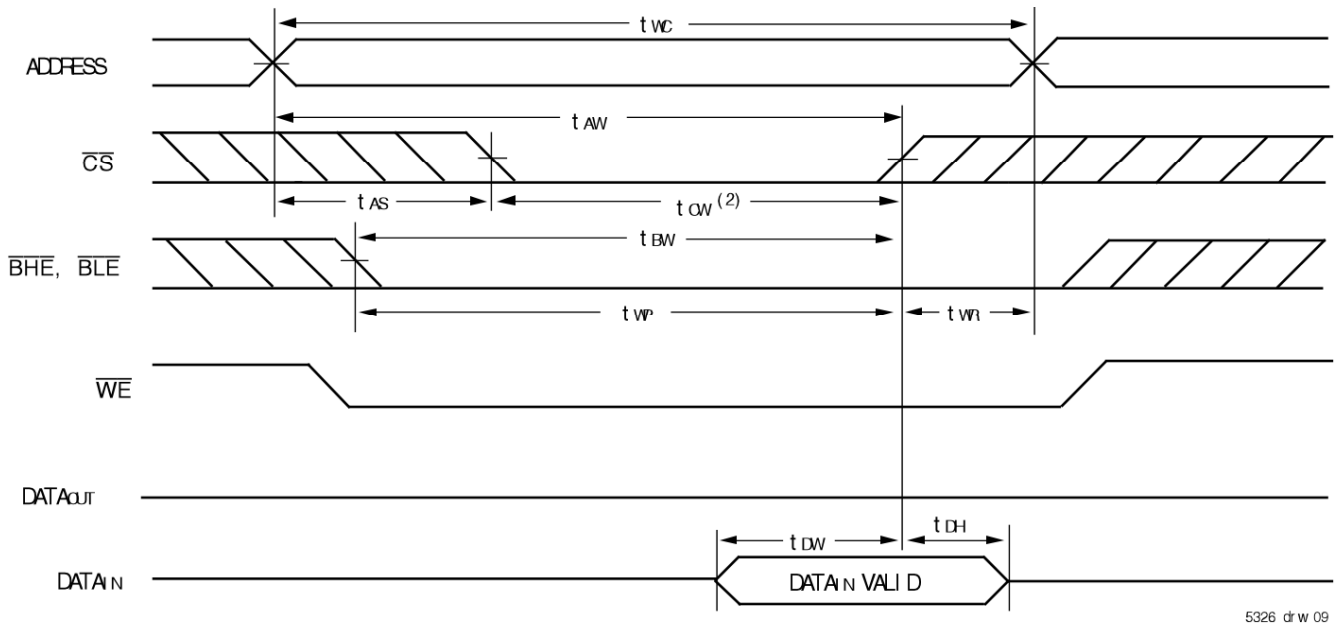


5326 drw 08

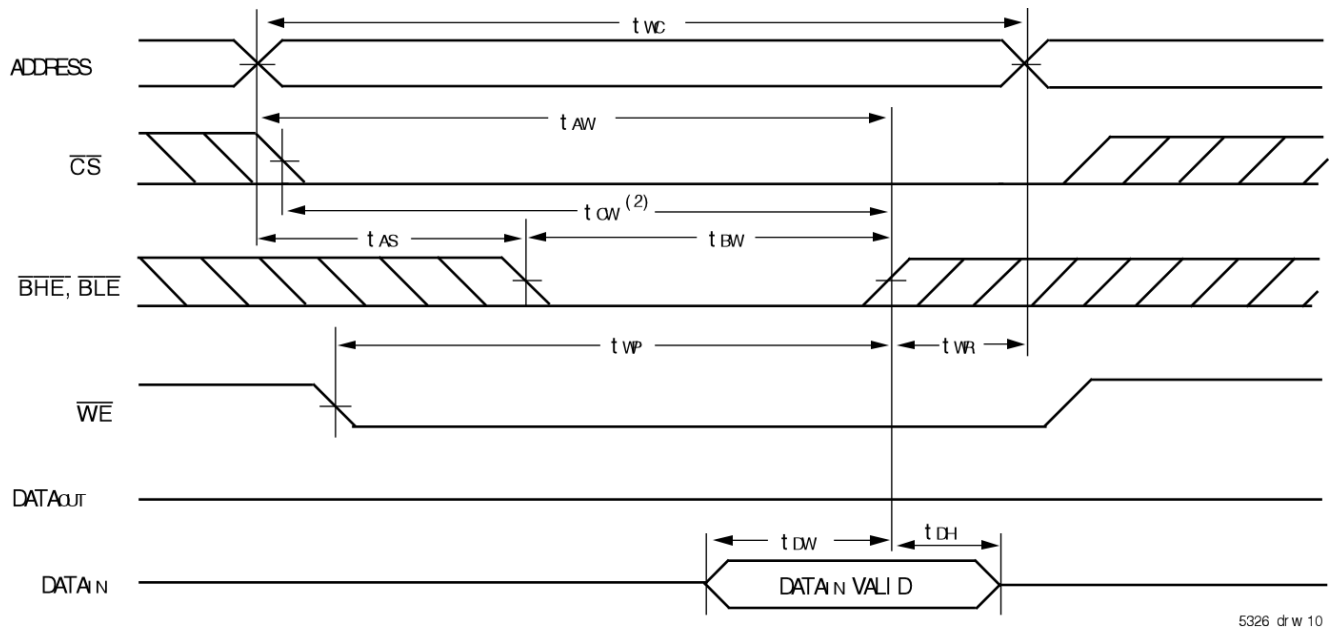
NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WZ} + t_{OW} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled Timing)^(1,4)



Timing Waveform of Write Cycle No. 3 ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ Controlled Timing)^(1,4)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{\text{CS}}$, LOW $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$, and a LOW $\overline{\text{WE}}$.
2. $\overline{\text{OE}}$ is continuously HIGH. If during a $\overline{\text{WE}}$ controlled write cycle $\overline{\text{OE}}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{OW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{\text{OE}}$ is HIGH during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{\text{CS}}$ LOW or $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ LOW transition occurs simultaneously with or after the $\overline{\text{WE}}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

[illegible]

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Datasheet Document History

<u>Rev</u>	<u>Date</u>	<u>Page</u>	<u>Description</u>
0	08/23/01		Created new datasheet
1	04/16/04	p. 1-8 p. 3	Updated datasheet to full release version. Updated overshoot and undershoot specifications and typical DC electrical characteristics.
2	07/14/08	p. 1,2,6,7	Corrected pin labels output enable, chip select, write enable, high and low byte enables to be $\overline{OE}$, $\overline{CS}$, $\overline{WE}$, $\overline{BHE}$, $\overline{BLE}$ to reflect active low nature.



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