



Single chip 802.11b/g WLAN radio

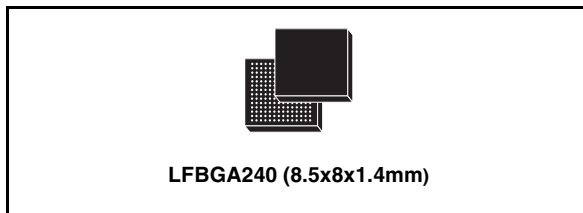
Data Brief

Features

- Extremely small footprint
- Ultra low power consumption
- Fully compliant with the IEEE 802.11b and 802.11g WLAN standards
- Support for 54, 48, 36, 24, 18, 12, 9, and 6 Mbit/s OFDM, 11 and 5.5 Mbit/s CCK and legacy 2 and 1 Mbit/s data rates
- Single chip 802.11b/g WLAN solution with fully integrated:
 - zero IF (ZIF) transceiver
 - voltage controlled oscillator (VCO)
 - high-speed A/D and D/A converters
 - OFDM and CCK baseband processor
 - ARM9 media access controller (MAC)
 - Mode selectable SPI or SDIO host interface (up to 48 Mbps)
 - passive components integration
 - PA bias control
 - flexible integrated power management unit
 - glueless FEM interface
- Intelligent power control, including 802.11 power save mode
- Fully integrated Bluetooth coexistence

Applications

- Cellular phones
- Personal digital assistants (PDA)
- Portable computers
- Hand-held data transfer devices
- Cameras
- Computer peripherals
- Cable replacement



Description

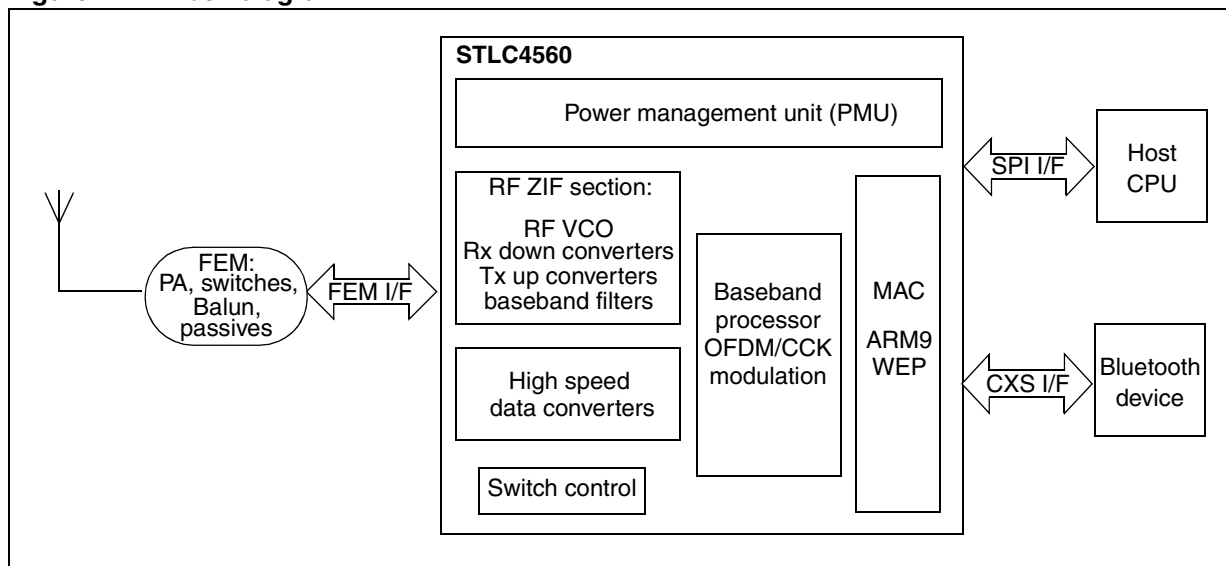
The STLC4560 is a single chip 802.11b/g WLAN radio for embedded, low-power and very small form factor mobile applications. The product conforms to the IEEE 802.11b and 802.11g protocols operating in the 2.45 GHz ISM frequency band supporting OFDM data rates of 54, 48, 36, 24, 18, 12, 9, and 6 Mbit/s as well as CCK data rates of 11 and 5.5 Mbit/s and legacy data rates of 2 and 1 Mbit/s.

The STLC4560 is a fully integrated wireless radio including a ZIF transceiver, RF Synthesizer/VCO, high-speed data converters, an OFDM/CCK digital baseband processor, an ARM9-based MAC and a complete power management unit with integrated PA bias control. In addition some passive components are integrated further reducing the overall reference design cost and size. An external FEM completes a highly integrated chip set solution.

Host control is provided by a flexible SPI or SDIO serial interface. The SPI interface supports a maximum clock rate of 48 MHz whereas the 4-bit SDIO supports a maximum clock rate of 25 MHz. For maximum flexibility, the STLC4560 accepts system reference clock frequencies of 19.2, 26, 38.4 and 40 MHz. A reference design evaluation platform of hardware and software is provided to system integrators to rapidly enable wireless connectivity to mobile platforms.

1 Block diagram

Figure 1. Block diagram



2 Electrical characteristics

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V _{CC}	PMU VBATT		-0.3	-	7.0	V
	Voltage on any other pin	Within shared voltage rails	-0.3	-	V _{CC} + 0.3	V
	V _{CC} to V _{CC}		-0.3	-	+0.3	V
	Any GND to GND		-0.3	-	+0.3	V

Table 2. Operating conditions and input power specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T _{OP}	Operating temperature range		-30		85	°C
VBATT supply	Input supply voltage	Power management unit VBATT supply input	3.0	3.6	5.5	V
	Average standby mode current	VBATT = 3.6 V		10		μA
VDIG	Input supply voltage	SWx (x={1, 2, 3, 4}) supply input	1.7		VBATT	V

Table 2. Operating conditions and input power specifications (continued)

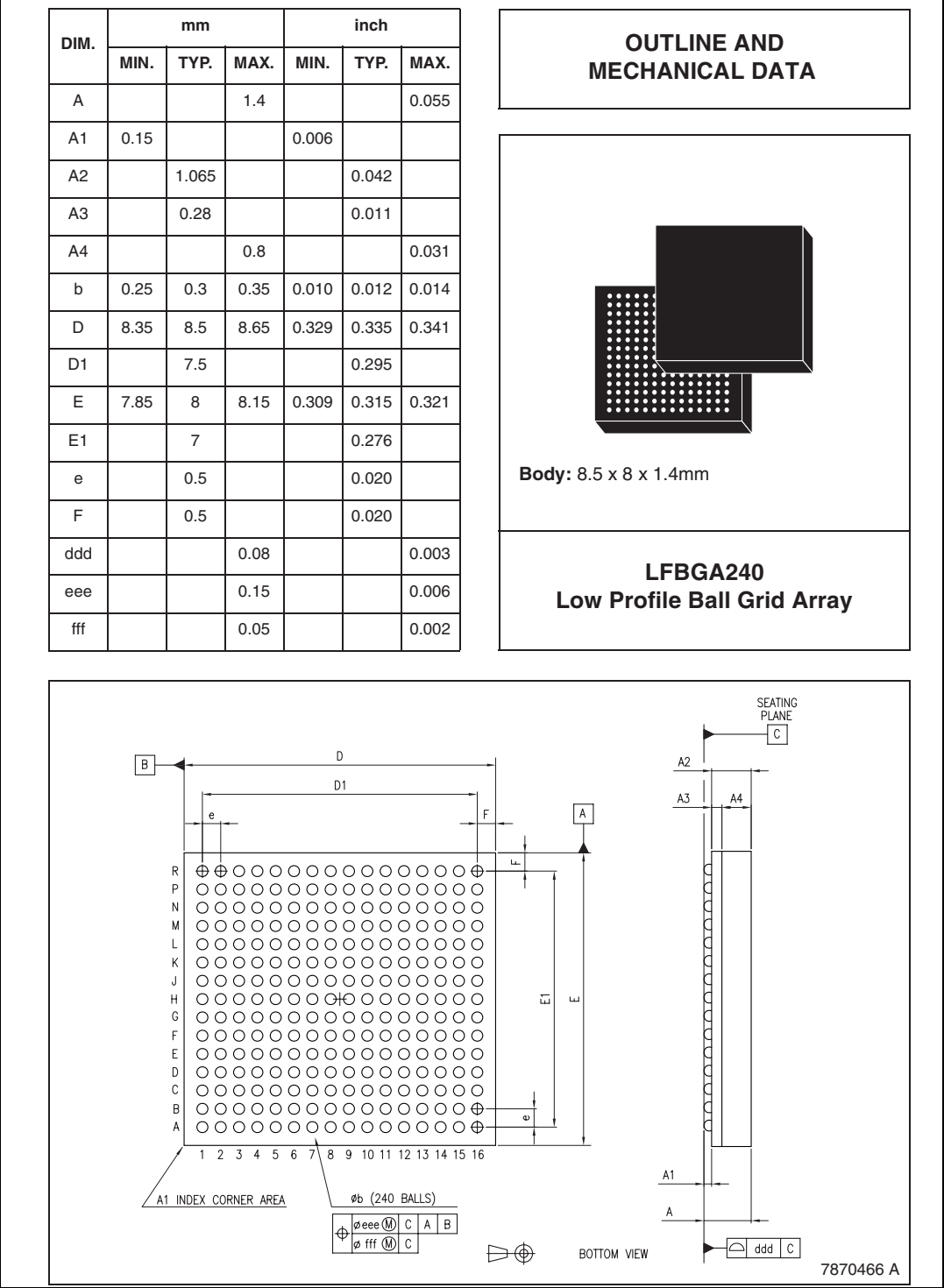
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power consumption						
VBATT	Input supply voltage	Power management unit VBATT supply input	3.0	3.6	5.5	V
	Standby current	25 °C, POWER_UP = 0V. The resulting current is mainly leakage		10		μA
	Sleep mode current	25 °C, POWERUP = 1.86 V. The radio is operating on the sleep clock at 32.768 kHz. Sleep mode is a subset of PSM.		120		μA
	Power save mode current	25 °C, 100 ms Beacon period, 75 byte Beacons @ 1 Mbit/s, short preamble, DTIM = 6		610		μA
	Receive or Idle current	25 °C, the radio is always on, receiving beacons, no TX		195		mA
	PSM Receive current	25 °C, PSM, receiving packets at 1.9Mbit/s at the application layer		76		mA
	Transmit current	25 °C, the radio is always on, transmitting 1.9Mbit/s at the application layer		199		mA
	PSM Transmit current	25 °C, PSM, transmitting 1.9Mbit/s at the application layer		49		mA
Supply						
VIO	Input supply voltage	VIO input supply determines host CMOS logic levels for: SPI_CSX, SPI_CLK, SPI_DIN, SPI_DOUT, HOST_IRQ, LF_XTAL_IN, FREQ, RF_ACTIVE, STATUS, TX_CONF	1.62	1.86	1.98	V
	Input supply current	VIO = 1.86 V		0.5	6	mA

3 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 2. LFBGA240 mechanical data and package dimensions



4 Ordering information

Table 3. Ordering information

Order codes	Operating temperature range	Package	Packing
STLC4560TRAY	-30°C to 85°C	LFBGA240- (8.5x8x1.4mm)	Tray
STLC4560	-30°C to 85°C	LFBGA240- (8.5x8x1.4mm)	Tape and reel

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
09-Jan-2008	1	Initial release.

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