



256K x 8 Static RAM

Features

- **Low voltage range:**
— 2.7–3.6V
- **Ultra-low active power**
- **Low standby power**
- **Easy memory expansion with \overline{CS}_1/CS_2 and \overline{OE} features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

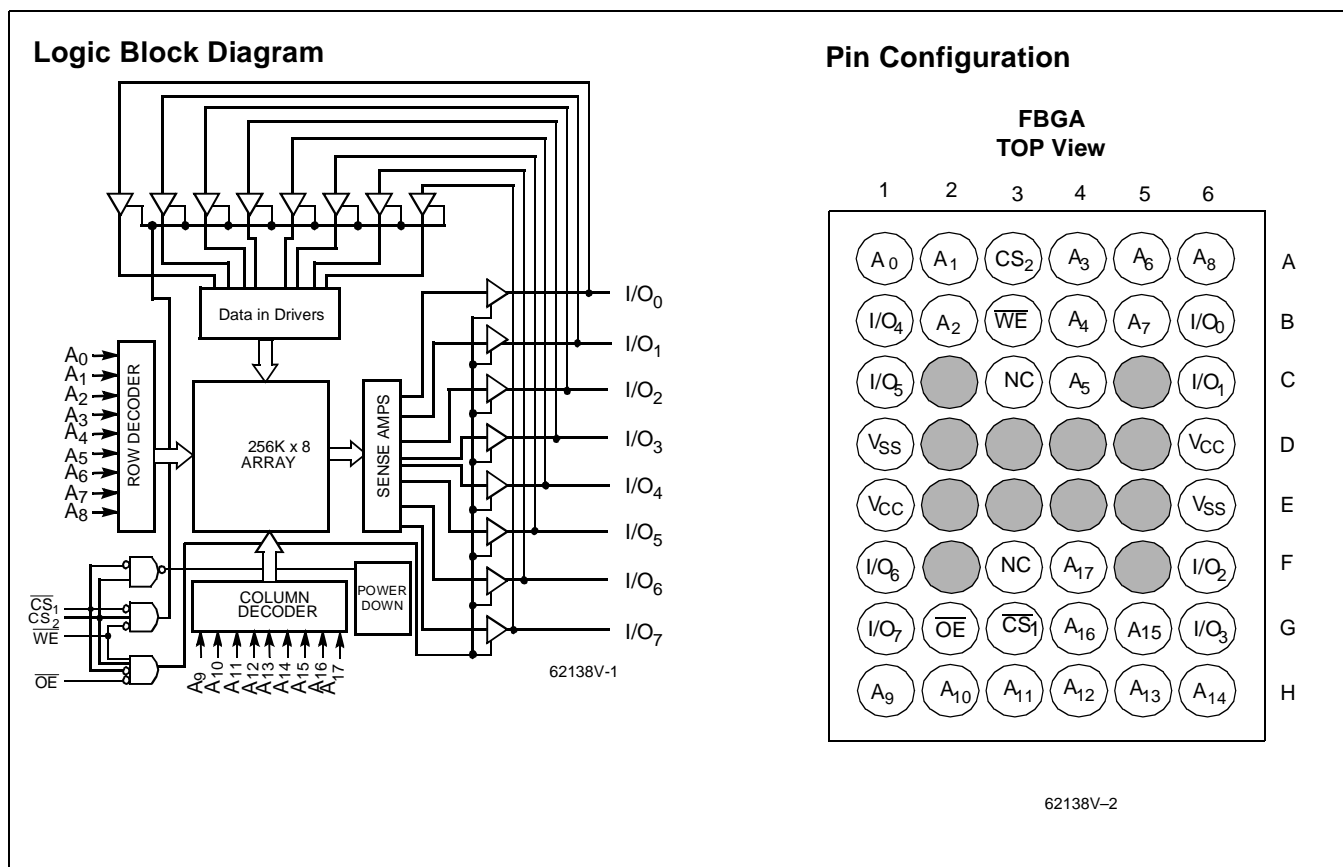
The CY62138V is a high-performance CMOS static RAM organized as 262,144 words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. The device can be put into standby mode when deselected (\overline{CS}_1 HIGH or CS_2 LOW).

Writing to the device is accomplished by taking Chip Enable One (\overline{CS}_1) and Write Enable (\overline{WE}) inputs LOW and Chip Enable Two (CS_2) HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable One (\overline{CS}_1) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) and Chip Enable Two (CS_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CS}_1 HIGH or CS_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CS}_1 LOW, CS_2 HIGH, and \overline{WE} LOW).

The CY62138V is available in a 36-ball FBGA.



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +4.6V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

| Device | Range | Ambient Temperature | V_{CC} |
|----------|------------|---------------------|--------------|
| CY62138V | Industrial | -40°C to +85°C | 2.7V to 3.6V |

Product Portfolio

| Product | V_{CC} Range | | | Speed | Power Dissipation (Industrial) | | | |
|----------|----------------|---------------------|---------------|-------|--------------------------------|---------|-----------------------|------------|
| | | | | | Operating (I_{CC}) | | Standby (I_{SB2}) | |
| | $V_{CC(min)}$ | $V_{CC(typ)}^{[2]}$ | $V_{CC(max)}$ | | Typ. ^[2] | Maximum | Typ. ^[2] | Maximum |
| CY62138V | 2.7V | 3.0V | 3.6V | 70 ns | 7 mA | 15 mA | 1 μ A | 15 μ A |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | CY62138V | | | Unit |
|------------------|---|---|------------------------|----------|---------------------|------------------------|------|
| | | | | Min. | Typ. ^[2] | Max. | |
| V _{OH} | Output HIGH Voltage | I _{OH} = −1.0 mA | V _{CC} = 2.7V | 2.4 | | | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 2.1 mA | V _{CC} = 2.7V | | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | V _{CC} = 3.6V | 2.2 | | V _{CC} + 0.5V | V |
| V _{IL} | Input LOW Voltage | | V _{CC} = 2.7V | −0.5 | | 0.8 | V |
| I _{IX} | Input Load Current | GND ≤ V _I ≤ V _{CC} | | −1 | ±1 | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _O ≤ V _{CC} , Output Disabled | | −1 | +1 | +1 | μA |
| I _{CC} | V _{CC} Operating Supply Current | I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} , CMOS Levels | V _{CC} = 3.6V | | 7 | 15 | mA |
| | | I _{OUT} = 0 mA, f = 1 MHz, CMOS Levels | | | 1 | 2 | mA |
| I _{SB1} | Automatic CE Power-Down Current—CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V, f = f _{MAX} | | | | 100 | μA |
| I _{SB2} | Automatic CE Power-Down Current—CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V, f = 0 | V _{CC} = 3.6V | LL | 1 | 15 | μA |

Notes:

- $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC Typ}$, $T_A = 25^\circ C$.

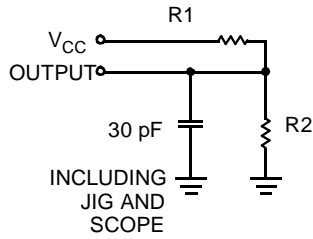
Capacitance^[3]

| Parameter | Description | Test Conditions | Max. | Unit |
|-----------|--------------------|---|------|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ C$, $f = 1$ MHz, $V_{CC} = V_{CC(typ)}$ | 6 | pF |
| C_{OUT} | Output Capacitance | | 8 | pF |

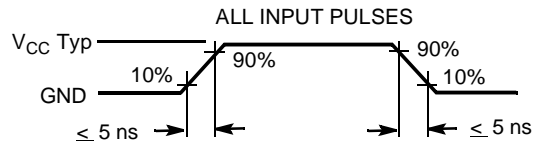
Note:

- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

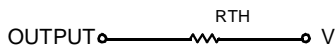


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Equivalent to: THÉVENIN EQUIVALENT

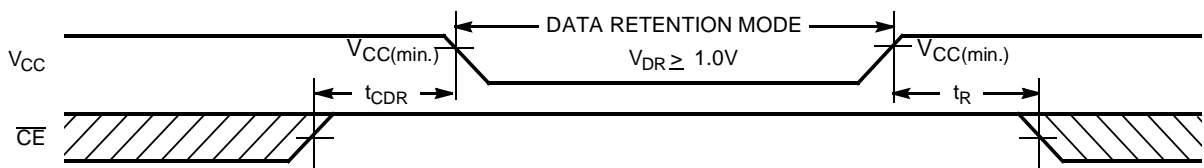


| Parameters | 3.0V | Unit |
|------------|------|-------|
| R1 | 1105 | Ohms |
| R2 | 1550 | Ohms |
| R_{TH} | 645 | Ohms |
| V_{TH} | 1.75 | Volts |

Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions ^[4] | Min. | Typ. ^[2] | Max. | Unit |
|-----------------|--------------------------------------|--|------|---------------------|------|---------|
| V_{DR} | V_{CC} for Data Retention | | 1.0 | | 3.6 | V |
| I_{CCDR} | Data Retention Current | $V_{CC} = 1.0V$ $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed $V_{CC} + 0.3V$ | LL | 0.1 | 5 | μA |
| $t_{CDR}^{[3]}$ | Chip Deselect to Data Retention Time | | 0 | | | ns |
| t_R | Operation Recovery Time | | 100 | | | μs |

Data Retention Waveform^[5]



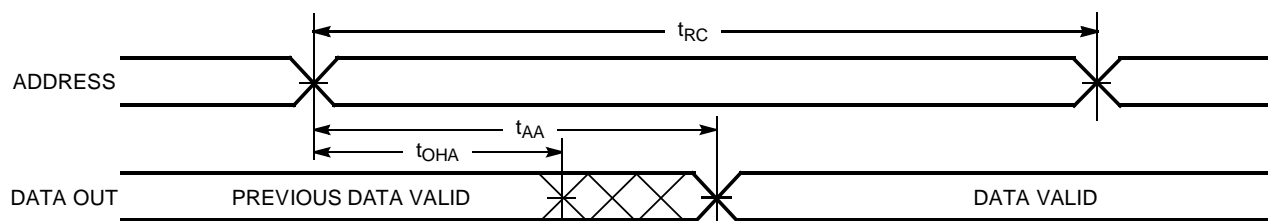
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Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- \overline{CE} is the combination of both \overline{CS}_1 and \overline{CS}_2 .

Switching Characteristics Over the Operating Range^[4]

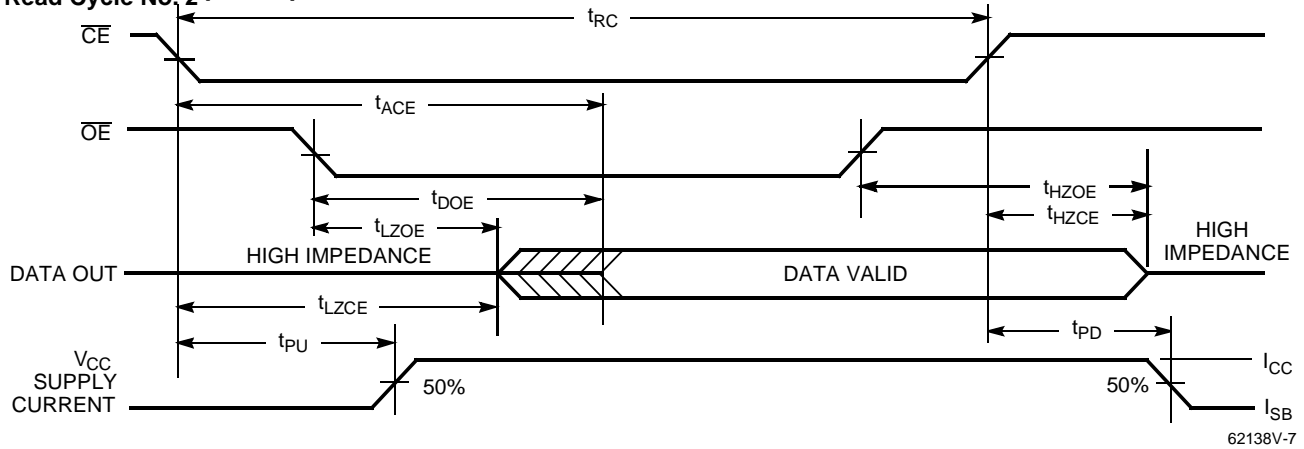
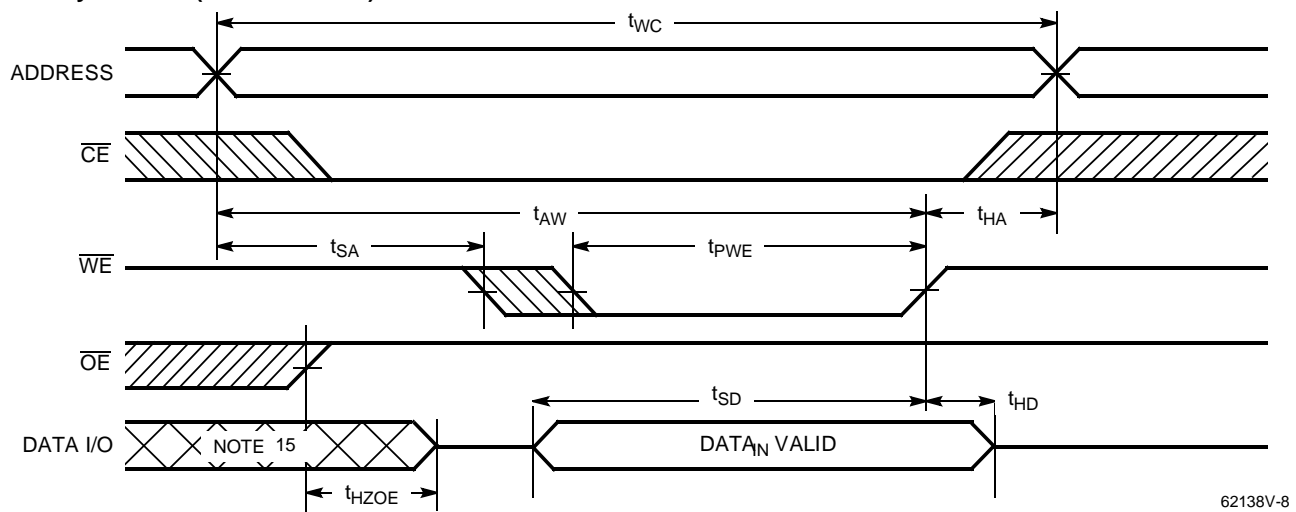
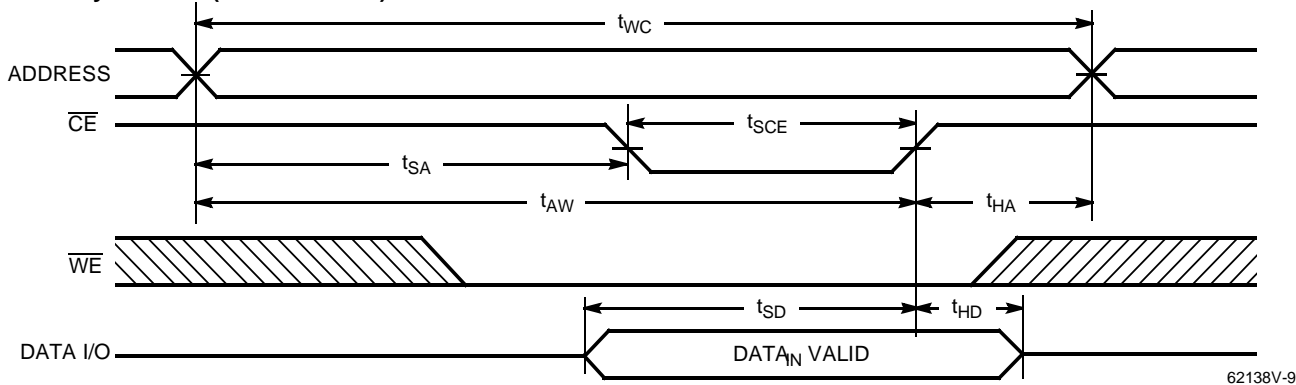
| Parameter | Description | 70 ns | | Unit |
|-------------------------------|--|-------|------|------|
| | | Min. | Max. | |
| READ CYCLE | | | | |
| t _{RC} | Read Cycle Time | 70 | | ns |
| t _{AA} | Address to Data Valid | | 70 | ns |
| t _{OHA} | Data Hold from Address Change | 10 | | ns |
| t _{ACE} | \overline{CE} LOW to Data Valid | | 70 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 35 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z ^[6] | 5 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[6, 7] | | 25 | ns |
| t _{LZCE} | \overline{CE} LOW to Low Z ^[6] | 10 | | ns |
| t _{HZCE} | \overline{CE} HIGH to High Z ^[6, 7] | | 25 | ns |
| t _{PU} | \overline{CE} LOW to Power-Up | 0 | | ns |
| t _{PD} | \overline{CE} HIGH to Power-Down | | 70 | ns |
| WRITE CYCLE ^[8, 9] | | | | |
| t _{WC} | Write Cycle Time | 70 | | ns |
| t _{SCE} | \overline{CE} LOW to Write End | 60 | | ns |
| t _{AW} | Address Set-Up to Write End | 60 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 50 | | ns |
| t _{SD} | Data Set-Up to Write End | 30 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[6, 7] | | 25 | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[6] | 10 | | ns |

Switching Waveforms
Read Cycle No. 1^[10, 11]


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Notes:

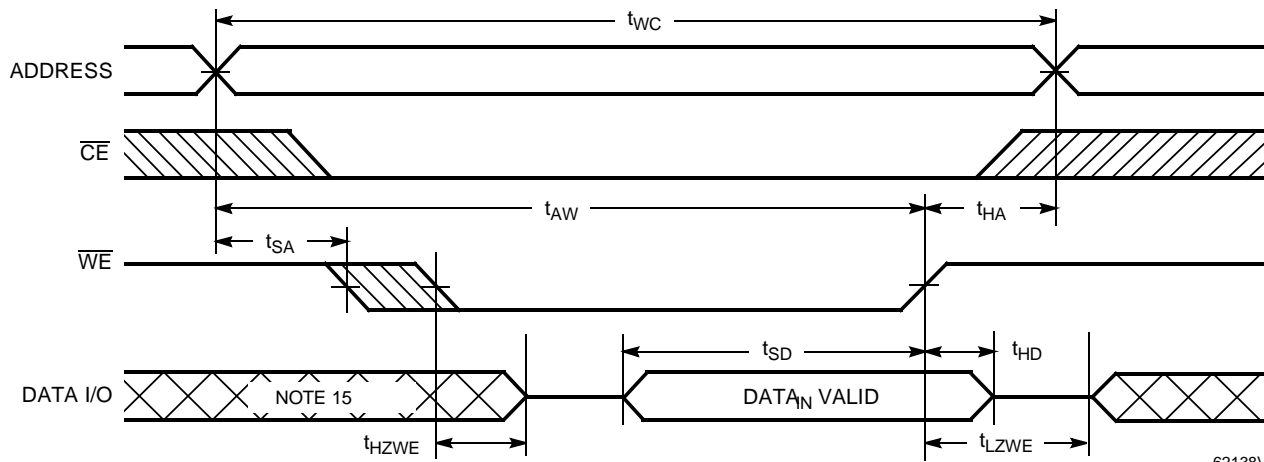
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .
10. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
11. \overline{WE} is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 [5., 11, 12]

Write Cycle No. 1 (\overline{WE} Controlled) [5, 8, 13, 14]

Write Cycle No. 2 (\overline{CE} Controlled) [5, 8, 13, 14]

Notes:

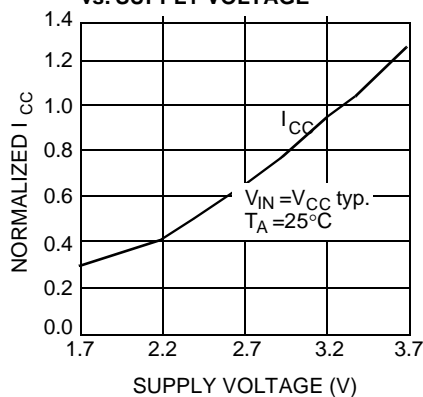
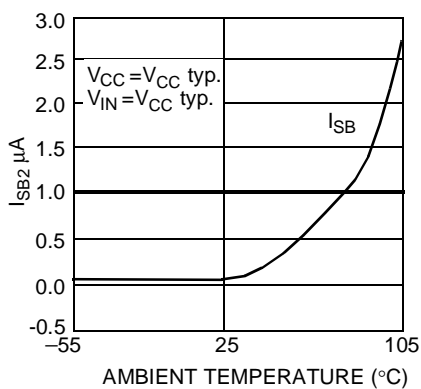
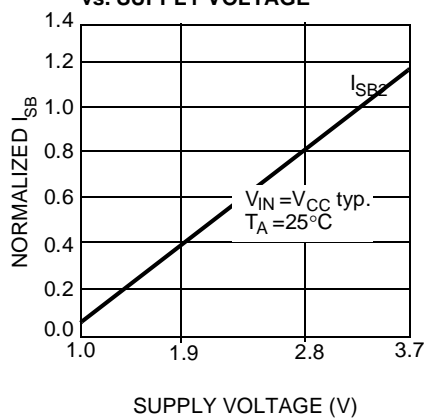
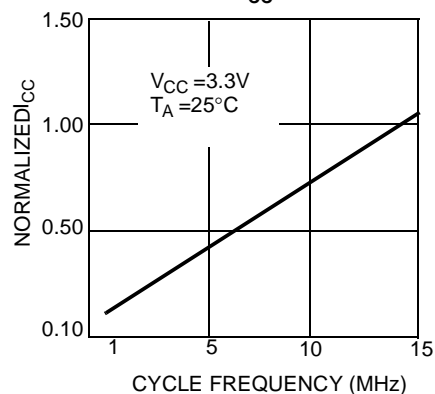
12. Address valid prior to or coincident with \overline{CE} transition LOW.
13. Data I/O is high impedance if $OE = V_{IH}$.
14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [5, 9, 14]



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Typical DC and AC Characteristics
**NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE**

**STANDBY CURRENT
vs. AMBIENT TEMPERATURE**

**NORMALIZED STANDBY CURRENT
vs. SUPPLY VOLTAGE**

NORMALIZED I_CC vs. CYCLE TIME

Truth Table

| \overline{CS}_1 | CS_2 | \overline{WE} | \overline{OE} | Inputs/Outputs | Mode | Power |
|-------------------|--------|-----------------|-----------------|----------------|---------------------------|----------------------|
| H | X | X | X | High Z | Deselect/Power-Down | Standby (I_{SB}) |
| X | L | X | X | High Z | Deselect/Power-Down | Standby (I_{SB}) |
| L | H | H | L | Data Out | Read | Active (I_{CC}) |
| L | H | L | X | Data In | Write | Active (I_{CC}) |
| L | H | H | H | High Z | Deselect, Output Disabled | Active (I_{CC}) |



| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|------------------|--------------|------------------------|-----------------|
| 70 | CY62138VLL-70BAI | BA48 | 48 Ball Fine Pitch BGA | Industrial |

Package Diagram

TOP VIEW

PIN 1 CORNER (LASER MARK)

1 2 3 4 5 6

A B C D E F G H

7.00±0.20

-B-

-A-

7.00±0.20

BOTTOM VIEW

PIN 1 CORNER (PATTEN ON SUBSTRATE)

6 5 4 3 2 1

A B C D E F G H

7.00±0.20

5.25

0.75

0.30±0.05(48X)

0.75

3.75

7.00±0.20

-B-

-A-

0.20(4X)

Side View

0.95

0.40±0.08

-C-

SEATING PLANE

0.21±0.05

0.15

1.10±0.10

51-85096-A

51-85096-A