

SN54HCT541, SN74HCT541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS306B – JANUARY 1996 – REVISED DECEMBER 2002

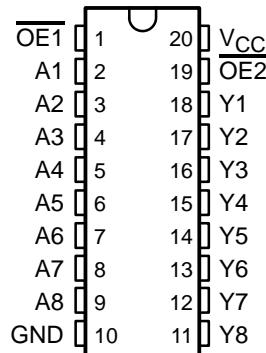
- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 12$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)

description/ordering information

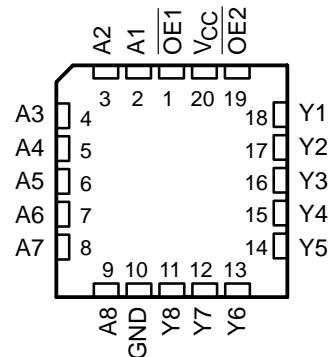
These octal buffers and line drivers are designed to have the performance of the popular 'HC240 series devices and to offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR. If either output-enable (\overline{OE}_1 or \overline{OE}_2) input is high, all eight outputs are in the high-impedance state. The 'HCT541 devices provide true data at the outputs.

SN54HCT541 . . . J OR W PACKAGE
SN74HCT541 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT541 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74HCT541N	SN74HCT541N
	SOIC – DW	Tube	SN74HCT541DW	HCT541
		Tape and reel	SN74HCT541DWR	
	SOP – NS	Tape and reel	SN74HCT541NSR	HCT541
	SSOP – DB	Tape and reel	SN74HCT541DBR	HT541
-55°C to 125°C	TSSOP – PW	Tape and reel	SN74HCT541PWR	HT541
	CDIP – J	Tube	SNJ54HCT541J	SNJ54HCT541J
	CFP – W	Tube	SNJ54HCT541W	SNJ54HCT541W
	LCCC – FK	Tube	SNJ54HCT541FK	SNJ54HCT541FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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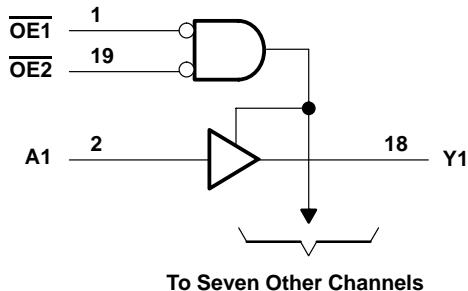
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FUNCTION TABLE (each buffer/driver)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

			SN54HCT541			SN74HCT541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise/fall time				500			500	ns
T _A	Operating free-air temperature		-55	125		-40	85		°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT541		SN74HCT541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	4.5 V	4.4	4.499		4.4		4.4		V
			3.98	4.3		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	4.5 V	0.001	0.1		0.1		0.1		V
			0.17	0.26		0.4		0.33		
I _I	V _I = V _{CC} or 0	5.5 V	±0.1	±100		±1000		±1000		nA
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL}	5.5 V	±0.01	±0.5		±10		±5		μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0	5.5 V			8	160		80		μA
ΔI _{CC} [†]	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}	5.5 V		1.4	2.4		3		2.9	mA
C _i		4.5 V to 5.5 V	3	10		10		10		pF

[†] This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT541		SN74HCT541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	4.5 V		13	23		34		29	ns
			5.5 V		12	21		31		26	
t _{en}	OE	Y	4.5 V		21	30		45		38	ns
			5.5 V		19	27		41		34	
t _{dis}	OE	Y	4.5 V		19	30		45		38	ns
			5.5 V		18	27		41		34	
t _t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

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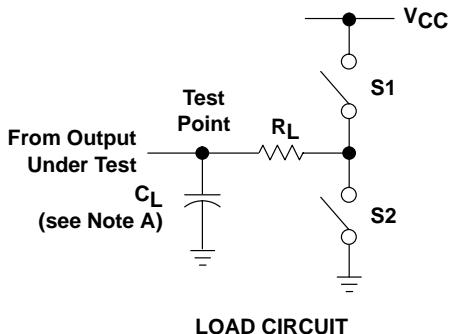
switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT541		SN74HCT541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	4.5 V	20	33	49	42				ns
			5.5 V	19	30	45	38				
t _{en}	OE	Y	4.5 V	26	40	60	50				ns
			5.5 V	25	36	54	45				
t _t		Y	4.5 V	17	42	63	53				ns
			5.5 V	14	38	57	48				

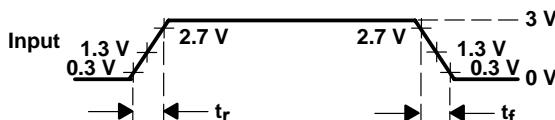
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per buffer/driver	No load	35	pF

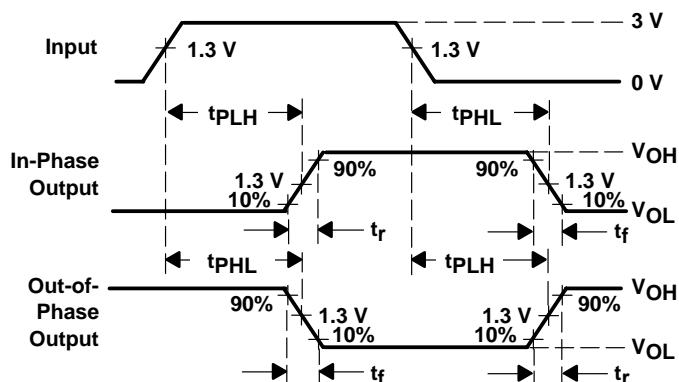
PARAMETER MEASUREMENT INFORMATION



PARAMETER	R _L	C _L	S1	S2	
t _{en}	t _{PZH}	1 k Ω	50 pF or 150 pF	Open	Closed
	t _{PZL}			Closed	Open
t _{dis}	t _{PHZ}	1 k Ω	50 pF	Open	Closed
	t _{PLZ}			Closed	Open
t _{pd} or t _t		—	50 pF or 150 pF	Open	Open

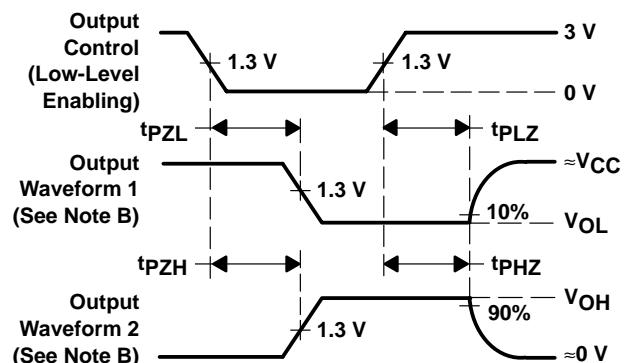


VOLTAGE WAVEFORM INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES:

- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PZH} and t_{PHI} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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