TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

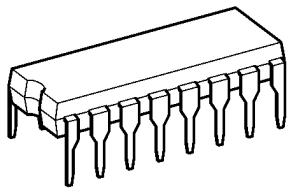
TC4094BP,TC4094BF

TC4094B 8-Stage Shift-and-Store Bus-Register

TC4094B is a SHIFT and STORE REGISTER that consists of an 8-bit shift register and an 8-bit latch. The read data in the shift register can be taken in the latch through the asynchronous STROBE input; therefore, the data transfer mode can hold output. And, since the parallel outputs is of 3-state construction, it can be directly connected to the 8-bit busline.

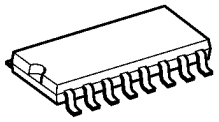
This register can be applied to Serial-to-parallel conversion, data receivers, etc.

TC4094BP



DIP16-P-300-2.54A

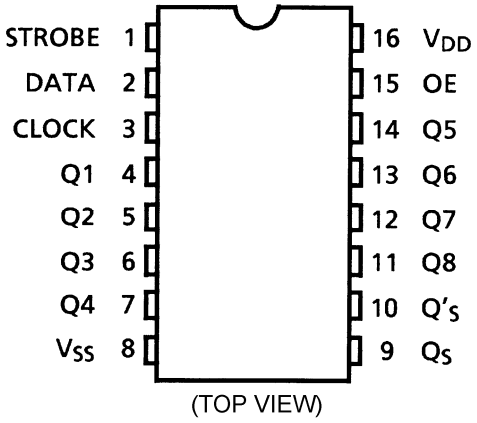
TC4094BF



SOP16-P-300-1.27A

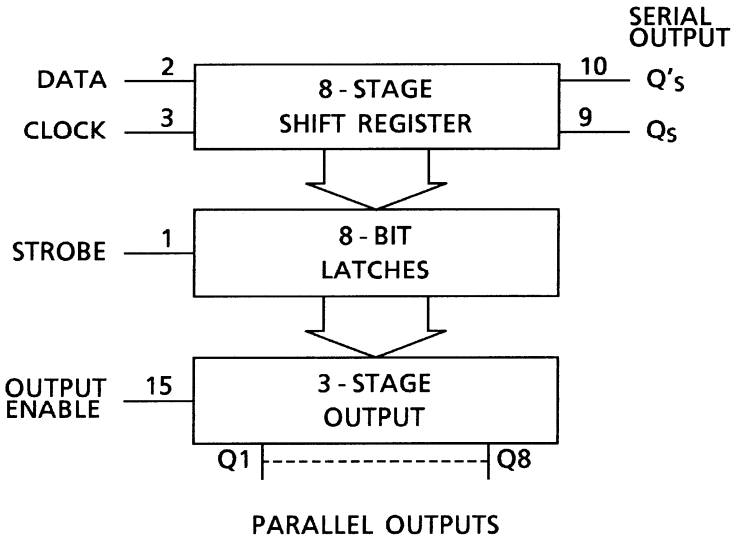
Weight
DIP16-P-300-2.54A : 1.00 g (typ.)
SOP16-P-300-1.27A : 0.18 g (typ.)

Pin Assignment



(TOP VIEW)

Block Diagram



Truth Table

CL	OE	ST	D	PO		SO	
				Q1	Qn	Qs	Q's
↑	H	H	L	L	Qn – 1	Q7	NC
↑	H	H	H	H	Qn – 1	Q7	NC
↑	H	L	X	NC	NC	Q7	NC
↑	L	X	X	HZ	HZ	Q7	NC
↓	H	X	X	NC	NC	NC	Qs
↓	L	X	X	HZ	HZ	NC	Qs

CL = Clock

OE = Output eneble

ST = Strobe

D = Data

PO = Parallel outputs

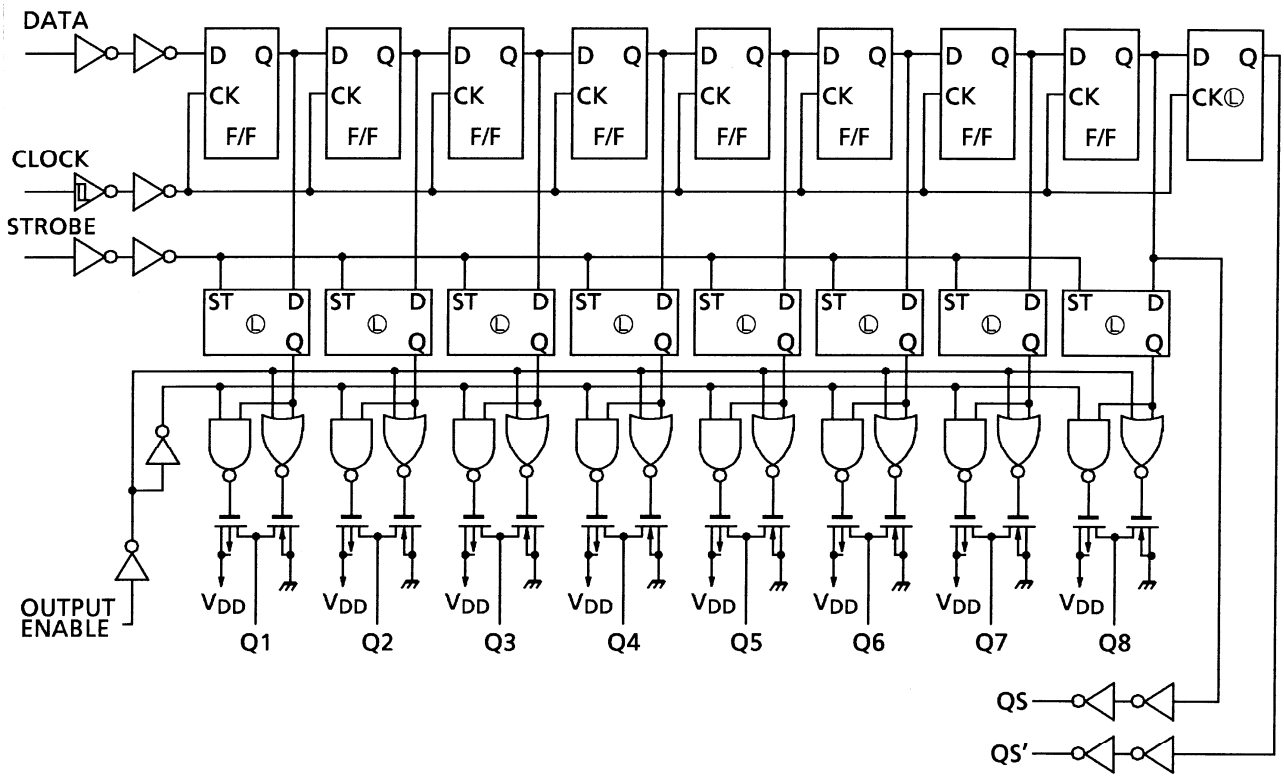
SO = Serial outputs

X = Don't care

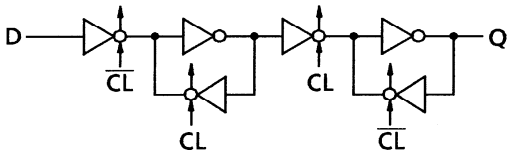
NC = No change

HZ = High impedance

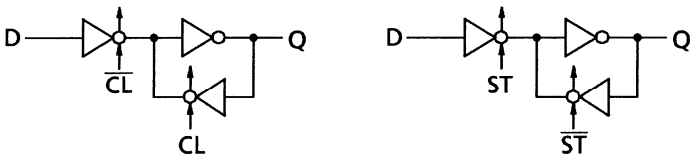
Logic Diagram



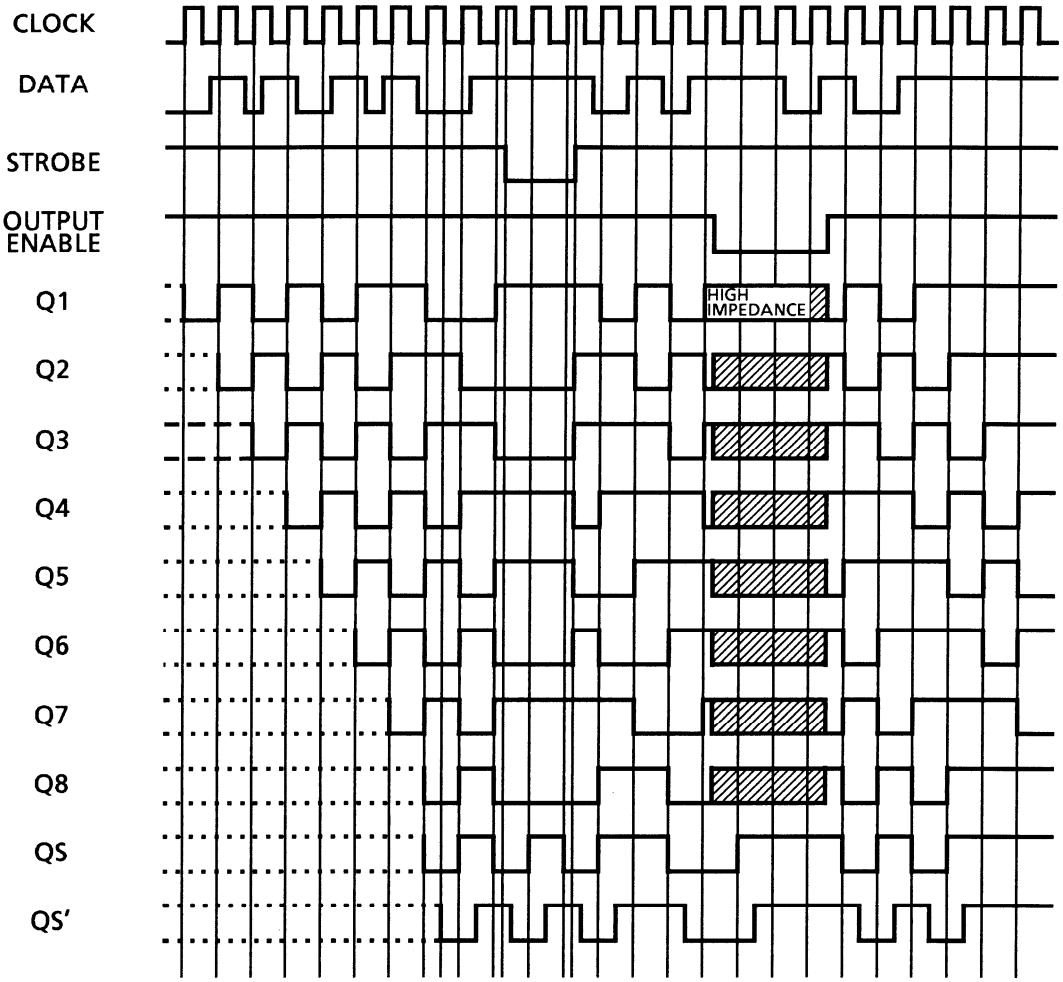
F / F



LATCH



Timing Chart



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	V_{SS} − 0.5 to V_{SS} + 20	V
Input voltage	V_{IN}	V_{SS} − 0.5 to V_{DD} + 0.5	V
Output voltage	V_{OUT}	V_{SS} − 0.5 to V_{DD} + 0.5	V
DC input current	I_{IN}	±10	mA
Power dissipation	P_D	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T_{opr}	−40 to 85	°C
Storage temperature range	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (V_{SS} = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	V_{DD}	—	3	—	18	V
Input voltage	V_{IN}	—	0	—	V_{DD}	V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{DD} or V_{SS}.

Static Electrical Characteristics (V_{SS} = 0 V)

Characteristics		Sym-bol	Test Condition		−40°C		25°C			85°C		Unit
				V_{DD} (V)	Min	Max	Min	Typ.	Max	Min	Max	
High-level output voltage		V_{OH}	$\|I_{OUT}\| < 1$ μA $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
				10	9.95	—	9.95	10.00	—	9.95	—	
				15	14.95	—	14.95	15.00	—	14.95	—	
Low-level output voltage		V_{OL}	$\|I_{OUT}\| < 1$ μA $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
				10	—	0.05	—	0.00	0.05	—	0.05	
				15	—	0.05	—	0.00	0.05	—	0.05	
Output high current		I_{OH}	V_{OH} = 4.6 V	5	−0.61	—	−0.51	−1.0	—	−0.42	—	mA
			V_{OH} = 2.5 V	5	−2.50	—	−2.10	−4.0	—	−1.70	—	
			V_{OH} = 9.5 V	10	−1.50	—	−1.30	−2.2	—	−1.10	—	
			V_{OH} = 13.5 V	15	−4.00	—	−3.40	−9.0	—	−2.80	—	
			$V_{IN} = V_{SS}, V_{DD}$									
Output low current		I_{OL}	V_{OL} = 0.4 V	5	0.61	—	0.51	1.2	—	0.42	—	mA
			V_{OL} = 0.5 V	10	1.50	—	1.30	3.2	—	1.10	—	
			V_{OL} = 1.5 V	15	4.00	—	3.40	12.0	—	2.80	—	
			$V_{IN} = V_{SS}, V_{DD}$									
Input high voltage		V_{IH}	V_{OUT} = 0.5 V, 4.5 V	5	3.5	—	3.5	2.75	—	3.5	—	V
			V_{OUT} = 1.0 V, 9.0 V	10	7.0	—	7.0	5.50	—	7.0	—	
			V_{OUT} = 1.5 V, 13.5 V	15	11.0	—	11.0	8.25	—	11.0	—	
			$\|I_{OUT}\| < 1$ μA									
Input low voltage		V_{IL}	V_{OUT} = 0.5 V, 4.5 V	5	—	1.5	—	2.25	1.5	—	1.5	V
			V_{OUT} = 1.0 V, 9.0 V	10	—	3.0	—	4.50	3.0	—	3.0	
			V_{OUT} = 1.5 V, 13.5 V	15	—	4.0	—	6.75	4.0	—	4.0	
			$\|I_{OUT}\| < 1$ μA									
Input current	"H" level	I_{IH}	V_{IH} = 18 V	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
	"L" level	I_{IL}	V_{IL} = 0 V	18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	
3-state output leakage current	"H" level	I_{DH}	V_{out} = 18 V	18	—	0.4	—	10^{-4}	0.4	—	12	μA
	"L" level	I_{DL}	V_{out} = 0 V	18	—	−0.4	—	-10^{-4}	−0.4	—	−12	
Quiescent supply current		I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ (Note)	5	—	5	—	0.005	5	—	150	μA
				10	—	10	—	0.010	10	—	300	
				15	—	20	—	0.015	20	—	600	

Note: All valid input combinations.

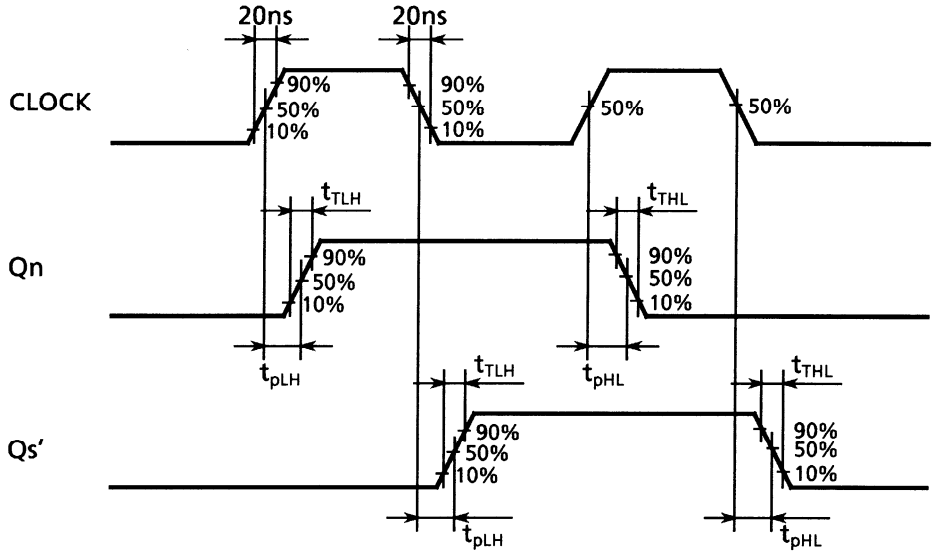
Dynamic Electrical Characteristics (Ta = 25°C, V_{SS} = 0 V, C_L = 50 pF)

Characteristics	Symbol	Test Condition	V_{DD} (V)	Min	Typ.	Max	Unit
Output transition time (low to high)	t_{TLH}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output transition time (high to low)	t_{THL}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Propagation delay time (CLOCK-Q_S)	t_{pLH} t_{pHL}	—	5	—	150	600	ns
			10	—	75	250	
			15	—	55	190	
Propagation delay time (CLOCK-Q_S')	t_{pLH} t_{pHL}	—	5	—	155	460	ns
			10	—	75	220	
			15	—	55	150	
Propagation delay time (CLOCK-Q_n)	t_{pLH} t_{pHL}	—	5	—	190	840	ns
			10	—	90	390	
			15	—	65	270	
Propagation delay time (STROBE-Q_n)	t_{pLH} t_{pHL}	—	5	—	150	580	ns
			10	—	70	290	
			15	—	50	200	
Three state disable time (OUTPUT ENABLE-Q_n)	t_{PHZ} t_{PZH}	R_L = 1 kΩ	5	—	60	200	ns
			10	—	35	100	
			15	—	30	80	
Three state disable time (OUTPUT ENABLE-Q_n)	t_{PLZ} t_{PZL}	R_L = 1 kΩ	5	—	70	200	ns
			10	—	40	100	
			15	—	35	80	
Min clock pulse width	t_W	—	5	—	45	200	ns
			10	—	20	100	
			15	—	15	80	
Min pulse width (STROBE)	t_{WH}	—	5	—	40	200	ns
			10	—	20	80	
			15	—	15	70	
Max clock frequency	f_{CL}	—	5	1.25	6	—	MHz
			10	2.50	12	—	
			15	3.00	16	—	
Min set-up time (DATA-CLOCK)	t_{SU}	—	5	—	0	120	ns
			10	—	0	55	
			15	—	0	35	
Min hold time (DATA-CLOCK)	t_H	—	5	—	10	40	ns
			10	—	10	20	
			15	—	5	15	
Min set-up time (CLOCK-STROBE)	t_{SU}	—	5	—	90	200	ns
			10	—	40	100	
			15	—	30	80	

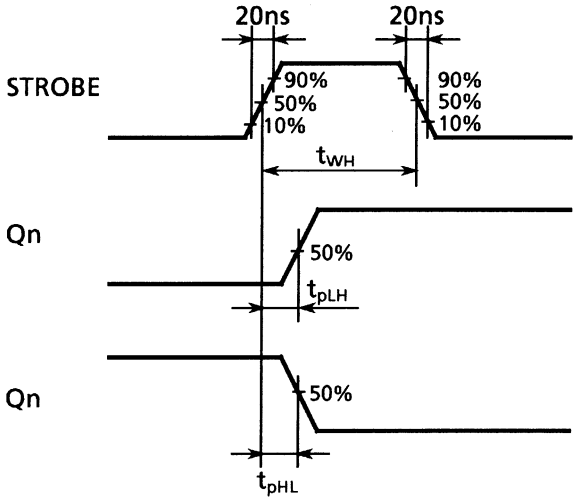
Characteristics	Symbol	Test Condition		Min	Typ.	Max	Unit
			V_{DD} (V)				
Min hold time (CLOCK-STROBE)	t_H	—	5	—	—	0	ns
			10	—	—	0	
			15	—	—	0	
Max clock input rise time	t_{rCL}	—	5	No limit			μs
Max clock input fall time	t_{fCL}		10				
			15				
Input capacitance	C_{IN}	—		—	5	7.5	pF

Waveforms for Measurement of Dynamic Characteristics

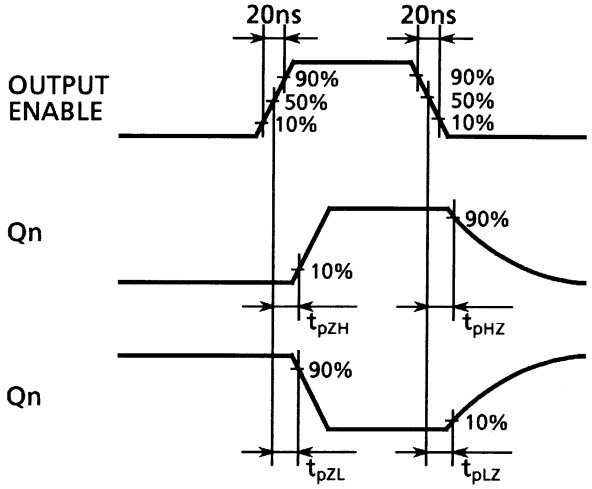
Waveform 1



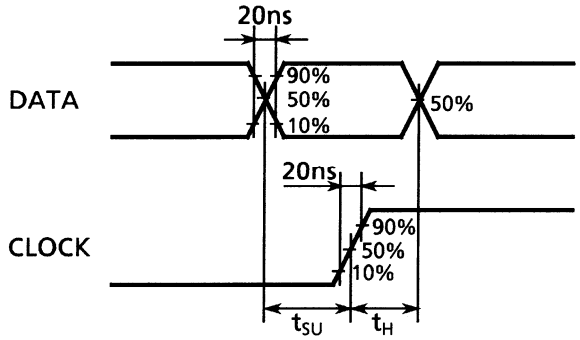
Waveform 2



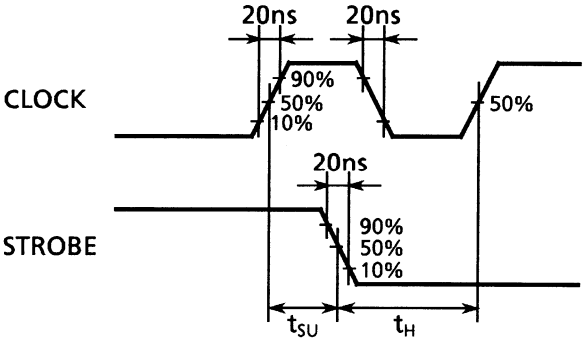
Waveform 3



Waveform 4

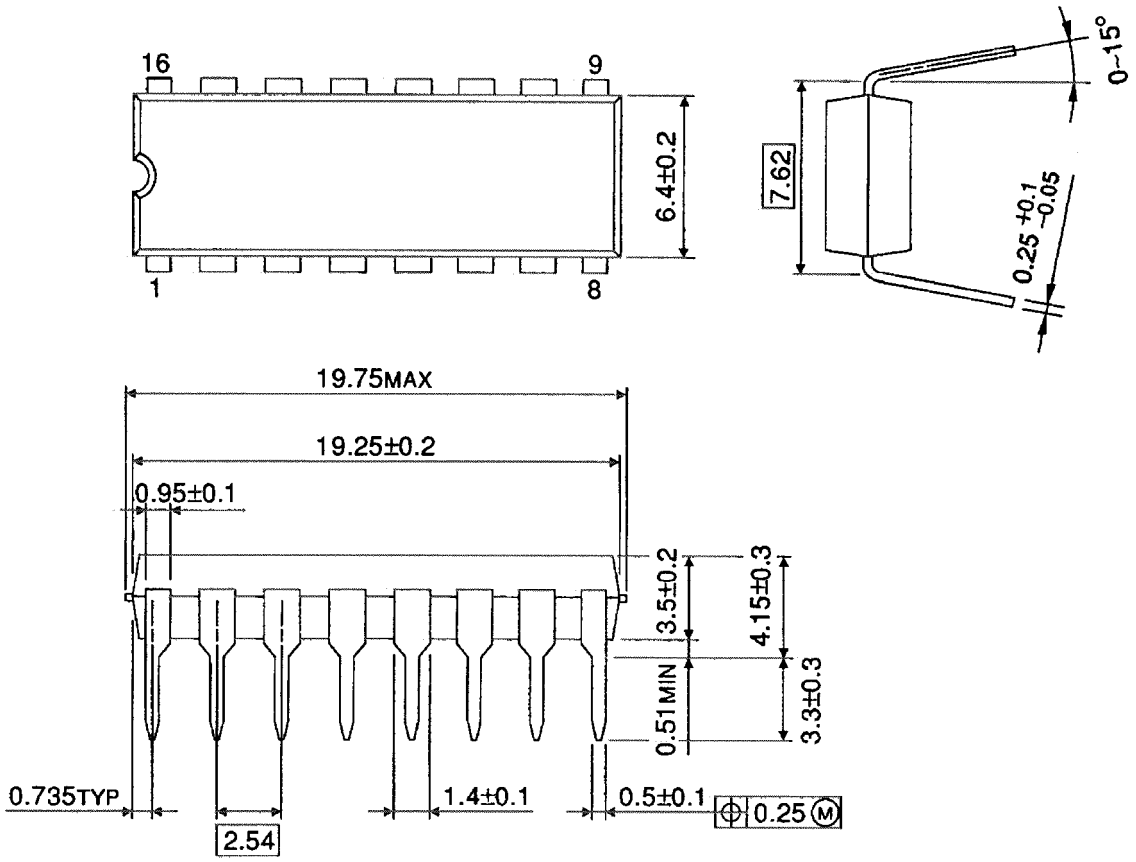


Waveform 5



Package Dimensions

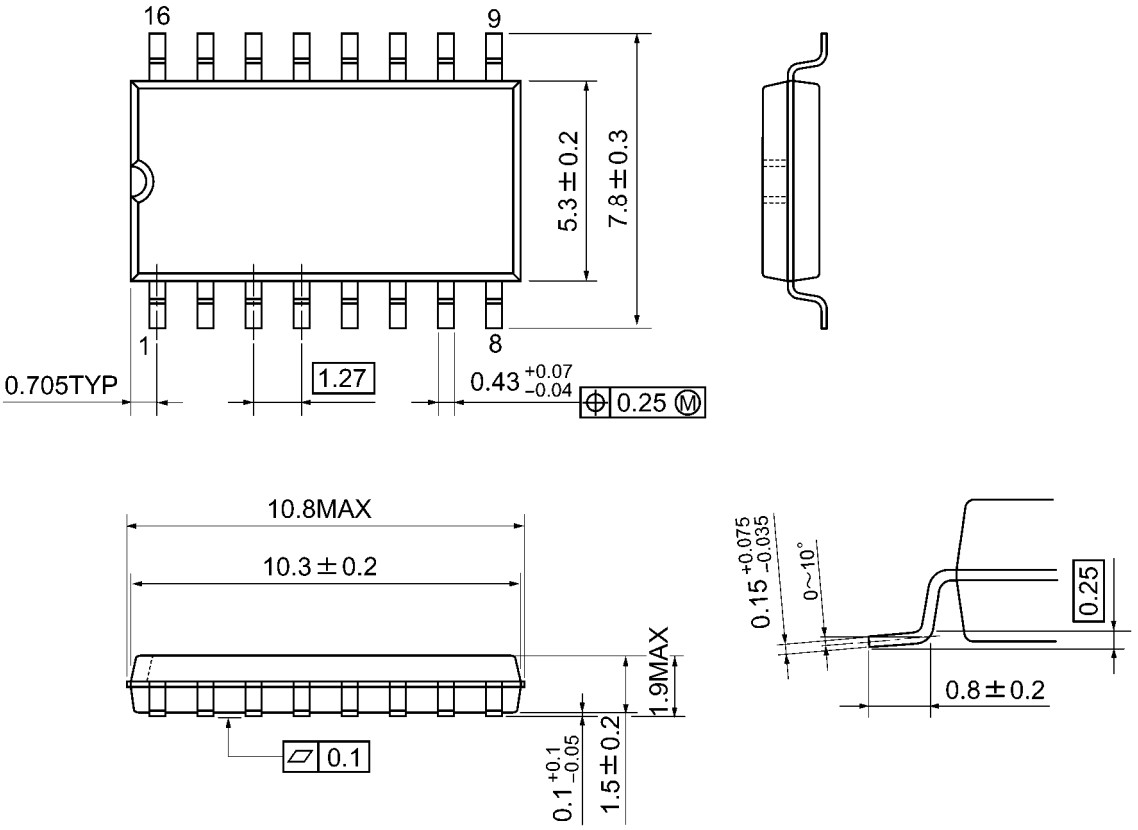
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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