AN5870K

Wide bandwidth analog switch IC

■ Overview

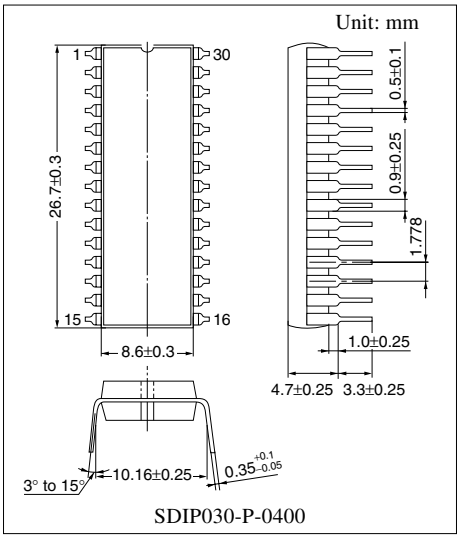
The AN5870K is a wide bandwidth analog switch IC of 300 MHz operation. It is usable for RGB signal and horizontal/vertical synchronizing signals, and it has a built-in 75 Ω driver for video signal. In addition, it has also realized a high speed operation by the adoption of CMOS process for its sync. signal processing circuit. It is usable in a broad range from a popular type monitor to a high definition monitor.

■ Features

- 2-input 1-output circuit (DC switch type)
- Built-in 6 dB amplifier for RGB signal (1.5 dB for 75 Ω termination)
- Built-in sync. separation circuit (Supporting sync. on green and power save)
- Higher speed horizontal / vertical sync. signal circuit (t_{delay} = 20 ns)

■ Applications

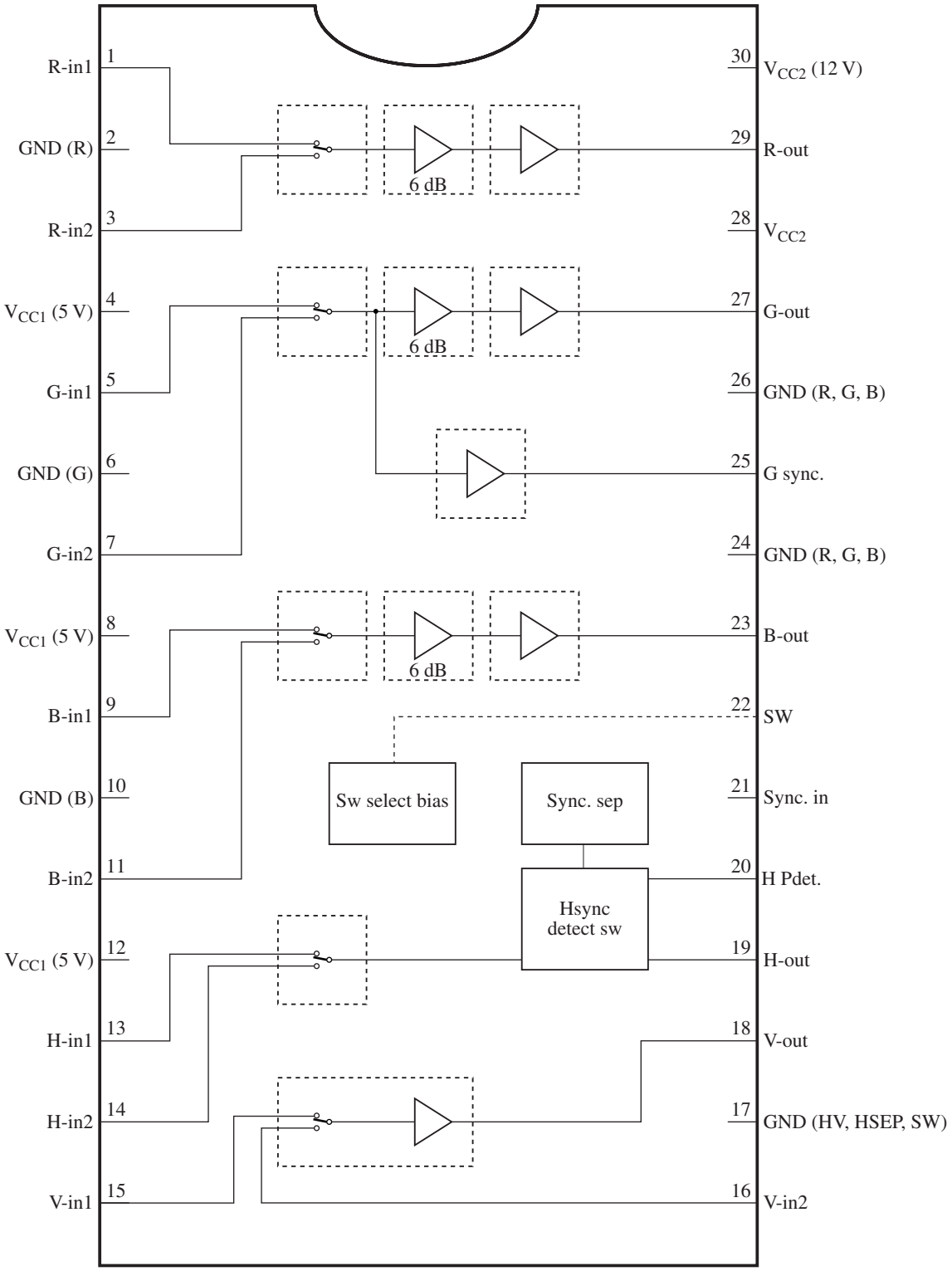
- Monitors



SDIP030-P-0400

Note) The package of this product will be changed to lead-free type (SDIP030-P-0400B). See the new package dimensions section later of this datasheet.

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	R input 1	16	V input 2
2	GND (R)	17	GND (HV, HSEP, SW)
3	R input 2	18	V output
4	V_{CC1} 5 V (G sync.)	19	H output
5	G input 1	20	H detect
6	GND (G)	21	Sync. input
7	G input 2	22	SW
8	V_{CC1} 5 V (RGB)	23	B output
9	B input 1	24	GND (RGB)
10	GND (B)	25	G sync. output
11	B input 2	26	GND (RGB)
12	V_{CC1} 5 V (HV, HSEP, SW)	27	G output
13	H input 1	28	V_{CC2} 12 V (RGB)
14	H input 2	29	R output
15	V input 1	30	V_{CC2} 12 V (RGB)

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC1} (pin 4, pin 8, pin 12)	5.5	V
	V_{CC2} (pin 28, pin 30)	12.9	
Supply current	I_{CC1} (pin 4, pin 8, pin 12)	22.5	mA
	I_{CC2} (pin 28, pin 30)	75.8	
Power dissipation *2	P_D	1.143	W
Operating ambient temperature *1	T_{opr}	−20 to +70	°C
Storage temperature *1	T_{stg}	−55 to +150	°C

Note) For the precautions related to surge and latch-up, refer to "■ Usage Notes".

∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

∗2: The power dissipation shown is for the independent IC package without a heat sink in free air at T_a = 70°C

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	4.5 to 5.25	V
	V_{CC2}	10.5 to 12.6	

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply						
Supply current (1)	I_{CC1}	Current at V_4, V_8, V_{12} = 5 V	13.0	16.0	19.0	mA
Supply current (2)	I_{CC2}	Current at V_{28}, V_{30} = 12 V	46.0	60.0	70.0	mA
Signal processing system						
Input DC voltage 1	V_{I1}	Pin 22: 0 V, pins 1, 5, 9: DC	2.6	2.9	3.2	V
Input DC voltage 2	V_{I2}	Pin 22: 5 V, pins 3, 7, 11: DC	2.6	2.9	3.2	V
Output DC voltage 1	V_{O1}	Pin 22: 0 V, pins 23, 27, 29: DC	5.7	6.2	6.7	V
Output DC voltage 2	V_{O2}	Pin 22: 5 V, pins 23, 27, 29: DC	5.7	6.2	6.7	V
Output DC voltage 3	V_{O3}	Pin 25: DC	1.9	2.3	2.7	V
Input impedance (1)	R_{I1}	Pin 22: 0 V, pins 1, 5, 9: Measurement	85	100	115	kΩ
Input impedance (2)	R_{I2}	Pin 22: 5 V, pins 3, 7, 11: Measurement	85	100	115	kΩ
Output impedance (1)	R_{O1}	Pin 23, 27, 29: Measurement	60	70	80	Ω
Output impedance (2)	R_{O2}	Pin 25: Measurement	50	70	90	Ω
Gain (1)	G_{V1}	Pin 22: 0 V, pins 1, 5, 9: SG1 signal, pins 23, 27, 29: Measurement	0.5	1.5	2.5	dB
Relative gain (1)	ΔG_{V1}	Relative difference to G_{V1}	− 0.4	0.0	0.4	dB
Gain (2)	G_{V2}	Pin 22: 5 V, pin 3, 7, 11: SG1 signal, pins 23, 27, 29: Measurement	0.5	1.5	2.5	dB
Relative gain (2)	ΔG_{V2}	Relative difference to G_{V2}	− 0.4	0.0	0.4	dB
Gain (3)	G_{V3}	Pin 22: 0 V or 5 V, pin 5 or 7: SG1 signal, pins 23, 27, 29: Measurement	−2.0	− 0.5	0.5	dB
Frequency characteristics 1 (100 MHz)	f_{C1}	Pin 22: 0 V, difference from G_{V1}, pins 1, 5, 9: SG4 signal, pins 23, 27, 29: Measurement	−1.3	− 0.3	0.7	dB
Relative frequency characteristics 1 (100 MHz)	Δf_{C1}	Relative difference to f_{C1}	− 0.5	0.0	0.5	dB
Relative frequency characteristics 2 (100 MHz)	f_{C2}	Pin 22: 5 V, difference from G_{V2}, pins 3, 7, 11: SG4 signal, pins 23, 27, 29: Measurement	−1.3	− 0.3	0.7	dB
Relative frequency characteristics 2 (100 MHz)	Δf_{C2}	Relative difference to f_{C2}	− 0.5	0.0	0.5	dB
Crosstalk between RGB 1 (10 MHz)	CTC_1	Pin 22: 0 V, pin 1 or 5 or 9: SG2 signal, pins 23, 27, 29: Measurement	—	−50	−45	dB
Crosstalk between RGB 2 (10 MHz)	CTC_2	Pin 22: 5 V, pin 3 or 7 or 11: SG2 signal, pins 23, 27, 29: Measurement	—	−50	−45	dB
Crosstalk between 2 inputs (1) (10 MHz)	CTI_1	Pin 22: 5 V, pin 1 or 5 or 9: SG2 signal, pins 29, 27, 23: Measurement	—	−60	−50	dB
Crosstalk between 2 inputs (2) (10 MHz)	CTI_2	Pin 22: 0 V, pin 3 or 7 or 11: SG2 signal, pins 29, 27, 23: Measurement	—	−60	−50	dB

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HV circuit system						
High level output voltage (1)	$V_{OH(H)}$	Pin 20: 2.5 V, pin 19: Measurement, pin 13 or 14: 5 V, pin 22: 0 V or 5 V	4.5	—	5.0	V
High level output voltage (2)	$V_{OH(V)}$	Pin 18: Measurement, pin 15 or 16: 5 V, pin 22: 0 V or 5 V	4.5	—	5.0	V
Low level output voltage (1)	$V_{OL(H)}$	Pin 20 2.5 V, pin 19: Measurement, pin 13 or 14: 0 V, pin 22: 0 or 5 V	0.0	—	0.5	V
Low level output voltage (2)	$V_{OL(V)}$	Pin 18: Measurement, pin 15 or 16: 0 V, pin 22: 0 V or 5 V	0.0	—	0.5	V
Input threshold voltage (1)	$V_{ITH(H)}$	Pin 20: 2.5 V, pin 19: Measurement, pin 13 or 14: 0 to 5 input, pin 22: 0 V or 5 V	1.2	1.5	1.8	V
Input threshold voltage (2)	$V_{ITH(V)}$	Pin 18: Measurement, pin 15 or 16: 0 to 5 input, pin 22: 0 V or 5 V	1.2	1.5	1.8	V
HDET voltage	$V_{O(DET)}$	Pin 22: 0 V, pin 13: SG6 signal, pin 20: DC measurement	2.2	2.5	2.8	V
Sync. separation circuit system						
Input clamp voltage	V_{C1}	Pin 21: DC measurement	1.0	1.35	1.7	V
Minimum sync. separation level	V_{Smin}	Pin 21: SG8 signal, pin 19: Sync. level measurement	—	—	100	mV
SW System						
Switch threshold voltage	$V_{ITH(SW)}$	Measurement when pin 15: DC 5 V, pin 16: DC 0 V, pin 22: 0 V to 2.5 V and pin 18: Becomes 0 V	1.2	1.7	2.2	V
Signal processing system						
Input dynamic range (1)	V_{DI1}	Pin 22: 0 V, pins 1, 5, 9: Input sweep, pins 23, 27, 29: Measurement	2.5	3.0	—	V
Input dynamic range (2)	V_{DI2}	Pin 22: 5 V, Pin 3, 7, 11: Input sweep, pins 23, 27, 29: Measurement	2.5	3.0	—	V
G-sync. dynamic range	V_{D0}	Pin 22: 0 V or 5 V, pin 5 or 7: Input sweep, pin 25: Measurement	2.5	3.0	—	V
Gain with power supply fluctuation (1)	G_{VH}	V_{CC1} = 5.25, V_{CC2} = 12.6, like G_{V1}, G_{V2}, difference from typ.	− 0.5	0.0	+0.5	dB
Gain with power supply fluctuation (2)	G_{VL}	V_{CC1} = 4.75, V_{CC2} = 11.4, like G_{V1}, G_{V2}, difference from typ.	− 0.5	0.0	+0.5	dB
Frequency characteristics 3 (300 MHz)	f_{C3}	Pin 22: 0 V, difference form value at 1MHz, pins 1, 5, 9: SG5 signal, pins 23, 27, 29: Measurement	−3.5	−2.0	− 0.5	dB
Relative frequency characteristics 3 (300 MHz)	Δf_{C3}	Relative difference to f_{C3}	−1.5	0.0	+1.5	dB
Frequency characteristics 4 (300 MHz)	f_{C4}	Pin 22: 5 V, difference form value at 1 MHz, pins 3, 7, 11: SG5 signal, pins 23, 27, 29: Measurement	−3.5	−2.0	− 0.5	dB

■ Electrical Characteristics at T_a = 25°C (continued)

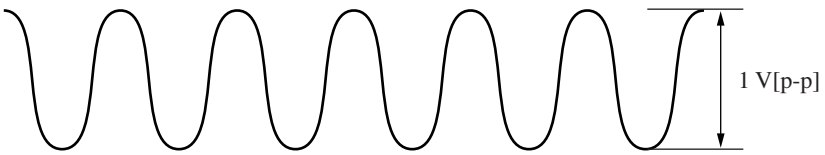
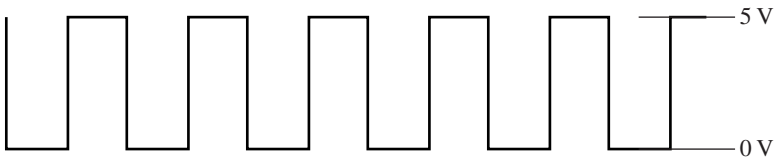
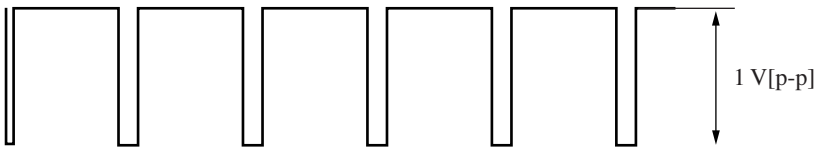
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal processing system (continued)						
Relative frequency characteristics 4 (300 MHz)	Δf_{C4}	Relative difference to f_{C4}	−1.5	0.0	+1.5	dB
G-sync. frequency characteristics (35 MHz)	f_{CGS}	Pin 22: 0 V or 5 V, pin 5 or 7: SG3 signal, pin 25: Measurement	−4.0	−2.5	−1.0	dB
Relative gain between 2 inputs	ΔG_{VCH1}	Relative difference at 1 MHz between same channel of G_{V1} and G_{V2}	− 0.5	0.0	+0.5	dB
Relative frequency characteristics between 2 inputs (1)	Δf_{C1}	Relative difference at 100 MHz between the same channels of f_{C1} and f_{C2}	− 0.5	0.0	+0.5	dB
Relative frequency characteristics between 2 inputs (2)	Δf_{C2}	Relative difference at 300MHz between the same channels of f_{C3} and f_{C4}	−1.0	0.0	+1.0	dB
Crosstalk between RGB 3 (100 MHz)	CTC_3	Pin 22: 0 V, pin 1 or 5 or 9: SG4 signal, pins 23, 27, 29: Measurement	—	−40	−30	dB
Crosstalk between RGB 4 (100 MHz)	CTC_4	Pin 22: 5 V, pin 3 or 7 or 11: SG4 signal, pins 23, 27, 29: Measurement	—	−40	−30	dB
Crosstalk between 2 inputs (3) (100 MHz)	CTI_3	Pin 22: 5 V, pin 1 or 5 or 9: SG4 signal, pins 29, 27, 23: Measurement	—	−50	−40	dB
Crosstalk between 2 inputs (4) (100 MHz)	CTI_4	Pin 22: 0 V, pin 3 or 7 or 11: SG4 signal, pins 29, 27, 23: Measurement	—	−50	−40	dB
Crosstalk between RGB 5 (300 MHz)	CTC_5	Pin 22: 0 V, pin 1 or 5 or 9: SG5 signal, pins 23, 27, 29: Measurement	—	−25	—	dB
Crosstalk between RGB 6 (300 MHz)	CTC_6	Pin 22: 5 V, pin 3 or 7 or 11: SG5 signal, pins 23, 27, 29: Measurement	—	−25	—	dB
Crosstalk between 2 inputs 5 (300 MHz)	CTI_5	Pin 22: 5 V, pin 1 or 5 or 9: SG5 signal, pins 23, 27, 29: Measurement	—	−30	—	dB
Crosstalk between 2 inputs 6 (300 MHz)	CTI_6	Pin 22: 0 V, pin 3 or 7or 11: SG5 signal, pins 23, 27, 29: Measurement	—	−30	—	dB
Rise time (1)	t_{r1}	Pin 22: 0 V, pin 1 or 5 or 9: SG9 signal, pins 23, 27, 29: Measurement	—	1.2	—	ns
Rise time (2)	t_{r2}	Pin 22: 5 V, pin 3 or 7or 11: SG9 signal, pins 23, 27, 29: Measurement	—	1.2	—	ns
Fall time (1)	t_{f1}	Pin 22: 0 V, pin 1 or 5 or 9: SG9 signal, pins 23, 27, 29: Measurement	—	1.2	—	ns
Fall time (2)	t_{f2}	Pin 22: 5 V, pin 3 or 7or 11: SG9 signal, pins 23, 27, 29: Measurement	—	1.2	—	ns
Output VSWR/75 Ω	Γ_o	Pin 23 or 27 or 29: SG5 signal, voltage standing ratio measurement	—	1.6	—	

■ Electrical Characteristics at T_a = 25°C (continued)

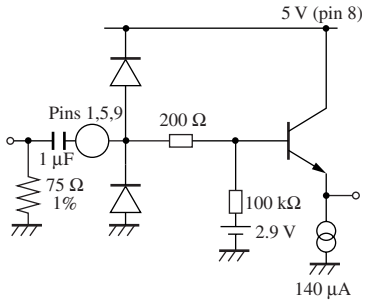
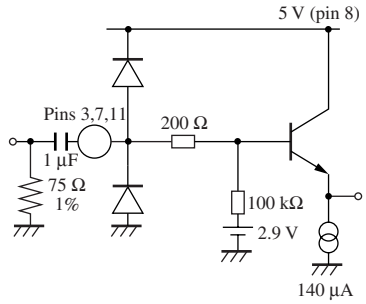
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HV circuit system						
Rise time (1)	$t_{r(H)}$	Pin 19: Measurement, pin 13 or 14: SG6 signal, pin 22: 0 V or 5 V	—	2	—	ns
Rise time (2)	$t_{r(V)}$	Pin 18: Measurement, pin 13 or 14: SG6 signal, pin 22: 0 V or 5 V	—	2	—	ns
Fall time (1)	$t_{f(H)}$	Pin 19: Measurement, pin 13 or 14: SG6 signal, pin 22: 0 V or 5 V	—	2	—	ns
Fall time (2)	$t_{f(V)}$	Pin 18: Measurement, pin 13 or 14: SG6 signal, pin 22: 0 V or 5 V	—	2	—	ns
Rise delay time (1)	$t_{rD(H)}$	Pin 19: Measurement, pin 13 or 14: SG6 signal, pin 22: 0 V or 5 V	—	20	50	ns
Rise delay time (2)	$t_{rD(V)}$	Pin 18: Measurement, pin 13 or 14: SG6 signal, pin 22: 0 V or 5 V	—	10	40	ns
Fall delay time (1)	$t_{fD(H)}$	Pin 19: Measurement, pin 13 or 14: SG6 signal, pin 22: 0 V or 5 V	—	15	45	ns
Fall delay time (2)	$t_{fD(V)}$	Pin 18: Measurement, pin 13 or 14: SG6 signal, pin 22: 0 V or 5 V	—	10	40	ns
Output impedance (3)	R_{O3}	Pin 18 or 19: Measurement	—	70	—	Ω
Sync. separation circuit system						
Rise time	$t_{r(SY)}$	Pin 21: SG7 signal, pin 19: Measurement	—	2	—	ns
Fall time	$t_{f(SY)}$	Pin 21: SG7 signal, pin 19: Measurement	—	2	—	ns
Rise delay time	$t_{rD(SY)}$	Pin 21: SG7 signal, pin 19: Measurement	—	2	—	ns
Fall delay time	$t_{fD(SY)}$	Pin 21: SG7 signal, pin 19: Measurement	—	2	—	ns
Slice level	I_{S1}	Pin 21: 2 V, pin 21 sink current value measurement	4.2	5.6	7.0	μA

■ Electrical Characteristic (continued)

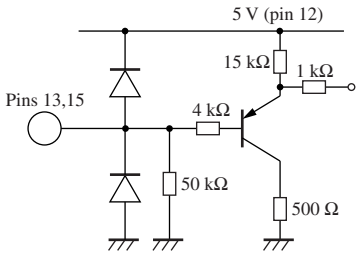
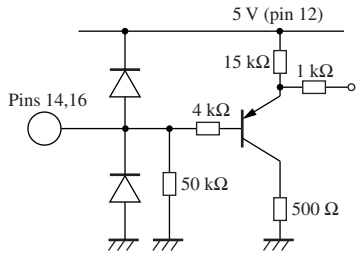
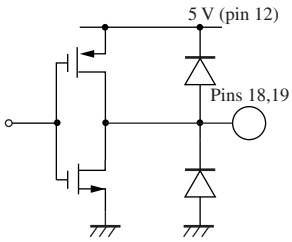
• Input signal for testing

Name	Input signal
SG1	Sine wave (f = 1 MHz, amplitude 1 V[p-p]) 
SG2	Sine wave (f = 10 MHz, amplitude 1 V[p-p])
SG3	Sine wave (f = 35 MHz, amplitude 1 V[p-p])
SG4	Sine wave (f = 100 MHz, amplitude 1 V[p-p])
SG5	Sine wave (f = 300 MHz, amplitude 1 V[p-p])
SG6	Square wave (f = 62.5 kHz, amplitude 5 V_{OP}, duty cycle 50%) 
SG7	Square wave (f = 62.5 kHz, amplitude 1 V[p-p], low period 1 µs) 
SG8	Square wave (f = 62.5 kHz, amplitude 0.1 V[p-p], low period 1 µs)
SG9	Square wave (f = 62.5 kHz, amplitude 0.7 V[p-p], low period 1 µs)

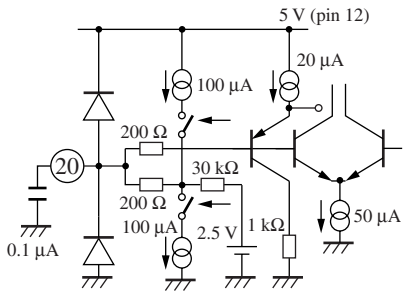
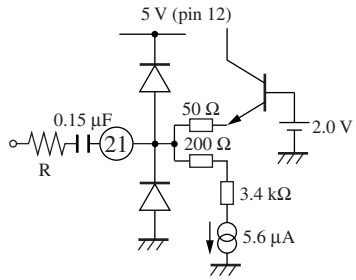
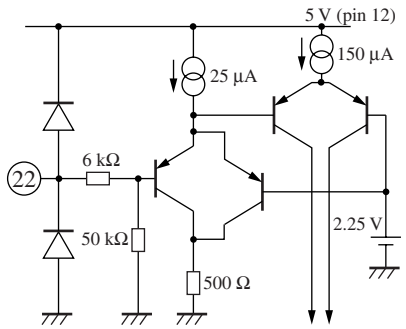
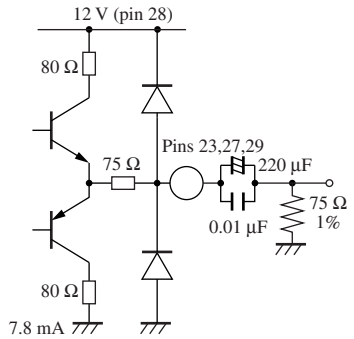
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Pin voltage (V)
1		R signal input pin 1: Input through a capacitor	Input with sync. signal (typ.) 1.0 V[p-p] DC 2.9 V
2	—	GND pin for 5 V: For R signal circuit	GND
3		R signal input pin 2: Input through a capacitor	Input with sync. signal (typ.) 1.0 V[p-p] DC 2.9 V
4	—	Power supply pin for 5 V: For G sync. circuit output	5 V
5	Refer to pin 1	G signal input pin 1: Input through a capacitor	Refer to pin 1
6	—	GND pin for 5 V: For G signal circuit	GND
7	Refer to pin 3	G signal input pin 2: Input through a capacitor	Refer to pin 3
8	—	Power supply pin for 5V: For RGB signal circuit	5 V
9	Refer to pin 1	B signal input pin 1: Input through a capacitor	Refer to pin 1
10	—	GND pin for 5 V: For B signal circuit	GND
11	Refer to pin 3	B signal input pin 2: Input through a capacitor	Refer to pin3
12	—	Power supply pin for 5 V: HV • Sync. separation • For SW circuit	5 V

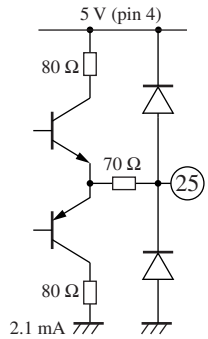
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Pin voltage (V)
13		H. sync. signal input pin 1:	(typ.) High-level: 5 V Low-level: 0 V threshold voltage: 1.5 V
14		H. sync. signal input pin 2:	(typ.) High-level: 5 V Low-level: 0 V threshold voltage: 1.5 V
15	Refer to pin 13	V sync. signal output pin 1:	Refer to pin 13
16	Refer to pin 14	V sync. signal output pin 2:	Refer to pin 14
17	—	GND pin for 5 V: HV • Sync. separation • For SW circuit	GND
18		V sync. signal output pin:	(typ.) High-level: 5 V Low-level: 0 V
19		H. sync. signal output pin:	

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Pin voltage (V)
20		H. sync. signal detection pin: • Pin 20 gives priority to high-level signal output H. sync. signal present: H. sync. signal output H. sync. not present: Sync. separation circuit output	When detecting high-level signal (typ.) 2.5 V
21		Sync. separation circuit input pin: • Sync. slice level is determined by the external resistor R. Referring to the following equation, adjust slice level according to equipment set; $\text{Slice level} = R \cdot \frac{5.6\ (\mu A)}{\text{Input frequency} \cdot \text{Sync. width}}$ • Open when the pin is unused.	Sync. signal (typ.) 0.3 V[p-p] DC 1.35 V
22		Input changeover signal input pin: • When input is high: Input pin 2 is selected (pins 3, 7, 11, 14, 16) When input is low: Input pin 1 is selected (pins 1, 5, 9, 13, 15)	(typ.) High-level: 5 V Low-level: 0 V threshold voltage: 1.7 V
23		B signal output pin: • Be sure to connect a capacitor to output pin. If the pin is not used with a 75 Ω terminating resistor, do not allow a 20 mA or more output current flow.	(typ.) DC 6.2 V

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Input resistance or pin voltage
24	—	GND pin for 12 V	GND
25		Sync. on green signal Output pin: • If terminating with a resistor, do not allow 10 mA or more output current flow.	(typ.) DC 2.3 V
26	—	• For RGB signal circuit For G sync. output	GND
27	Refer to pin 23	G signal output pin: • Be sure to connect a capacitor to output pin. If the pin is not used with a 75 Ω terminating resistor, do not allow a 20 mA or more output current flow.	Refer to pin 23
28	—	Power supply pin for 12 V: • For RGB signal circuit	12 V
29	Refer to pin 23	R signal output pin: • Be sure to connect a capacitor to output pin. If the pin is not used with a 75 Ω terminating resistor, do not allow a 20 mA or more output current to flow.	Refer to pin 23
30	—	Power supply pin for 12 V: • For RGB signal circuit	12 V

■ Technical Information

• Operational explanation

1. SW block

Switches over R, G, B, H, V signal of 2 systems.

SW pin (pin 22)	Selected pins
In low-level	R in 1 (pin 1), G in 1 (pin 5), B in 1 (pin 9), H in 1 (pin 13), V in 1 (pin 15)
In high-level	R in 2 (Pin 3), G in 2 (pin 7), B in 2 (pin 11), H in 2 (pin 14), V in 2 (pin 16)

2. High-level signal detection block

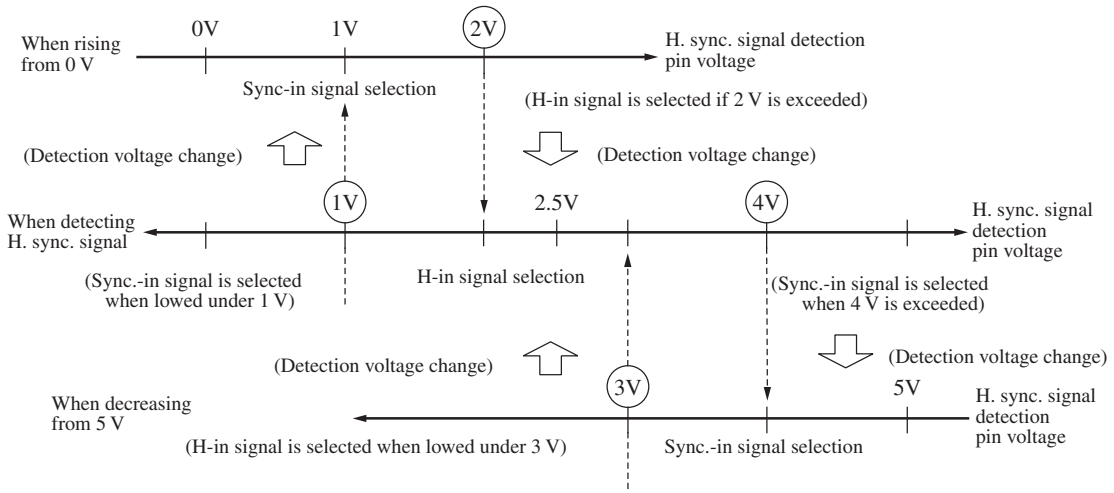
Sync.-in pin (pin 21) is a pin for inputting the sync.-on green signal and it is separated into the composite sync. signal (composite sync.) inside. H-in 1 and 2 pins (pin 13 or pin 14) are input pins for the video signal and the separated horizontal signal.

The high-level signal detection block discriminates the presence of H-in signal which is selected in SW block and provides the output to H-out pin (pin 19) in the following manner.

Input signal		Output signal
Sync.-in pin (pin 21)	H-in pin (pin 13 · pin 14)	H-out pin (pin 19)
●	●	H-in signal
●		Sync.in signal
	●	H-in signal
		DC (state of sync.-in pin)

H signal detection pin (pin 20) voltage becomes under 1 V or over 4 V if H. sync. signal is not inputted.

The output signal for the H. sync. signal detection pin voltage becomes as follows and it has hysteresis characteristics. It is possible to adjust the H. sync. signal detection time by means of an external capacitor.



■ Usage Notes

1. About C22 0.01 µF capacitor (refer to ■ Application Circuit Example)

In the case of evaluation board for this IC without heat sink, a resonance phenomena takes place at approx. 400 MHz between pin 23 B-out pin and pin 22 SW pin and affects the frequency characteristic of B-out pin.

To solve the above problem, the correction can be made by attaching C22 0.01 µF capacitor between pin 22 SW pin and GND at a place as close to the IC as possible.

In the case of using this IC, study if the correction is necessary.

2. About latch-up

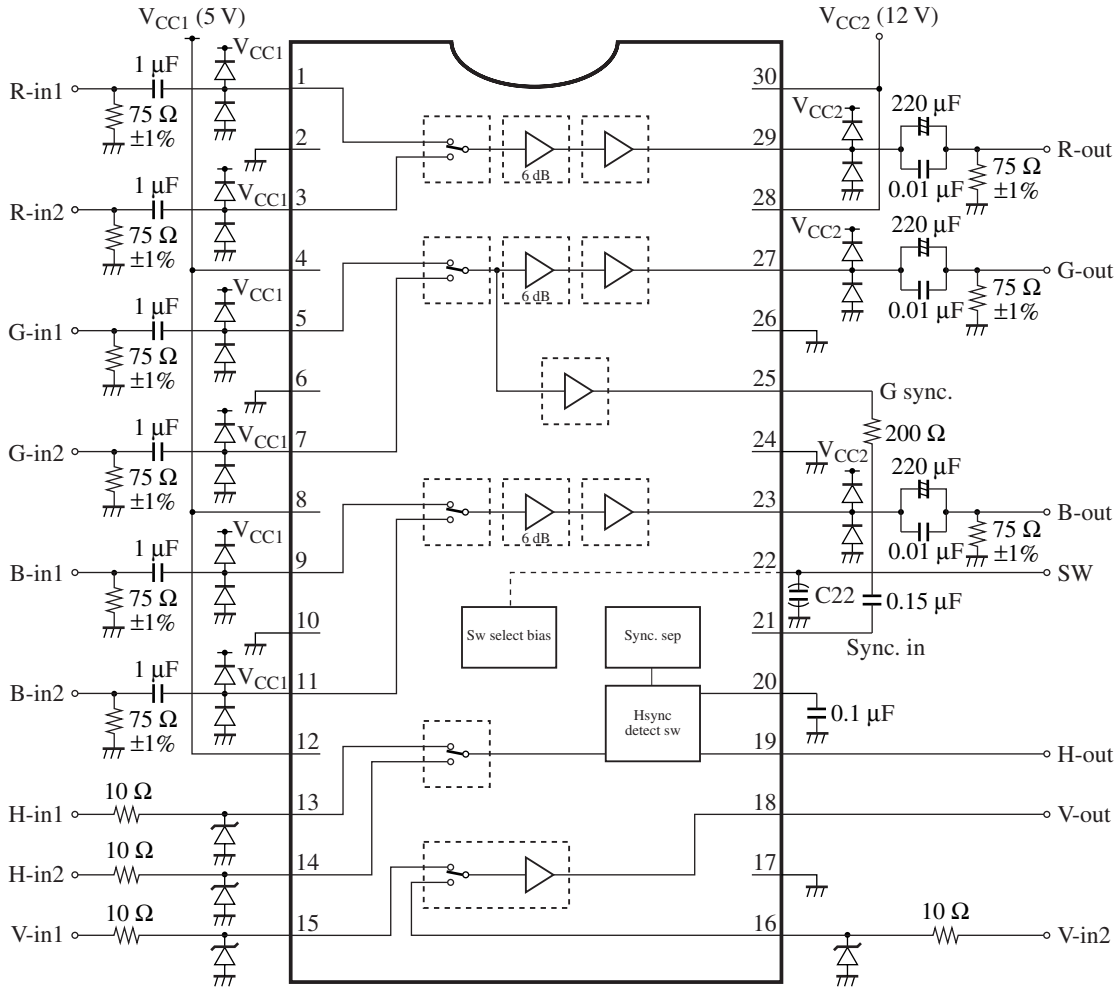
In our latch-up testing, a voltage charged to 200 pF capacitor is applied to the IC pin, in the state of providing only a voltage to the power supply pin of the IC, and we confirm that the latch-up does not occur up to 200 V.

It is confirmed that this IC does not cause latch-up up to 200 V under a condition including the peripheral components. (Refer to ■ Application Circuit Example).

Be careful to pin 20, pin 21, pin 28 and pin 30 which are especially weak.

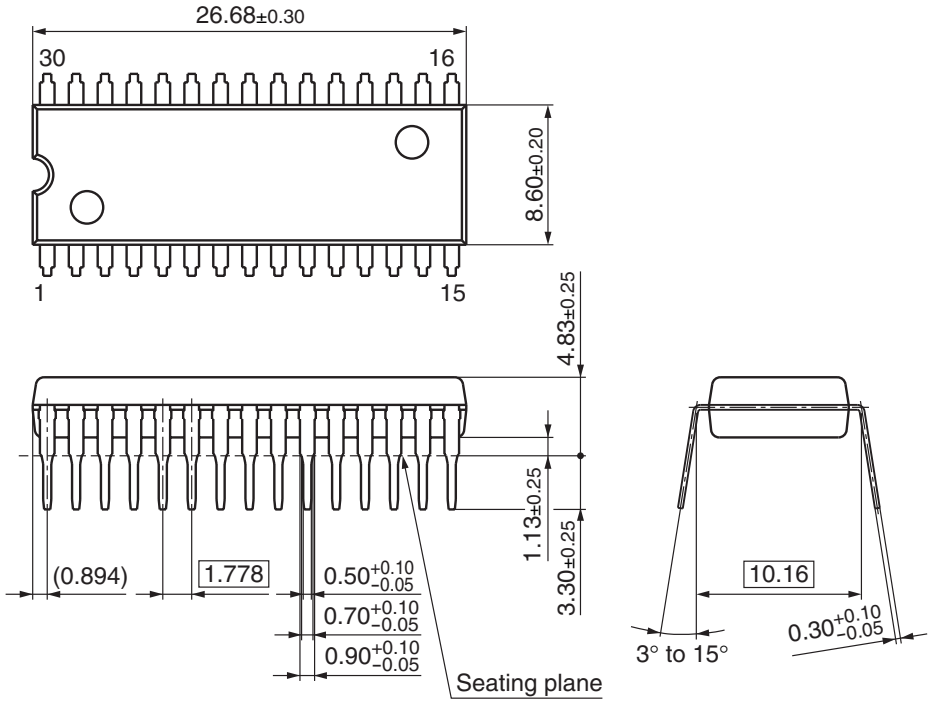
In the case of using this IC, the peripheral components to be attached externally should be placed as close to the IC as possible.

■ Application Circuit Example



■ New Package Dimensions (Unit: mm)

• SDIP030-P-0400B (Lead-free package)



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