Opto-Isolated Serial Output 5.8µs 12-Bit A/D Converter

General Description

The MAX171 is a complete 5.8µs, 12-bit analog-to-digital converter (ADC) that provides over 1,500V_{RMS} electrical isolation between its analog input and the digital interface pins. It combines a serial output 12-bit ADC, three opto-couplers, and a low-drift buried-zener voltage reference in a standard 16-lead plastic DIP package (0.3").

Required external components are limited to supply and reference decoupling capacitors and three resistors. The 2.5MHz clock input can be driven from an external clock source such as a divided microprocessor clock. The MAX171 works with +5V and -12V to -15V supply voltages and typically dissipates 265mW.

The MAX171 is useful in applications where an analog signal must be electrically isolated from control electronics to avoid hazardous electrical conditions, provide noise immunity, or bridge large differences in ground potential. These situations have traditionally required an instrumentation or isolation amplifier with suitably high common mode rejection. If the analog signal must be digitized at some point in the signal chain, the MAX171 can replace these isolating amplifiers while providing high performance and lower cost.

Applications

Ground-Loop Interruption

Process Control

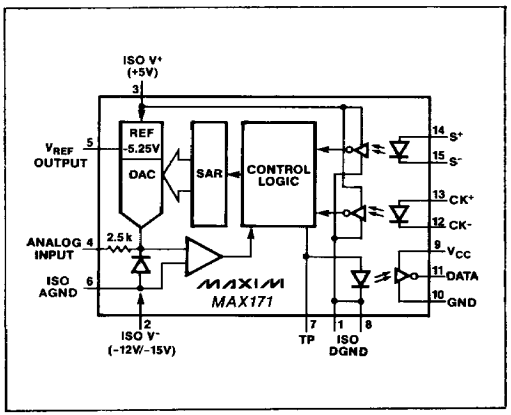
Isolated Industrial Data Acquisition

Electro-Mechanical Systems

Robotics

Automatic Test Equipment

Functional Diagram



Features

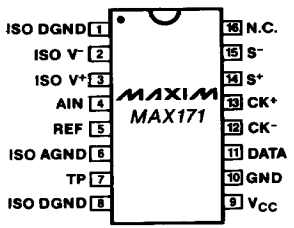
- **Optical Isolation to Over 1,500V_{RMS}**
- **UL Recognized in File E118032 to UL1577**
- **12-Bit Resolution and Linearity**
- **5.8µs Conversion Time**
- **No Missing Codes Over Temperature**
- **Serial Output**
- **Complete with On-Chip Reference**
- **Standard 16-Lead Plastic DIP Package**

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
MAX171ACPE	0°C to +70°C	Plastic DIP	±½ LSB
MAX171BCPE	0°C to +70°C	Plastic DIP	±1 LSB
MAX171AEPE	-40°C to +85°C	Plastic DIP	±½ LSB
MAX171BEPE	-40°C to +85°C	Plastic DIP	±1 LSB

Pin Configuration

TOP VIEW



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Opto-Isolated Serial Output 5.8µs 12-Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS

$V_{ISO\ V+}$ to ISO GND ..... -0.3V to +7V
$V_{ISO\ V-}$ to ISO GND ..... +0.3V to -17V
AIN to ISO GND ..... ±15V
V_{CC} to GND ..... -0.3V to +7V
DATA Output Current 60mA
DATA Output Voltage 5.5V
Digital Inputs: S^+ to S^- and CK^+ to CK^-:
LED Current 15mA
LED Reverse Voltage 5V

Isolation Voltage
1 second ..... 1,500 V_{RMS}
1 minute ..... 1,200 V_{RMS}
Continuous ..... 130 V_{RMS}
Operating Temperature Ranges
MAX171XC ..... 0°C to +70°C
MAX171XE ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, $V_{ISO\ V+}$ = +5V ±5%, $V_{ISO\ V-}$ = -11.4V to -15.75V; f_{CLK} = 2.5MHz; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ISOLATION (T_A = +25°C, Note 1)							
Test Voltage	V_{ISO}	1 second withstand 1 minute withstand (Note 2)		1500 1200			V_{RMS} V_{RMS}
Leakage Current	I_{ISO}	V_{ISO} = 130V_{RMS}, 60Hz			2	50	μA_{RMS}
Resistance	R_{ISO}	V_{ISO} = 500VDC			10^{10}		Ω
Capacitance	C_{ISO}				5		pF
ACCURACY							
Resolution				12			Bits
Integral Non-Linearity	INL		MAX171AC MAX171AE MAX171B			±1/2 ±3/4 ±1	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Specified Temperature Range				±1	LSB
Offset Error (Note 3)			MAX171A MAX171B			±3 ±5	LSB
Full Scale Error (Note 4)		T_A = 25°C				±10	LSB
Full Scale Tempco (Notes 5, 6)						±45	ppm/°C
Conversion Time	t_{CONV}	14 Clock Cycles + Opto-Coupler Delay				5.8	µs
ANALOG INPUT							
Input Voltage Range				0		+5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 7)						±40	ppm/°C
Output Current Sink Capability		(Note 8)				5	mA
POWER SUPPLY REJECTION							
Positive Supply Rejection	V_{DD}	FS Change, V_{SS} = -15V or -12V	V_{DD} = 4.75V to 5.25V		±1/2		LSB
Negative Supply Rejection	V_{SS}	FS Change, V_{DD} = +5V	V_{SS} = -14.25V to -15.75V V_{SS} = -11.4V to -12.6V		±1/8 ±1/8		LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±5%, $V_{ISO\ V+}$ = +5V ±5%, $V_{ISO\ V-}$ = -11.4V to -15.75V; f_{CLK} = 2.5MHz; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (S^+ to S^- and CK^+ to CK^-)						
LED Operating Current	I_{IN}		8	10	15	mA
LED Forward Operating Voltage	V_{IN}	I_{IN} = 10mA		1.55	1.75	V
LED Capacitance (Note 9)	C_{IN}			60		pF
LOGIC OUTPUT (DATA)						
Output Low Voltage	V_{OL} V_{OL}	I_{SINK} = 1.6mA I_{SINK} = 13mA	0.25		0.4 0.6	V
Output High Current	I_{OH}	V_{DATA} = 5.5 V		0.02	250	µA
POWER REQUIREMENTS						
Analog Positive Supply Voltage	$V_{ISO\ V+}$	±5% for Specified Performance	4.75		5.25	V
Analog Negative Supply Voltage (Note 10)	$V_{ISO\ V-}$	±5% for Specified Performance	-15.75		-11.4	V
Analog Positive Supply Current	$I_{ISO\ V+}$	START = V_{DD}, AIN = 0V		25	44	mA
Analog Negative Supply Current	$I_{ISO\ V-}$	START = V_{DD}, AIN = 0V		-6	-12	mA
Digital Positive Supply Voltage	V_{CC}		4.75		5.25	V
Digital Positive Supply Current	I_{CC}			10	18	mA
Power Dissipation		$V_{ISO\ V+}$ = +5V, $V_{ISO\ V-}$ = -15V, V_{CC} = +5V		265	495	mW
TIMING CHARACTERISTICS (Note 11)						
CLOCK Pulse Width	t_{CH} t_{CL}	CLOCK HIGH CLOCK LOW	60 80			ns
START Pulse Width	t_{SH} t_{SL}	START HIGH START LOW	60 80			ns
START to CLOCK Skew	t_{SC0} t_{SC1}	Leading CLOCK Leading CLOCK + 1	250		100	ns
CLOCK to DATA Delay	t_{PD}	T_A = 25°C		175	250	ns

Note 1: Isolation voltage is measured between pins 1 to 8 connected together and pins 9 to 16 connected together.
Note 2: Guaranteed by the "2 second withstand test voltage," which is 100% production tested.
Note 3: Typical change over temp is ±1 LSB.
Note 4: $V_{ISO\ V+}$ = +5V, $V_{ISO\ V-}$ = -15V, FS = +5.000V or +2.500V. Ideal last code transition = FS - 3/2LSB
Note 5: Full Scale Tempco = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 6: Includes internal reference drift.
Note 7: V_{REF} Tempco = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 8: Output current should not change during conversion.
Note 9: Guaranteed by design, not subject to test.
Note 10: Specified performance with -12V supply is guaranteed by testing offset and full scale errors.
Note 11: Timing specifications are sample tested to LTPD = 10 at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

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Pin Description

PIN DIP	NAME	FUNCTION
1	ISO DGND	Isolated Digital Ground
2	ISO V^-	Analog Negative Supply, -12V or -15V
3	ISO V^+	Analog Positive Supply, +5V
4	AIN	Analog Input, 0V to +5V Unipolar
5	REF	Reference Voltage Output, -5.25V
6	ISO AGND	Isolated Analog Ground. Normally tied to ISO DGND
7	TP	Test Pin. Leave unconnected
8	ISO DGND	Isolated Digital Ground
ELECTRICAL ISOLATION BARRIER		
9	V_{CC}	Digital Positive Supply. +5V
10	GND	Digital Ground
11	DATA	Serial Data Output
12	CK^-	Clock$^-$ Input
13	CK^+	Clock$^+$ Input
14	S^+	Conversion Start$^+$ Input
15	S^-	Conversion Start$^-$ Input
16	N.C.	No Connect

Converter Operation

A/D Converter

The MAX171 combines a successive approximation A/D converter and three opto-couplers to convert an unknown analog input to an electrically isolated 12-bit serial output code. The opto-coupled digital interface works with three interface signals: Conversion Start Input (S^+, S^-), Clock Input (CK^+, CK^-), and the Serial Data Output (DATA). Most applications require only a few external passive components to perform the analog-to-digital function. Figure 1 shows the MAX171 in its simplest operational configuration.

Figure 2 shows the MAX171 analog equivalent circuit. The internal digital-to-analog converter (DAC) is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 2.5kΩ resistor. The comparator is essentially a zero-crossing detector with its output feeding back to the SAR input.

Opto-Couplers

The Start (S^+, S^-) and Clock (CK^+, CK^-) inputs to the MAX171 are unbuffered LEDs and require a series resistor of typically 470Ω to a TTL or 5V-CMOS gate to set the drive current. The preferred connection is to tie the resistor from +5V to the LED anode and then connect logic LED cathode as shown in Figure 1. Alternatively, logic drive current may be sourced to a grounded LED, but this requires opposite logic polarity from Figure 1 for both the Start and Clock signals.

The serial data output is an open-collector NPN bipolar transistor, and normally requires a 470Ω pull-up resistor to a +5V supply. The external stray capacitance at the DATA output pin should be kept below 10pF for operation at the maximum clock rate. A low signal at the DATA output represents a logical "1" in the output word.

Power Supplies

The MAX171 requires three power supplies: +5V and -12V to -15V is required on the isolated analog side of the package (ISO V^+, ISO V^-). A separate +5V voltage source (V_{CC}) is required on the digital side of the isolation barrier for the DATA output transmitter.

Digital Interface

Clock — Data Skew

While the opto-isolators used in the MAX171 are fast enough for the specified conversion speed of 5.8µs, they do add a time delay that impacts high speed operation. The A/D cannot begin processing a clock edge before it crosses the isolation barrier. Therefore, the digital I/O signals at the A/D lag/lead the digital signals at the input/output pins. For example, as each successive approximation decision is sent out, it appears at the DATA pin following a delay induced by the opto-coupler. At low conversion rates (below 1MHz clock) these delays are negligible and Clock and Start signals may be applied simultaneously to the MAX171 and to the output register. At clock speeds above 1MHz, these delays become a significant portion of the clock cycle and must be compensated for best performance. Figure 3 illustrates using delay lines in the start and clock signals applied to the output register.

Timing and Control

A conversion cycle is initiated on the rising edge of the conversion start signal that is coincident with a falling edge of the Clock signal. Figure 4 shows a single conversion cycle with a continuous Clock. Once started, a conversion cannot be stopped and transitions at the Start input have no effect until the CURRENT conversion is completed (minimum of 14 clock cycles from the last rising edge of the conversion start signal).

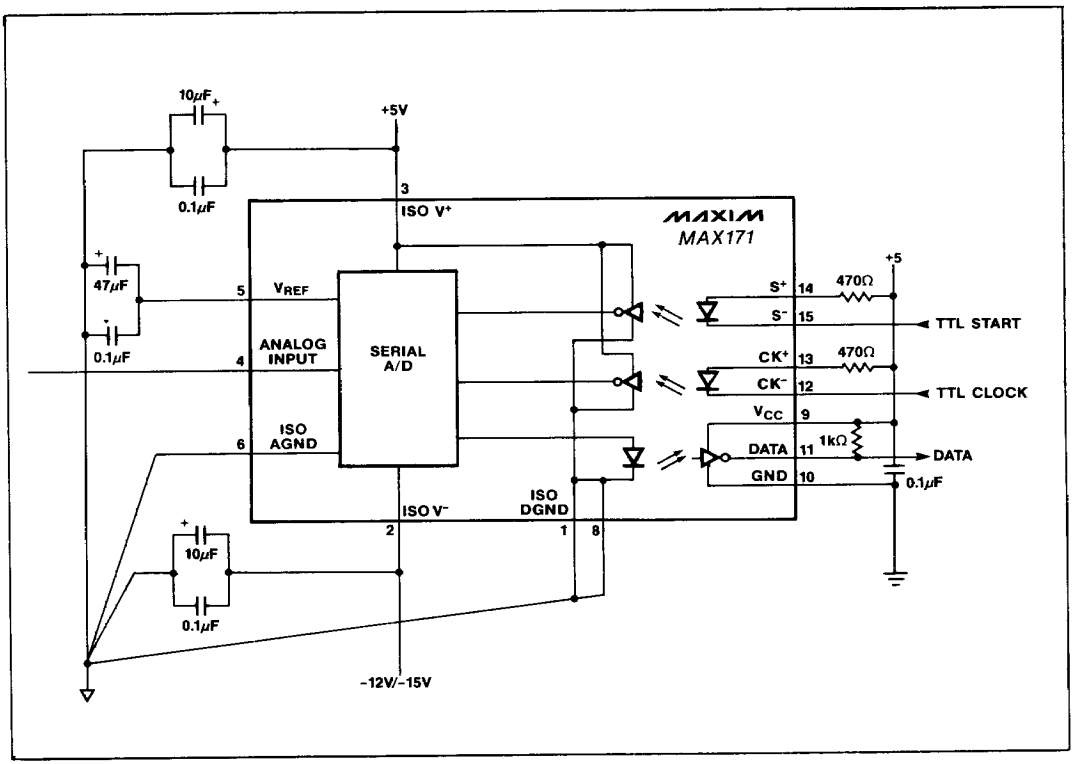

Figure 1. MAX171 Operating Circuit

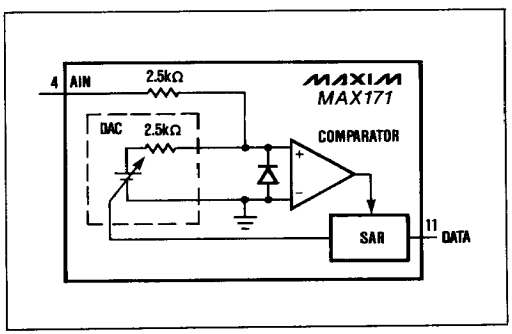

Figure 2. MAX171 Analog Equivalent Circuit

The Conversion Start transition causes the SAR to set B11 (MSB), driving the DAC output to half-scale. The analog input is compared to this value from the time of the conversion start transition until the second falling Clock edge which latches the MSB result and sets the SAR to compare the next bit. The MSB result appears at the DATA output after a delay, t_{PD} from the falling edge of Clock. Each subsequent bit conversion proceeds similarly until all 12 bits of the DAC have been tried. The conversion is completed at the falling edge of the 13th Clock cycle. The DATA output returns high at the falling edge of the 14th Clock cycle and remains so until the next conversion sends out its MSB result.

The next conversion can be started on the 14th Clock cycle of a previous conversion as shown in Figure 4. This allows the maximum throughput rate, one conversion per 14 Clock cycles.

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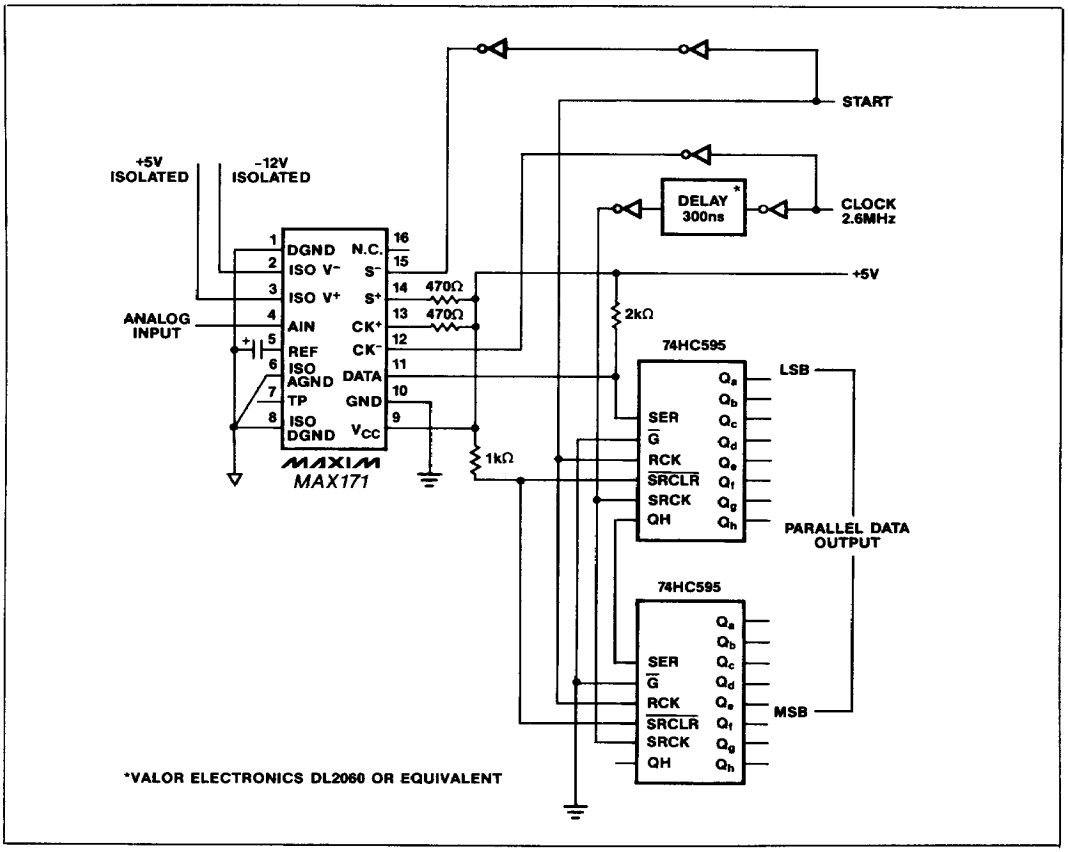

Figure 3. MAX171 Opto-Isolated Conversion with Parallel Data Output

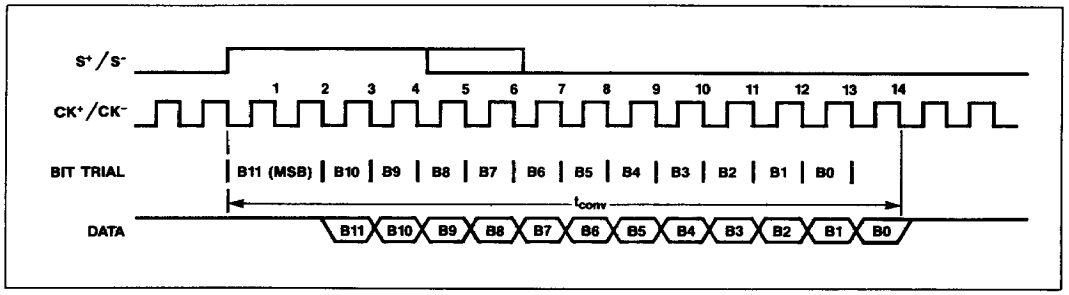

Figure 4. MAX171 Conversion Cycle Timing

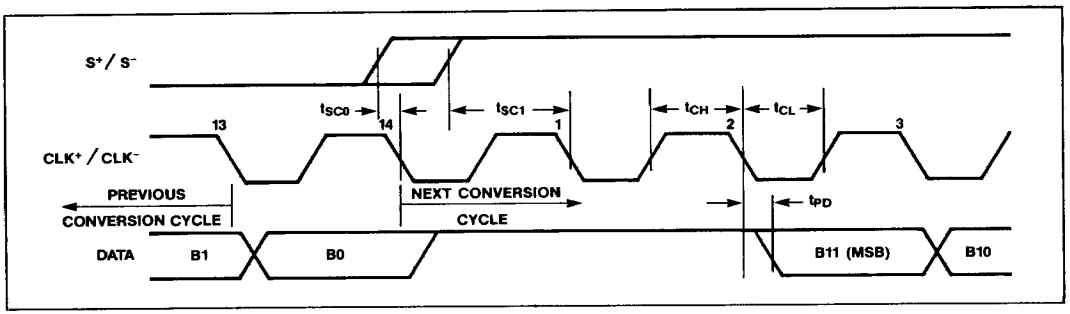

Figure 5. MAX171 Timing Diagram

Conversion Start Timing

Conversion start transitions must arrive within the setup limits t_{SC0} and t_{SC1} relative to the falling edge of the Clock. This guarantees that the serial DATA output stream starts at the second Clock cycle, as shown in Figure 5. Limits on t_{SC0} and t_{SC1} apply whether a conversion is started directly after a previous cycle on the 14th Clock, or if idle Clock pulses occur between conversions. Note that bringing the Start input high on the falling edge of the 14th Clock cycle allows the maximum time for the internal DAC to settle.

Output Coding

The data output from MAX171 is in Straight Binary Code. Other common binary codes, such as 2's complement, offset binary or complementary codes, can be obtained by inverting either the serial data, or the appropriate bit(s) of the parallel data in software or hardware.

Applications

Unipolar Input Operation

Figure 6 shows the nominal input/output transfer function of the MAX171. Code transitions occur halfway between successive integer LSB values. The output coding is binary with 1LSB = 1.22mV (5V/4096).

Offset and Full Scale Adjustment

In applications where the offset and full scale range have to be adjusted for the ADC, use the circuit shown in Figure 7. Note that the amplifier shown could also have been a sample-and-hold. The offset should be adjusted first. Apply 1/2 LSB (0.61mV) at the analog input and adjust the offset of the amplifier until the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

To adjust the full scale range, apply FS - 3/2LSB (4.9817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

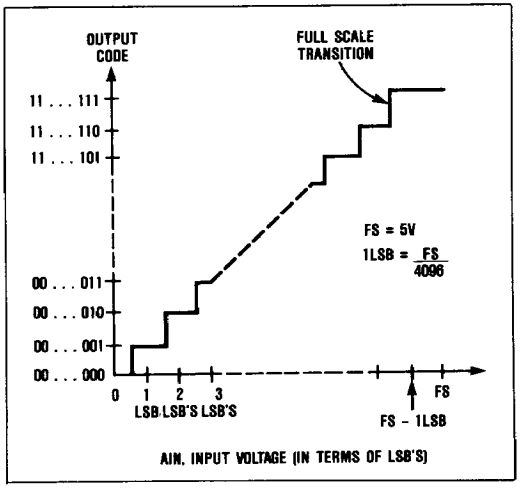

Figure 6. MAX171 Transfer Function

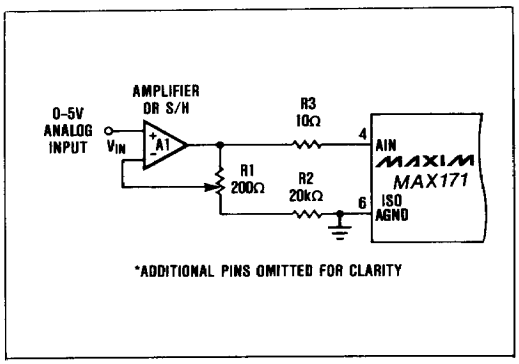

Figure 7. Full-Scale Adjustment

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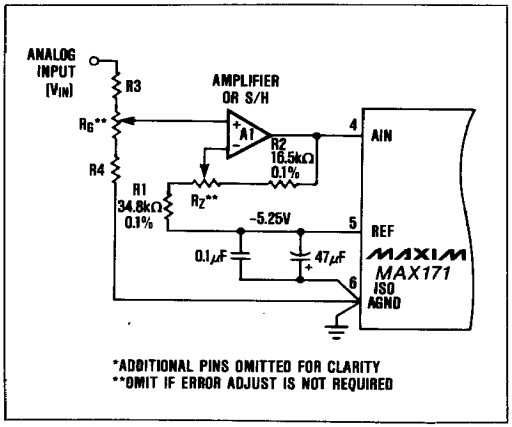

Figure 8. MAX171 Non-Inverting Bipolar Operation

Table 1. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 8

V_{IN} Range (Volts)	R3* (kΩ)	R4* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	3.83	8.25	500	500	0.61	2.49817
±5.0	33.2	16.9	500	1000	1.22	4.99634
±10.0	47.5	9.53	500	500	2.44	9.99268

*R3 and R4 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

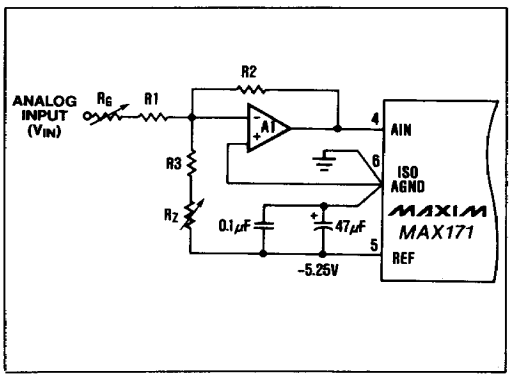

Figure 9. MAX171 Inverting Bipolar Operation

Table 2. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 9

V_{IN} Range (Volts)	R1* (kΩ)	R2* (kΩ)	R3* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2 -3/2 LSBs (Volts)
±2.5	20	20.5	42.2	2000	1000	0.61	2.49817
±5.0	20	10.2	21	1000	1000	1.22	4.99634
±10.0	20	5.11	10.5	500	1000	2.44	9.99268

*R1, R2 and R3 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases, the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 1 and 2.

Figure 8 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 10 shows the ideal transfer function for this mode.

Figure 9 shows the bipolar operation in the inverting mode where the output coding is complementary offset binary. Figure 10 shows the ideal transfer function for the circuit in Figure 9.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drift. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply +1/2LSB to the analog input (see Tables 1 and 2) and adjust R_Z until the output code flickers bewteen the following codes:

For Non-Inverting (Figure 8)	1000 0000 0000 1000 0000 0001
For Inverting (Figure 9)	0111 1111 1111 0111 1111 1110

Apply FS - 3/2LSB (See Tables 1 and 2) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-Inverting (Figure 8)	1111 1111 1110 1111 1111 1111
For Inverting (Figure 9)	0000 0000 0001 0000 0000 0000

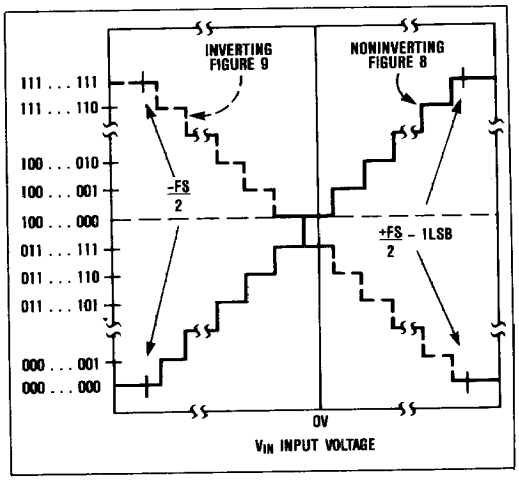

Figure 10. Ideal Input/Output Transfer Characteristics for the Bipolar Circuits in Figures 8 and 9

MAX171 to Sample-and-Hold Interface

The analog input to the MAX171 must be stable to within ±1/2LSB during the entire conversion for specified 12-bit accuracy. This limits the input signal bandwidth to a few Hertz for sinusoidal inputs. For higher bandwidth signals a sample-and-hold should be used.

The signal that starts a conversion can be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. Note that this signal is not available on the isolated side of the barrier and must be separately coupled. The MAX171's DAC is switched at approximately the same time as the sample-and-hold amplifier starts holding the signal. The sample-and-hold amplifier should switch to the HOLD mode before there are any disturbances on the input signal, otherwise code dependent errors will be observed. These can be avoided by starting the MAX171 slightly after the TRACK/HOLD signal by using a gate delay. For synchronous conversion start and CK^+, CK^- as described above, the maximum allowable hold settling time for the sample-and-hold is 600ns.

Circuit Layout

For best system performance printed circuit boards should be used for the MAX171. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX171 package.

The pin configuration of the MAX171 is designed to provide optimum electrical isolation in printed circuit layouts. To maintain this capability, connections from the analog side (Pins 1-8) of the A/D should be separated from the digital side (Pins 9-16) and should not reach or run underneath the package. In some cases it may be best to "notch" or cut out the circuit board material to form an air gap between the pin rows.

Grounding

No special precautions are necessary for the ground connection on the digital side of the MAX171. Connect GND (Pin 10) near the ground of the device that will receive the data. The isolated analog ground (ISO AGND, Pin 6) must be connected to the isolated digital ground pins (ISO DGND, Pins 1 and 8), and together they should be tied to the ground of the analog signal. No connection is needed between GND (Pin 10) and the isolated grounds.

Power-Supply Bypassing

The comparator in the MAX171 is sensitive to high frequency noise in the analog power supplies (ISO V^+, ISO V^-). These supplies should be bypassed close to the device with 0.1μF and 10μF capacitors with minimum lead length. If ISO V^+ is very noisy, a small resistor (10Ω to 20Ω) or inductor can be connected in series to form a low-pass filter with the by-pass capacitors. The digital +5V supply (V_{CC}) should be bypassed to GND with 0.1μF for best performance.

Internal Reference

The MAX171's on-chip reference is laser-trimmed to -5.25V ±1%. The reference output is available at REF (Pin 5) as a reference source for other components and also drives the internal DAC.

For minimum noise, REF must be bypassed with a 47μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor to maintain a low impedance at high frequencies (Figure 1). This capacitance also stabilizes the internal reference buffer amplifier preventing oscillations. No series resistance should be used between REF and the bypass capacitors.

Driving the Analog Input

The input signal leads to AIN and GND should be as short as possible to minimize noise pick-up. If the leads must be long use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5kΩ. The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion. The output impedance of the driving amplifier is reduced by the loop gain at the frequency of interest. With a maximum clock rate of 2.5MHz, amplifiers like the OP-42, AD711, or OP-27 are recommended. At a 1MHz clock rate, a MAX400 or OP-07 can be used.

LH17 Module Product Reliability

For reliability data on Maxim's Module Product Line, consult factory for Reliability Report RR-4A.