Data Sheet | October 12, 2004 | FN6096.1

## Ultra Low ON-Resistance, Low-Voltage, Single Supply, Dual 4 to 1 Analog Multiplexer

The Intersil ISL43L840 device is a precision, bidirectional, analog switches configured as a dual 4-channel multiplexer/demultiplexer, designed to operate from a single +1.6V to +3.6V supply.

ON resistance is 0.5Ω with a +3V supply and 0.62Ω with a single +1.8V supply. Each switch can handle rail to rail analog signals. The off-leakage current is only 4nA max at +25°C and 30nA max at +85°C with a +3.3V supply.

All digital inputs are 1.8V logic-compatible when using a single +3V supply.

The ISL43L840 is a dual 4 to 1 multiplexer device that is offered in a 16 Ld TSSOP and 16 Ld 3x3 QFN packages.

Table 1 summarizes the performance of this family.

**TABLE 1. FEATURES AT A GLANCE**

| | ISL43L840 |
|---|---|
| Configuration | Dual 4:1 Mux |
| **3V $R_{ON}$** | 0.5Ω |
| **3V $t_{RANS}$** | 19ns |
| **1.8V $R_{ON}$** | 0.62Ω |
| **1.8V $t_{RANS}$** | 24ns |
| **Packages** | 16 Ld TSSOP, 16 Ld 3x3 QFN |

## Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

## Features

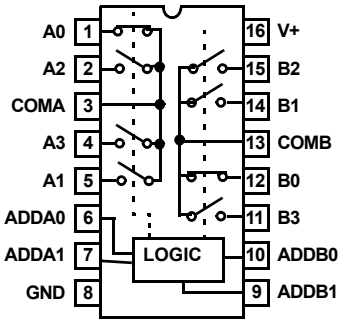
- ON Resistance ($R_{ON}$)
  - V+ = +3.0V . . . . . 0.5Ω
  - V+ = +1.8V . . . . . 0.62Ω
- $R_{ON}$ Matching Between Channels. . . . . .0.12Ω
- $R_{ON}$ Flatness Across Signal Range . . . . . .0.056Ω
- Single Supply Operation. . . . . +1.6V to +3.6V
- Low Power Consumption (PD). . . . . <0.2µW
- Fast Switching Action ($V_S$ = +3V)
  - $t_{RANS}$ . . . . . 19ns
- Guaranteed Break-Before-Make
- High Current Handling Capacity (300mA Continuous)
- Available in 16 Ld 3x3 QFN and 16 Ld TSSOP
- 1.8V CMOS-Logic Compatible (+3V Supply)
- Pb-Free Available as an Option (RoHS Compliant) (see Ordering Info)

## Applications

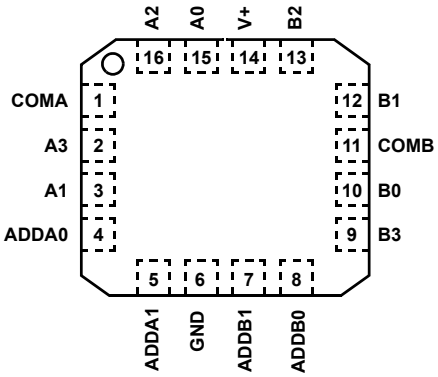
- Battery Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and Video Switching

## Pinouts (Note 1)

**ISL43L840 (TSSOP)**
TOP VIEW




**ISL43L840 (3X3 QFN)**




NOTE:

1. Switches Shown for Logic “0” Inputs.

## Truth Table

| ISL43L840 | | | | |
|---|---|---|---|---|
| **ADDA1** | **ADDA0** | **ADDB1** | **ADDB0** | **SWITCH ON** |
| 0 | 0 | X | X | A0 |
| 0 | 1 | X | X | A1 |
| 1 | 0 | X | X | A2 |
| 1 | 1 | X | X | A3 |
| X | X | 0 | 0 | B0 |
| X | X | 0 | 1 | B1 |
| X | X | 1 | 0 | B2 |
| X | X | 1 | 1 | B3 |

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V, with a 3V supply. X = Don’t Care.

## Pin Descriptions

| PIN | FUNCTION |
|---|---|
| V+ | System Power Supply Input (1.6V to 3.6V) |
| GND | Ground Connection |
| COMA | Analog Switch Channel A Output |
| COMB | Analog Switch Channel B Output |
| A0-A3 | Analog Switch Channel A Input |
| B0-B3 | Analog Switch Channel B Input |
| ADDAx | Address Input Pin |
| ADDBx | Address Input Pin |

## Ordering Information

| PART NO. | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| ISL43L840IV | -40 to 85 | 16 Ld TSSOP | M16.173 |
| ISL43L840IV-T | -40 to 85 | 16 Ld TSSOP Tape & Reel | M16.173 |
| ISL43L840IR | -40 to 85 | 16 Ld 3x3 QFN | L16.3x3 |
| ISL43L840IR-T | -40 to 85 | 16 Ld 3x3 QFN Tape & Reel | L16.3x3 |
| ISL43L840IVZ (See Note) | -40 to 85 | 16 Ld TSSOP (Pb-free) | M16.173 |
| ISL43L840IVZ-T (See Note) | -40 to 85 | 16 Ld TSSOP Tape and Reel (Pb-free) | M16.173 |
| ISL43L840IRZ (See Note) | -40 to 85 | 16 Ld 3x3 QFN (Pb-free) | L16.3x3 |
| ISL43L840IRZ-T (See Note) | -40 to 85 | 16 Ld 3x3 QFN Tape and Reel (Pb-free) | L16.3x3 |

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

## Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to 4.7V
Input Voltages
Ax, Bx, ADDx (Note 2) . . . . . -0.3 to (V+) + 0.3V
Output Voltages
COMx (Note 2) . . . . . -0.3 to (V+) + 0.3V
Continuous Current NO or COM . . . . . ±300mA
Peak Current NO or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD Rating
HBM . . . . . >4kV

## Thermal Information

| Thermal Resistance (Typical, Note 3) | $\theta_{JA}$ (°C/W) |
|---|---|
| 16 Ld TSSOP Package | 150 |
| 16 Ld 3x3 QFN Package | 75 |

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

## Operating Conditions

Temperature Range
ISL43L840IX . . . . . -40°C to 85°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

2. Signals on Ax, Bx, COMx, ADDx exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications - 3V Supply

Test Conditions: $V_{SUPPLY}$ = +2.7V to +3.3V, GND = 0V, $V_{INH}$ = 1.4V, $V_{INL}$ = 0.5V (Notes 4, 8), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | (NOTE 5) MIN | TYP | (NOTE 5) MAX | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON Resistance, $R_{ON}$ | V+ = 2.7V, $I_{COM}$ = 100mA, $V_{Ax\ or}$ $V_{Bx}$ = 0V to V+, (See Figure 5) | 25 | - | 0.5 | 0.75 | Ω |
| | | Full | - | - | 0.8 | Ω |
| $R_{ON}$ Matching Between Channels, $\Delta R_{ON}$ | V+ = 2.7V, $I_{COM}$ = 100mA, $V_{Ax\ or}$ $V_{Bx}$ = Voltage at max $R_{ON}$, (Note 6) | 25 | - | 0.12 | 0.2 | Ω |
| | | Full | - | - | 0.2 | Ω |
| $R_{ON}$ Flatness, $R_{FLAT(ON)}$ | V+ = 2.7V, $I_{COM}$ = 100mA, $V_{Ax\ or}$ $V_{Bx}$ = 0V t0 V+, (Note 7) | 25 | - | 0.056 | 0.15 | Ω |
| | | Full | - | - | 0.15 | Ω |
| Ax or Bx OFF Leakage Current, $I_{Ax(OFF)}$ or $I_{Bx(OFF)}$ | V+ = 3.3V, $V_{COM}$ = 0.3V, 3V, $V_{Ax\ or}$ $V_{Bx}$ = 3V, 0.3V | 25 | -4 | - | 4 | nA |
| | | Full | -30 | - | 30 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 3.3V, $V_{COM}$ = $V_{Ax\ or}$ $V_{Bx}$ = 0.3V, 3V | 25 | -8 | - | 8 | nA |
| | | Full | -60 | - | 60 | nA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage High, $V_{INH}$, $V_{ADDH}$ | | Full | 1.4 | - | - | V |
| Input Voltage Low, $V_{INL}$, $V_{ADDL}$ | | Full | - | - | 0.5 | V |
| Input Current, $I_{INH}$, $I_{INL}$, $I_{ADDH}$, $I_{ADDL}$ | V+ = 3.6V, $V_{INH}$ = $V_{ADD}$ = 0V or V+ (Note 10) | Full | -0.5 | - | 0.5 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Address Transition Time, $t_{TRANS}$ | V+ = 2.7V, $V_{Ax\ or}$ $V_{Bx}$ = 1.5V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 1, Note 10)) | 25 | - | 19 | 28 | ns |
| | | Full | - | - | 30 | ns |
| Break-Before-Make Time, $t_{BBM}$ | V+ = 3.3V, $V_{Ax\ or}$ $V_{Bx}$ = 1.5V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 3, Note 10) | 25 | - | 4 | - | ns |
| | | Full | 1 | - | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω, (See Figure 2) | 25 | - | -96 | - | pC |
| Input OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{Ax\ or}$ $V_{Bx}$ = $V_{COM}$ = 0V, (See Figure 7) | 25 | - | 62 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{Ax\ or}$ $V_{Bx}$ = $V_{COM}$ = 0V, (See Figure 7) | 25 | - | 232 | - | pF |

**Electrical Specifications - 3V Supply** Test Conditions: $V_{SUPPLY}$ = +2.7V to +3.3V, GND = 0V, $V_{INH}$ = 1.4V, $V_{INL}$ = 0.5V (Notes 4, 8), Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | (NOTE 5) MIN | TYP | (NOTE 5) MAX | UNITS |
|---|---|---|---|---|---|---|
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 35pF, f = 100kHz, (See Figures 4 and 6) | 25 | - | 65 | - | dB |
| Crosstalk, (Note 9) | | 25 | - | -100 | - | dB |
| Total Harmonic Distortion (THD) | f = 20Hz to 20kHz, 0.5Vp-p, $R_L$ = 32Ω | 25 | - | 0.02 | - | % |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Range | | Full | 1.6 | - | 3.6 | V |
| Positive Supply Current, I+ | V+ = 3.6V, $V_{INH}$, $V_{ADD}$ = 0V or V+, Switch On or Off | 25 | - | - | 0.05 | µA |
| | | Full | - | - | 0.9 | µA |

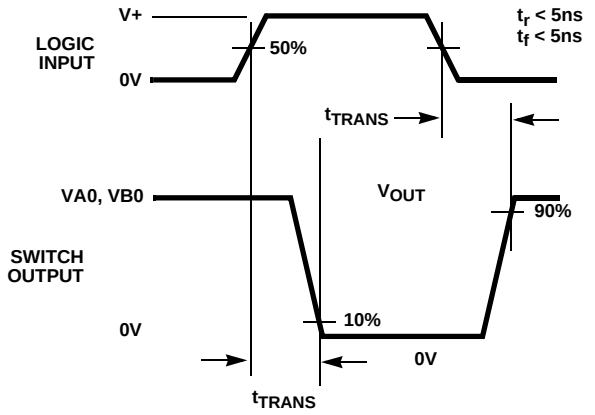
NOTES:

4. $V_{IN}$ = Input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. $R_{ON}$ matching between channels is calculated by subtracting the channel with the highest max Ron value from the channel with lowest max Ron value.
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. Parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.
9. Between any two switches.
10. Guaranteed but not tested.

**Electrical Specifications: 1.8V Supply** Test Conditions: V+ = +1.8V, GND = 0V, $V_{INH}$ = 1V, $V_{INL}$ = 0.4V (Note 4, 8), Unless Otherwise Specified

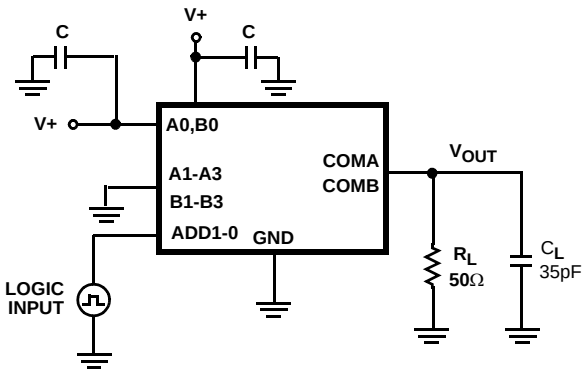
| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (NOTE 5) | TYP | MAX (NOTE 5) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON Resistance, $R_{ON}$ | V+ = 1.8V, $I_{COM}$ = 10.0mA, $V_{Ax}$ or $V_{Bx}$= 1.0V, (See Figure 5) | 25 | - | 0.62 | 0.85 | Ω |
| | | Full | - | - | 0.9 | Ω |
| $R_{ON}$ Matching Between Channels, $\Delta R_{ON}$) | V+ = 1.8V, $I_{COM}$ = 10.0mA, $V_{Ax}$ or $V_{Bx}$ = 1.0V, (See Figure 5) | 25 | - | 0.12 | - | Ω |
| | | Full | - | 0.12 | - | Ω |
| $R_{ON}$ Flatness, $R_{FLAT(ON)}$ | V+ = 1.8V, $I_{COM}$ = 10.0mA, $V_{Ax}$ or $V_{Bx}$ = 0V, 0.9V, 1.6V, (See Figure 5) | 25 | - | 0.14 | - | Ω |
| | | Full | - | 0.14 | - | Ω |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage High, $V_{INH}$, $V_{ADDH}$ | | Full | 1 | - | - | V |
| Input Voltage Low, $V_{INL}$, $V_{ADDL}$ | | Full | - | - | 0.4 | V |
| Input Current, $I_{INH}$, $I_{INL}$, $I_{ADDH}$, $I_{ADDL}$ | V+ = 1.8V, $V_{INH}$, $V_{ADD}$ = 0V or V+ (Note 10) | Full | -0.5 | - | 0.5 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Address Transition Time, $t_{TRANS}$ | V+ = 1.8V, $V_{Ax}$ or $V_{Bx}$ = 1.0V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 1, Note 10) | 25 | - | 24 | 33 | ns |
| | | Full | - | - | 35 | ns |
| Break-Before-Make Time, $t_{BBM}$ | V+ = 1.8V, $V_{Ax}$ or $V_{Bx}$ = 1.0V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 3, Note 10) | 25 | - | 9 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω, (See Figure 2) | 25 | - | -46 | - | pC |

## Test Circuits and Waveforms




Logic input waveform is inverted for switches that have the opposite logic sense.

**FIGURE 1A. ADDRESS $t_{TRANS}$ MEASUREMENT POINTS**




Repeat test for other switches. $C_L$ includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

**FIGURE 1B. ADDRESS $t_{TRANS}$ TEST CIRCUIT**

**FIGURE 1. SWITCHING TIMES**

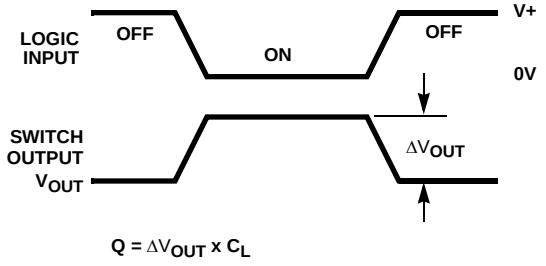
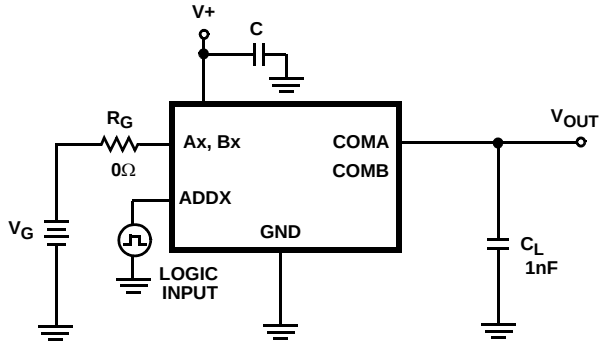



**FIGURE 2A. Q MEASUREMENT POINTS**




Repeat test for other switches.

**FIGURE 2B. Q TEST CIRCUIT**

**FIGURE 2. CHARGE INJECTION**

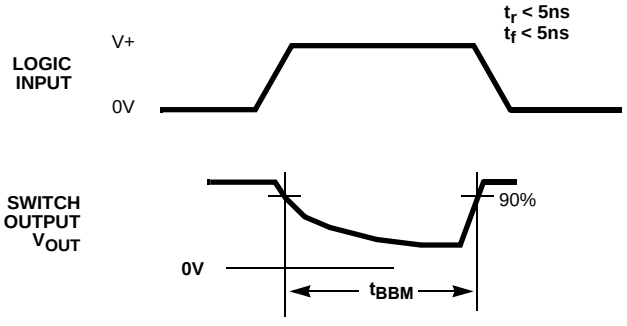
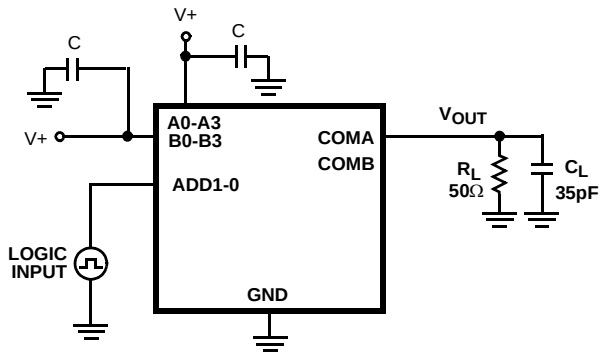



**FIGURE 3A. $t_{BBM}$ MEASUREMENT POINTS**




Repeat test for other switches. $C_L$ includes fixture and stray capacitance.

**FIGURE 3B. $t_{BBM}$ TEST CIRCUIT**

**FIGURE 3. BREAK-BEFORE-MAKE TIME**

## Test Circuits and Waveforms (Continued)

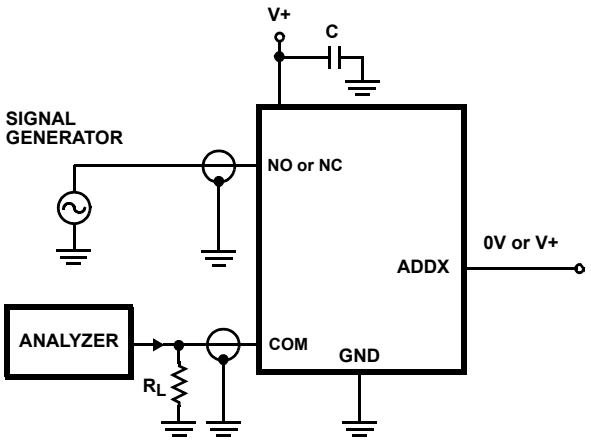



FIGURE 4. OFF ISOLATION TEST CIRCUIT

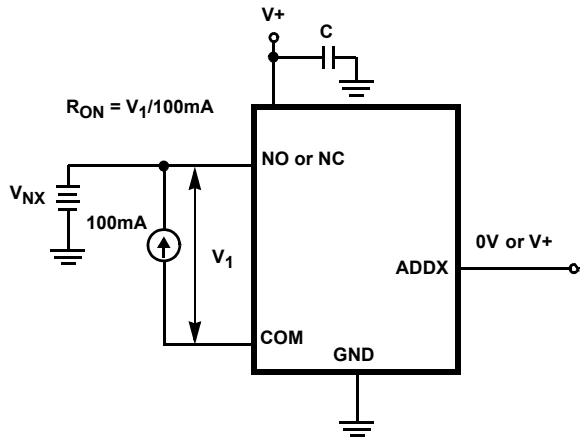



FIGURE 5. $R_{ON}$ TEST CIRCUIT

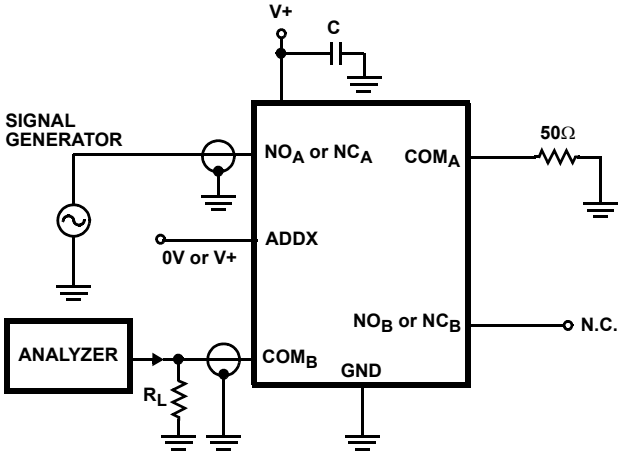



FIGURE 6. CROSSTALK TEST CIRCUIT

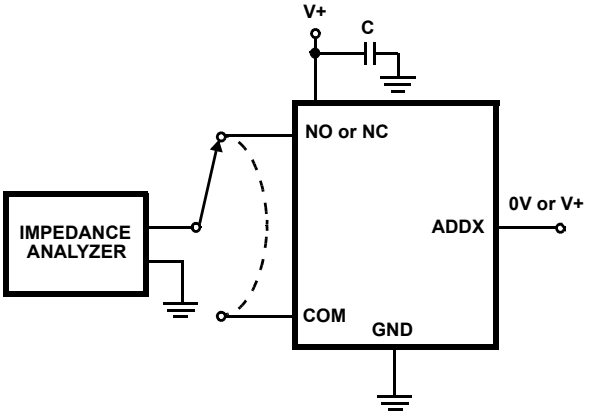



FIGURE 7. CAPACITANCE TEST CIRCUIT

## Detailed Description

The ISL43L840 analog switches offer precise switching capability from a single 1.6V to 3.6V supply with low on-resistance (0.5Ω) and high speed operation ($t_{RANS}$ = 19ns). The device is especially well-suited to portable battery powered equipment thanks to the low operating supply voltage (1.6V), low power consumption (0.2µW), and low leakage currents (60nA max). High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

### Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low $R_{ON}$ switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch signal range is

reduced and the resistance may increase, especially at low supply voltages.

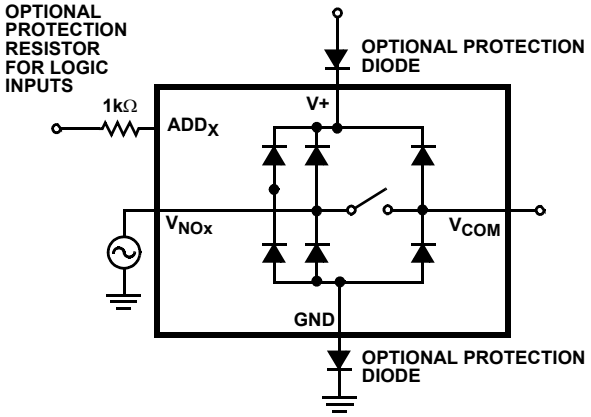



**FIGURE 8. OVERVOLTAGE PROTECTION**

### *Power-Supply Considerations*

The ISL43L840 construction is typical of most CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL43L840 4.7V maximum supply voltage provides plenty of room for the 10% tolerance of 3.6V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.6V but the part will operate with a supply below 1.5V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

### *Logic-Level Thresholds*

The device is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2.0V to 3.6V (see Figure 13). At 3.6V the $V_{IH}$ level is about 1.27V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

### *High-Frequency Performance*

In 50Ω systems, signal response is reasonably flat even past 10MHz with a -3dB bandwidth of 70MHz (see Figure 15). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off Isolation is the resistance to this feed-through, while Crosstalk indicates the amount of feed-through from one switch to another. Figure 16 details the high Off Isolation and Crosstalk rejection provided by this family. At 100kHz, Off Isolation is about 65dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

### *Leakage Considerations*

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

## Typical Performance Curves $T_A$ = 25°C, Unless Otherwise Specified

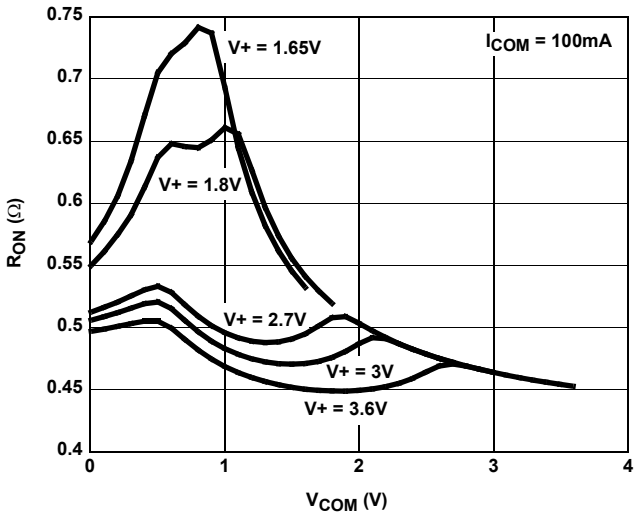



FIGURE 9. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

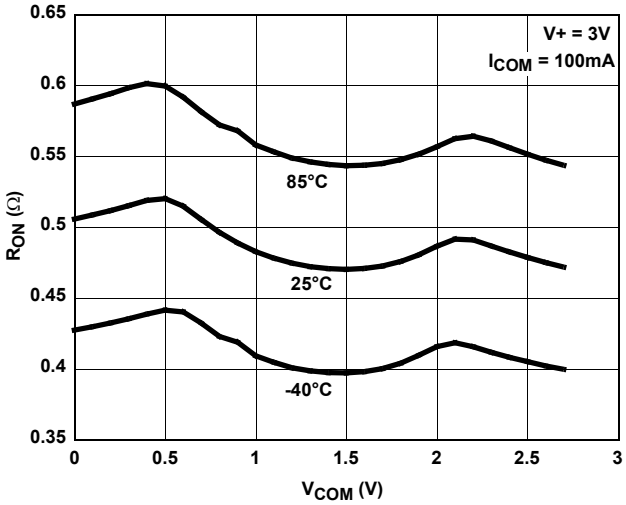



FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

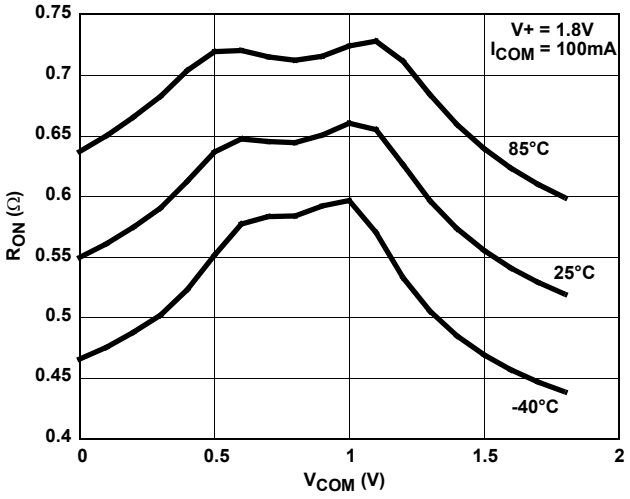



FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

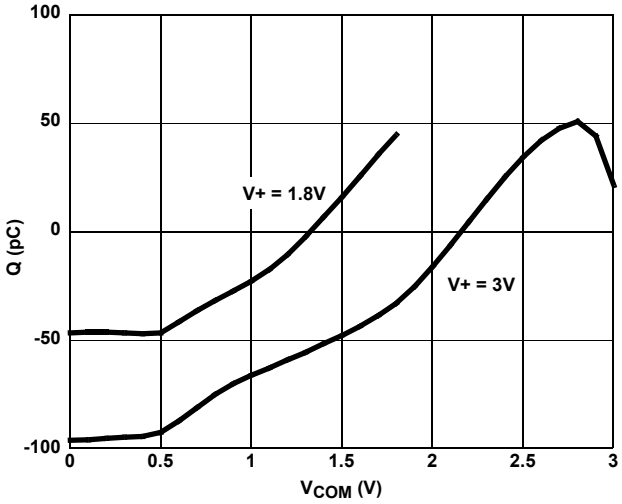



FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

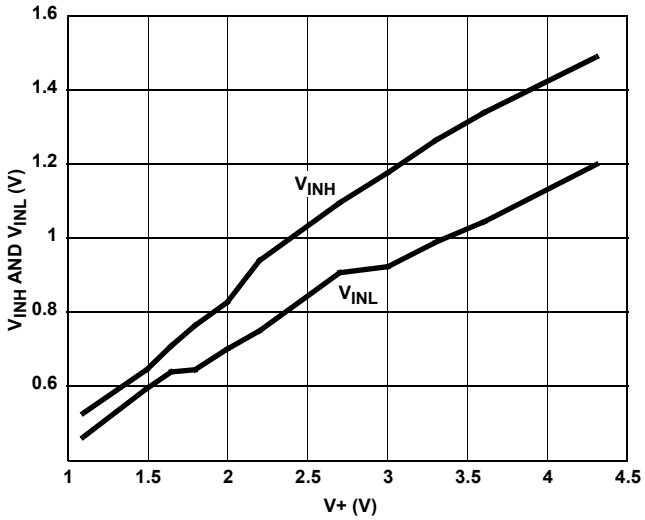



FIGURE 13. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

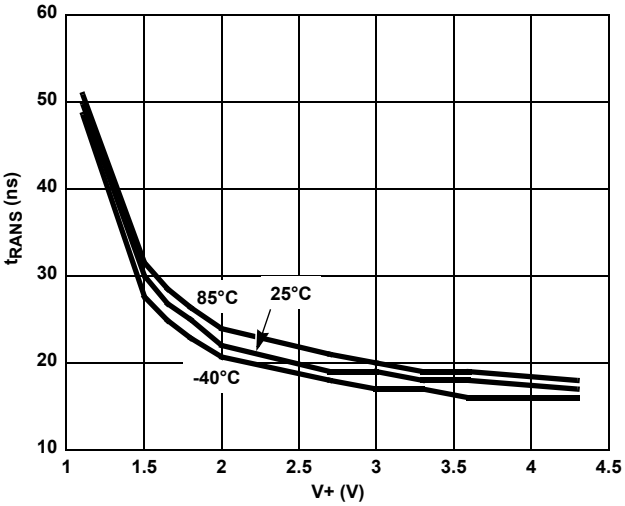



FIGURE 14. ADDRESS TRANS TIME vs SUPPLY VOLTAGE

## Typical Performance Curves $T_A$ = 25°C, Unless Otherwise Specified **(Continued)**

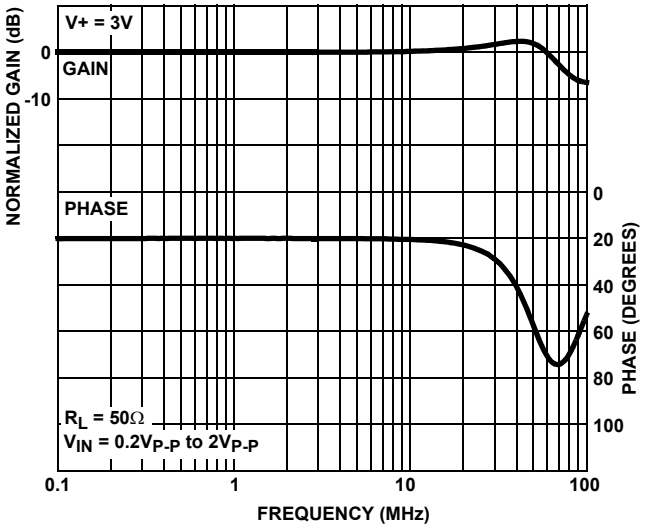



FIGURE 15. FREQUENCY RESPONSE

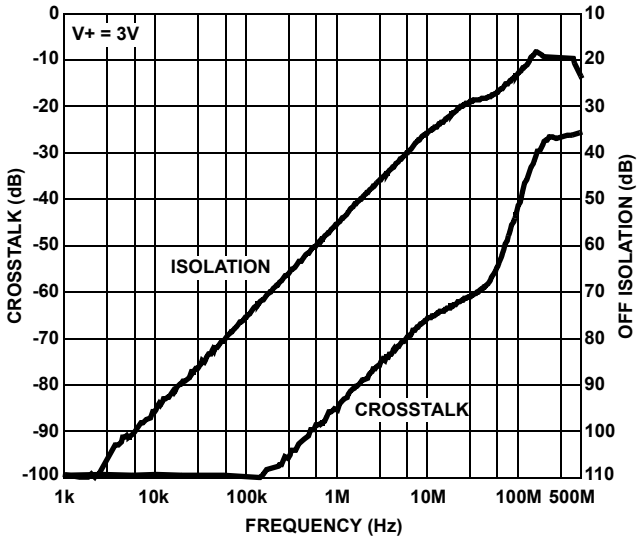



FIGURE 16. CROSSTALK AND OFF ISOLATION

## Die Characteristics

**SUBSTRATE POTENTIAL (POWERED UP):**

GND (QFN Paddle Connection: To Ground or Float)

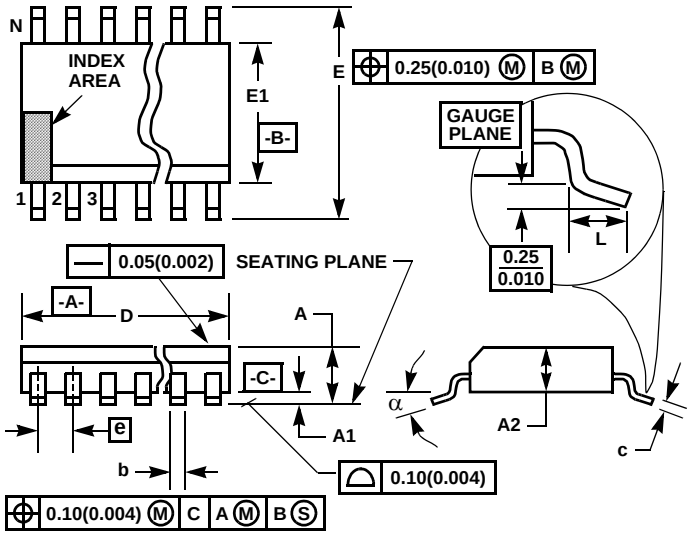
**TRANSISTOR COUNT:**

228

**PROCESS:**

Submicron CMOS

## Thin Shrink Small Outline Plastic Packages (TSSOP)




NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

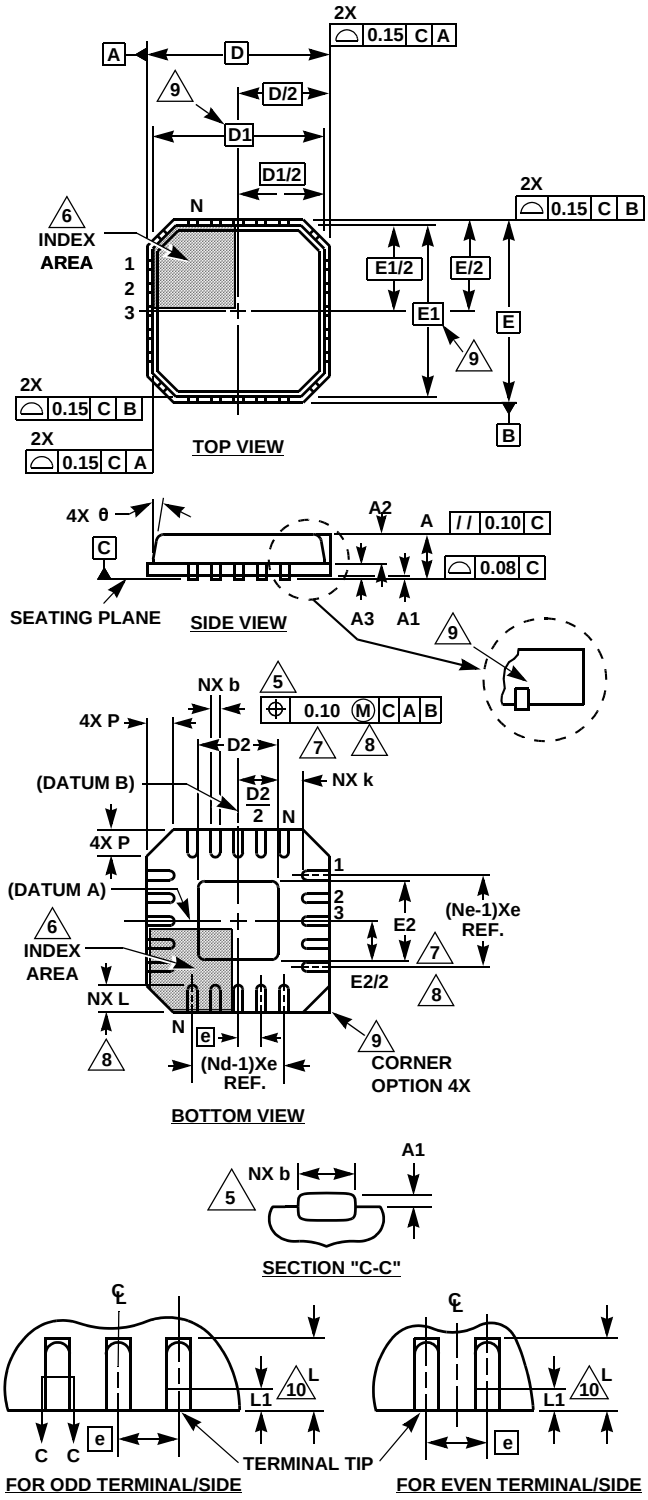
### M16.173

**16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.043 | - | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.033 | 0.037 | 0.85 | 0.95 | - |
| b | 0.0075 | 0.012 | 0.19 | 0.30 | 9 |
| c | 0.0035 | 0.008 | 0.09 | 0.20 | - |
| D | 0.193 | 0.201 | 4.90 | 5.10 | 3 |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 | 4 |
| e | 0.026 BSC | | 0.65 BSC | | - |
| E | 0.246 | 0.256 | 6.25 | 6.50 | - |
| L | 0.020 | 0.028 | 0.50 | 0.70 | 6 |
| N | 16 | | 16 | | 7 |
| α | $0^o$ | $8^o$ | $0^o$ | $8^o$ | - |

Rev. 1 2/02

## *Quad Flat No-Lead Plastic Package (QFN)*
## *Micro Lead Frame Plastic Package (MLFP)*




## L16.3x3

**16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**

| SYMBOL | MILLIMETERS | | | NOTES |
|---|---|---|---|---|
| | MIN | NOMINAL | MAX | |
| A | 0.80 | 0.90 | 1.00 | - |
| A1 | - | - | 0.05 | - |
| A2 | - | - | 1.00 | 9 |
| A3 | | 0.20 REF | | 9 |
| b | 0.18 | 0.23 | 0.30 | 5, 8 |
| D | | 3.00 BSC | | - |
| D1 | | 2.75 BSC | | 9 |
| D2 | 1.35 | 1.50 | 1.65 | 7, 8, 10 |
| E | | 3.00 BSC | | - |
| E1 | | 2.75 BSC | | 9 |
| E2 | 1.35 | 1.50 | 1.65 | 7, 8, 10 |
| e | | 0.50 BSC | | - |
| k | 0.20 | - | - | - |
| L | 0.30 | 0.40 | 0.50 | 8 |
| N | | 16 | | 2 |
| Nd | | 4 | | 3 |
| Ne | | 4 | | 3 |
| P | - | - | 0.60 | 9 |
| $\theta$ | - | - | 12 | 9 |

Rev. 1 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & $\theta$ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220VEED-2 Issue C, except for the E2 and D2 MAX dimension.