

Low Voltage / Low Power CMOS 16-bit MICROCONTROLLERS

TMP93CW40DF / TMP93CW41DF

1. OUTLINE AND DEVICE CHARACTERISTICS

TMP93CW40/W41 are high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP93CW40/CW41 enable low-voltage and low consumption power operation.

The TMP93CW40/W41 are housed in 100-pin flat package.

The device characteristics are as follows:

- (1) Original 16-bit CPU (900/L CPU)
 - TLCS-90 instruction mnemonic upward compatible
 - 16M-byte linear address space
 - General-purpose registers and register bank system
 - 16-bit multiplication / division and bit transfer / arithmetic instructions
 - High-speed micro DMA : 4 channels (1.6 μ s / 2 bytes at 20 MHz)
- (2) Minimum instruction execution time : 200 ns at 20 MHz
- (3) Internal RAM : 4K byte
Internal ROM :

TMP93CW40	128K-byte ROM
TMP93CW41	None

- (4) External memory expansion
 - Can be expanded up to 16M bytes (for both programs and data).
 - AM8 / $\overline{16}$ pin (select the external data bus width)
 - Can mix 8- and 16-bit external data buses.
... Dynamic data bus sizing
- (5) 8-bit timer : 2 channels
- (6) 8-bit PWM timer : 2 channels
- (7) 16-bit timer : 2 channels
- (8) Pattern generator : 4 bits, 2 channels
- (9) Serial interface : 2 channels
- (10) 10-bit A/D converter : 8 channels
- (11) Watchdog timer
- (12) Chip select / wait controller : 3 blocks
- (13) Interrupt functions
 - 2 CPU interrupts..... SWI instruction, and Illegal instruction
 - 14 internal interrupts
 - 6 external interrupts 7-level priority can be set.
- (14) I/O ports
79 pins for TMP93CW40 and 61 pins for TMP93CW41
- (15) Standby function : 4 halt modes (Run, Idle2, Idle1, Stop)

- (16) Clock Gear Function
- Dual clock Operation
 - Clock gear : High-frequency clock can be changed f_c to $f_c / 16$.
- (17) Wide Operating Voltage
- $V_{cc} = 2.7$ to 5.5 V
- (18) Package

Type No.	Package
TMP93CW40DF TMP93CW41DF	QFP100-P-1414-0.50C

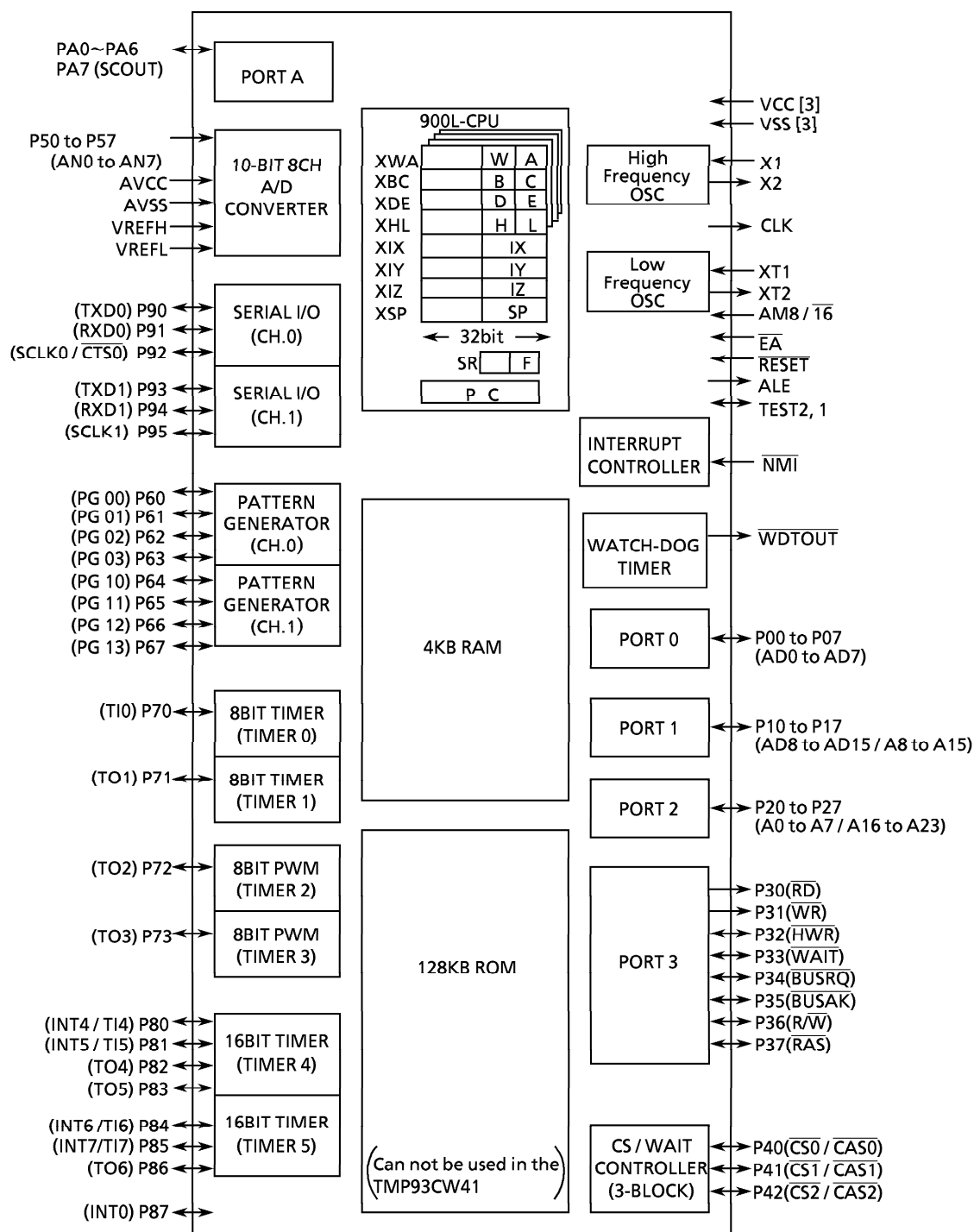


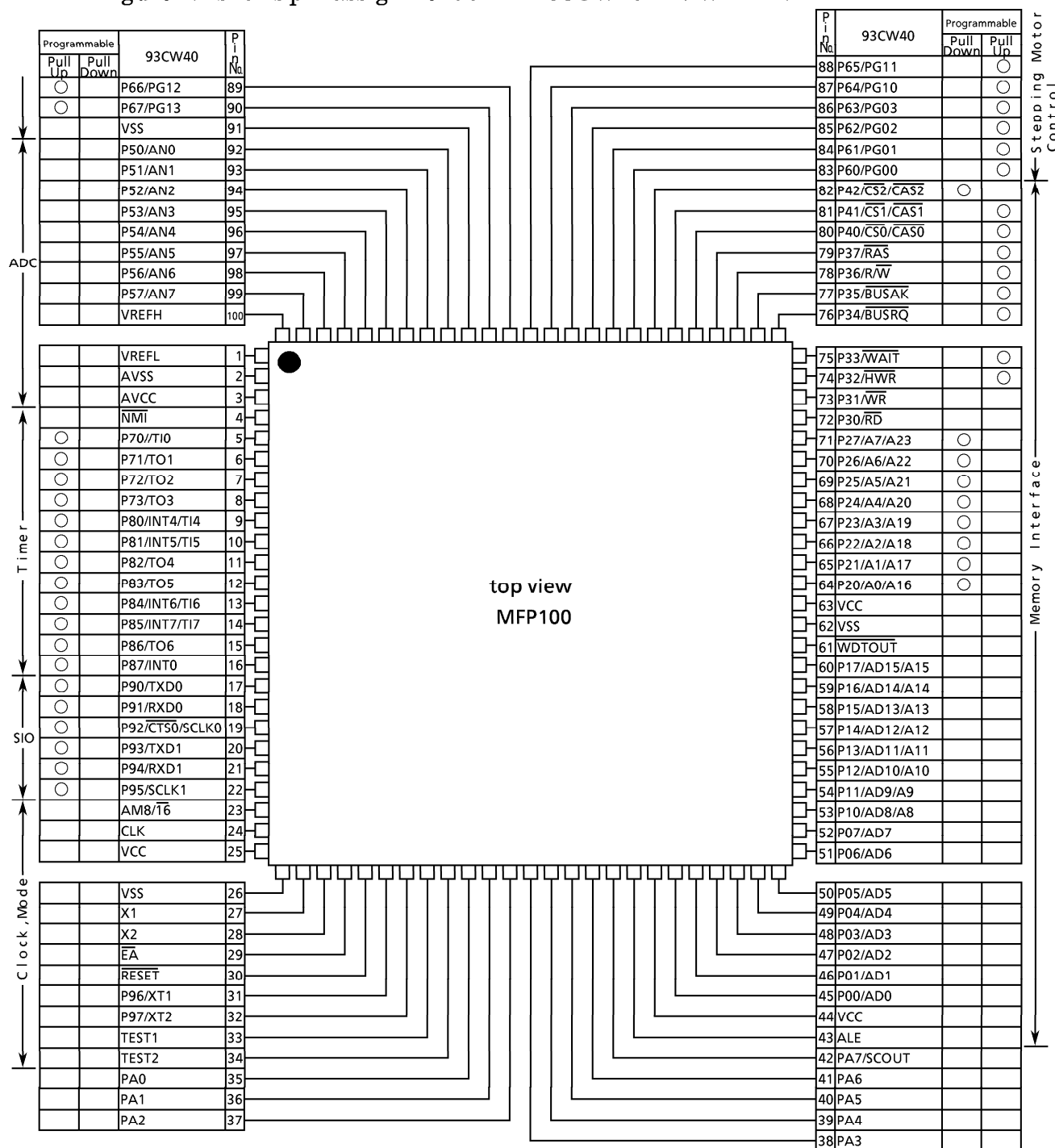
Figure 1 TMP93CW40/TMP93CW41 Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input / output pins for the TMP93CW40/W41, their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP93CW40DF / W41DF.



(Note) Because the TMP93CW41 does not have an internal ROM, P00 to P17 pins are fixed to AD0 to AD15 (the case of AM8 / T6 = 0), or to AD0 to AD7, A8 to A15 (the case of AM8 / T6 = 1); P30 to RD; and P31 to WR.

Figure 2.1 Pin Assignment (100-pin MFP)

2.2 Pin Names and Functions

The names of input / output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected on a bit basis Address/data (lower): 0 to 7 for address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected on a bit basis Address data (upper): 8 to 15 for address/data bus Address: 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: 0 to 7 for address bus Address: 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0 - 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, $\overline{R/W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, $\overline{R/W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving $\overline{BUSRQ}$. (For external DMAC)
P36 $\overline{R/W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs RAS strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs CAS strobe for DRAM when address is within specified address area.

Note : With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins.

Pin name	Number of pins	I/O	Functions
P41 CS1 CAS1	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs CAS strobe for DRAM if address is within specified address area.
P42 CS2 CAS2	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs CAS strobe for DRAM if address is within specified address area.
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Input port Analog input: Input to A/D converter
VREFH	1	Input	Pin for reference voltage input to A/D converter (H)
VREFL	1	Input	Pin for reference voltage input to A/D converter (L)
P60 to P63 PG00 to PG03	4	I/O Output	Ports 60 - 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 00 - 03
P64 to P67 PG10 to PG13	4	I/O Output	Ports 64 - 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor) Pattern generator ports: 10 - 13
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count / capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count / capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Pin name	Number of pins	I/O	Functions
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count / capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count / capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level / rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 CTS0 SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial Clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
PA0 to PA6	7	I/O	Port A: I/O ports
PA7 SCOUT	1	I/O Output	Port A7: I/O port System Clock Output: Outputs system clock or 1/2 oscillation clock for synchronizing to external circuit.
WDTOUT	1	Output	Watchdog timer output pin
NMI	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs $\lceil \text{System Clock} \div 2 \rceil$ Clock. Pulled-up during reset. can be set to Output Disable for reducing noise.
EA	1	Input	External access: "0" should be inputted with TMP93CW41. "1" should be inputted with TMP93CW40.

Pin name	Number of pins	I/O	Functions
AM8 / $\overline{16}$	1	Input	Address Mode: Selects external Data Bus width. (the case of TMP93CW40) "1" should be inputted. The Data Bus Width for external access is set by Chip Select / WAIT Control register, Port 1 Control register. (the case of TMP93CW41) "0" should be inputted with fixed 16bit Bus Width or 16bit Bus interlarded with 8bit Bus. "1" should be inputted with fixed 8bit Bus Width.
ALE	1	Output	Address Latch Enable Can be set to Output Disable for reducing noise.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
XT1 P96	1	Input I/O	Low Frequency Oscillator connecting pin Port 96: I/O port (Open Drain Output)
XT2 P97	1	Output I/O	Low Frequency Oscillator connecting pin Port 97: I/O port (Open Drain Output)
TEST1 / TEST2	2	Output / Input	TEST1 Should be connected with TEST2 pin.
VCC	3		Power supply pin
VSS	3		GND pin (0 V)
AVCC	1		Power supply pin for A/D converter
AVSS	1		GND pin for A/D converter (0 V)

Note : Pull-up / pull-down resistor can be released from the pin by software.

3. OPERATION

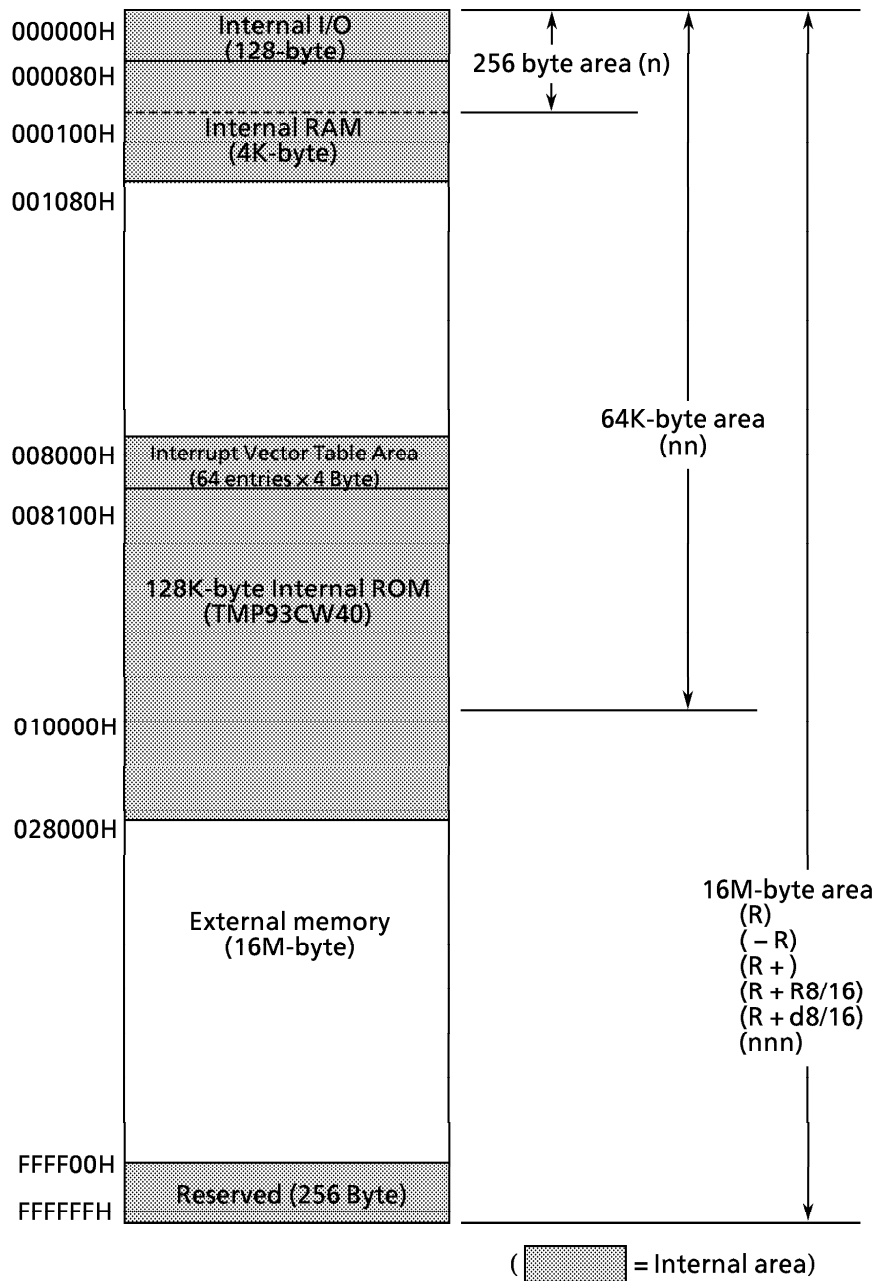
This section describes in blocks the functions and basic operations of TMP93CW40/W41 devices.

3.1 CPU

The TMP93CW40 / W41 devices have a built-in high-performance 16-bit CPU (900/L CPU). (For CPU operation, see TLCS-900/L CPU in the previous section).

3.2 Memory Map

Figure 3.2 is a memory map of the TMP93CW40/W41.



Note : Resetting sets the stack pointer (XSP) to 100H.
The 256 Byte Area from FFFF00H to FFFFFFH can not be used.

Figure3.2 Memory map

4. ELECTRICAL CHARACTERISTICS (PRELIMINARY)

4.1 Absolute Maximum Ratings

(TMP93CW40DF, TMP93CW41DF)

"X" used in an expression shows a frequency of clock f_{ppH} selected by $SYSCR1 < SYSCK >$. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value in an example is calculated at f_c , $gear = 1/f_c$ ($SYSCR1 < SYSCK$, $GEAR_{2\text{ to }0} = "0000"$).

Symbol	Parameter	Rating	Unit
V _{CC}	Power Supply Voltage	− 0.5 to 6.5	V
V _{IN}	Input Voltage	− 0.5 to V _{CC} + 0.5	V
Σ I _{OL}	Output Current (total)	120	mA
Σ I _{OH}	Output Current (total)	− 80	mA
P _D	Power Dissipation (Ta = 85 °C)	600	mW
T _{SOLDER}	Soldering Temperature (10 s)	260	°C
T _{STG}	Storage Temperature	− 65 to 150	°C
T _{OPR}	Operating Temperature	− 40 to 85	°C

4.2 DC Characteristics (1/2)

Ta = − 40 to 85 °C

Symbol	Parameter		Min.	Typ (note 1)	Max.	Unit	Condition
V _{CC}	Power Supply Voltage (AV _{CC} = V _{CC} AV _{SS} = 0V)		4.5 2.7		5.5	V	f _c = 4 to 20 MHz f _s = 30 to 34 kHz f _c = 4 to 12.5 MHz
V _{IL}	Input Low Voltage	AD0 to 15			0.8	V	V _{CC} ≥ 4.5 V
V _{IL1}		Port 2 to A (except P87)			0.6		V _{CC} < 4.5 V
V _{IL2}		RESET, NMI, INT0			0.3 V _{CC}		V _{CC} = 2.7 to 5.5 V
V _{IL3}		EA, AM8/16			0.25 V _{CC}		
V _{IL4}		X1			0.3		
V _{IL}	Input High Voltage	AD0 to 15	2.2 2.0				V _{CC} ≥ 4.5 V
V _{IH1}		Port 2 to A (except P87)			V _{CC} + 0.3		V _{CC} < 4.5 V
V _{IH2}		RESET, NMI, INT0	0.7V _{CC}				V _{CC} = 2.7 to 5.5 V
V _{IH3}		EA, AM8/16	V _{CC} − 0.3				
V _{IH4}		X1	0.8V _{CC}				
V _{OL}	Output Low Voltage				0.45	V	I _{OL} = 1.6 mA (V _{CC} = 2.7 to 5.5 V)
V _{OH1}	Output High Voltage		2.4				I _{OH} = − 400 μA (V _{CC} = 3 V ± 10 %)
V _{OH2}			4.2				I _{OH} = − 400 μA (V _{CC} = 5 V ± 10 %)

(note1) Typical values are for Ta = 25 °C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Symbol	Parameter	Min.	Typ. (Note 1)	Max.	Unit	Condition
I DAR (note 2)	Darlington Drive Current (8 Output Pins Max)	- 1.0		- 3.5	mA	V EXT = 1.5 V R EXT = 1.1 k Ω (when V CC = 5 V $\pm$ 10 %)
I LI	Input Leakage Current		0.02	$\pm$ 5	μ A	0.0 $\leq$ V IN $\leq$ V CC
I LO	Output Leakage Current		0.05	$\pm$ 10	μ A	0.2 $\leq$ V IN $\leq$ V CC - 0.2
V STOP	Powerdown Voltage (at Stop, RAM Back-up)	2.0		6.0	V	V IL2 = 0.2V CC, V IH2 = 0.8V CC
R RST	RESET Pull-up Resistor	50 80		150 200	k Ω	V CC = 5 V $\pm$ 10 % V CC = 3 V $\pm$ 10 %
C IO	Pin Capacitance			10	pF	f c = 1 MHz
V TH	Schmitt Width RESET, NMI, INT0	0.4	1.0		V	
RKL	Programmable Pull-down Resistor	10 30		80 150	k Ω	V CC = 5 V $\pm$ 10 % V CC = 3 V $\pm$ 10 %
RKH	Programmable Pull-up Resistor	50 100		150 300	k Ω	V CC = 5 V $\pm$ 10 % V CC = 3 V $\pm$ 10 %
I CC	Normal (note 3)		19	25	mA	V CC = 5 V $\pm$ 10 % f c = 20 MHz
	Normal2 (note 4)		24	30		
	Run		17	25		
	Idle2		10	15		
	Idle1		3.5	5		
	Normal (note 3)		6.5	10	mA	V CC = 3 V $\pm$ 10 % f c = 10 MHz (Typ: V CC = 3.0 V)
	Normal2 (note 4)		9.5	13		
	Run		5.0	9		
	Idle2		3.0	5		
	Idle1		0.8	1.5		
	Slow (note 3)		20	35	μ A	V CC = 3 V $\pm$ 10 % f s = 32.768 kHz (Typ: V CC = 3.0 V)
	Run		16	30		
	Idle2		10	20		
	Idle1		5	15		
	Stop		0.2	10		V CC = 2.7 to 5.5 V

(note1) Typical values are for Ta = 25 °C and V CC = 5 V unless otherwise noted.

(note2) I-DAR is guranteed for total of up to 8 ports.

(note3) The condition of measurement of I CC (Normal / Slow).

Only CPU operates. Output ports are open and input ports fixed.

(note 4) The condition of measurement of I CC (Normal 2).

CPU and all peripherals operate. Output ports are open and input ports fixed.

4.3 AC Characteristics

(1) $V_{CC} = 5\text{ V} \pm 10\%$

No.	Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	50	31250	62.5		50		ns
2	t_{CLK}	CLK Width	$2x - 40$		85		60		ns
3	t_{AK}	A0 to A23 Valid $\rightarrow$ CLK Hold	$0.5x - 20$		11		5		ns
4	t_{KA}	CLK Valid $\rightarrow$ A0 to A23 Hold	$1.5x - 70$		24		5		ns
5	t_{AL}	A0 to A15 Valid $\rightarrow$ ALE Fall	$0.5x - 15$		16		10		ns
6	t_{LA}	ALE Fall $\rightarrow$ A0 to A15 Hold	$0.5x - 20$		11		5		ns
7	t_{LL}	ALE High Width	$x - 40$		23		10		ns
8	t_{LC}	ALE Fall $\rightarrow$ RD/WR Fall	$0.5x - 25$		6		0		ns
9	t_{CL}	RD/WR Rise $\rightarrow$ ALE Rise	$0.5x - 20$		11		5		ns
10	t_{ACL}	A0 to A15 Valid $\rightarrow$ RD/WR Fall	$x - 25$		38		25		ns
11	t_{ACH}	A0 to A23 Valid $\rightarrow$ RD/WR Fall	$1.5x - 50$		44		25		ns
12	t_{CA}	RD/WR Rise $\rightarrow$ A0 to A23 Hold	$0.5x - 25$		6		0		ns
13	t_{ADL}	A0 to A15 Valid $\rightarrow$ D0 to D15 Input		$3.0x - 55$		133		95	ns
14	t_{ADH}	A0 to A23 Valid $\rightarrow$ D0 to D15 Input		$3.5x - 65$		154		110	ns
15	t_{RD}	RD Fall $\rightarrow$ D0 to D15 Input		$2.0x - 60$		65		40	ns
16	t_{RR}	RD Low Pulse Width	$2.0x - 40$		85		60		ns
17	t_{HR}	RDRise $\rightarrow$ D0 to D15 Hold	0		0		0		ns
18	t_{RAE}	RDRise $\rightarrow$ A0 to A15 Output	$x - 15$		48		35		ns
19	t_{WW}	WR Low Pulse Width	$2.0x - 40$		85		60		ns
20	t_{DW}	D0 to D15 Valid $\rightarrow$ WR Rise	$2.0x - 55$		70		45		ns
21	t_{WD}	WR Rise $\rightarrow$ D0 to D15 Hold	$0.5x - 15$		16		10		ns
22	t_{AWH}	A0 to A23 Valid $\rightarrow$ WAIT Input ^(1 WAIT + n mode)		$3.5x - 90$		129		85	ns
23	t_{AWL}	A0 to A15 Valid $\rightarrow$ WAIT Input ^(1 WAIT + n mode)		$3.0x - 80$		108		70	ns
24	t_{CW}	RD/WR Fall $\rightarrow$ WAIT Hold ^(1 WAIT + n mode)	$2.0x + 0$		125		100		ns
25	t_{APH}	A0 to A23 Valid $\rightarrow$ PORT Input		$2.5x - 120$		36		5	ns
26	t_{APH2}	A0 to A23 Valid $\rightarrow$ PORT Hold	$2.5x + 50$		206		175		ns
27	t_{CP}	WR Rise $\rightarrow$ PORT Valid		200		200		200	ns
28	t_{ASRH}	A0 to A23 Valid $\rightarrow$ RAS Fall	$1.0x - 40$		23		10		ns
29	t_{ASRL}	A0 to A15 Valid $\rightarrow$ RAS Fall	$0.5x - 15$		16		10		ns
30	t_{RAC}	RAS Fall $\rightarrow$ D0 to D15 Input		$2.5x - 70$		86		55	ns
31	t_{RAH}	RAS Fall $\rightarrow$ A0 to A15 Hold	$0.5x - 15$		16		10		ns
32	t_{RAS}	RAS Low Pulse Width	$2.0x - 40$		85		60		ns
33	t_{RP}	RAS High Pulse Width	$2.0x - 40$		85		60		ns
34	t_{RSH}	CAS Fall $\rightarrow$ RAS Rise	$1.0x - 40$		23		10		ns
35	t_{RSC}	RAS Rise $\rightarrow$ CAS Rise	$0.5x - 25$		6		0		ns
36	t_{RCD}	RAS Fall $\rightarrow$ CAS Fall	$1.0x - 40$		23		10		ns
37	t_{CAC}	CAS Fall $\rightarrow$ D0 to D15 Input		$1.5x - 65$		29		10	ns
38	t_{CAS}	CAS Low Pulse Width	$1.5x - 30$		64		40		ns

AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
(However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, RD, WR, HWR, R/W, CLK, RAS, CAS0 to CAS2)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
High 0.8 V_{CC} / Low 0.2 V_{CC} (Except for AD0 to AD15)

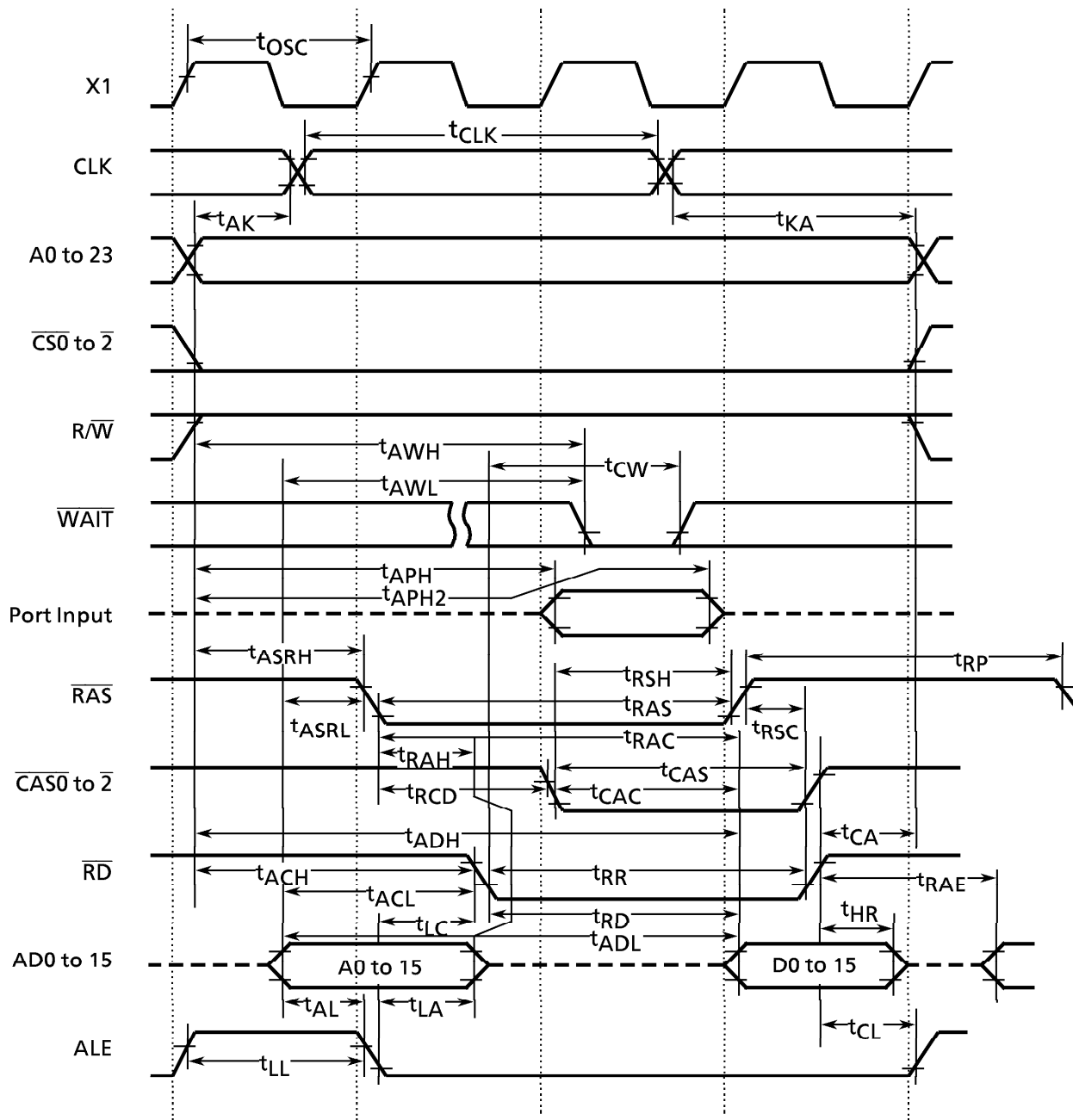
(2) $V_{CC} = 3\text{ V} \pm 10\%$

No.	Symbol	Parameter	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	80	250	80		ns
2	t_{CLK}	CLK width	$2x - 40$		120		ns
3	t_{AK}	A0-23 Valid $\rightarrow$ CLK Hold	$0.5x - 30$		10		ns
4	t_{KA}	CLK Valid $\rightarrow$ A0-23 Hold	$1.5x - 80$		40		ns
5	t_{AL}	A0-15 Valid $\rightarrow$ ALE fall	$0.5x - 35$		5		ns
6	t_{LA}	ALE fall $\rightarrow$ A0-15 Hold	$0.5x - 35$		5		ns
7	t_{LL}	ALE High width	$x - 60$		20		ns
8	t_{LC}	ALE fall $\rightarrow$ $\overline{RD}/\overline{WR}$ fall	$0.5x - 35$		5		ns
9	t_{CL}	$\overline{RD}/\overline{WR}$ rise $\rightarrow$ ALE rise	$0.5x - 40$		0		ns
10	t_{ACL}	A0-15 Valid $\rightarrow$ $\overline{RD}/\overline{WR}$ fall	$x - 50$		30		ns
11	t_{ACH}	A0-23 Valid $\rightarrow$ $\overline{RD}/\overline{WR}$ fall	$1.5x - 50$		70		ns
12	t_{CA}	$\overline{RD}/\overline{WR}$ rise $\rightarrow$ A0-23 Hold	$0.5x - 40$		0		ns
13	t_{ADL}	A0-15 Valid $\rightarrow$ D0-15 input		$3.0x - 110$		130	ns
14	t_{ADH}	A0-23 Valid $\rightarrow$ D0-15 input		$3.5x - 125$		155	ns
15	t_{RD}	$\overline{RD}$ fall $\rightarrow$ D0-15 input		$2.0x - 115$		45	ns
16	t_{RR}	$\overline{RD}$ Low width	$2.0x - 40$		120		ns
17	t_{HR}	$\overline{RD}$ rise $\rightarrow$ D0-15 Hold	0		0		ns
18	t_{RAE}	$\overline{RD}$ rise $\rightarrow$ A0-15 output	$x - 25$		55		ns
19	t_{WW}	$\overline{WR}$ Low width	$2.0x - 40$		120		ns
20	t_{DW}	D0-15 Valid $\rightarrow$ $\overline{WR}$ rise	$2.0x - 120$		40		ns
21	t_{WD}	$\overline{WR}$ rise $\rightarrow$ D0-15 Hold	$0.5x - 40$		0		ns
22	t_{AWH}	A0-23 Valid $\rightarrow$ $\overline{WAIT}$ input ($\overline{WAIT} + n\text{ mode}$)		$3.5x - 130$		150	ns
23	t_{AWL}	A0-15 Valid $\rightarrow$ $\overline{WAIT}$ input ($\overline{WAIT} + n\text{ mode}$)		$3.0x - 100$		140	ns
24	t_{CW}	$\overline{RD}/\overline{WR}$ fall $\rightarrow$ $\overline{WAIT}$ Hold ($\overline{WAIT} + n\text{ mode}$)	$2.0x + 0$		160		ns
25	t_{APH}	A0-23 Valid $\rightarrow$ PORT input		$2.5x - 120$		80	ns
26	t_{APH2}	A0-23 Valid $\rightarrow$ PORT Hold	$2.5x + 50$		250		ns
27	t_{CP}	$\overline{WR}$ rise $\rightarrow$ PORT Valid		200		200	ns
28	t_{ASRH}	A0-23 Valid $\rightarrow$ $\overline{RAS}$ fall	$1.0x - 60$		20		ns
29	t_{ASRL}	A0-15 Valid $\rightarrow$ $\overline{RAS}$ fall	$0.5x - 40$		0		ns
30	t_{RAC}	$\overline{RAS}$ fall $\rightarrow$ D0-15 input		$2.5x - 90$		110	ns
31	t_{RAH}	$\overline{RAS}$ fall $\rightarrow$ A0-15 Hold	$0.5x - 25$		15		ns
32	t_{RAS}	$\overline{RAS}$ Low width	$2.0x - 40$		120		ns
33	t_{RP}	$\overline{RAS}$ High width	$2.0x - 40$		120		ns
34	t_{RSH}	$\overline{CAS}$ fall $\rightarrow$ $\overline{RAS}$ rise	$1.0x - 55$		25		ns
35	t_{RSC}	$\overline{RAS}$ rise $\rightarrow$ $\overline{CAS}$ rise	$0.5x - 25$		15		ns
36	t_{RCD}	$\overline{RAS}$ fall $\rightarrow$ $\overline{CAS}$ fall	$1.0x - 40$		40		ns
37	t_{CAC}	$\overline{CAS}$ fall $\rightarrow$ D0-15 input		$1.5x - 120$		0	ns
38	t_{CAS}	$\overline{CAS}$ Low width	$1.5x - 40$		80		ns

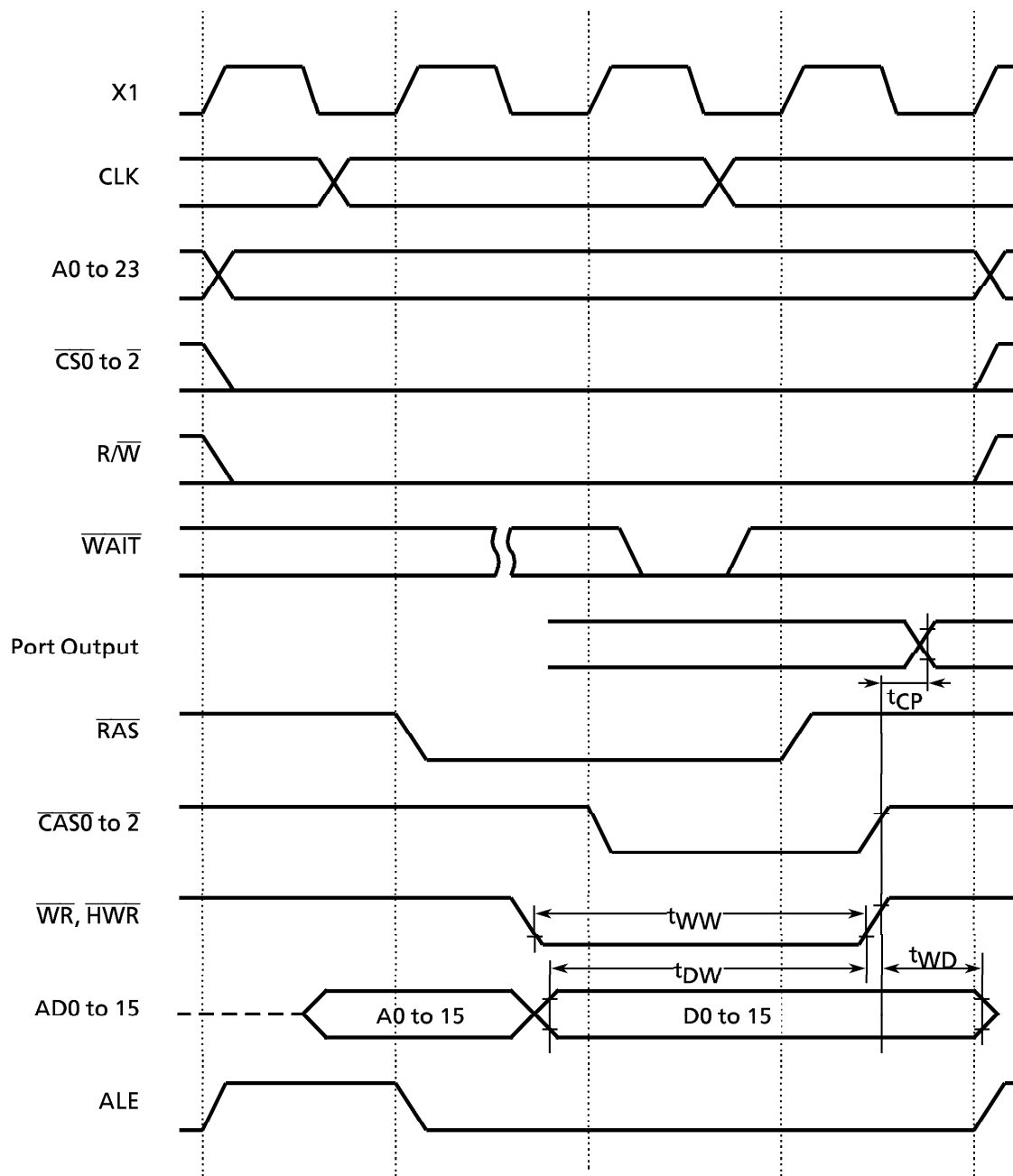
AC Measuring Conditions

- Output Level : High $0.7 \times V_{CC}$ / Low $0.3 \times V_{CC}$, CL = 50 pF
- Input Level : High $0.9 \times V_{CC}$ / Low $0.1 \times V_{CC}$

(1) Read Cycle



(2) Write Cycle



4.4 A/D Conversion Characteristics

AVCC = VCC, AVSS = VSS

Symbol	Parameter	Power Supply	Min	Typ	Max	Unit
V _{REFH}	Analog reference voltage (+)	V _{CC} = 5V ± 10 %	V _{CC} - 1.5V	V _{CC}	V _{CC}	V
		V _{CC} = 3V ± 10 %	V _{CC} - 0.2V	V _{CC}	V _{CC}	
V _{REFL}	Analog reference voltage (-)	V _{CC} = 5V ± 10 %	V _{SS}	V _{SS}	V _{SS} + 0.2V	
		V _{CC} = 3V ± 10 %	V _{SS}	V _{SS}	V _{SS} + 0.2V	
V _{AIN}	Analog input voltage range		V _{REFL}		V _{REFH}	
I _{REF} (V _{REFL} = 0 V)	Analog current for analog reference voltage	V _{CC} = 5V ± 10 %		0.5	1.5	mA
	<V _{REFON} > = 1	V _{CC} = 3V ± 10 %		0.3	0.9	
	<V _{REFON} > = 0	V _{CC} = 2.7 to 5.5V		0.02	5.0	μA
-	Error (excluding quantizing error)	V _{CC} = 5V ± 10 %		± 1.0	± 3.0	LSB
		V _{CC} = 3V ± 10 %		± 1.0	± 3.0	

Note 1 : 1LSB = (V_{REFH} - V_{REFL}) / 2¹⁰ [V]

Note 2 : Minimum operation frequency

The operation of the A/D converter is guaranteed only when f_c (high-frequency oscillator) is used. (It is not guaranteed when f_s is used.) Additionally, it is guaranteed when the clock frequency which is selected by the clock gear is 4 MHz or more.

Note 3 : The value I_{CC} includes the current which flows through the AV_{CC} pin.

4.5 Serial Channel Timing

(1) I/O Interface Mode

① SCLK Input Mode

Symbol	Parameter	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16X		488 μs		1.28		0.8		μs
t_{OSS}	Output Data $\rightarrow$ Rising edge or SCLK	$t_{SCY}/2 - 5X - 50$		91.5 μs		190		100		ns
t_{OHS}	SCLK rising edge $\rightarrow$ Output Data hold	$5X - 100$		152 μs		300		150		ns
t_{HSR}	SCLK rising edge $\rightarrow$ Input Data hold	0		0		0		0		ns
t_{SRD}	SCLK rising edge $\rightarrow$ effective data input		$t_{SCY} - 5X - 100$		336 μs		780		450	ns

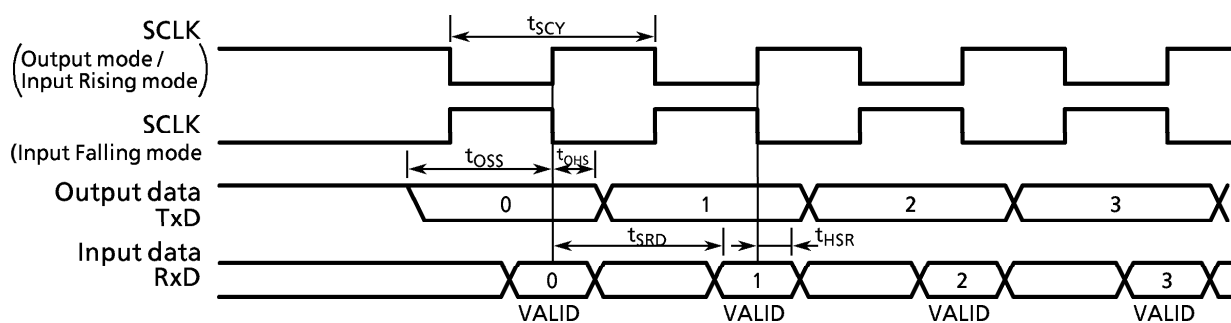
Note : When fs is used as system clock (fsys) or fs is used as input clock to prescaler.

*) SCLK rising / falling timing ... SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

② SCLK Output Mode

Symbol	Parameter	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (programmable)	16X	8192X	488 μs	250 ms	1.28	655.36	0.8	409.6	μs
t_{OSS}	Output Data $\rightarrow$ SCLK rising edge	$t_{SCY} - 2X - 150$		427 μs		970		550		ns
t_{OHS}	SCLK rising edge $\rightarrow$ Output Data hold	$2X - 80$		60 μs		80		20		ns
t_{HSR}	SCLK rising edge $\rightarrow$ Input Data hold	0		0		0		0		ns
t_{SRD}	SCLK rising edge $\rightarrow$ effective data input		$t_{SCY} - 2X - 150$		428 μs		970		550	ns

Note : When fs is used as system clock (fsys) or fs is used as input clock to prescaler.



4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock Cycle	$8X + 100$		740		500		ns
t_{VCKL}	Low level clock Pulse width	$4X + 40$		360		240		ns
t_{VCKH}	High level clock Pulse width	$4X + 40$		360		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low Level Pulse Width	4X		320		200		ns
t_{INTAH}	$\overline{NMI}$, INT0 High Level Pulse Width	4X		320		200		ns

(2) INT4 to 7 interrupts, capture

Input pulse width of INT4 to 7 depends on the operation clock of CPU and Timer (9-bit prescaler). The following shows the pulse width in each clock.

System clock selected <SYSCK>	Prescaler clock selected <PRCK1 to 0>	t_{INTBL} (INT4 to 7 low level pulse width)		t_{INTBH} (INT4 to 7 high level pulse width)		Unit
		Variable	20 MHz	Variable	20 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	$8X + 100$	500	$8X + 100$	500	ns
	01 (fs)	$8XT + 0.1$	244.3	$8XT + 0.1$	244.3	
	10 (fc/16)	$128X + 0.1$	6.5	$128X + 0.1$	6.5	
1 (fs) (Note 2)	00 (f_{FPH})	$8XT + 0.1$	244.3	$8XT + 0.1$	244.3	μs
	01 (fs)					

Note 1: XT represents the cycle of the low frequency clock fs. Calculated at $f_s = 32.768$ kHz.

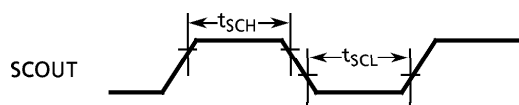
Note 2: When fs is used as the system clock, fc/16 can not be selected for the prescaler clock.

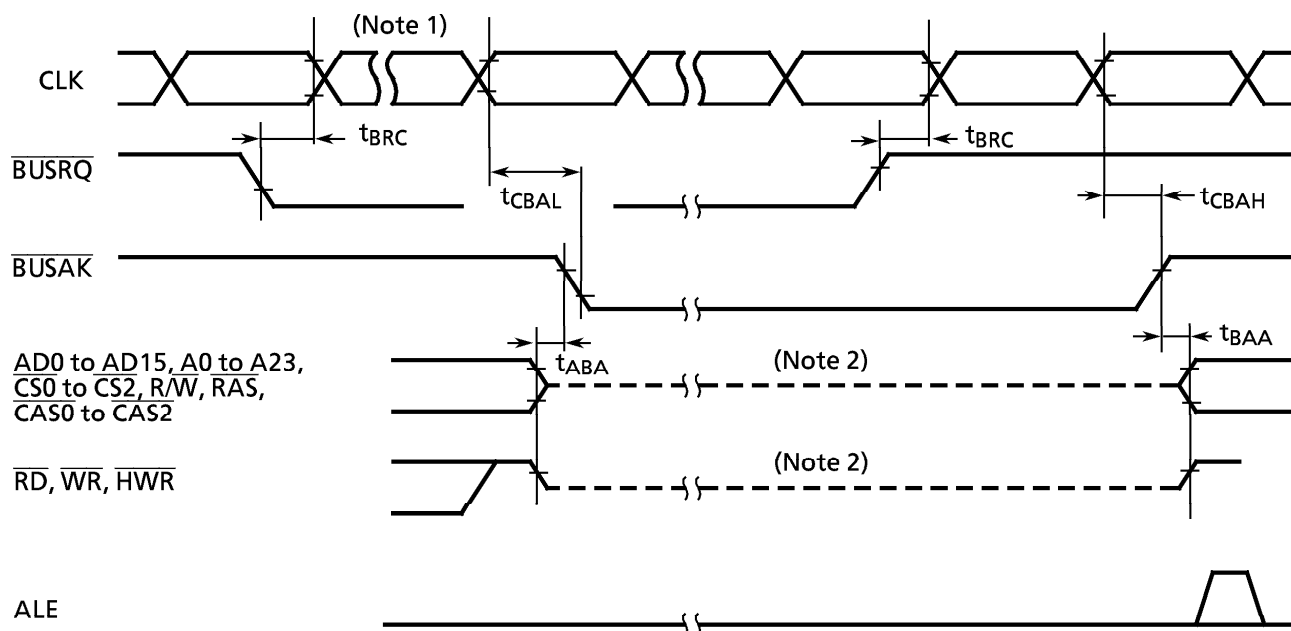
4.8 SCOUT pin AC characteristics

Symbol	Parameter		Variable		10 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
t_{SCH}	High-Level Pulse Width	$V_{CC} = 5V \pm 10\%$	$0.5X - 10$		40		15		ns
		$V_{CC} = 3V \pm 10\%$	$0.5X - 20$		30		–	–	
t_{SCL}	Low-Level Pulse Width	$V_{CC} = 5V \pm 10\%$	$0.5X - 10$		40		15		ns
		$V_{CC} = 3V \pm 10\%$	$0.5X - 20$		30		–	–	

Measurement condition

- Output level: High 2.2 V / Low 0.8 V, CL = 10 pF



4.9 Timing Chart for Bus Request ($\overline{\text{BUSRQ}}$) / Bus Acknowledge ($\overline{\text{BUSAK}}$)

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{BRC}	$\overline{\text{BUSRQ}}$ Set-up Time to CLK	120		120		120		ns
t_{CBAL}	CLK $\rightarrow$ $\overline{\text{BUSAK}}$ Falling Edge		$1.5X + 120$		270		195	ns
t_{CBAH}	CLK $\rightarrow$ $\overline{\text{BUSAK}}$ Rising Edge		$0.5X + 40$		80		65	ns
t_{ABA}	Output Buffer off to $\overline{\text{BUSAK}}$	0	80	0	80	0	80	ns
t_{BAA}	$\overline{\text{BUSAK}}$ to Output Buffer on	0	80	0	80	0	80	ns

Note 1 : The Bus will be released after the $\overline{\text{WAIT}}$ request is inactive, when the $\overline{\text{BUSRQ}}$ is set to "0" during "Wait" cycle.

Note 2 : This line only shows the output buffer is off-state.

It doesn't indicate the signal level is fixed.

Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level-fix will be delayed.

The internal programmable pull-up/pull-down resistor is switched active/non-active by an internal signal.