SC1205H
High Speed Synchronous Power MOSFET Driver

Description

The SC1205H is a cost effective, **High Drive Voltage**, Dual MOSFET Driver designed for switching High and Low side Power MOSFETs. Each driver is capable of Ultra-fast rise/fall times as well as a 20ns max propagation delay from input transition to the gate of the power FET's. An internal Overlap Protection circuit prevents shoot-through from Vin to GND in the main and synchronous MOSFETs. The Adaptive Overlap Protection circuit ensures the Bottom FET does not turn on until the Top FET source has reached a voltage low enough to prevent cross-conduction.

Higher gate voltage drive capability of 8V (top and bottom) optimally reduces Rds_on of power MOSFETs without excessive driver and FET switching losses. The high current drive capability (5A peak) allows fast switching, thus reducing switching losses at high (up to 1MHz) frequencies without causing thermal stress on the driver.

The high voltage CMOS process allows operation from 5-18 Volts at top MOSFET drain, thus making SC1205H suitable for battery powered applications. Connecting Enable pin (EN) to logic low shuts down both drives and reduces operating current to less than 10µA.

An under-voltage-lock-out and overtemperature shutdown feature is included to guarantee proper and safe operation. The SC1205H is offered in a standard SO-8 package.

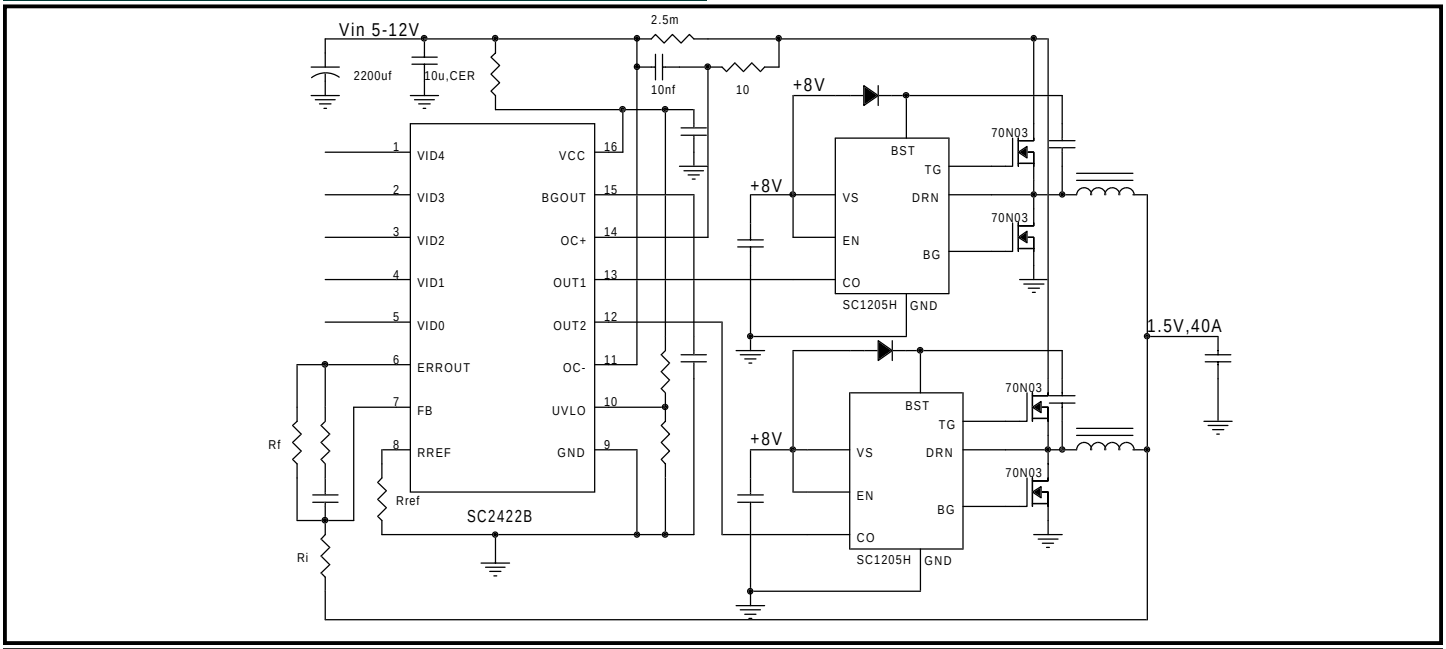
Features

- Higher efficiency (>90%)
- Fast rise and fall times (15ns typical with 3000pf load)
- **Higher gate drive voltage (8V) for optimum MOSFET RDS_ON at minimum switching loss**
- Ultra-low (<20ns) propagation delay (BG going low)
- **5 Amp peak drive current**
- Adaptive non-overlapping gate drives provide shoot-through protection
- Floating top drive switches up to 18V
- Under-voltage lock-out
- Over-temperature shutdown
- Less than 10µA supply current when EN is low
- Low cost

Applications

- Intel Pentium™ power supplies
- AMD Athlon™ and K8™ power supplies
- High efficiency portable and notebook computers
- Battery powered applications
- High frequency (to 1.0 MHz) operation allows use of small inductors and low cost caps in place of electrolytics

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Conditions	Maximum	Units
V_{CC} Supply Voltage	V_{IMAXSW}		11	V
BST to PGND	$VMAX_{BST-PGND}$		30	V
BST to DRN	$VMAX_{BST-DRN}$		11	V
DRN to PGND	$VMAX_{DRN-PGN}$		-2 to 25	V
DRN to PGND Pulse	$VMAX_{PULSE}$	t_{PULSE} < 100ns	-5 to 25	V
		t_{PULSE} < 20ns	-10 to 25	
EN to PGND	$VMAX_{OVP\ S-PGND}$		12	V
Input Pin	CO		-0.3 to 12	V
Continuous Power Dissipation	P_D	Tamb = 25°C, T_J = 125°C Tcase = 25°C, T_J =125°C	0.66 2.56	W
Thermal Resistance Junction to Case	θ_{JC}		40	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}		150	°C/W
Operating Temperature Range	T_J		0 to +125	°C
Storage Temperature Range	T_{STG}		-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}		300	°C

Note:
(1) Specification refers to application circuit in Figure 1.

Electrical Characteristics

Unless specified: -0 < θ_J < 125°C; V_{CC} = 5V; 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{CC}	V_{CC}	4.2	5	9.0	V
Quiescent Current, Operating	Iq_op	V_{CC} = 5V, C_O = OV		1		mA
Quiescent Current	Iq_stby	EN = OV			10	µA
Under Voltage Lockout						
Start Threshold	V_{START}		4.2	4.4	4.75	V
Hysteresis	$Vhys_{UVLO}$			0.05		V

Electrical Characteristics (Cont.)

Unless specified: -0 < θ_J < 125°C; V_{CC} = 5V; 4V ≤ V_{BST} ≤ 26V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CO						
High Level Input Voltage	V_{IH}		2.0			V
High Level Input Voltage	V_{IH}	V_{CC} = 9V	2.65			V
Low Level Input Voltage	V_{IL}				0.8	V
EN						
High Level Input Voltage	V_{IH}		2.0			V
High Level Input Voltage	V_{IH}	V_{CC} = 9V	2.2			V
Low Level Input Voltage	V_{IL}				0.8	V
Thermal Shutdown						
Over Temperature Trip Point	T_{OTP}			165		°C
Hysteresis	T_{HYST}			10		°C
High Side Driver						
Peak Output Current	I_{PKH}			3		A
Output Resistance	$Rsrc_{TG}$ $Rsink_{TG}$	duty cycle < 2%, tpw < 100 µs, T_J = 125°C, V_{BST} - V_{DRN} = 4.5V, V_{TG} = 4.0V (src) +V_{DRN} or V_{TG} = 0.05V (sink) +V_{DRN}		1 .7		Ω
Low-Side Driver						
Peak Output Current	I_{PKL}			3		A
Output Resistance	$Rsrc_{BG}$ $Rsink_{BG}$	duty cycle < 2%, tpw < 100 µs, T_A = 25°C, V_{VS} = 4.6V, V_{BG} = 4V (src), or V_{LOWDR} = 0.5V (sink)		1.2 1.0		Ω Ω

AC Operating Specifications

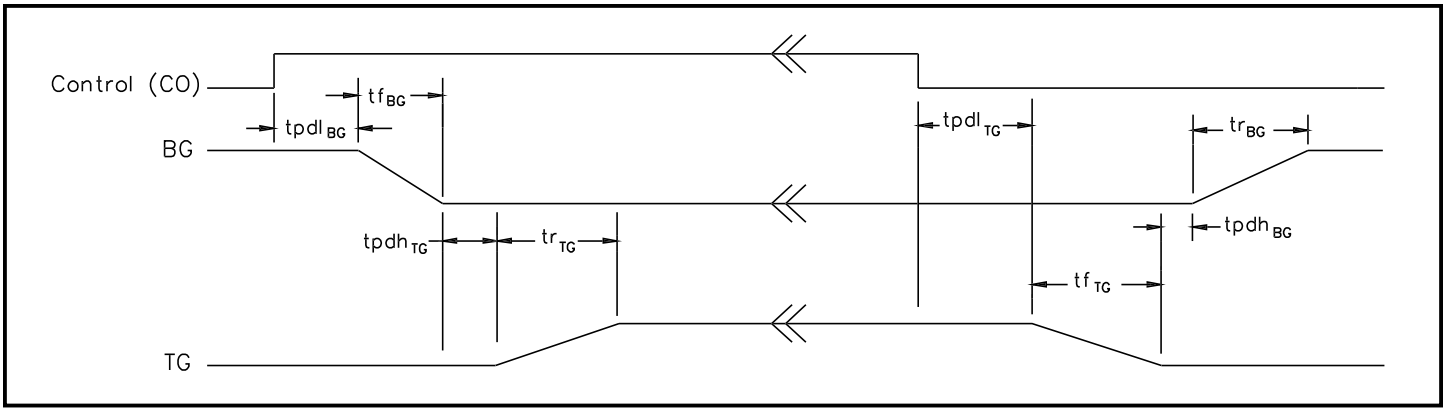
Parameter	Symbol	Conditions	Min	Typ	Max	Units
High Side Driver						
Rise Time	tr_{TG1}	Cl = 3nF, V_{BST} - V_{DRN} = 8V		14		ns
Fall Time	tf_{TG}	Cl = 3nF, V_{BST} - V_{DRN} = 8V		12		ns
Propagation Delay Time, TG Going High	$tpdh_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 8V		20		ns
Propagation Delay Time, TG Going Low	$tpdl_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 8V		15		ns

AC Operating Specifications (Cont.)

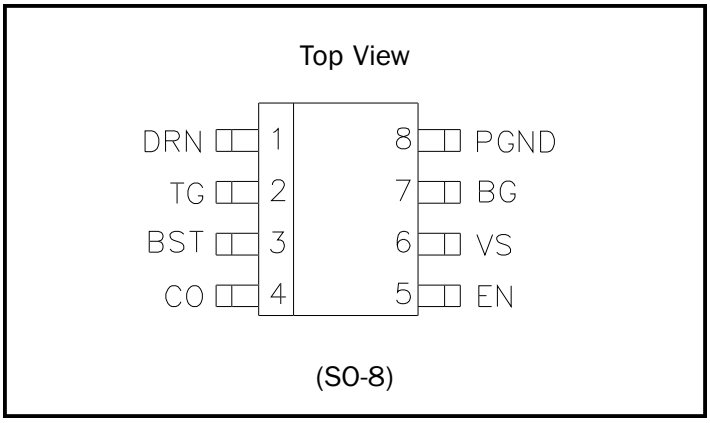
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low-Side Driver						
Rise Time	tr_{BG}	Cl = 3nF, V_{VS} = 8V		15		ns
Fall Time	tr_{BG}	Cl = 3nF, V_{VS} = 8V		13		ns
Propagation Delay Time BG Going High	$tpdh_{BGHI}$	Cl = 3nF, V_{VS} = 8V		12		ns
Propagation Delay Time BG Going Low	$tpdl_{BGHI}$	Cl = 3nF, V_{VS} = 8V		7		ns
Under-Voltage Lockout						
V_5 ramping up	$tpdh_{UVLO}$	EN is High			10	µs
V_5 ramping down	$tpdL_{UVLO}$	EN is High			10	µs

Note:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Timing Diagrams



Pin Configuration



Ordering Information

Device (1)	Package	Temp Range (T_J)
SC1205HSTR	SO-8	0° to 125°C

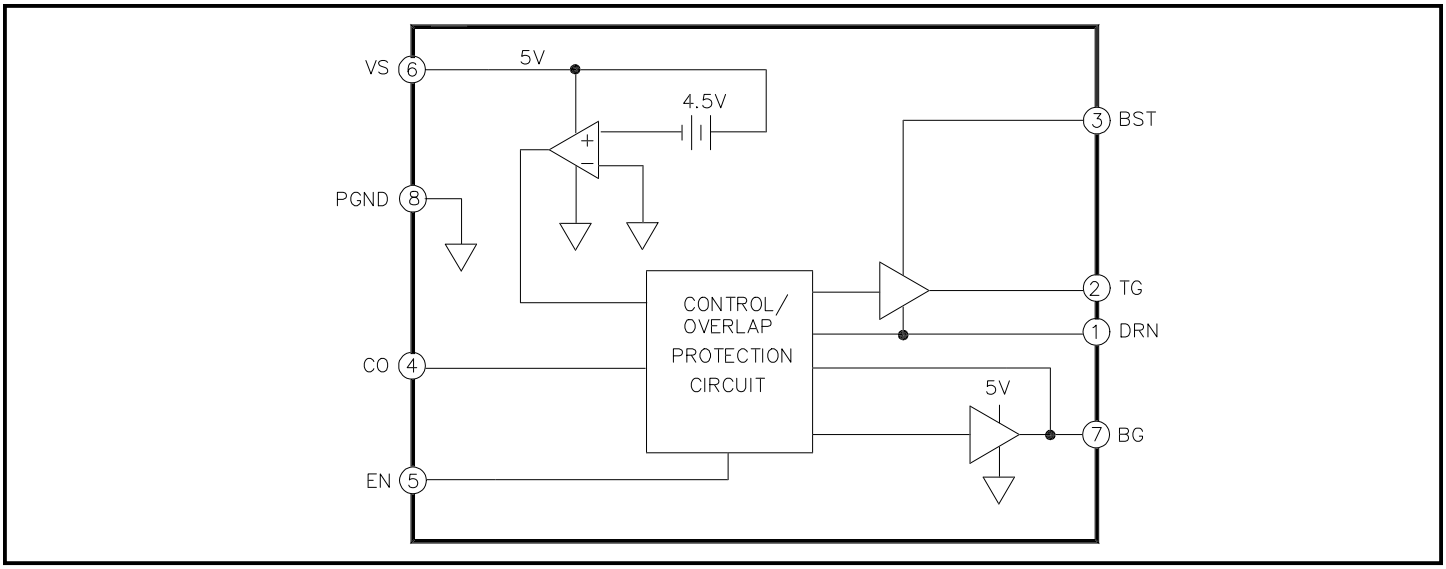
Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	DRN	This pin connects to the junction of the switching and synchronous MOSFETs . This pin can be subjected to a -2V minimum relative to PGND without effecting operation.
2	TG	Output gate drive for the switching (high-side) MOSFET.
3	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1µF and 1µF (ceramic).
4	CO	TTL-level input signal to the MOSFET drivers.
5	EN	When high, this pin enables the internal circuitry of the device. When low, TG and BG are forced low and the supply current (5V) is less than 10µA.
6	VS	5V-9.0V supply. A .22-1µF ceramic capacitor should be connected from 5V to PGND very close to this pin.
7	BG	Output drive for the synchronous (bottom) MOSFET.
8	PGND	Ground. Keep this pin close to the synchronous MOSFETs source.

Note:
(1) All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Applications Information

Theory of Operation

SC1205H is the higher gate drive voltage version of it predecessor, the SC1205. It is designed for optimum enhancement of Low Rds_On power MOSFET's with ultra-low rise/fall times and propagation delays. Higher MOSFET enhancement has been made possible by optimally increasing the gate drive voltage while maintaining low switching losses at minimum RDS_ON. The SC1205H is designed for a gate drive voltage of 8V, without compromising features that allow fast switching and low propagation delays.

Fast Switching Drives

As the switching frequency of PWM controllers is increased to reduce power supply volume and cost, fast rise and fall times are necessary to minimize switching losses (TOP MOSFET) and reduce dead-time (BOTTOM MOSFET) losses. While low Rds_On MOSFET's present a power saving in I^2R losses, the MOSFETs die area is larger and the effective input capacitance of the MOSFET is increased. Often a 50% decrease in Rds_On doubles the effective input gate charge, which must be supplied by the driver. The Rds_On power savings can be offset by the switching and dead-time losses with a suboptimum driver. While discrete solution can achieve reasonable drive capability, implementing shoot-through, programmable delay and other housekeeping functions necessary for safe operation can become cumbersome and costly. The SC1205H presents a total solution for the high-speed, high power density applications. Wide input supply range of 4.5V-18V allows use in battery powered applications, new high voltage, distributed power servers.

Shoot Through Protection

The control input (CO) to the SC1205H is typically supplied by a PWM controller that regulates the power supply output. (See Application Evaluation Schematic, Figure 6). The timing diagram demonstrates the sequence of events by which the top and bottom drive signals are applied. The shoot-through protection is implemented by holding the bottom FET off until the voltage at the phase node (intersection of top FET source, the output inductor and the bottom FET drain) has dropped below 1V. This assures that the top FET has turned off and that a direct current path does not exist between the input supply and ground, a shoot-through condition during which both the top and bottom FET's could be on momentarily. The top FET is also prevented from turning on until the bottom FET is off. This time is internally set to 20ns (typical).

The EN (enable) pin may be used to turn both TG and BG drives off. This would allow lower power operation by reducing the quiescent current draw of the SC1205H to less than 10µA.

Applications Information (Cont.)

LAYOUT GUIDELINES

As with any high speed , high current, switching regulator circuit, proper layout is critical in achieving optimum performance of the SC1205H. The Evaluation board schematic (Refer to figure 6) shows a two-phase synchronous design with all surface mountable components.

Tight placement and short, wide traces must be used in layout of The gate drives, DRN, and especially PGND pin. The top gate driver supply voltage is provided by bootstrapping the boost supply and adding it to the phase node (DRN) voltage. Since the bootstrap capacitor supplies the charge to the top gate, it must be less than .5" away from the SC1205H. Ceramic X7R capacitors are a good choice for supply bypassing near the chip.

Supply Voltage

The Vcc supply must be derived from a voltage that does not vary significantly with output load. This is especially true if the MOSFET drain voltage is a +5V supply bus and the Vcc of the SC1205H is connected to +5V. As the load increases, or during sudden load transients, the 5V supply dips significantly due to trace resistance and inductance. If the Vcc of the SC1205H is derived from the end of this +5V bus, the drop in the +5V can cause the Vcc to fall lower than the required under voltage lockout threshold of the SC1205H and cause intermittent drive shutdown. To avoid this occurrence, connect the Vcc of the SC1205H to the beginning point of the +5V bus with a separate trace, directly to the input connector.

The Vcc pin bypass capacitor must also be less than .5" away from the SC1205H. The ground node of this capacitor, the SC1205H PGND pin and the Source of the bottom FET must be very close to each other, preferably with common PCB copper land with multiple vias to the ground plane (if used). The parallel Schottky (if used) must be physically next to the Bottom FET's drain and source pins. Any trace or lead inductance in these connections will drive current way from the Schottky and allow it to flow through the FET's Body diode, thus reducing efficiency.

Preventing Inadvertent Bottom FET Turn-on

At high input voltages, (12V and greater) a fast turn-on of the top FET creates a positive going spike on the Bottom FET's gate through the Miller capacitance, Crss of the bottom FET. The voltage appearing on the gate due to this spike is:

$$V_{SPIKE} = \frac{Vin * crss}{(Crss + ciss}$$

Where Ciss is the input gate capacitance of the bottom FET. This is assuming that the impedance of the drive path is too high compared to the instantaneous impedance of the capacitors. (since dV/dT and thus the effective frequency is very high). If the BG pin of the SC1205H is very close to the bottom FET, Vspike will be reduced depending on trace inductance, rate of rise of current, etc.

While not shown in Figure 6, a capacitor may be added from the gate of the Bottom FET to its source, preferably less than .5" away. This capacitor will be added to Ciss in the above equation to reduce the effective spike voltage.

The bottom MOSFET must be selected with attention paid to the Crss/Ciss ratio. A low ratio reduces the Miller feedback and thus reduces Vspike. Also MOSFETs with higher Turn-on threshold voltages will conduct at a higher voltage and will not turn on during the spike. The MOSFET shown in the schematic (Figure 6) has a 2 volt threshold and will require approximately 4.5 volts Vgs to be conducting, thus reducing the possibility of shoot-through. A zero ohm bottom FET gate resistor will obviously help keeping the gate voltage low during off time.

Ultimately, slowing down the top FET by adding gate resistance will reduce di/dt which will in turn make the effective impedance of the capacitors higher, thus allowing the BG driver to hold the bottom gate voltage low. It does this at the expense of increased switching times (and switching losses) for the top FET.

Applications Information (Cont.)

The top MOSFET source must be close to the bottom MOSFET drain to prevent ringing and the possibility of the phase node going negative. This frequency is determined by:

$$Fring = \frac{1}{(2\Pi * Sqrt\ (L_{ST} * Coss))}$$

-Where:

L_{st} = The effective stray inductance of the top FET added to trace inductance of the connection between top FET's source and the bottom FET's drain added to the trace resistance of the bottom FET's ground connection.
Coss = Drain to source capacitance of bottom FET. If there is a Schottky used, the capacitance of the Schottky is added to this value.

Although this ringing does not pose any power losses due to a fairly high Q, it could cause the phase node to go too far negative, thus causing improper operation, double pulsing or at worst driver damage. On the SC1205H, the drain node, DRN, can go as far as 2V below ground without affecting operation or sustaining damage.

The ringing is also an EMI nuisance due to its high resonant frequency. Adding a capacitor, typically 1000-2000pf, in parallel with Coss of the bottom FET can often eliminate the EMI issue.

Prevent Driver Overvoltage

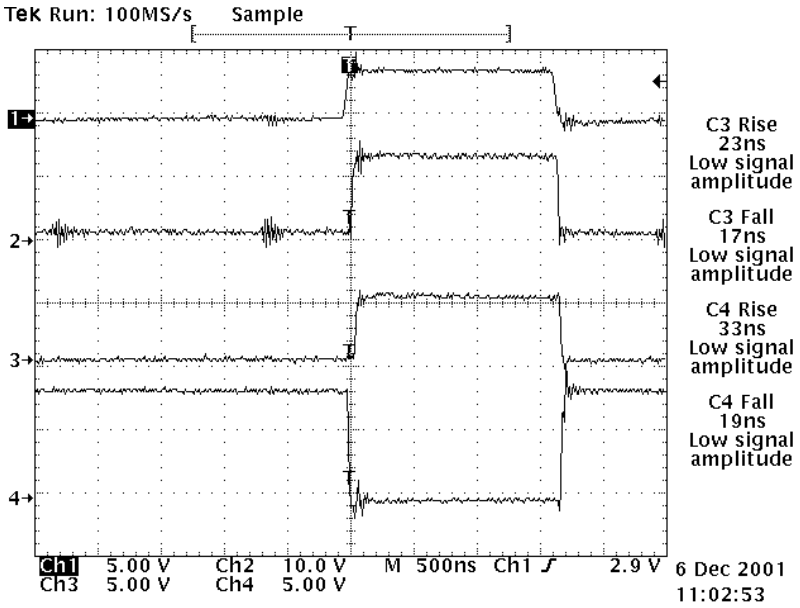
The negative voltage spikes on the phase node adds to the bootstrap capacitor voltage, thus increasing the voltage between VBST - VDRN. *This is of special importance if higher boost voltages are used.* If the phase node negative spikes are too large, the voltage on the boost capacitor could exceed device's absolute maximum rating of 12V. To eliminate the effect of the ringing on the boost capacitor voltage, place a 4.7 - 10 Ohm resistor between boost Schottky diode and Vcc to filter the negative spikes on DRN Pin. Alternately, a Silicon diode, such as the commonly available 1N4148 can substitute for the Schottky diode and eliminate the need for the series resistor.
Proper layout will guarantee minimum ringing and eliminate the need for external components. Use of SO-8 or other surface mount MOSFETs while increasing thermal resistance, will reduce lead inductance as well as radiated EMI.

Over Temperature Shutdown

The SC1205H will shutdown by pulling both driver if its junction temperature, T_J, exceeds 165°C.

Typical Performance Plots

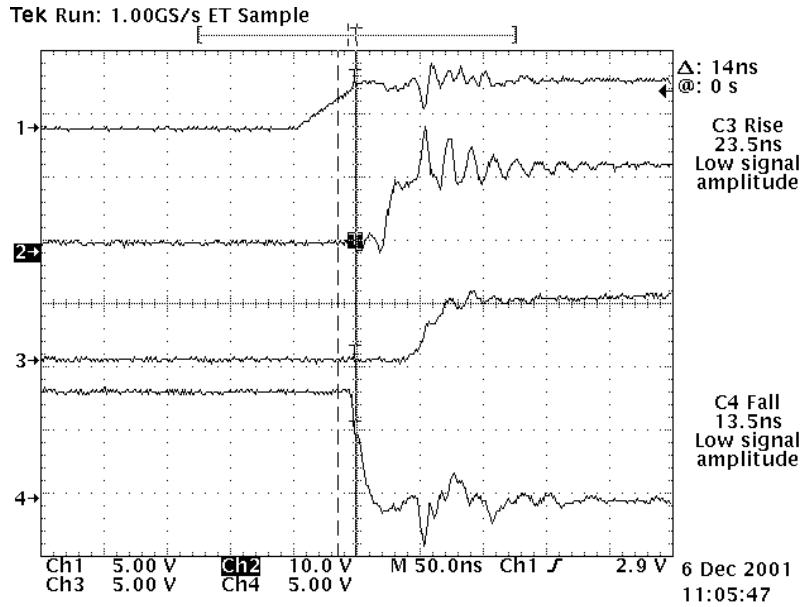
Figure 1: Rise and fall time and propagation delay of SC1205H



SC1205H Rise Time and Fall Time
Vin = 5V
Vcc/Vbst = 8V
I out = 20A
Chan. 1 = CO pin
Chan. 2 = Top gate
Chan. 3 = Phase node
Chan. 4 = Bottom gate

See Schematic, Figure 6

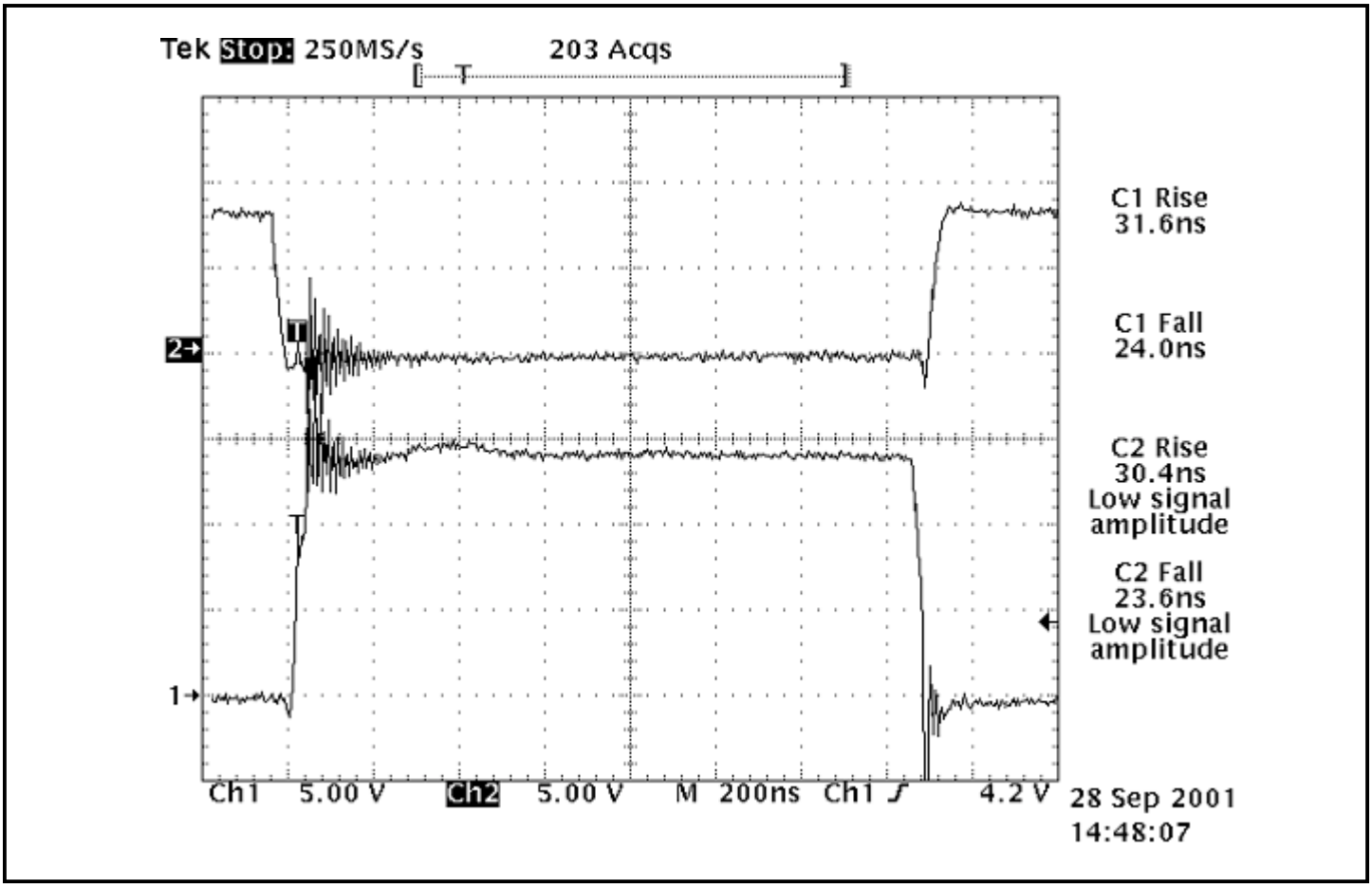
Figure 2: Rise and fall time and propagation delay of SC1205H



SC1205H Rise Time and Fall Time
Vin = 5V
Vcc/Vbst = 8V
I out = 20A
Chan. 1 = CO pin
Chan. 2 = Top gate
Chan. 3 = Phase node
Chan. 4 = Bottom gate, Propagation delay between CO pin and Bottom Gate = 14ns

See Schematic, Figure 6

Figure 3: Rise and fall time and propagation delay of SC1205H, driving two top and two bottom FETs, All FETS , FDB7030BL

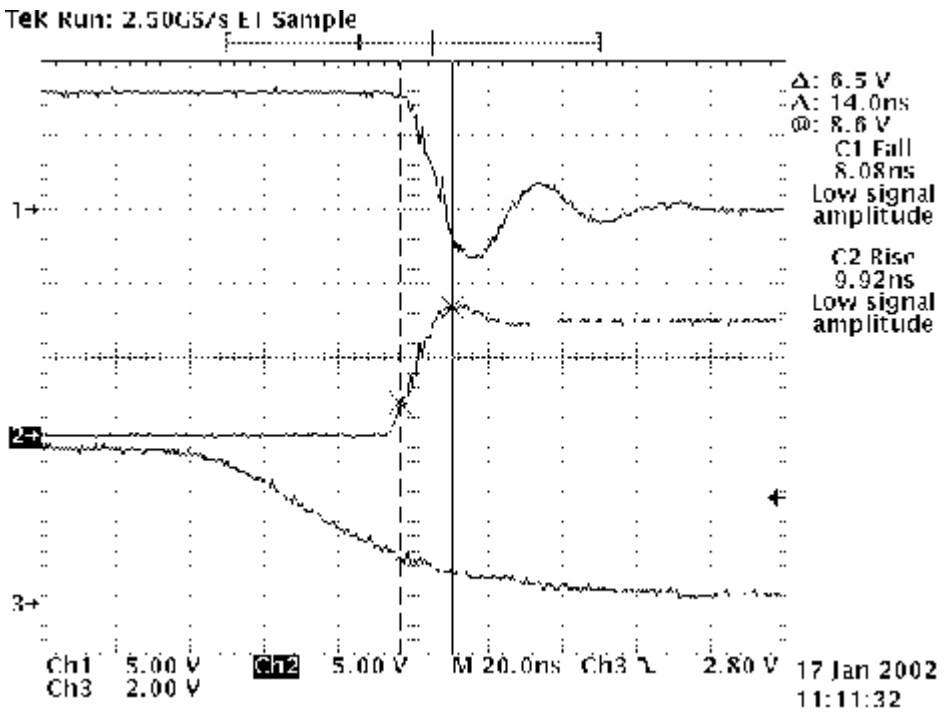


Rise and fall time of gate drives of the SC1205H with **VCC = VBST = +8V**.
Ch1:Top gate drive, Ch2:Bottom Gate drive

Note that these rise and fall times are achieved while driving 2X FDB7030BL MOSFETs on top and 2X FDB7030BL on the bottom (synchronous).

Vin = 5V
Vcc = Vbst = 8V
Iout = 20A/phase
All gate drive resistors are set to zero for this test.

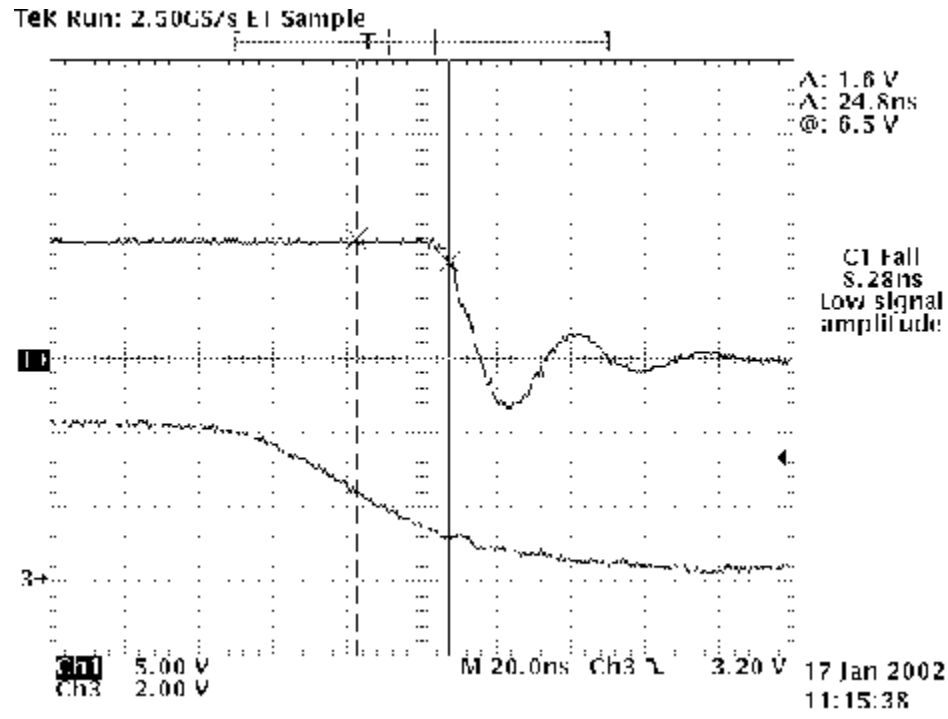
Figure 4: SC1205H driving a 3nF capacitive load. $V_{CC} = V_{BOOST} = 8V$.



SC1205H
Timing Delay

Chan. 1 = Top gate
Fall time
Chan. 2 = Bott. Gate rise time
Chan. 3 = CO pin going low

Figure 5: SC1205H driving a 3nF capacitive load. $V_{CC} = V_{BOOST} = 8V$.

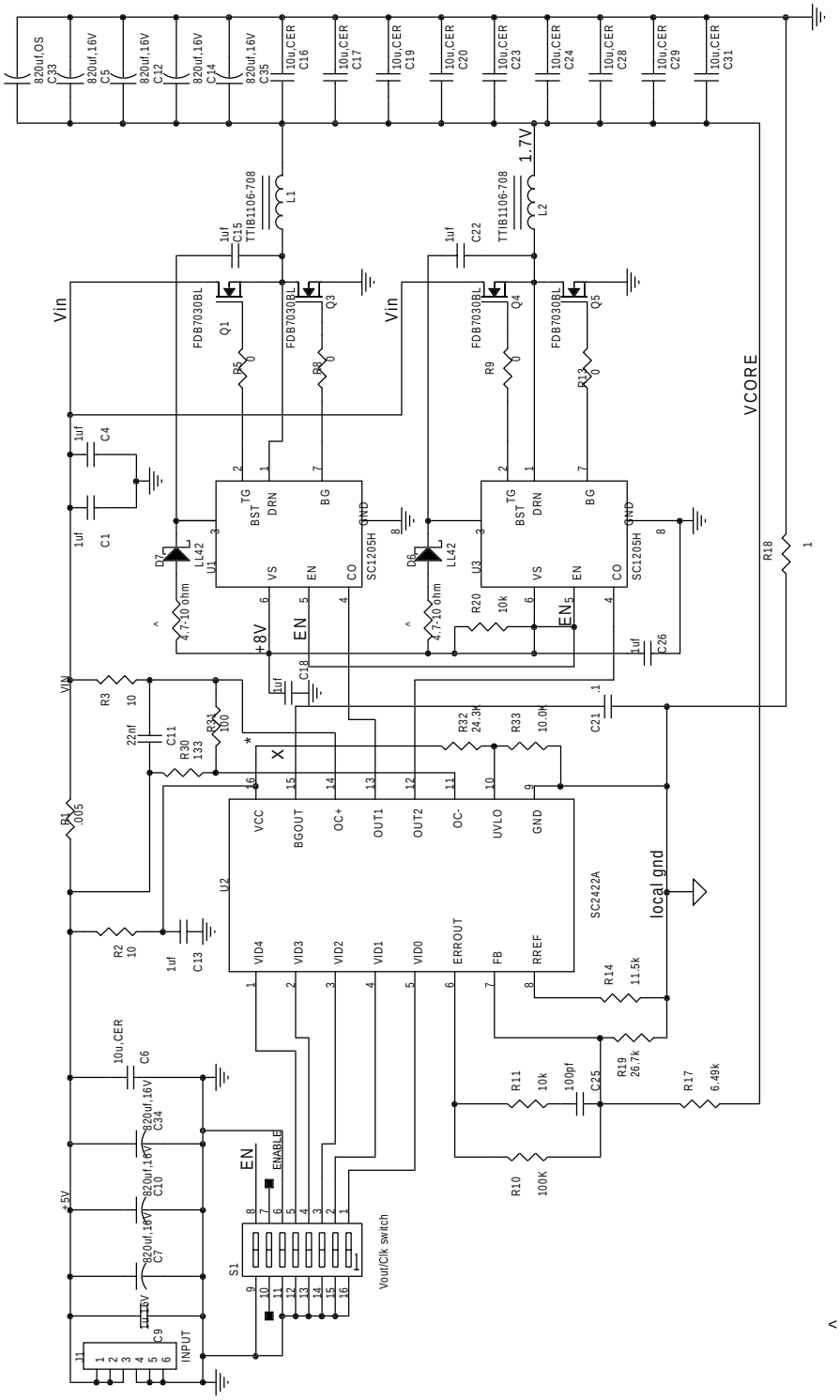


SC1205H
Propagation Delay

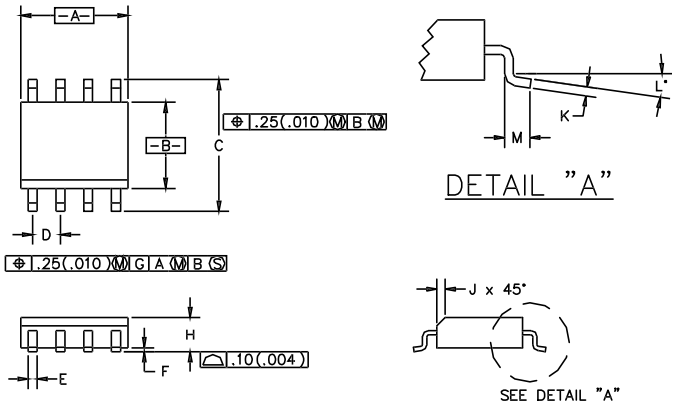
Chan. 1 = Top gate
Fall time
Chan. 3 = CO pin going low

Evaluation Board Schematic - SC1205H

Figure 6: Microprocessor Core Supply

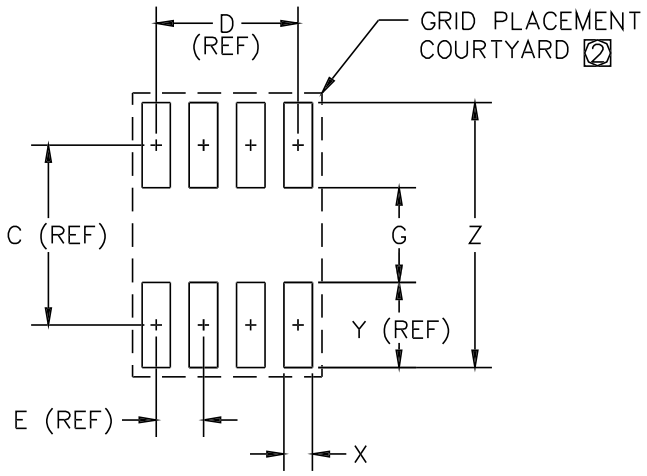


Outline Drawing - SO-8



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

Land Pattern - SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS

Contact Information

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