

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT MULTI-CHIP

# TA8490F

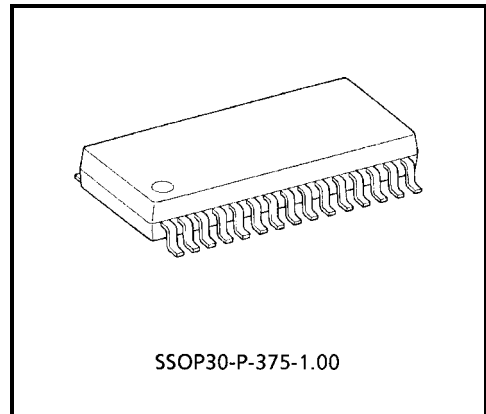
## 3-PHASE FULL WAVE BRUSHLESS DC MOTOR DRIVER IC FOR CD-ROM DRIVES

This 3-phase, full-wave, brushless DC motor driver IC has been developed for use in CD-ROM drive spindle motors. The TA8490F contains in its upper stage a discrete power transistor which, thanks to its low-saturation characteristic, enables the IC to provide superior thermal efficiency.

Furthermore, the multi-chip structure of this device facilitates dispersion of the heat generated inside the package, making it possible to suppress heat concentration.

### FEATURES

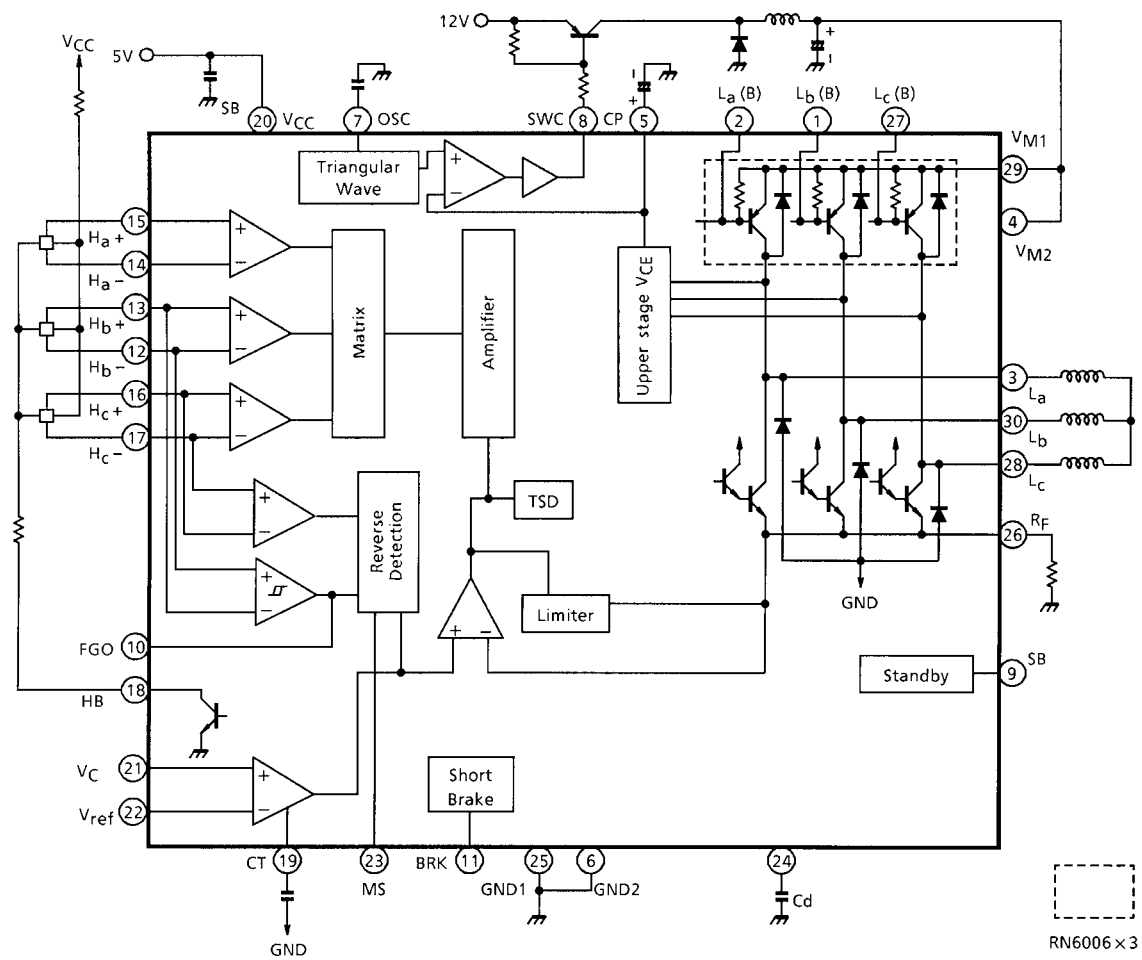
- Multi-chip structure (3 RN6006 chips built-in)
- 3-phase, full-wave, semi-linear drive
- Current drive / current control
- Built-in current limiter :  $I_{LIM} = 0.6A$  (typ.) (at  $R_F = 0.3 \Omega$ )
- Built-in reversing brake / short brake functions
- FG signal output (using hall element output signal)
- Built-in switching regulator controller
- Built-in hall bias
- Built-in thermal shutdown circuit



SSOP30-P-375-1.00

Weight : 0.63 g (typ.)

## BLOCK DIAGRAM



## PIN ASSIGNMENT

TERMINAL No.	TERMINAL SYMBOL	FUNCTION	REMARKS
1	L <sub>b</sub> (B)	b-phase upper side power transistor (base) output terminal	Keep open.
2	L <sub>a</sub> (B)	a-phase upper side power transistor (base) output terminal	Keep open.
3	L <sub>a</sub>	a-phase output terminal	Connect to the coil.
4	V <sub>M2</sub>	Supply voltage terminal for motor drive	Connect to V <sub>M1</sub> externally.
5	CP	Switching power source system phase compensator terminal	Connect a capacitor between this terminal and GND.
6	GND2	GND	—
7	OSC	Triangular wave oscillation terminal	Connect a capacitor between this terminal and GND.
8	SWC	Switching regulator control signal output terminal	Connect to the base of the switching external transistor.
9	SB	RUN / STOP control terminal	H: RUN, L: STOP
10	FGO	FG amplifier output terminal	Outputs a signal whose frequency is determined by the CD rotation frequency.
11	BRK	Brake mode select terminal	Output mode when V <sub>C</sub> > V <sub>ref</sub>
12	H <sub>b</sub> <sup>-</sup>	b-phase negative hall signal input terminal	Connect to hall element output terminal.
13	H <sub>b</sub> <sup>+</sup>	b-phase positive hall signal input terminal	Connect to hall element output terminal.
14	H <sub>a</sub> <sup>-</sup>	a-phase negative hall signal input terminal	Connect to hall element output terminal.
15	H <sub>a</sub> <sup>+</sup>	a-phase positive hall signal input terminal	Connect to hall element output terminal.
16	H <sub>c</sub> <sup>+</sup>	c-phase positive hall signal input terminal	Connect to hall element output terminal.
17	H <sub>c</sub> <sup>-</sup>	a-phase negative hall signal input terminal	Connect to hall element output terminal.
18	HB	Hall element bias terminal	Open collector output. Connect to the negative side of hall element bias line.
19	CT	Control system phase compensator terminal	Connect a capacitor between this terminal and GND.
20	V <sub>CC</sub>	Supply voltage terminal for control circuits	V <sub>CC (opr)</sub> = 4.5~5.5 V

TERMINAL No.	TERMINAL SYMBOL	FUNCTION	REMARKS
21	V <sub>C</sub>	Control amplifier input terminal	Use the control signal as input.
22	V <sub>ref</sub>	Control amplifier reference voltage input terminal	Use the reference voltage for the control amplifier as input.
23	MS	Mode select terminal	Determines output mode.
24	Cd	Forward / reverse changeover gain adjustment terminal	Adjust a rotation direction changeover gain
25	GND1	GND	—
26	R <sub>F</sub>	Output current detection terminal	Sets limiter current value and current gain.
27	L <sub>c</sub> (B)	c-phase upper side power transistor (base) output terminal	Keep open.
28	L <sub>c</sub>	c-phase output terminal	Connect to the coil.
29	V <sub>M1</sub>	Supply voltage terminal for motor drive	Connect to V <sub>M2</sub> externally.
30	L <sub>b</sub>	b-phase output terminal	Connect to the coil.

### ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V <sub>CC</sub>	7	V
	V <sub>M</sub>	16	
Output Current	I <sub>O</sub>	1.2	A
Power Dissipation	P <sub>D</sub> (Note 1)	1.0	W
Junction Temperature	T <sub>j</sub>	150	°C
Operating Temperature	T <sub>opr</sub>	-20~75	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

Note 1: unmounted

### OPERATING VOLTAGE RANGE

CHARACTERISTIC	SYMBOL	OPERATING RATING	UNIT
Power Supply Voltage	V <sub>CC</sub>	4.5~5.5	V
	V <sub>M</sub>	3~14	

ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5\text{ V}$ ,  $V_M = 12\text{ V}$ ,  $T_a = 25^\circ\text{C}$ .)

CHARACTERISTICS		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage		$I_{CC1}$	1	Stop mode	—	2	4.5	mA
		$I_{CC2}$		Run mode, output open	—	7	15	
Hall Amp.	Input Current	$I_{INH}$	2	$V_{CMRH} = 2.5\text{ V}$	—	—	2	$\mu\text{A}$
	Common Mode Input Voltage Range	$V_{CMRH}$	—	—	1.5	—	4.0	V
	Input Amplitude	$V_H$		—	60	—	—	mV <sub>P-P</sub>
Hall Element Bias Saturation Voltage		$V_{HB}$	2	$I_{HB} = 10\text{ mA}$	—	1.3	2.0	V
Control Amp.	Common Mode Input Voltage Range	$V_{CMRC}$	2	—	1.0	—	4.0	V
	Input Current	$I_{INC}$	2	$V_C = V_{ref} = 2.5\text{ V}$	—	—	5.0	$\mu\text{A}$
	Dead Zone Voltage Width	$V_{DZ}$	—	$V_{REF} = 2.5\text{ V}$ , $R_F = 0.3\ \Omega$	—	100	—	mV
	Input Offset Voltage	$\Delta V_{OFF} (F)$	3	CW mode, $V_{ref} = 2.5\text{ V}$ , $R_F = 0.3\ \Omega$	20	50	150	mV
		$\Delta V_{OFF} (R)$		CCW mode, $V_{ref} = 2.5\text{ V}$ , $R_F = 0.3\ \Omega$	20	50	150	
Current Limit Amp.	Limit Current	$I_{LIM}$	3	$R_F = 0.3\ \Omega$	480	600	720	mA
RUN / STOP Control Circuit	Input Voltage (H)	$V_{INS} (H)$	1	(RUN)	3.0	—	$V_{CC}$	V
	Input Voltage (L)	$V_{INS} (L)$		(STOP)	GND	—	1.0	
	Input Current	$I_{INS} (L)$		$V_{INS} = \text{GND}$	—	—	1	$\mu\text{A}$
Output Circuit	Saturation Voltage (Upper Side)	$V_{sat} (U)$	4	$I_o = 0.6\text{ A}$	—	0.1	1.3	V
	Saturation Voltage (Lower Side)	$V_{sat} (L)$	4	$I_o = 0.6\text{ A}$	—	0.6	1.0	
	Cut-off Current (Upper Side)	$I_L (U)$	5	$V_L = 16\text{ V}$	—	—	10	$\mu\text{A}$
	Cut-off Current (Lower Side)	$I_L (L)$	5	$V_L = 16\text{ V}$	—	—	10	
Mode Select Circuit	Input Voltage (H)	$V_{MS} (H)$	6	CCW mode $V_C > V_{ref}$ , BRK : L	3.0	—	$V_{CC}$	V
	Input Voltage (L)	$V_{MS} (L)$	6	Reversing brake mode $V_C > V_{ref}$ , BRK : L	—	—	0.5	
	Input Current	$I_{INMS}$	6	$V_{MS} = \text{GND}$	—	—	1	$\mu\text{A}$

CHARACTERISTICS		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
FG Amp.	Hysteresis Voltage	$V_{HYS}$	6	—	5	20	45	mV <sub>p-p</sub>
	Output Voltage (H)	$V_{OFG (H)}$	7	Source current : 10 $\mu$ A	$V_{CC}$ -0.5	—	—	V
	Output Voltage (L)	$V_{OFG (L)}$	7	Sink current : 10 $\mu$ A	—	—	0.5	
Short Brake Circuit	Input Voltage (H)	$V_{BRK (H)}$	6	—	3.0	—	$V_{CC}$	V
	Input Voltage (L)	$V_{BRK (L)}$	6	—	—	—	0.5	
	Input Current	$I_{INBRK}$	6	$V_{BRK} = GND$	—	—	1	$\mu$ A
Triangular Oscillation Circuit	Oscillation Frequency	$f_{OSC}$	—	$C = 250Pf$ (Note)	—	100	—	kHz
	Charge Current	$I_{OSC}^{+}$	7	$V_{OSC} = 1.8 V$	50	100	200	$\mu$ A
	Discharge Current	$I_{OSC}^{-}$	7	$V_{OSC} = 3.2 V$	-200	-100	-50	$\mu$ A
SW-REG Control Circuit	Saturation Voltage	$V_{sat-sw}$	8	$I_{sw} = 20 mA$	—	1.0	3.0	V
Thermal Shut-down Operating Temperature		$T_{SD}$	—	Junction temperature (according to design specification) (Note)	—	175	—	$^{\circ}C$

Note: this is not tested.

FUNCTION TABLE

			FORWARD			REVERSE		
H <sub>a</sub>	H <sub>b</sub>	H <sub>c</sub>	L <sub>a</sub>	L <sub>b</sub>	L <sub>c</sub>	L <sub>a</sub>	L <sub>b</sub>	L <sub>c</sub>
H	L	L	H	L	M	L	H	M
H	H	L	H	M	L	L	M	H
L	H	L	M	H	L	M	L	H
L	H	H	L	H	M	H	L	M
L	L	H	L	M	H	H	M	L
H	L	H	M	L	H	M	H	L

<Forward>

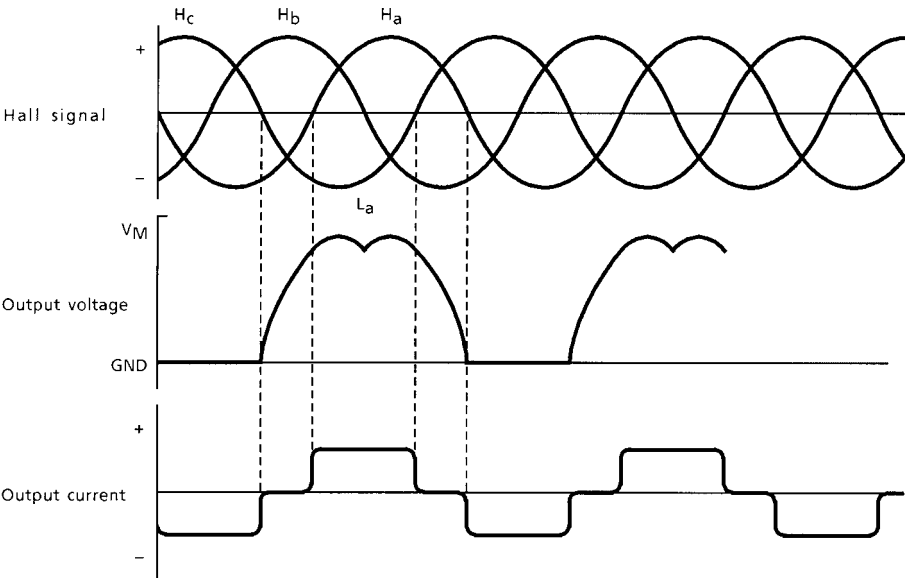
$L_a = -(H_c - H_a)$   
 $L_b = -(H_a - H_b)$   
 $L_c = -(H_b - H_c)$

<Reverse>

$L_a = (H_c - H_a)$   
 $L_b = (H_a - H_b)$   
 $L_c = (H_b - H_c)$

TIMING DIAGRAM

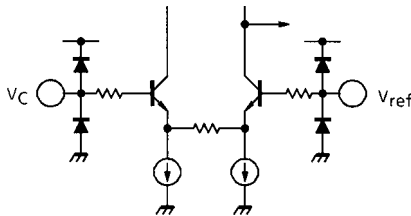
<Forward>



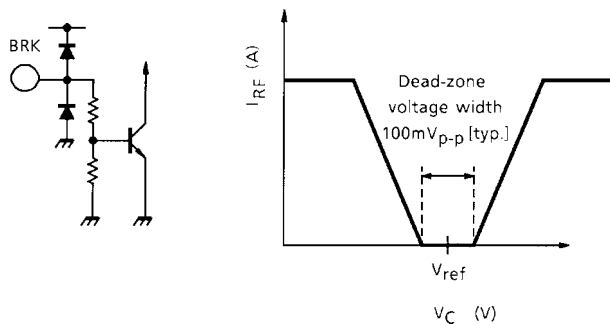
## FUNCTIONAL DESCRIPTION

This IC is a 3-phase, full-wave brushless DC motor driver of the current-control / current-drive type. It contains in its upper stage a PNP discrete power transistor, which, because of the Multi-Chip Package (MCP) structures provides high torque and thermal efficiency. In addition, when combined with a switching regulator, its efficiency can be increased still further.

- Control amp input circuit

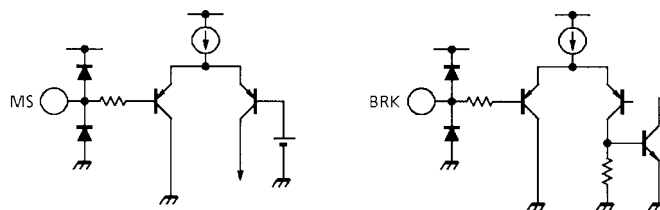


The Common mode input voltage ranges for both  $V_C$  and  $V_{ref}$  are 1.0 to 4.0 V. The control input-to-drive output gain is 1.0A / V (typ.), whose characteristic is shown below. The input is provided with a dead-zone area whose voltage width is 100 mV (typ.)



$$g_m = \frac{\Delta I_{RF}}{\Delta V_C} = 1.0 [A/V] (\text{typ.}) (\text{at } R_F = 0.3\Omega)$$

- Mode select / short brake circuit





When  $V_C > V_{ref}$ , one of three modes (Reverse Rotation, Reversing Brake or Short Brake mode) can be selected by setting the MS and BRK pins appropriately.

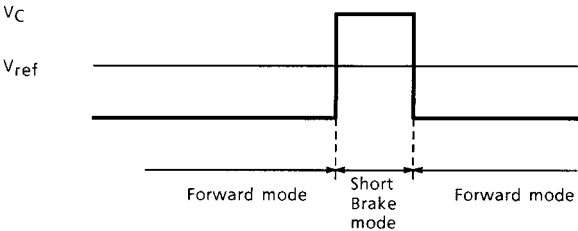
<Function>

$V_C < V_{ref}$				$V_C > V_{ref}$			
		BRK				BRK	
		H	L			H	L
MS	H	Forward	Forward	MS	H	Short brake	Reverse
	L	Forward	Forward		L	Short brake	Reversing brake

In Short Brake mode, the upper-stage power transistor is turned on and the lower-stage power transistor is turned off.  
In Reversing Brake mode, all outputs are cut off after detection of reverse rotation, causing the motor to stop.

(Short brake)

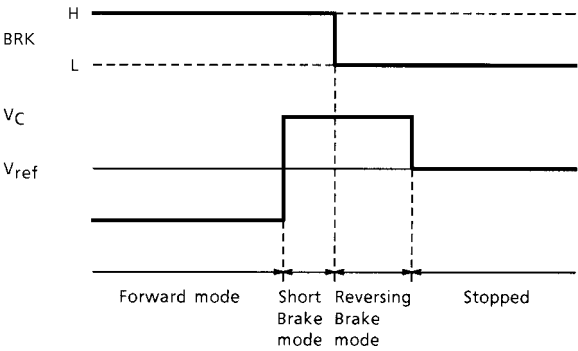
MS : H or L, BRK : H



(Reversing brake)

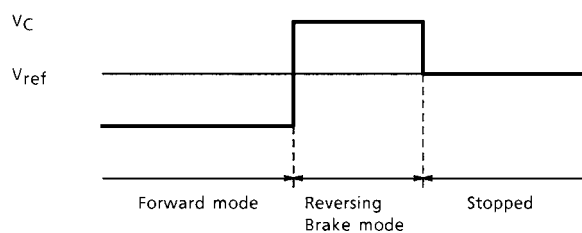
(1) When stopping the motor by applying a reversing brake after a short brake

MS : L



## (2) When stopping the motor using Reversing Brake mode

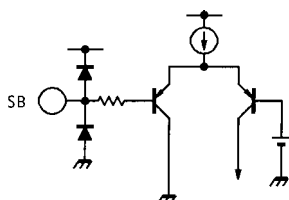
MS : L, BRK : L



Note: For an explanation of the Reversing Brake mode stopping sequence, refer to the explanation of the reverse rotation detection circuit.

The short brake generates less heat than the reversing brake. Therefore Toshiba recommends a combined use of the short and reversing brakes when stopping the motor.

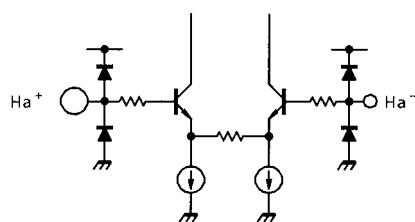
- Run / stop control circuit



When the driver IC is standing by, all of its circuits except the FG amp and the hall amp are turned off.

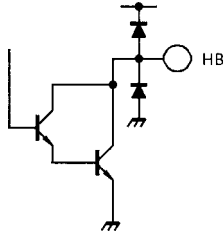
H : start  
L : standby

- Hall amp circuit



The common mode input voltage range for  $V_{CMRH}$  is 1.5 to 4.0 V.

- Hall element bias circuit

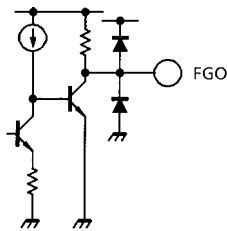


The hall element bias current is turned off when the driver IC is in standby state. Make sure that the negative hall bias line is connected to the HB pin. The remaining voltage is as follows :

$$V_{HB} = 1.2 \text{ [V] (typ.)} \quad \text{at } I_{HB} = 10 \text{ mA}$$

Furthermore, this circuit cannot be used if FG output is necessary in standby state. When the HB terminal is not used, the negative hall bias line must be connected to GND with a resistor in between.

- FG amp circuit



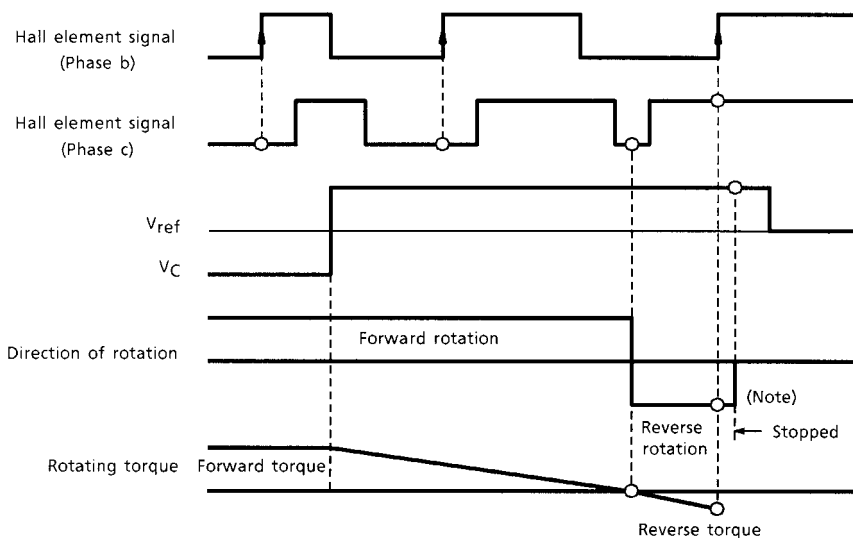
This circuit uses a hall element signal which is output to FGO after a Schmitt stage. The FG amp has a hysteresis of 20 [mV<sub>p-p</sub>] (typ.) and its output voltages are

$$\begin{aligned} \text{High level} &: V_{CC} - 0.5 \sim V_{CC} \text{ [V]} \\ \text{Low level} &: \text{GND} \sim 0.5 \text{ [V] at } I_{OFG} = 10 \mu\text{A} \end{aligned}$$

The FG amp is active when it is in standby state. When the hall element signal is input, the FG signal is output.

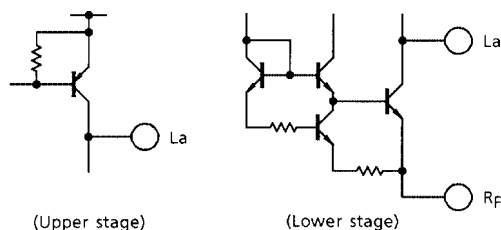
- Reverse rotation detection circuit

By comparing the two phases of the Hall element signal, this circuit detects a state where the phases are inverted, at which time the torque is reduced to 0. The detection accuracy is determined by the number of pulses per rotation of Hall element output.



Note: Due to its inertial force, the motor does not stop immediately after the torque is reduced to 0.

- Output circuit



This circuit uses the power transistor's base current to regulate the circuit's output current.

The upper-stage power transistor consists of a PNP discrete transistor (RN6006), which gives high torque efficiency.

- Current limiter circuit

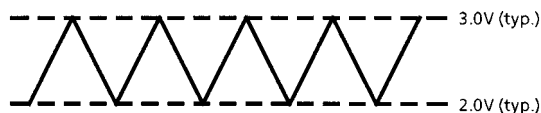
The current limit value is determined by the equation below.

$$I_{LIM} \approx \frac{0.24}{R_F + 0.1} \text{ [A] (typ.)}$$

- Triangular wave oscillator circuit

Triangular waves are generated by connecting a capacitor between the OSC pin and GND. The charging / discharging currents are  $\pm 50 \mu\text{A}$ , and the oscillation frequency is as

$$f_{\text{OSC}} = \frac{100 (\mu\text{A})}{2 \times C (\text{pF})} [\text{Hz}]$$

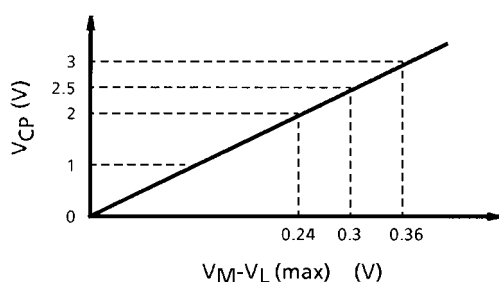


Taking into account efficiency considerations and the effects of noise, Toshiba recommends using the IC with an oscillation frequency of more or less 100kHz.

- $V_M$  output voltage (3-phase maximum) detection circuit

This circuit selects the highest voltage from the three phases of output voltages and then outputs the voltage difference between the selected voltage and  $V_M$  as a voltage referenced to GND ( $V_{CE}$  for the upper output stage). This voltage is filtered by a capacitor at the CP pin and compared with the triangular wave before being output on the SWC pin.

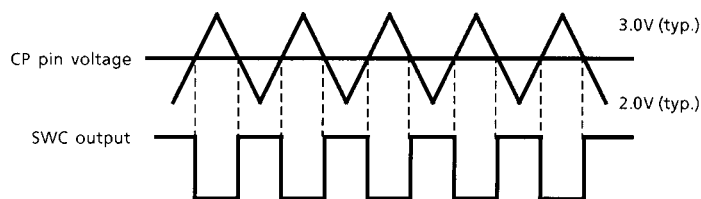
When using a switching regulator, the driver IC operates in a closed loop with a  $V_{CE}$  of 0.3V (typ.) for the upper output stage.



- Switching regulator control signal output circuit

This circuit outputs the result of comparison between  $V_{CE}$  for the upper stage and the triangular wave from one of the open-collector output terminals. By controlling an external PNP transistor in this way, the circuit controls  $V_M$ .

The output function is as follows :



- Thermal shut down circuit

This circuit turns off output when  $T_j = 175^\circ\text{C}(\text{typ.})$  (according to design specification).

## EXTERNAL PARTS

TERMINAL No.	FUNCTION	RECOMMENDED VALUE	REMARKS
C <sub>1</sub>	Control system phase correction	0.01 $\mu$ F	(Note 1)
C <sub>2</sub>	Triangular wave oscillation	250 pF	See Page 12.
C <sub>3</sub>	Power supply line oscillation prevention	0.22 $\mu$ F	—
C <sub>4</sub>	Filter	1 $\mu$ F (Electrolytic capacitor)	(Note 2)
C <sub>5</sub>	Forward / reverse changeover gain adjustment	0.01 $\mu$ F	(Note 3)
C <sub>6</sub>	For switching regulator	100 $\mu$ F (Electrolytic capacitor)	—
R <sub>1</sub>	Hall element bias	—	(Note 4)
R <sub>2</sub>	Control amp reference voltage	—	(Note 5)
R <sub>3</sub>	Output current detection	0.3 $\Omega$	See Page 11.
R <sub>4</sub>	Base current control for switching regulator PNP transistor	1 k $\Omega$	(Note 6)
R <sub>5</sub>	Leakage absorption of switching regulator PNP transistor	10 k $\Omega$	(Note 7)
L <sub>1</sub>	For switching regulator	68 $\mu$ H	—

Note 1: Check carefully to see that there is no output oscillation.

Note 2: This is used to filter the output of the difference between the three-phase output voltage and  $V_M$ .

Note 3: This is used to adjust the rotation direction changeover gain.

The capacitance value and the gain are in inverse.

This capacitance is to prevent from output through current.

Note 4: Be sure to set this bias so that the hall element output amplitude and common mode input voltage fall within the ranges specified in the table of electrical characteristics.

Note 5: This voltage must be set to fall within the Common mode input voltage range of the control amp. Toshiba recommends setting it to  $V_{CC} / 2$ .

Also, consider the Vref pin's input current: 1.3  $\mu$ A (typ.) (when  $V_C \ll V_{ref}$ ) when setting the resistance value.

Note 6: The SWC pin is an open-collector, so that when the internal transistor saturates, its switching characteristic is degraded. Toshiba recommends that when SWC is low, its pin voltage should be 2V or above.

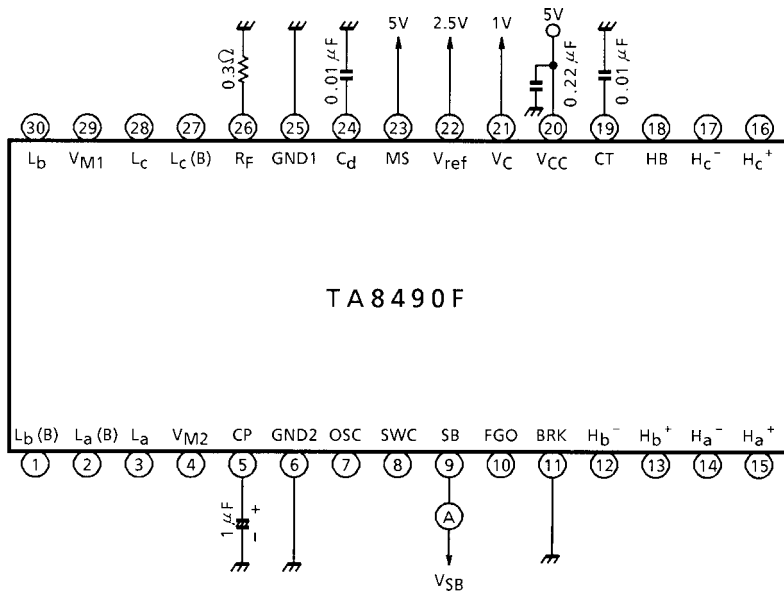
Note 7: The external PNP transistor used for the switching regulator has its offset voltage determined by this resistance. Use a resistance of between several k $\Omega$  and 10 k $\Omega$  according to the switching characteristics.

\*: Tr.1: 2SA1241

D1 : U1GWJ44

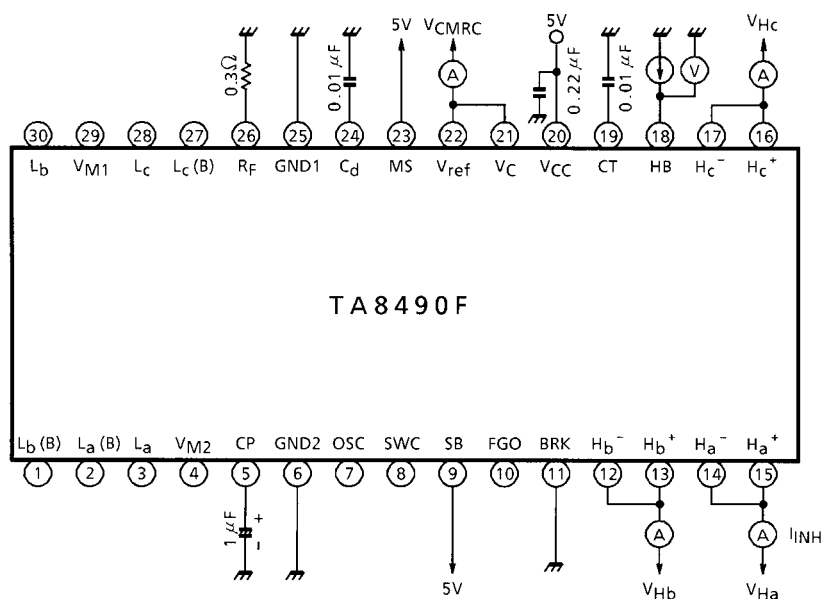
## TEST CIRCUIT

### 1. $I_{CC1}$ , $I_{CC2}$ , $V_{INS}$ (H), $V_{INS}$ (L), $I_{INS}$



- $I_{CC1}$  :  $V_{SB} = 3.0 \text{ V}$
- $I_{CC2}$  :  $V_{SB} = 0.5 \text{ V}$
- $V_{INS}$  (H),  $V_{INS}$  (L): Jndged by the gap between  $I_{CC1}$  and  $I_{CC2}$
- $V_{INS}$  :  $V_{INS} = 0 \text{ V}$

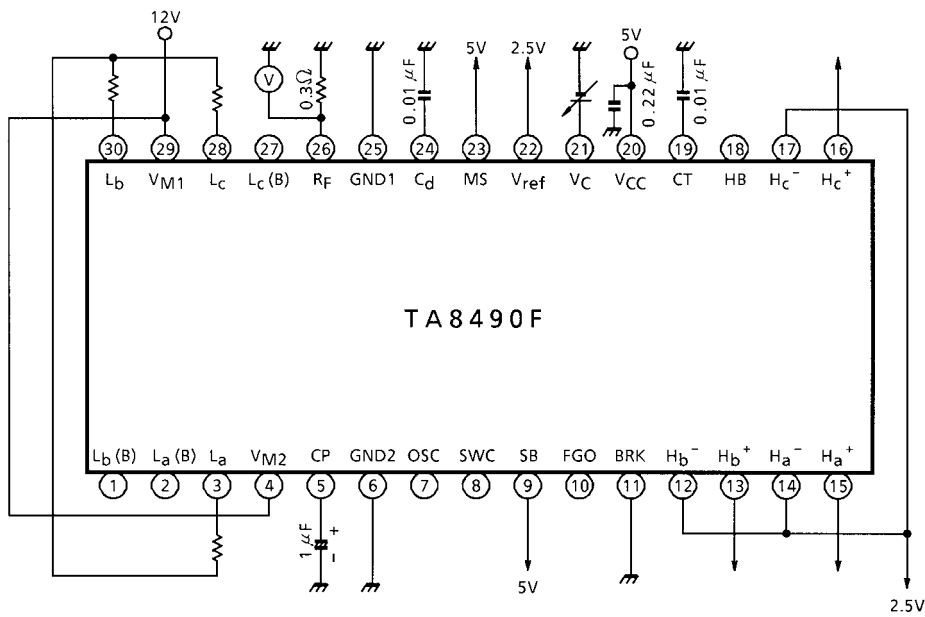
**2.  $I_{INH}$ ,  $I_{CMRH}$ ,  $V_{HB}$ ,  $I_{INC}$ ,  $V_{CMRC}$**



- $I_{INH}$  : Total of a phase negative and positive input current.  $V_{Ha} = V_{Hb} = V_{Hc} = 2.5\text{ V}$
- $V_{CMRH}$  : Measure the  $I_{INH}$  gap between  $V_{Ha} = 1.5\text{ V}$  and  $V_{Ha} = 4.0\text{ V}$ .  
b and c phase are measured the same method.
- $V_{HB}$  :  $I_{HB} = 10\text{ mA}$
- $V_{INC}$  : Total of  $V_C$  and  $V_{ref}$  input current. At  $V_{CMRC} = 2.5\text{ V}$ .
- $V_{CMRC}$  : Measure the  $I_{INC}$  gap between  $V_{CMRC} = 1.0\text{ V}$  and  $V_{CMRC} = 4.0\text{ V}$ .

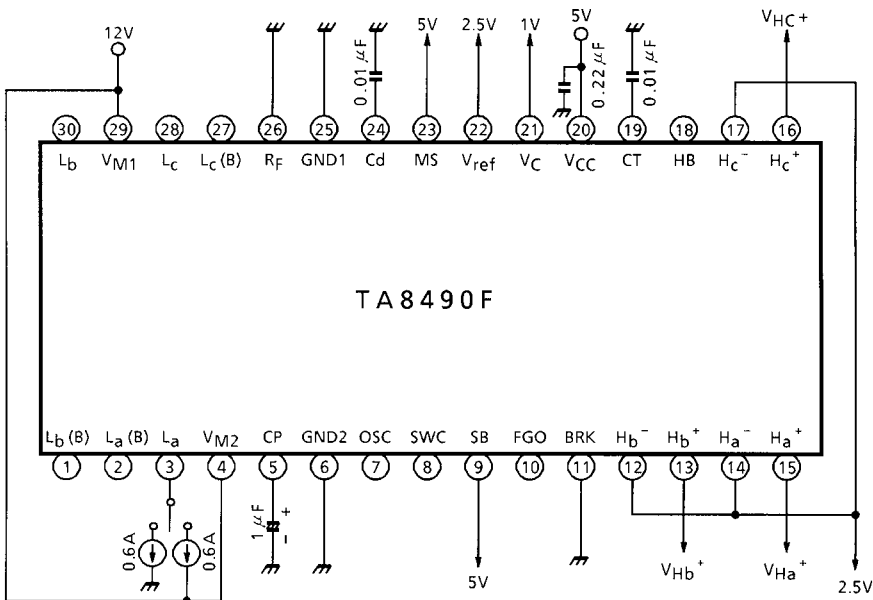


### 3. $\Delta V_{OFF} (F)$ , $\Delta V_{OFF} (R)$ , $I_{LIM}$



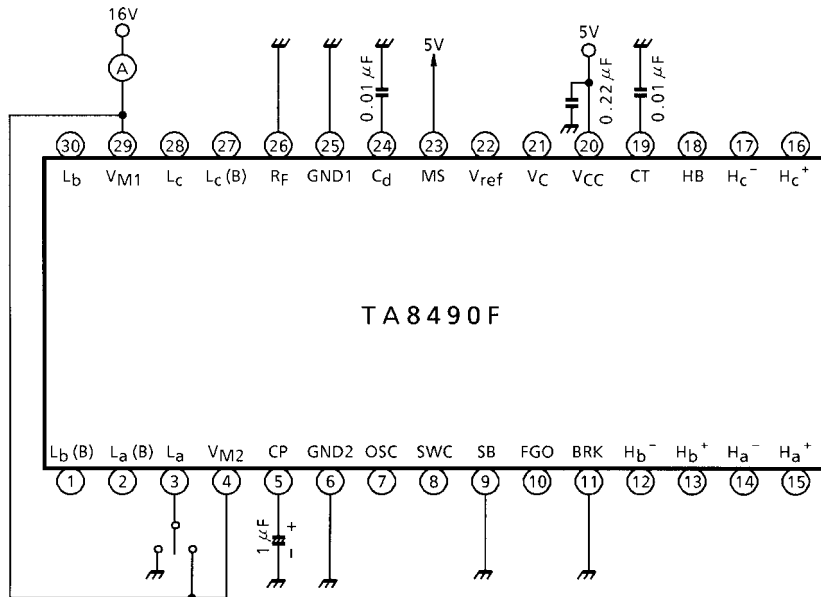
- $\Delta V_{OFF} (F)$  : Measure  $V_{RF}$  at  $V_C = 2.48 \text{ V} / 2.35 \text{ V}$ .
- $\Delta V_{OFF} (R)$  : Measure  $V_{RF}$  at  $V_C = 2.52 \text{ V} / 2.65 \text{ V}$ .
- $I_{LIM}$  : Change to current value after measuring  $V_{RF}$  at  $V_C = 1.0 \text{ V}$

### 4. $V_{sat} (U)$ , $V_{sat} (L)$



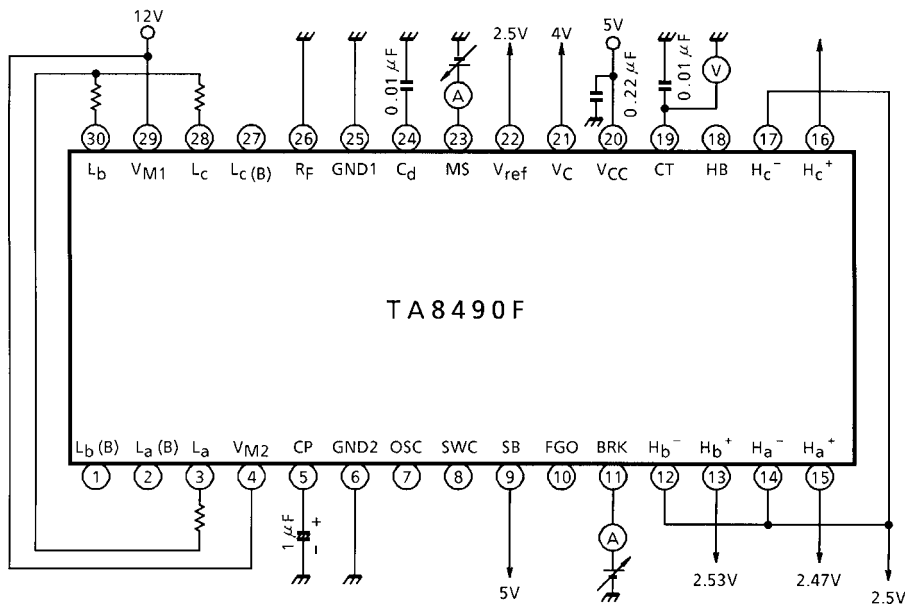
- $V_{sat} (U)$  : Determined output function by  $V_{Ha}^+$ ,  $V_{Hb}^+$ ,  $V_{Hc}^+$  (2.4 V / 2.6 V). Measure voltage value between  $V_M$  and  $L_a$ . b phase and c phase are measured the same method.
- $V_{sat} (L)$  : Determined output function by  $V_{Ha}^+$ ,  $V_{Hb}^+$ ,  $V_{Hc}^+$  (2.4 V / 2.6 V). Measure voltage value between  $L_a$  and GND. b phase and c phase are measured the same method.

## 5. $I_L(U)$ , $I_L(L)$



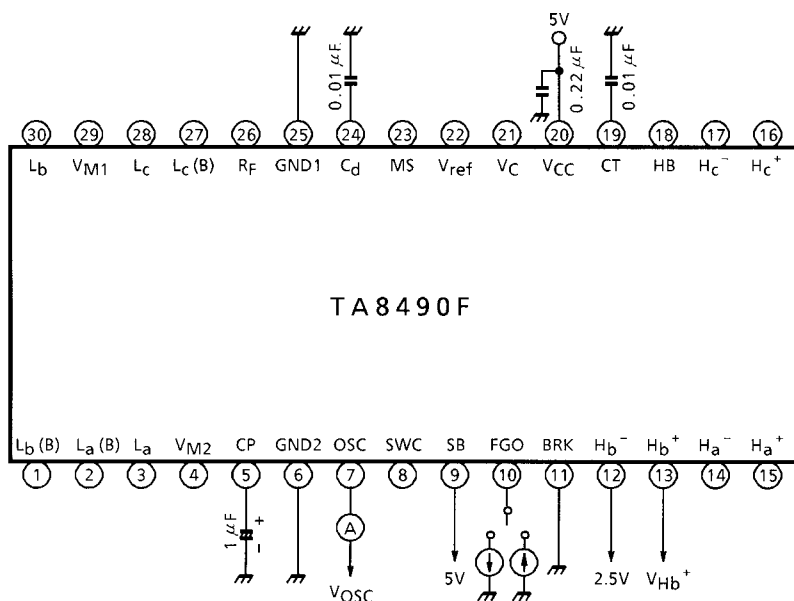
- $I_L(U)$  : Measure  $I_M$  when  $L_a$  and GND are shorted. b phase and c phase are measured the same method.
- $I_L(L)$  : Measure  $I_M$  when  $V_M$  and  $L_a$  are shorted. b phase and c phase are measured the same method.

## 6. $V_{MS}(H)$ , $V_{MS}(L)$ , $I_{INS}$ , $V_{BRK}(H)$ , $V_{BRK}(L)$ , $I_{INBRK}$



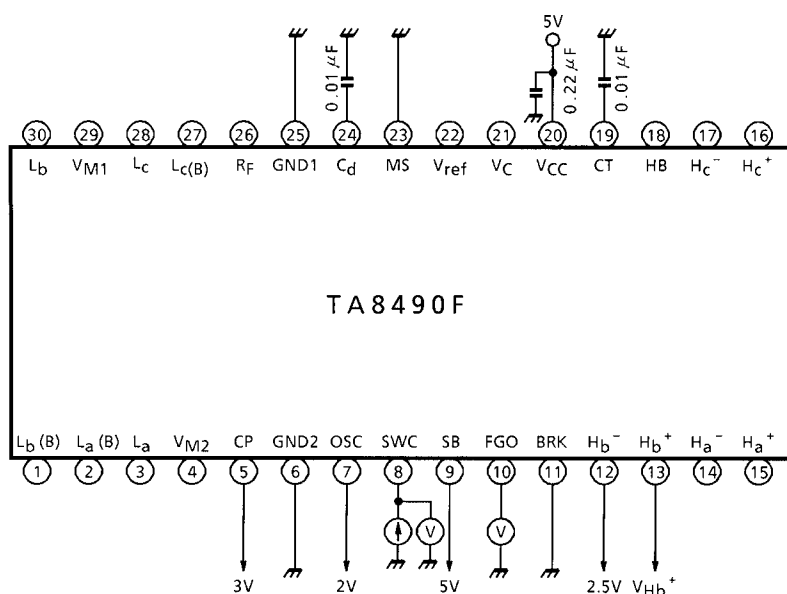
- $V_{MS}(H)$  :  $V_{MS} = 3.0\text{ V}$ ,  $V_{BRK} = 0\text{ V}$ , verify that output function is reverse mode.
- $V_{MS}(L)$  :  $V_{MS} = 0.5\text{ V}$ ,  $V_{BRK} = 0\text{ V}$ , verify that  $V_{CT} \approx 0\text{ V}$
- $I_{INS}(L)$  :  $V_{MS} = 0\text{ V}$ ,  $V_{BRK} = 0\text{ V}$
- $V_{BRK}(H)$  :  $V_{MS} = 5\text{ V}$ ,  $V_{BRK} = 3.0\text{ V}$ , verify that  $L_a = L_b = L_c : H$
- $V_{BRK}(L)$  :  $V_{MS} = 5\text{ V}$ ,  $V_{BRK} = 0.5\text{ V}$ , verify that output function is reverse mode.

## 7. $V_{OFG}(H)$ , $V_{OFG}(L)$ , $I_{osc}^+$ , $I_{osc}^-$



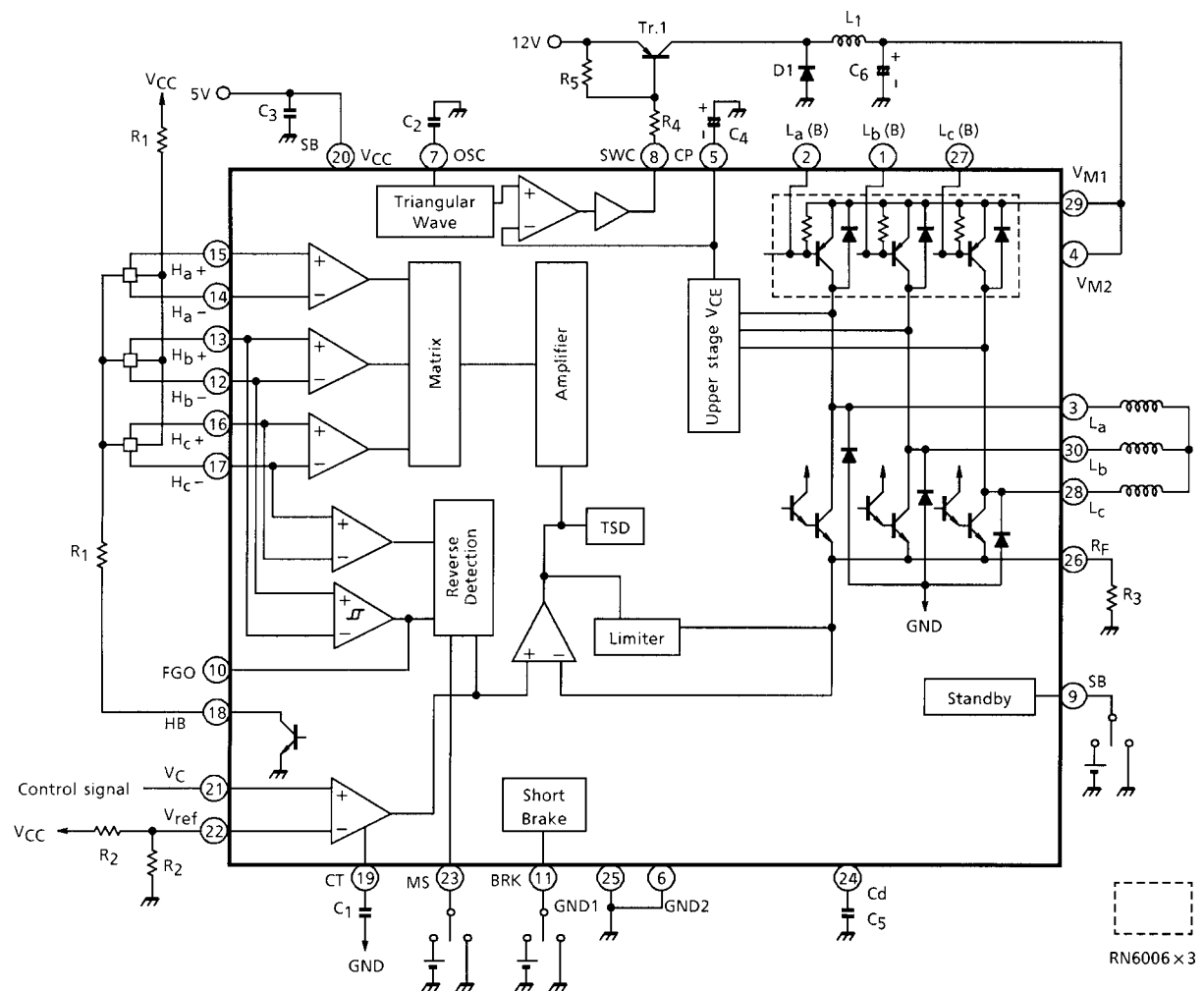
- $V_{OFG}(H)$  :  $V_{Hb}^+ = 2.53\text{ V}$ ,  $I_{FGO} = 10\text{ }\mu\text{A}$  (source)
- $V_{OFG}(L)$  :  $V_{Hb}^+ = 2.47\text{ V}$ ,  $I_{FGO} = 10\text{ }\mu\text{A}$  (sink)
- $I_{osc}^+$  :  $V_{OSC} = 2\text{ V}$
- $I_{osc}^-$  :  $V_{OSC} = 3\text{ V}$

## 8. $V_{sat-sw}$ , $V_{HYS}$



- $V_{sat-sw}$  :  $I_{swc} = 20\text{ mA}$
- $V_{HYS}$  : Switch the  $V_{Hb}^+$  from high (H) to low (L) and from L to H. Measure the  $V_{Hb}^+$  at the point when FGO function changes.

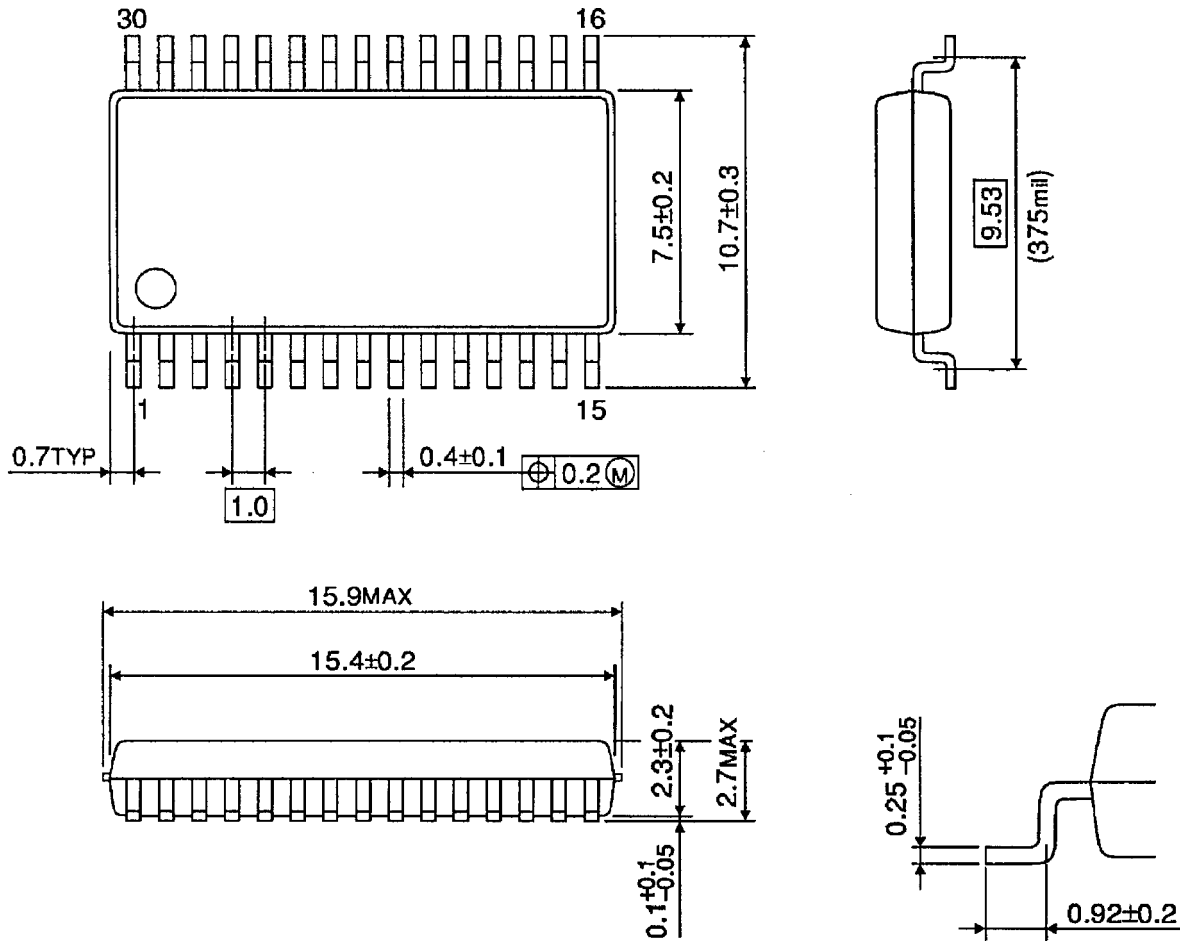
## APPLICATION CIRCUIT



PACKAGE DIMENSIONS

SSOP30-P-375-1.00

Unit : mm



Weight : 0.63 g (Typ.)

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