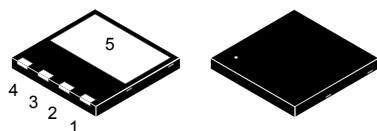
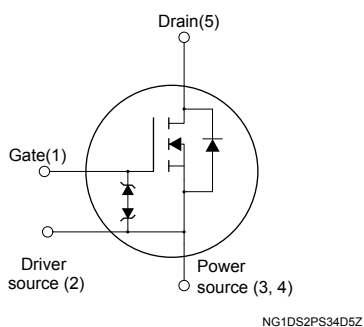


N-channel 600 V, 0.184 Ω typ., 16 A MDmesh™ M2 EP Power MOSFET in a PowerFLAT™ 8x8 HV package



PowerFLAT™ 8x8 HV



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on)}$ max.	I_D
STL25N60M2-EP	650 V	0.205 Ω	16 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for Very High Frequency Converters ($f > 150$ kHz)

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 EP enhanced performance technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Product status	
STL25N60M2-EP	
Device summary	
Order code	STL25N60M2-EP
Marking	25N60M2EP
Package	PowerFLAT™ 8x8 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	16	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	10	A
$I_{DM}^{(1)}$	Drain current (pulsed)	64	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	125	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 16\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	45	$^{\circ}\text{C}/\text{W}$

1. When mounted on FR-4 board of inch^2 , 2oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	3.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	180	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$		0.184	0.205	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1090	-	pF
C_{oss}	Output capacitance		-	56	-	pF
C_{rss}	Reverse transfer capacitance		-	1.6	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	255	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	7	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 18\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Gate charge test circuit)	-	29	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching Energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% V_{GS} to 0% I_D)	$V_{DD} = 400\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	7	-	μJ
		$V_{DD} = 400\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	8	-	μJ

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 9\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14. Switching times test circuit for resistive load and Figure 19. Switching time waveform)	-	15	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	61	-	ns
t_f	Fall time		-	16	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		64	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 16\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	360		ns
Q_{rr}	Reverse recovery charge		-	5		μC
I_{RRM}	Reverse recovery current		-	28		A
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	445		ns
Q_{rr}	Reverse recovery charge		-	6.5		μC
I_{RRM}	Reverse recovery current		-	29		A

1. Pulse width is limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

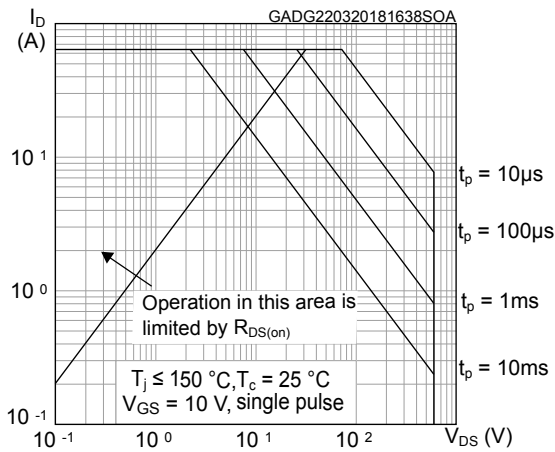


Figure 2. Thermal impedance

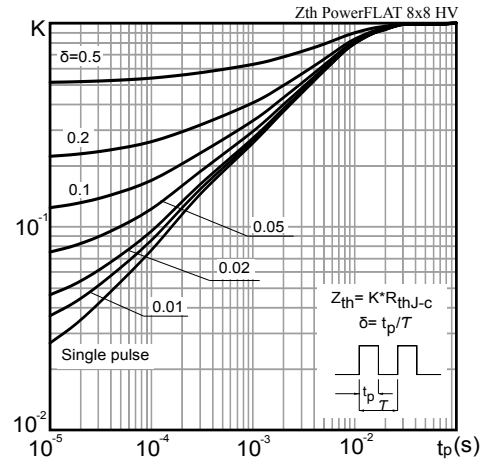


Figure 3. Output characteristics

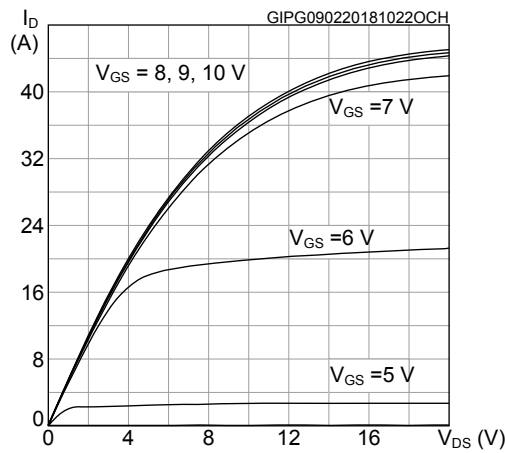


Figure 4. Transfer characteristics

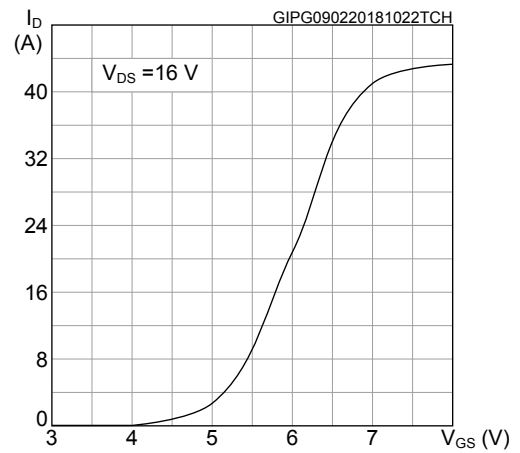


Figure 5. Gate charge vs gate-source voltage

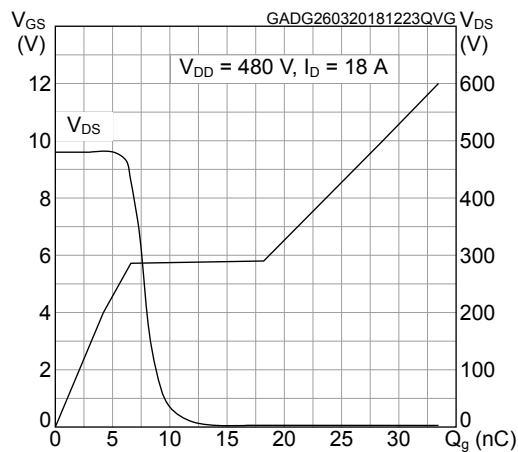


Figure 6. Static drain-source on-resistance

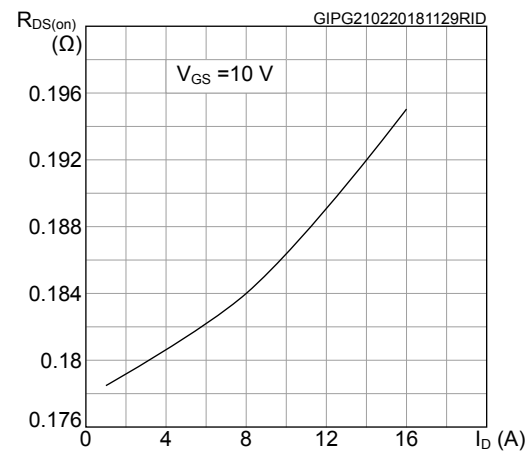


Figure 7. Capacitance variations

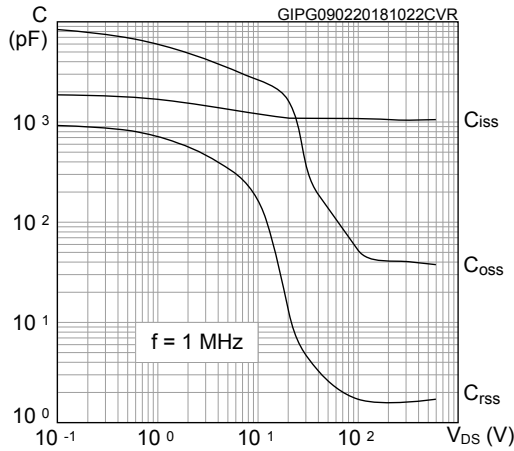


Figure 8. Output capacitance stored energy

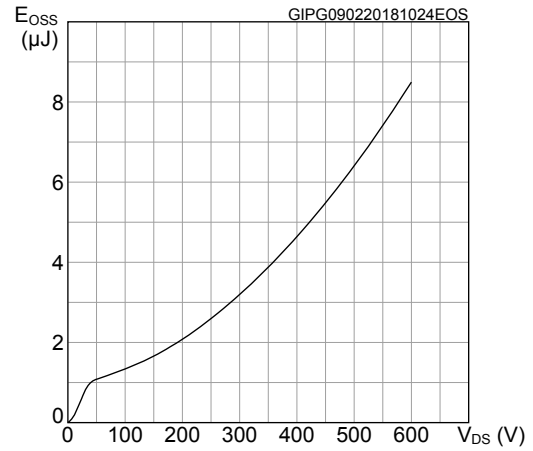


Figure 9. Turn-off switching energy vs drain current

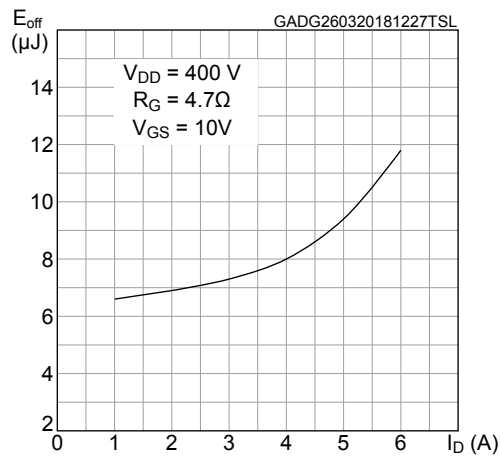


Figure 10. Normalized gate threshold voltage vs temperature

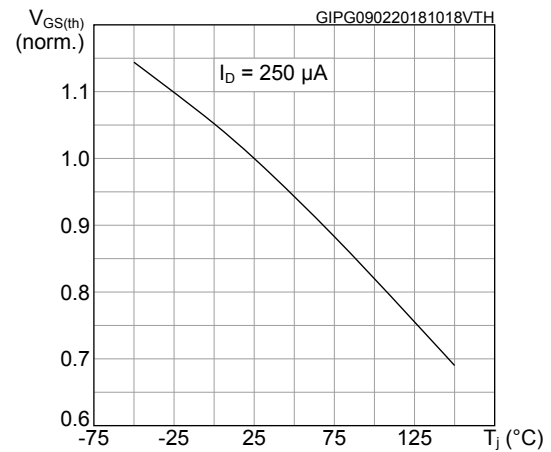


Figure 11. Normalized on-resistance vs temperature

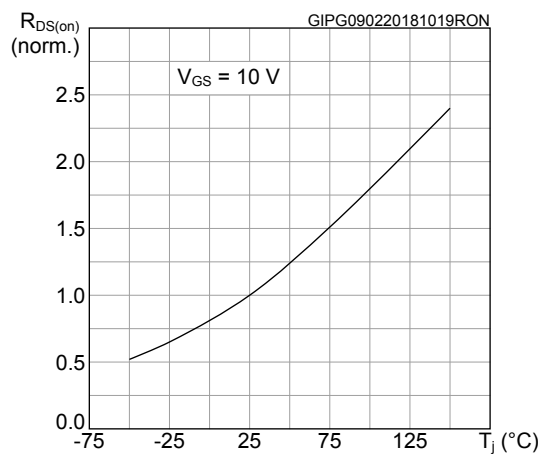


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

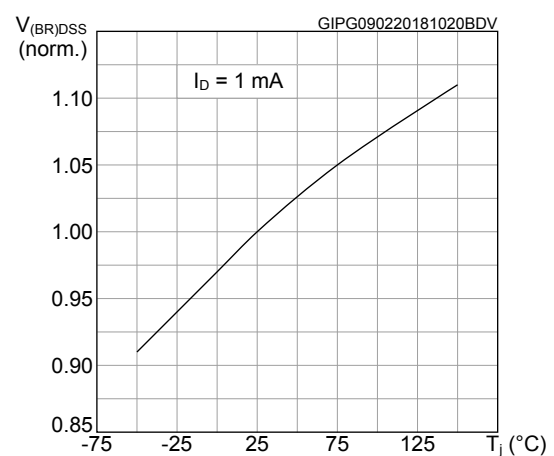
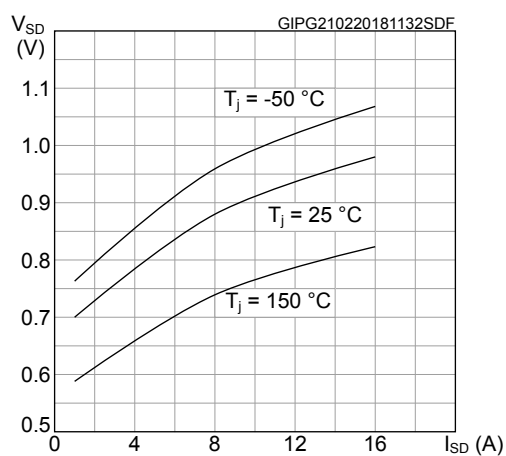
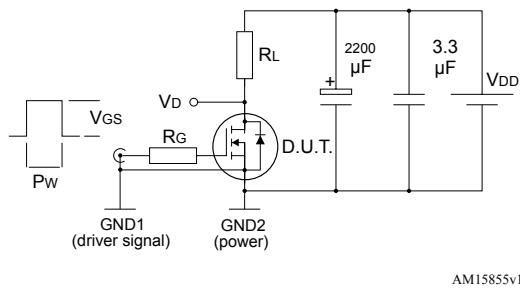
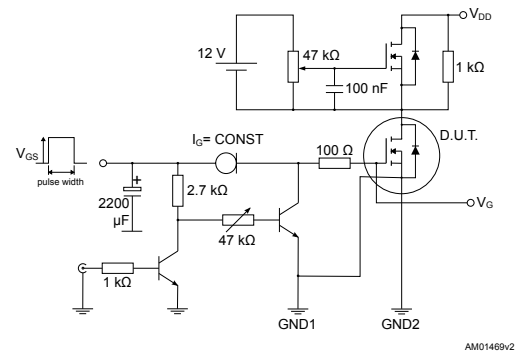
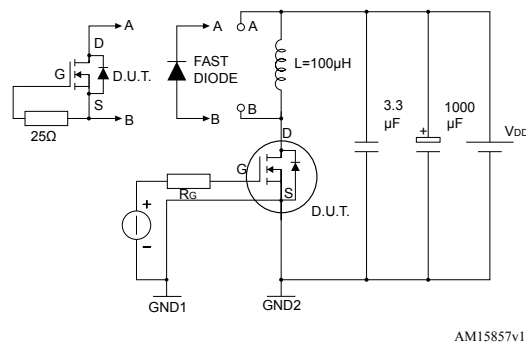
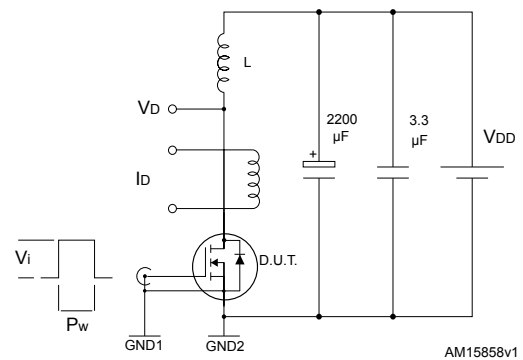
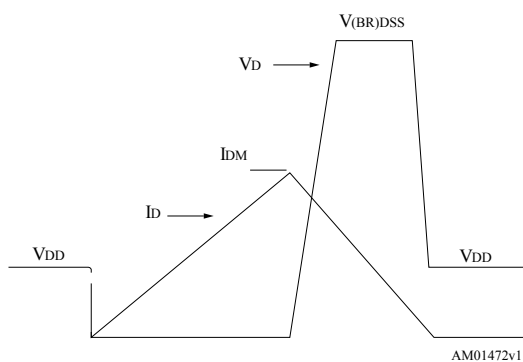
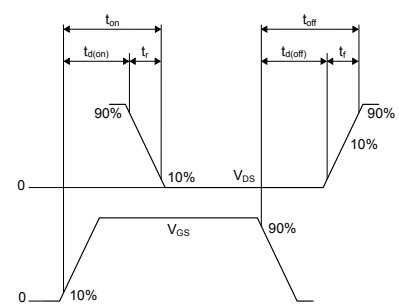


Figure 13. Source-drain diode forward characteristics



3 Test circuits

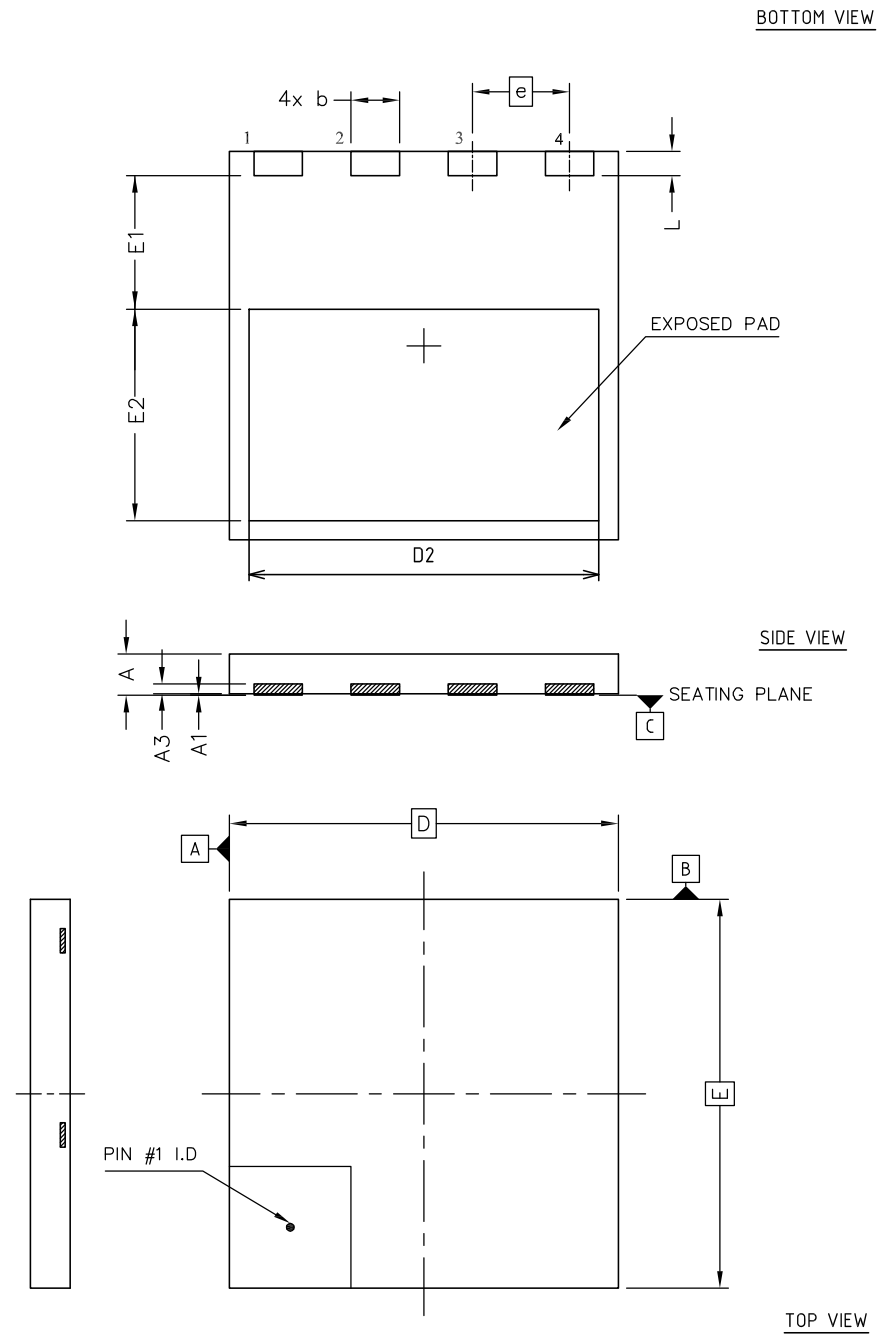
Figure 14. Switching times test circuit for resistive load

Figure 15. Gate charge test circuit

Figure 16. Test circuit for inductive load switching and diode recovery times

Figure 17. Unclamped inductive load test circuit

Figure 18. Unclamped inductive waveform

Figure 19. Switching time waveform


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 8x8 HV package information

Figure 20. PowerFLAT™ 8x8 HV package outline

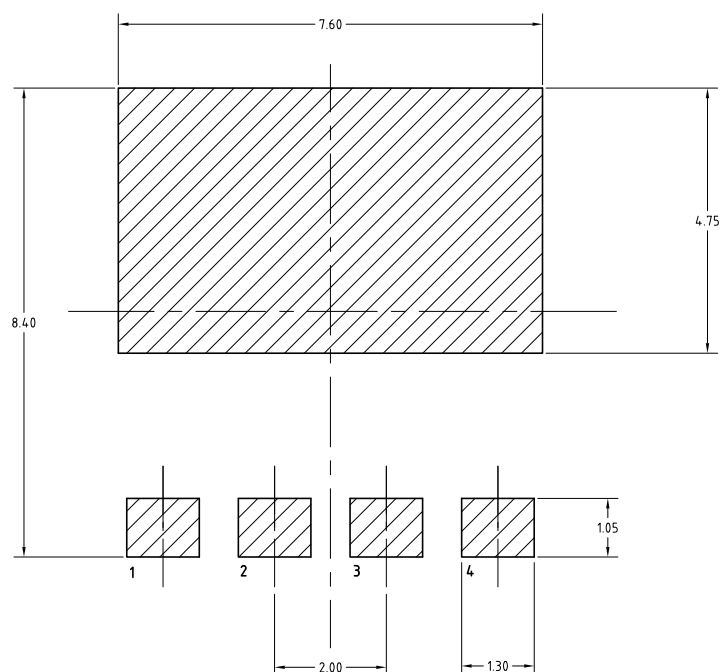


8222871_Rev_4

Table 9. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

Figure 21. PowerFLAT™ 8x8 HV footprint

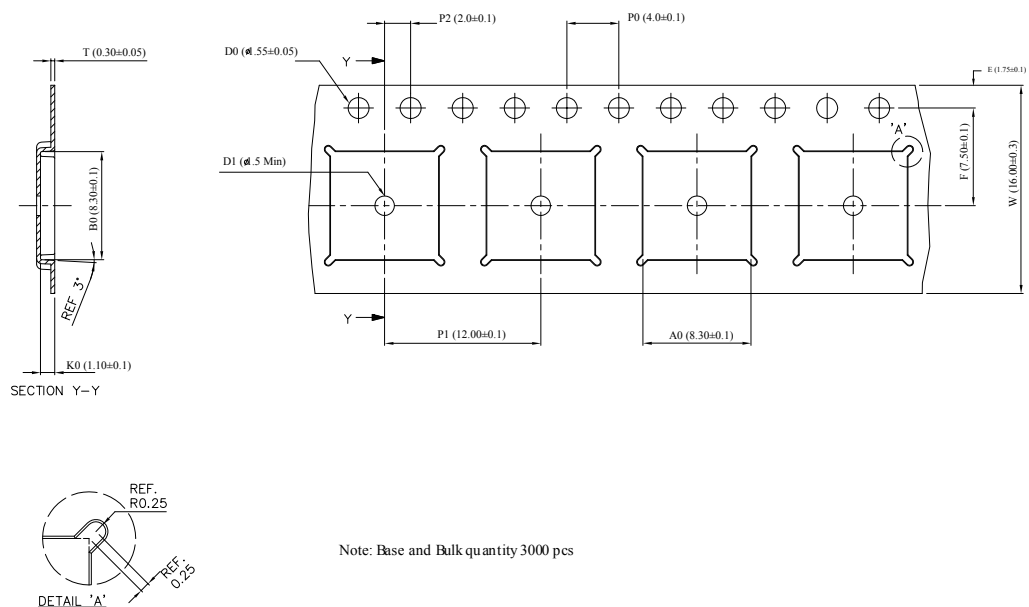


8222871_REV_4_footprint

Note: All dimensions are in millimeters.

5 PowerFLAT™ 8x8 HV packing information

Figure 22. PowerFLAT™ 8x8 HV tape



8229819_Tape_revA

Note: All dimensions are in millimeters.

Figure 23. PowerFLAT™ 8x8 HV package orientation in carrier tape

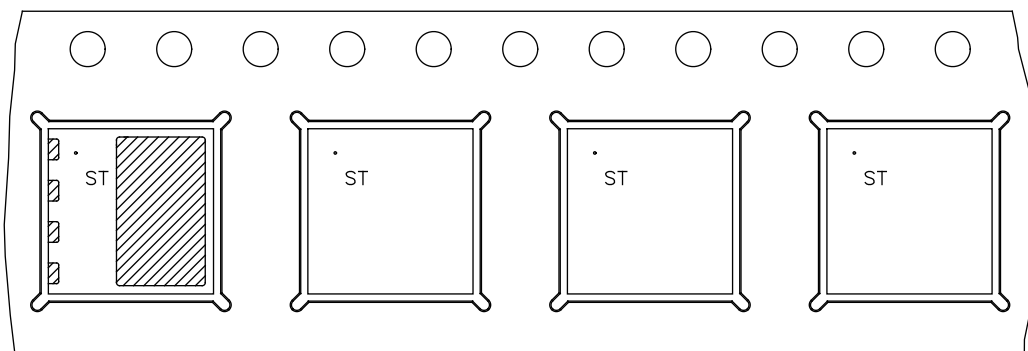
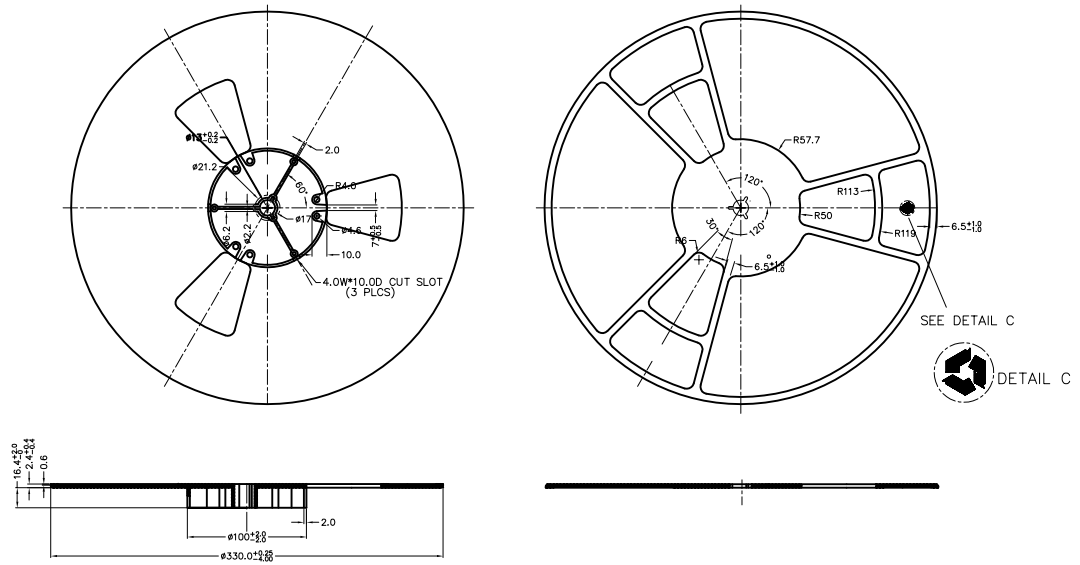


Figure 24. PowerFLAT™ 8x8 HV reel



8229819_Reel_revA

Note: All dimensions are in millimeters.

Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Dec-2014	1	First release.
12-Jan-2015	2	Updated product status from "preliminary data" to "production data".
20-Nov-2015	3	Updated: cover image and <i>Figure 1: "Internal schematic diagram"</i> Updated: <i>Section 3: "Test circuits"</i> Modified: <i>Section 4.1: "PowerFLAT 8x8 HV package information"</i> Minor text changes
21-Feb-2018	4	Removed maturity status indication from cover page. The document status is production data. Modified <i>Table 1. Absolute maximum ratings</i> , <i>Table 4. On/off states</i> , <i>Table 5. Dynamic</i> , <i>Table 6. Switching Energy</i> , <i>Table 7. Switching times</i> and <i>Table 8. Source drain diode</i> . Modified the entire <i>Section 2.1 Electrical characteristics (curves)</i> . Minor text changes.
26-Mar-2018	5	Modified <i>Table 1. Absolute maximum ratings</i> , <i>Table 4. On/off states</i> , <i>Table 5. Dynamic</i> , <i>Table 6. Switching Energy</i> , <i>Table 7. Switching times</i> , <i>Table 8. Source drain diode</i> and <i>Section 2.1 Electrical characteristics (curves)</i> . Minor text changes.

Contents

1	Electrical ratings.....	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics (curves).....	5
3	Test circuits	8
4	Package information.....	9
4.1	PowerFLAT™ 8x8 HV package information	9
5	PowerFLAT™ 8x8 HV packing information	12
	Revision history	14
	Contents	15
	Disclaimer.....	16

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved