NXP level-shifting and hot-swappable I²C/SMBus buffers PCA9510A/11A/12B/13A/14A

I²C/SMBus buffers for backplane multi-point and hot-swap applications

These bus buffers isolate the backplane and card capacitance to permit the design of larger systems. They support live insertion with idle detect and precharge features, provide bidirectional operation, and are suitable for multi-master environments.

Key features

- Bidirectional buffering for live insertion/removal from backplane
- Compatible with I²C-bus Standard- and Fast-mode, and SMBus
- Support clock stretching, multiple master arbitration, and synchronization
- Operating power-supply voltage: 2.7 to 5.5 V
- Operating temperature: -40 to +85 °C
- 8-pin SO and TSSOP (MSOP) packages

Key benefits

- Enable 24/7 system operation
- Use I²C/SMBus in multi-point architectures
- Build expandable systems without modifying current architecture
- Simple implementation requires no programming
- Small footprint

Applications

- Insertion/removal of unpowered cards into active I²C/SMBus
- Increasing the number of I²C/SMBus devices
- Increasing the I²C/SMBus wiring capacitance beyond the 400 pF limit
- Supporting different operating supply voltages or logic voltage levels within a system
- Isolating sections of the I²C/SMBus
- Long bus wiring or multi-point backplane traces

PCA951x bus buffers allow insertion of an I/O card into a live backplane without corrupting the clock or data buses. They are compatible with the IPMI system-management architecture and support PICMG 2.9 CompactPCI/VME and PICMF 3.x Advanced TCA cards.

The devices provide bidirectional buffering for the I²C-bus clock (SCL) and data (SDA) lines, so they increase fanout and prevent corruption of the active I²C-bus data during board insertion or removal from the backplane.

They are suitable for use in multi-master I²C/SMBus environments, since they support bus arbitration and contention with master devices located on any I²C-bus segments. They operate at up to 400 kHz with a supply voltage from 2.7 to 5.5 V and are not 5 V tolerant due to the rise time accelerator except for the PCA9510A since it doesn't have the rise time accelerator. They are compatible with I²C-bus Standard-mode (0-100 kHz), Fast-mode (0-400 kHz), and the SMBus (10-100 kHz).

Control circuitry prevents the backplane I²C-bus from being connected to the card I²C-bus until a Stop command or Bus Idle occurs on the backplane. When the connection is made, the bus buffers provide bidirectional buffering, keeping the backplane and card capacitances isolated.

Rise-time accelerator circuitry support the use of weaker DC pull-up resistors while meeting rise-time requirements. In the PCA9513A and the PCA9514A, the threshold for the rise-time accelerator has been moved from 0.6 V to 0.8 V, to provide better noise margin. In the PCA9510A, the rise-time accelerator is deactivated.

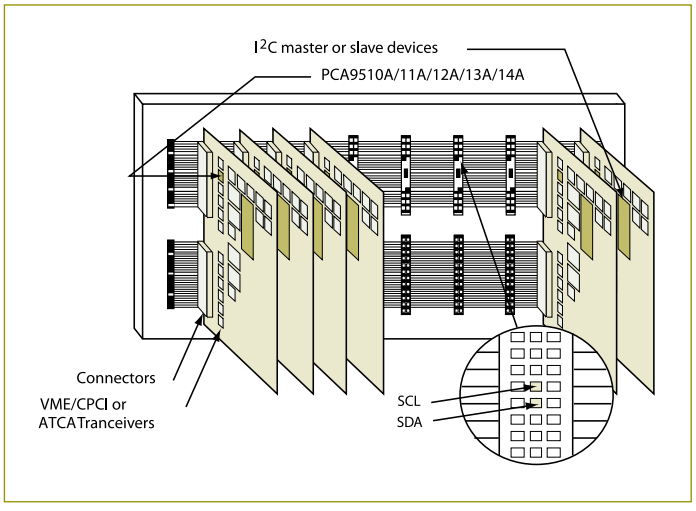
During insertion, the PCA9510A/11A SDA and SCL lines are precharged to 1 V. This minimizes the current required to charge the parasitic capacitance of the chip and prevents the I²C-bus from glitching. The PCA9513A and the PCA9514A don't have this feature, so they can support those live-insertion applications where the precharge is detrimental and new resistive-tip pins are more effective.

For PICMB applications, instead of using pull-up resistors, the PCA9513A supplies a 92 µA current source to the SCLIN and SDAIN pins. Including the current source in the device reduces part count and provides a consistent RC time constant while cards are removed or inserted into the backplane. As more cards are added, thereby increasing the bus capacitance, the effective pull-up resistance decreases because there are more current sources in parallel and thus maintains the RC time constant.

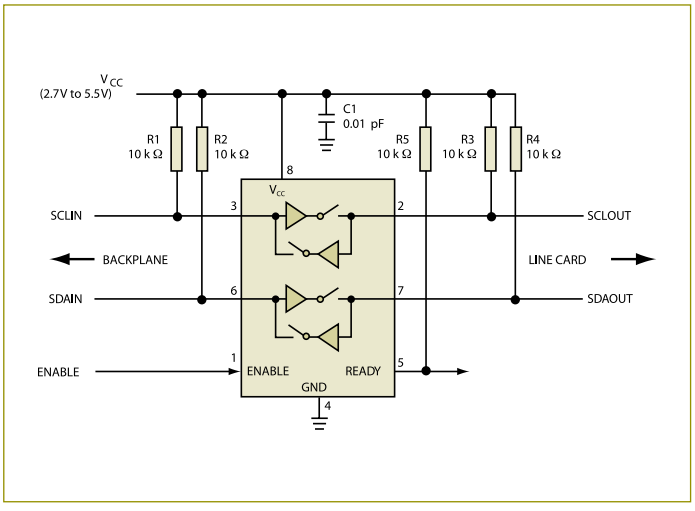
On the PCA9510A, PCA9511A, PCA9513A, and the PCA9514A, a digital ENABLE input pin enables the device when asserted HIGH and forces the device into a low-current mode when asserted LOW. An open-drain READY output pin indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

The PCA9512B is similar to the PCA9511A, but without the digital ENABLED input pin and the open-drain READY output pin. It replaces the ENABLED pin with a dedicated pin for supply voltage (V_{CC2}) on the card side. This provides level shifting, with optimal noise margin, between 3.3 and 5 V systems. The backplane and the card can both be powered with supply voltages ranging from 2.7 to 5.5 V with no constraints on which supply voltage is higher or when the supply voltage is applied. The PCA9512B replaces the READY pin with a digital CMOS input pin (ACC), which enables when connected to V_{CC2} and disables when connected to the ground of the rise-time accelerator current for lightly loaded circuits.

PCA951x devices in hot-swap application

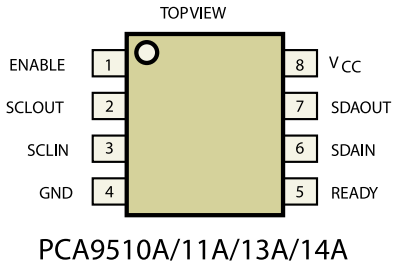


PCA9510A/11A/13A/14A application diagram



R1 and R2 are not required for PCA9513A applications since the internal 92 µA current source maintains the SCLIN and SDAIN lines high.

PCA9510A/11A/13A/14A pinout diagram

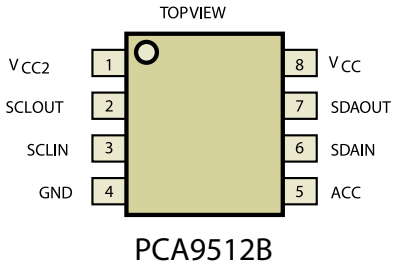


PCA9510A/11A/13A/14A

Pin description

Pin	Symbol	Description
1	ENABLE	Chip enable pin. Grounding this pin puts the part in a low-current (<1 μA) mode. It also disables the rise-time accelerators. Isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT.
2	SCLOUT	Serial clock output to and from the SCL bus on the card.
3	SCLIN	Serial clock input to and from the SCL bus on the backplane.
4	GND	Ground. Connect this pin to a ground plane for best results.
5	READY	This is an open-drain output that pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and turns off when the two sides are connected.
6	SDAIN	Serial data input to and from the SDA bus on the backplane.
7	SDAOUT	Serial data output to and from the SDA bus on the card.
8	V_{CC}	Power supply.

PCA9512AB pinout diagram

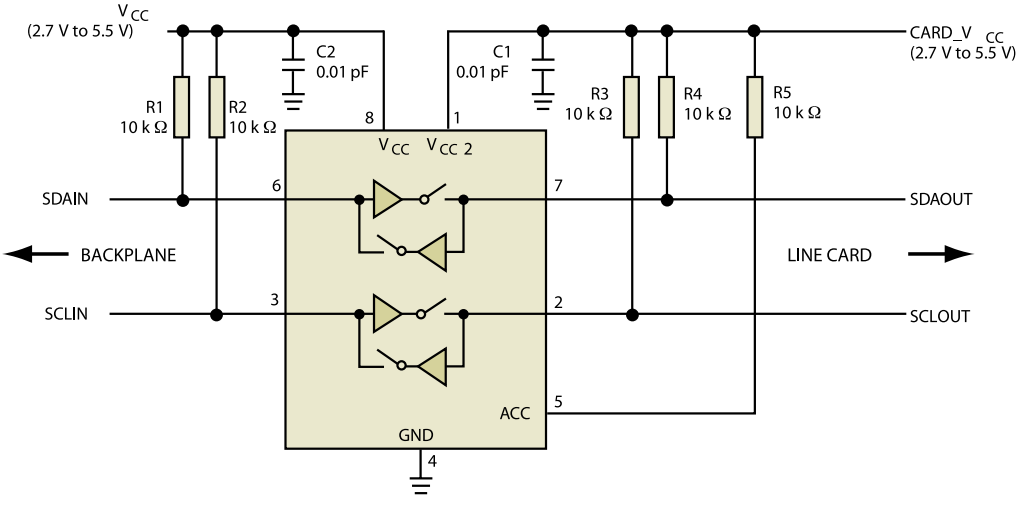


PCA9512B

Pin description

Pin	Symbol	Description
1	V_{CC2}	Supply voltage for devices on each card's I²C-bus. Connect it to the pull-up resistors of SDAUT and SCLOUT.
2	SCLOUT	Serial clock output to and from the SCL bus on the card.
3	SCLIN	Serial clock input to and from the SCL bus on the backplane.
4	GND	Ground. Connect this pin to a ground plane for best results.
5	ACC	CMOS-threshold digital-input pin that enables and disables the rise-time accelerators on all four SDA and SCL pins. ACC enables all accelerators when set to V_{CC2}, and turns them off when set to GND.
6	SDAIN	Serial data input to and from the SDA bus on the backplane/long-distance bus.
7	SDAOUT	Serial data output to and from the SDA bus on the card.
8	V_{CC}	Power supply from the backplane. Connect it to the pull-up resistors from SDAIN and SCLIN.

PCA9512B application diagram



Selection guide

Features	PCA9510A	PCA9511A	PCA9512B	PCA9513A	PCA9514A
Idle detect	Yes	Yes	Yes	Yes	Yes
High-impedance SDA, SCL, pins for V_{CC} = 0 V	Yes	Yes	Yes	Yes	Yes
Rise-time accelerator circuitry on all SDA and SCL lines	-	Yes	Yes	Yes	Yes
Rise-time accelerator circuitry hardware disable pin for lightly loaded systems	-	-	Yes	-	-
Rise-time accelerator threshold 0.8 vs. 0.6 V (improves noise margin)	-	-	Yes	Yes	Yes
Ready open-drain output	Yes	Yes	-	Yes	Yes
Two V_{CC} pins to support level translation from 5.0 to 3.3 V with improved noise margins	-	-	Yes*	-	-
1 V precharge on all SDA and SCL lines	In only	Yes	Yes	-	-
92 µA current source on SCLIN and SDAIN for PICMG applications	-	-	-	Yes	-
5 V overvoltage tolerance	Yes	-	-	-	-

* PCA9512A requires that both supplies be applied simultaneously. The PCA9512B can be supplied either simultaneously or independently, such as in redundant applications.

Ordering information

Package	Container	PCA9510A	PCA9511A	PCA9512B	PCA9513A	PCA9514A
SO	Tube	PCA9510D, 112	PCA9511D, 112	PCA9512BD, 112	PCA9513AD, 112	PCA9514AD, 112
	T & R	PCA9510AD, 118	PCA9511AD, 118	PCA9512BD, 118	PCA9513AD, 118	PCA9514AD, 118
TSSOP	T & R	PC A9510ADP, 118	PC A9511ADP, 118	PC A9512BDP, 118	PC A9513ADP, 118	PC A9514ADP, 118

Additional technical information can be found in Application Note AN10160 (www.standardics.nxp.com/support/documents) and additional information on packages, including outline dimensions, MSL ratings, Theta JA can be found at www.standardics.nxp.com/packaging.

www.nxp.com

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