ADC08131/ADC08134/ADC08138 8-Bit High-Speed Serial I/O A/D Converters with Multiplexer Options, Voltage Reference, and Track/Hold Function

Check for Samples: ADC08131, ADC08134, ADC08138

FEATURES

- **Serial Digital Data Link Requires Few I/O Pins**
- **Analog Input Track/Hold Function**
- **4- or 8-Channel Input Multiplexer Options with Address Logic**
- **On-Chip 2.5V Band-Gap Reference (±2% Over Temperature Ensured)**
- **No Zero or Full Scale Adjustment Required**
- **TTL/CMOS Input/Output Compatible**
- **0V to 5V Analog Input Range with Single 5V Power Supply**

APPLICATIONS

- **Digitizing Automotive Sensors**
- **Process Control/Monitoring**
- **Remote Sensing in Noisy Environments**
- **Embedded Diagnostics**

KEY SPECIFICATIONS

- **Resolution: 8 Bits**
- **Conversion Time (f_C = 1 MHz): 8 µs (Max)**
- **Power Dissipation: 20 mW (Max)**
- **Single Supply: 5 V_{DC} (±5%)**
- **Total Unadjusted Error: ±½ LSB and ±1 LSB**
- **Linearity Error (V_{REF} = 2.5V): ±½ LSB**
- **No Missing Codes (Over Temperature)**
- **On-Board Reference: +2.5V ±1.5% (Max)**

DESCRIPTION

The ADC08131/ADC08134/ADC08138 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the MICROWIRE serial data exchange standard for easy interface to the COPS™ family of controllers, and can easily interface with standard shift registers or microprocessors.

All three devices provide a 2.5V band-gap derived reference with ensured performance over temperature.

A track/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. In addition, input voltage spans as small as 1V can be accommodated.

Connection Diagrams

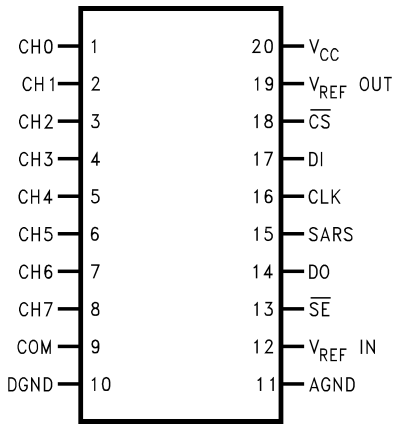


Figure 1. ADC08138CIWM Small Outline Packages

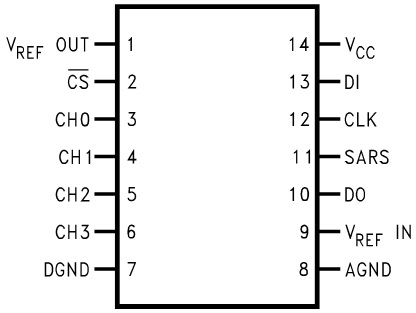


Figure 2. ADC08134CIWM Small Outline Packages

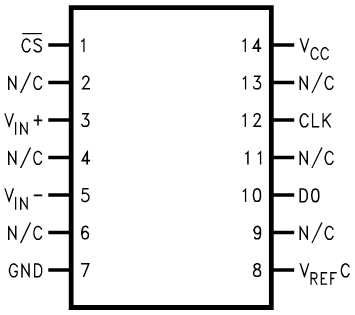


Figure 3. ADC08131CIWM Small Outline Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage (V_{CC})			6.5V
Voltage at Inputs and Outputs			−0.3V to V_{CC} + 0.3V
Input Current at Any Pin(4)			±5 mA
Package Input Current(4)			±20 mA
Power Dissipation at T_A = 25°C(5)			800 mW
ESD Susceptibility(6)			1500V
Soldering Information	N Package (10 sec.)		260°C
	SOIC Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
Storage Temperature			−65°C to +150°C

(1) All voltages are measured with respect to AGND = DGND = 0 V_{DC}, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < (AGND or DGND) or V_{IN} > AV_{CC}) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For these devices T_{JMAX} = 125°C. The typical thermal resistances (θ_{JA}) of these parts when board mounted for the ADC 08131 and the ADC08134 is 140°C/W and 91°C/W for the ADC08138.
(6) Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Operating Ratings(1)(2)

Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_{CC})	4.5 V_{DC} to 6.3 V_{DC}

(1) Operating Ratings indicate conditions for which the device is functional. These ratings do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to AGND = DGND = 0 V_{DC}, unless otherwise specified.

Electrical Characteristics

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +2.5 V_{DC} and f_{CLK} = 1 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical(1)	Limits(2)	Units (Limits)
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
	Linearity Error	V_{REF} = +2.5 V_{DC}		**±1**	LSB (max)
	Full Scale Error	V_{REF} = +2.5 V_{DC}		**±1**	LSB (max)
	Zero Error	V_{REF} = +2.5 V_{DC}		**±1**	LSB (max)
	Total Unadjusted Error	V_{REF} = +5 V_{DC}(3)		**±1**	LSB (max)
	Differential Linearity	V_{REF} = +2.5 V_{DC}		**8**	Bits (min)
R_{REF}	Reference Input Resistance	See(4)	3.5	 **1.3** **6.0**	kΩ kΩ (min) kΩ (max)
V_{IN}	Analog Input Voltage	See(5)		**(V_{CC} + 0.05)** **(GND − 0.05)**	V (max) V (min)
	DC Common-Mode Error	V_{REF} = 2.5 V_{DC}		±½	LSB (max)
	Power Supply Sensitivity	V_{CC} = +5V ±5%, V_{REF} = +2.5 V_{DC}		**±¼**	LSB (max)
	On Channel Leakage Current(6)	On Channel = 5V, Off Channel = 0V		0.2 **1**	µA (max)
		On Channel = 0V, Off Channel = 5V		−0.2 **−1**	µA (max)
	Off Channel Leakage Current(6)	On Channel = 5V, Off Channel = 0V		−0.2 **−1**	µA (max)
		On Channel = 0V, Off Channel = 5V		0.2 **1**	µA (max)
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical “1” Input Voltage	V_{CC} = 5.25V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_{CC} = 4.75V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 5.0V		**1**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V		**−1**	µA (max)
$V_{OUT(1)}$	Logical “1” Output Voltage	V_{CC} = 4.75V: I_{OUT} = −360 µA I_{OUT} = −10 µA		 **2.4** **4.5**	 V (min) V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**	V (max)

(1) Typicals are at T_J = 25°C and represent the most likely parametric norm.
(2) Ensured to AOQL (Average Outgoing Quality Level).
(3) Total unadjusted error includes zero, full-scale, linearity, and multiplexer error. Total unadjusted error with V_{REF} = +5V only applies to the ADC08134 and ADC08138. See Note 7 on the following page.
(4) Cannot be tested for the ADC08131.
(5) For $V_{IN(-)} \geq V_{IN(+)}$ the digital code will be 0000 0000. Two on-chip diodes are tied to each analog input (see ADC08138 Simplified Block Diagram) which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. During testing at low V_{CC} levels (e.g., 4.5V), high level analog inputs (e.g., 5V) can cause an input diode to conduct, especially at elevated temperatures. This will cause errors for analog inputs near full-scale. The specification allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. Achievement of an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.
(6) Channel leakage current is measured after a single-ended channel is selected and the clock is turned off. For off channel leakage current the following two cases are considered: one, with the selected channel tied high (5 V_{DC}) and the remaining seven off channels tied low (0 V_{DC}), total current flow through the off channels is measured; two, with the selected channel tied low and the off channels tied high, total current flow through the off channels is again measured. The two cases considered for determining on channel leakage current are the same except total current flow through the selected channel is measured.

Electrical Characteristics (continued)

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +2.5 V_{DC} and f_{CLK} = 1 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical(1)	Limits(2)	Units (Limits)
I_{OUT}	TRI-STATE Output Current	V_{OUT} = 0V		**−3.0**	µA (max)
		V_{OUT} = 5V		**3.0**	µA (max)
I_{SOURCE}	Output Source Current	V_{OUT} = 0V		**−6.5**	mA (min)
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		**8.0**	mA (min)
I_{CC}	Supply Current				
	ADC08134, ADC08138	$\overline{CS}$ = HIGH		**3.0**	mA (max)
	ADC08131(7)			**6.0**	mA (max)

(7) For the ADC08131 V_{REF}IN is internally tied to the on chip 2.5V band-gap reference output; therefore, the supply current is larger because it includes the reference current (700 µA typical, 2 mA maximum).

Electrical Characteristics

The following specifications apply for V_{CC} = +5 V_{DC}, and f_{CLK} = 1 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical(1)	Limits(2)	Units (Limits)
REFERENCE CHARACTERISTICS					
V_{REF}OUT	Output Voltage	DC08134, ADC08138	**2.5 ±2%**	2.5 ±1.5%	V
$\Delta V_{REF}/\Delta T$	Temperature Coefficient		40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Load Regulation(3)	Sourcing ($0 \le I_L \le +4$ mA) ADC08134, ADC08138	0.003	**0.1**	%/mA (max)
		Sourcing ($0 \le I_L \le +2$ mA) ADC08131	0.003	**0.1**	
		Sinking ($-1 \le I_L \le 0$ mA) ADC08134, ADC08138	0.2	**0.5**	
		Sinking ($-1 \le I_L \le 0$ mA) ADC08131	0.2	**0.5**	
	Line Regulation	$4.75V \le V_{CC} \le 5.25V$	0.5	**6**	mV (max)
I_{SC}	Short Circuit Current	V_{REF} = 0V ADC08134, ADC08138	8	**25**	mA (max)
		V_{REF} = 0V ADC08131	8	**25**	
T_{SU}	Start-Up Time	V_{CC}: 0V → 5V C_L = 100 µF	20		ms
$\Delta V_{REF}/\Delta t$	Long Term Stability		200		ppm/1 kHr

(1) Typicals are at T_J = 25°C and represent the most likely parametric norm.
(2) Ensured to AOQL (Average Outgoing Quality Level).
(3) Load regulation test conditions and specifications for the ADC08131 differ from those of the ADC08134 and ADC08138 because the ADC08131 has the on-board reference as a permanent load.

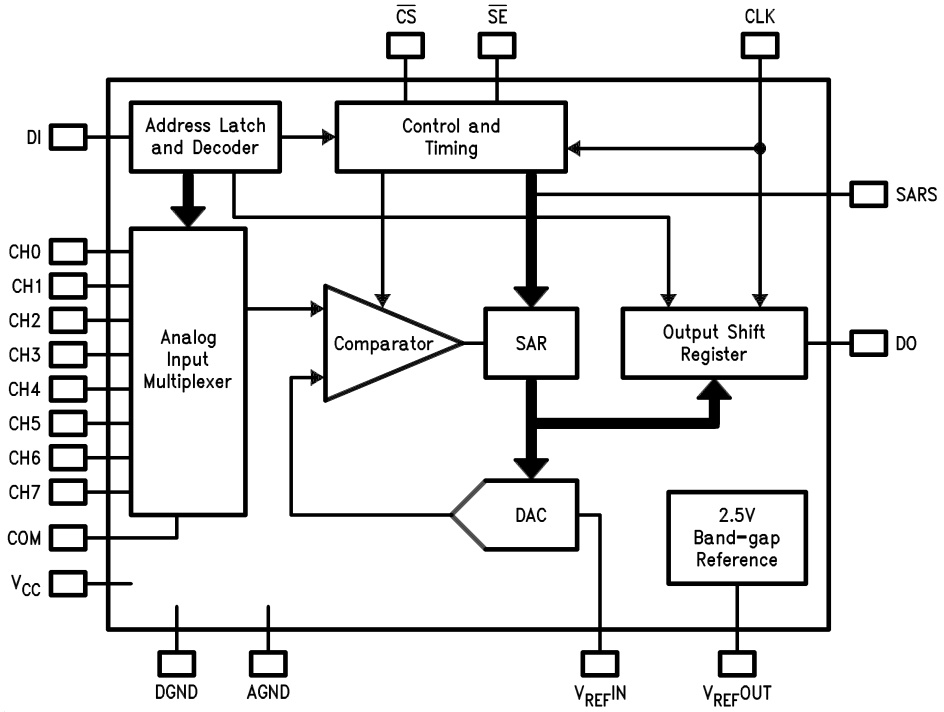
Electrical Characteristics

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +2.5 V_{DC} and $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical[1]	Limits[2]	Units (Limits)
f_{CLK}	Clock Frequency		10		kHz (min)
				1	MHz (max)
	Clock Duty Cycle[3]			**40**	% (min)
				60	% (max)
T_C	Conversion Time (Not Including MUX Addressing Time)	f_{CLK} = 1 MHz		**8**	$1/f_{CLK}$ (max)
				8	µs (max)
t_{CA}	Acquisition Time			**½**	$1/f_{CLK}$ (max)
t_{SELECT}	CLK High while $\overline{CS}$ is High		50		ns
t_{SET-UP}	$\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge			**25**	ns (min)
t_{HOLD}	Data Input Valid after CLK Rising Edge			**20**	ns (min)
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid[4]	C_L = 100 pF:			
		Data MSB First		**250**	ns (max)
		Data LSB First		**200**	ns (max)
t_{1H}, t_{0H}	TRI-STATE Delay from Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	C_L = 10 pF, R_L = 10 kΩ (see TRI-STATE Test Circuits and Waveforms)	50		ns
		C_L = 100 pF, R_L = 2 kΩ		**180**	ns (max)
C_{IN}	Capacitance of Logic Inputs		5		pF
C_{OUT}	Capacitance of Logic Outputs		5		pF

(1) Typicals are at T_J = 25°C and represent the most likely parametric norm.
(2) Ensured to AOQL (Average Outgoing Quality Level).
(3) A 40% to 60% duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits the minimum time the clock is high or low must be at least 450 ns. The maximum time the clock can be high or low is 100 µs.
(4) Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see ADC08138 Simplified Block Diagram) to allow for comparator response time.

ADC08138 Simplified Block Diagram



Typical Converter Performance Characteristics(1)

Linearity Error vs Reference Voltage

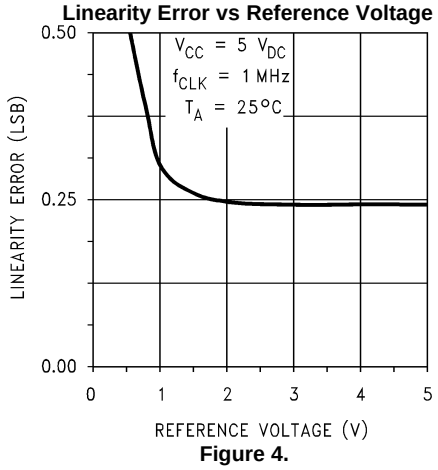


Figure 4.

Linearity Error vs Temperature

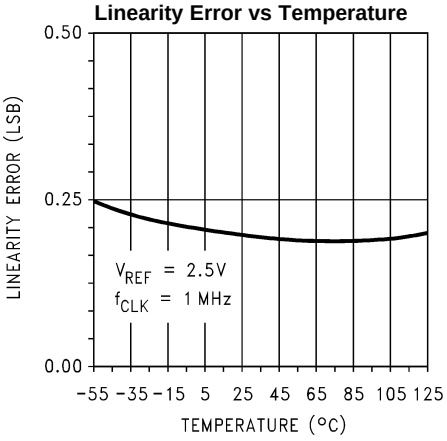


Figure 5.

Linearity Error vs Clock Frequency

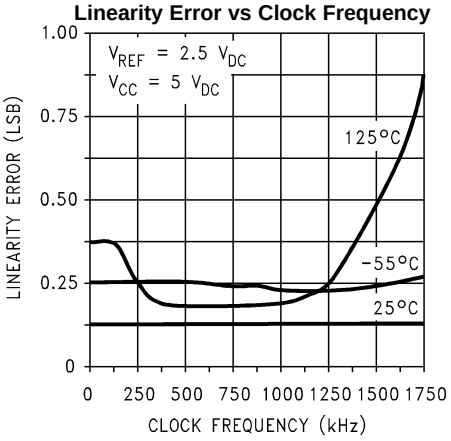


Figure 6.

Power Supply Current vs Temperature (ADC08138, ADC08134)

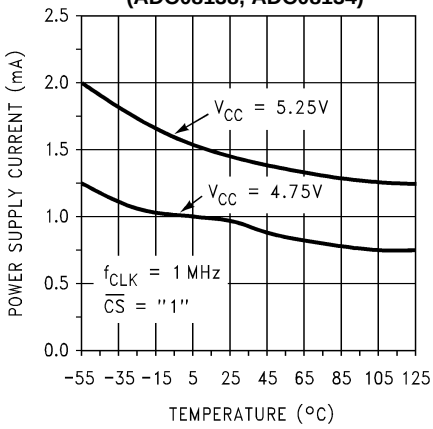


Figure 7.

Output Current vs Temperature

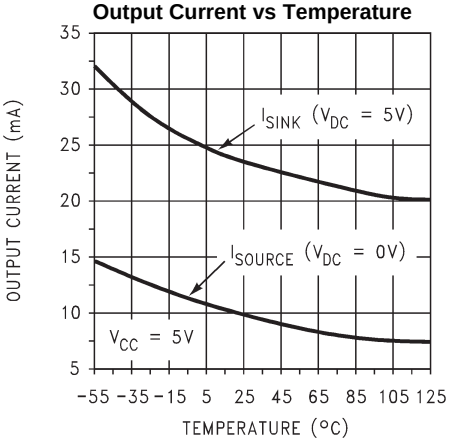


Figure 8.

Power Supply Current vs Clock Frequency

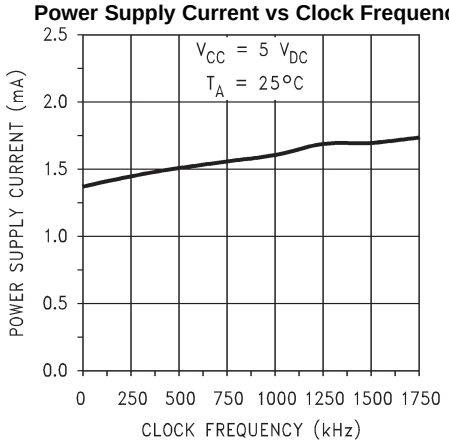


Figure 9. (2)

(1) For ADC08131 add I_{REF}

(2) For the ADC08131 V_{REF}IN is internally tied to the on chip 2.5V band-gap reference output; therefore, the supply current is larger because it includes the reference current (700 µA typical, 2 mA maximum).

Typical Reference Performance Characteristics

Load Regulation (1)

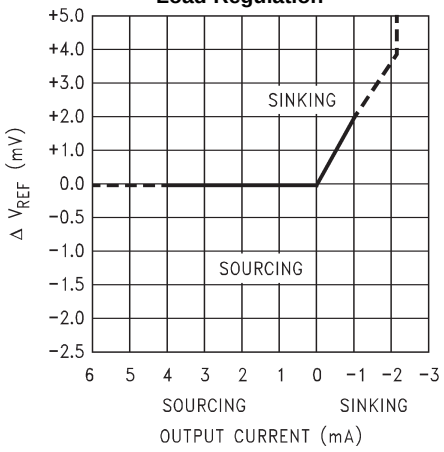


Figure 10.

Line Regulation (3 Typical Parts)

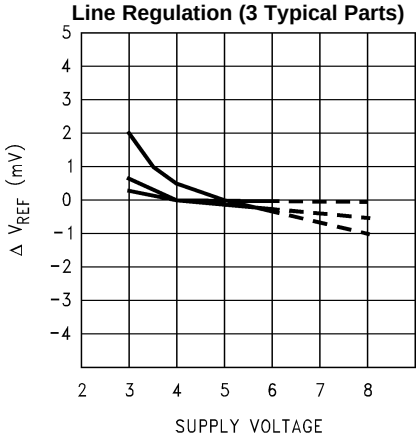


Figure 11.

Output Drift vs Temperature (3 Typical Parts)

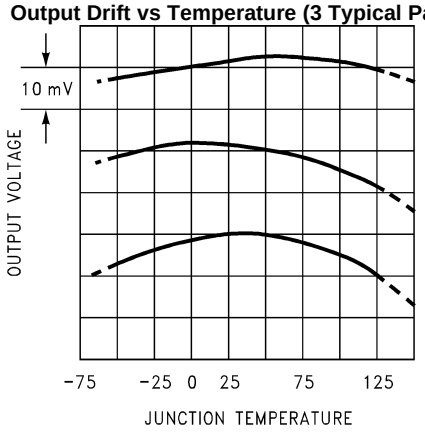


Figure 12.

Available Output Current vs Supply Voltage

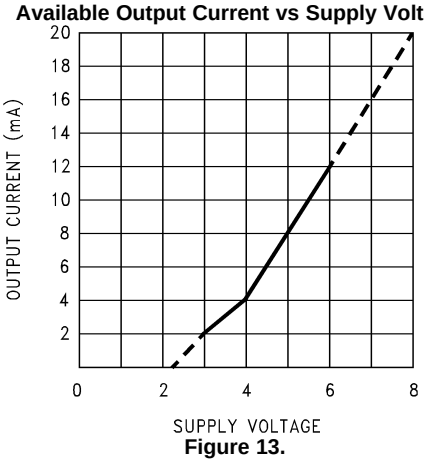


Figure 13.

(1) Load regulation test conditions and specifications for the ADC08131 differ from those of the ADC08134 and ADC08138 because the ADC08131 has the on-board reference as a permanent load.

TRI-STATE Test Circuits and Waveforms

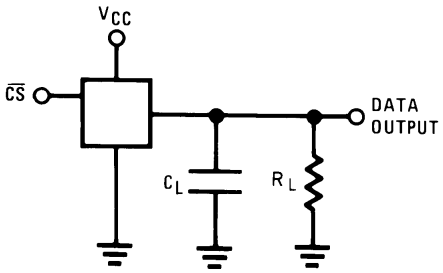


Figure 14. t_{1H}

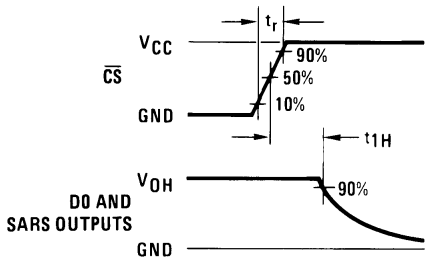


Figure 15. t_{1H}

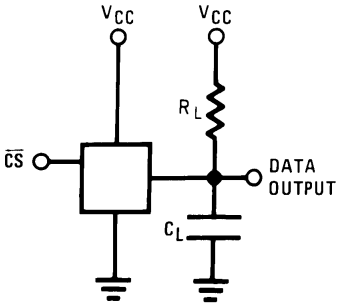


Figure 16. t_{0H}

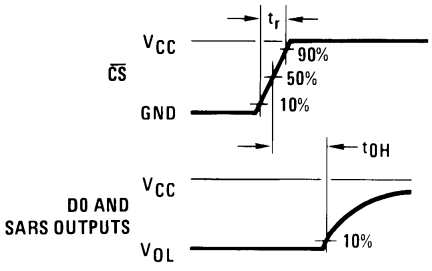
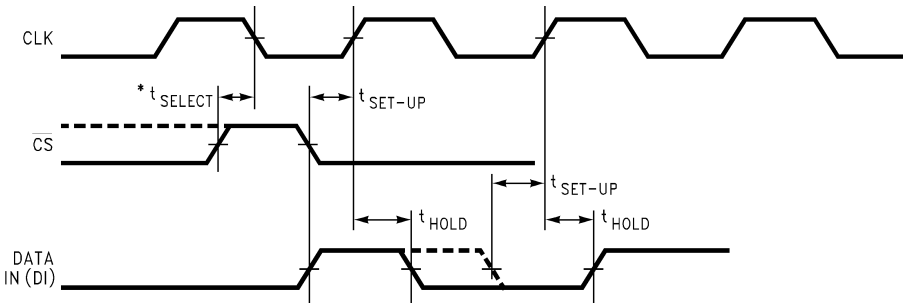


Figure 17. t_{0H}

Timing Diagrams



*To reset these devices, CLK and $\overline{CS}$ must be simultaneously high for a period of t_{SELECT} or greater. Otherwise these devices are compatible with industry standards ADC0831/4/8.

Figure 18. Data Input Timing

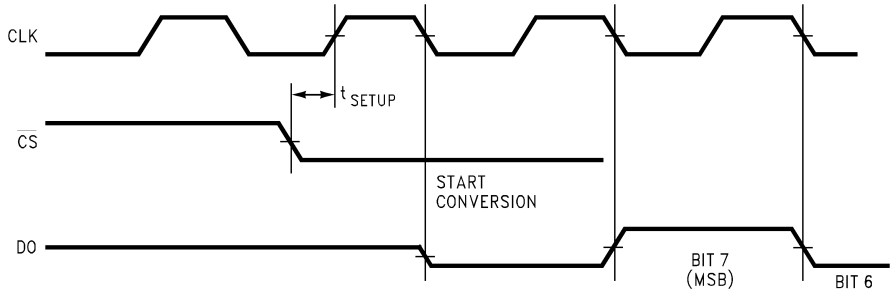


Figure 19. Data Output Timing

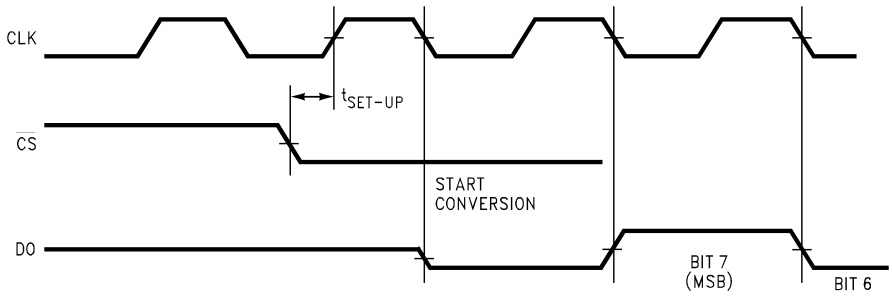
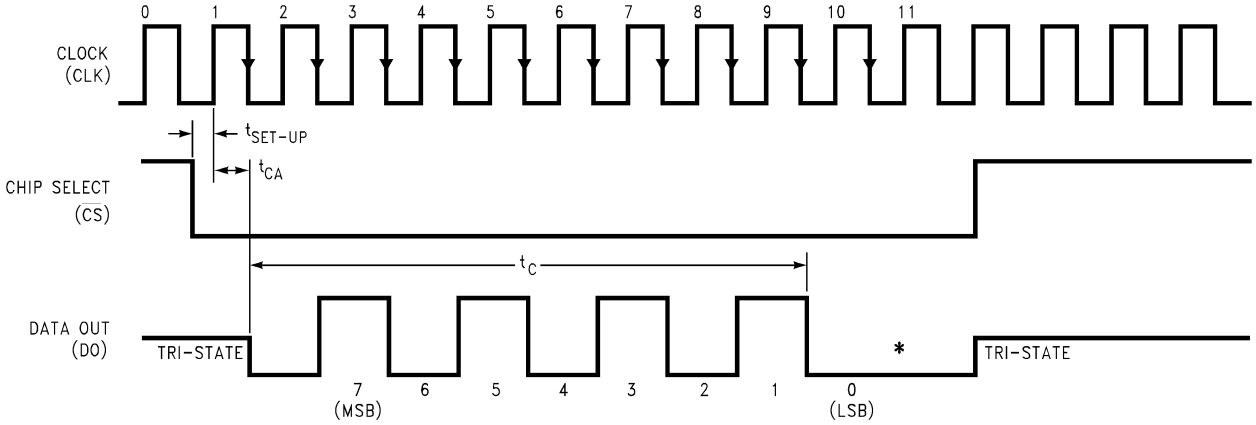


Figure 20. ADC08131 Start Conversion Timing



*LSB first output not available on ADC08131.
LSB information is maintained for remainder of clock periods until $\overline{CS}$ goes high.

Figure 21. ADC08131 Timing

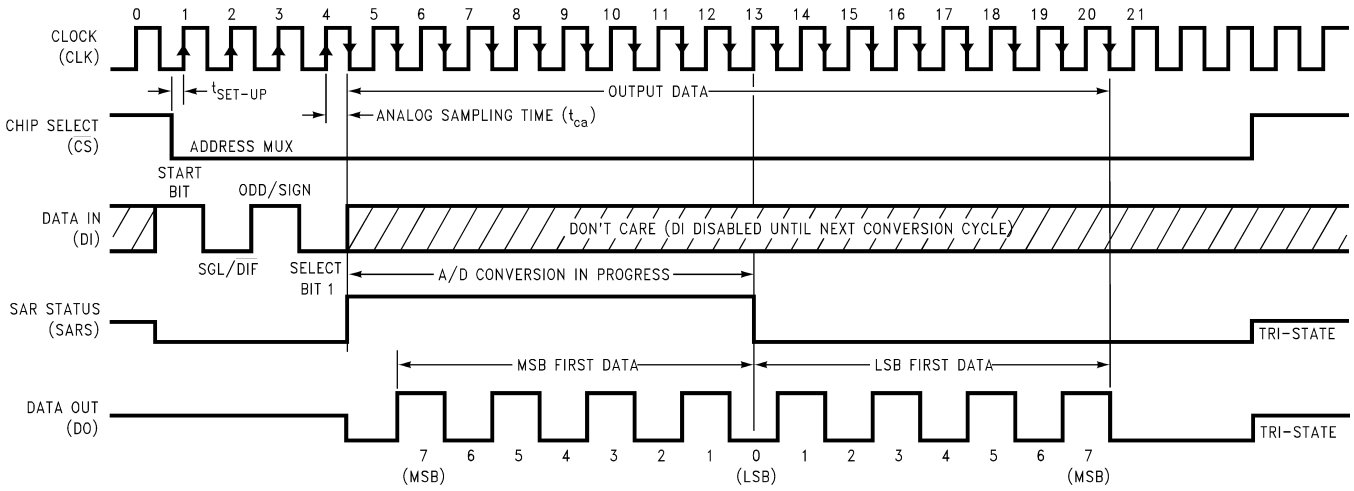
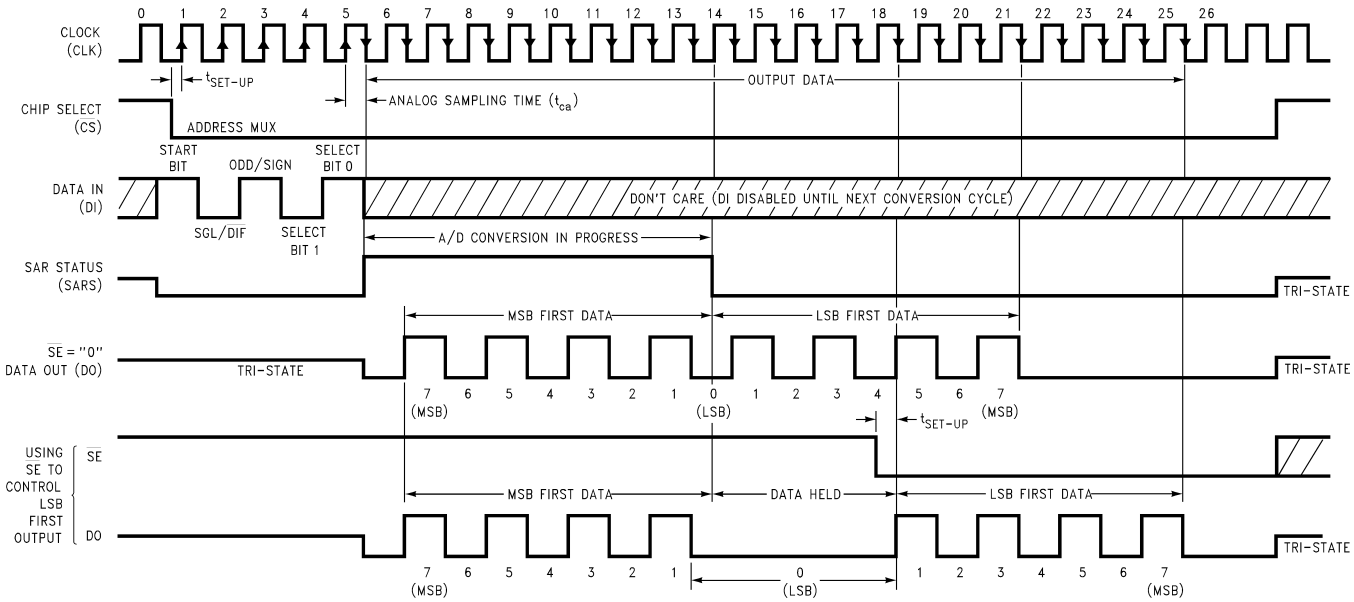


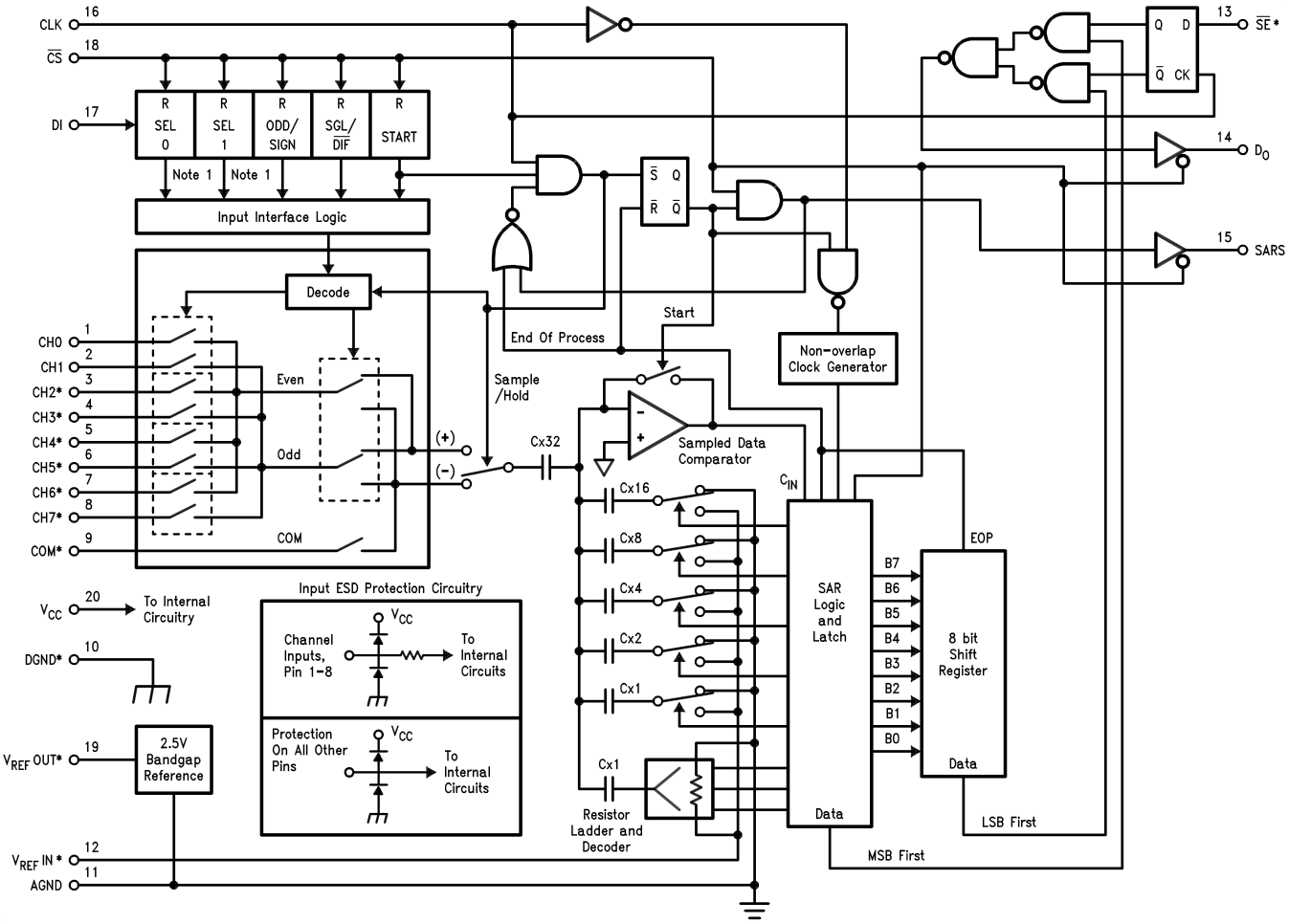
Figure 22. ADC08134 Timing



*Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

Figure 23. ADC08138 Timing

ADC08138 Functional Block Diagram



*Some of these functions/pins are not available with other options.

For the ADC08134, the “SEL 1” Flip-Flop is bypassed. For the ADC08131, V_{REFOUT} and V_{REFIN} are internally tied together.

Functional Description

MULTIPLEXER ADDRESSING

The design of these converters utilizes a comparator structure with built-in sample-and-hold which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair indicates which line the converter expects to be the most positive. If the assigned "+" input voltage is less than the "−" input voltage the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or pseudo-differential (which will convert the difference between the voltage at any analog input and a common terminal) operation. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the polarity may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC08131 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line (COM) on the ADC08138 can be used as a pseudo-differential input. In this mode the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply applications where the analog circuity may be biased up to a potential other than ground and the output signals are all referred to this potential.

Table 1. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC08131	1	1	8
ADC08134	4	2	14
ADC08138	8	4	20

Table 2. MUX Addressing: ADC08138

Single-Ended MUX Mode													
MUX Address					Analog Single-Ended Channel #								
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT		0	1	2	3	4	5	6	7	COM
			1	0									
1	1	0	0	0	+								−
1	1	0	0	1			+						−
1	1	0	1	0					+				−
1	1	0	1	1							+		−
1	1	1	0	0		+							−
1	1	1	0	1				+					−
1	1	1	1	0						+			−
1	1	1	1	1								+	−

Table 3. MUX Addressing: ADC08138

Differential MUX Mode												
MUX Address					Analog Differential Channel-Pair #							
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT		0		1		2		3	
			1	0	0	1	2	3	4	5	6	7
1	0	0	0	0	+	−						
1	0	0	0	1			+	−				
1	0	0	1	0					+	−		
1	0	0	1	1							+	−
1	0	1	0	0	−	+						
1	0	1	0	1			−	+				
1	0	1	1	0					−	+		
1	0	1	1	1							−	+

Table 4. MUX Addressing: ADC08134(1)

Single-Ended MUX Mode							
MUX Address				Channel #			
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT 1	0	1	2	3
1	1	0	0	+			
1	1	0	1			+	
1	1	1	0		+		
1	1	1	1				+

(1) COM is internally tied to AGND

Differential MUX Mode							
MUX Address				Channel #			
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT 1	0	1	2	3
1	0	0	0	+	−		
1	0	0	1			+	−
1	0	1	0	−	+		
1	0	1	1			−	+

Since the input configuration is under software control, it can be modified as required before each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. Figure 24 illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows many functions to be included in a small package and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and ADC08138 Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate timing diagram is shown for each device.

1. A conversion is initiated by pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.
2. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic “1” that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.
3. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period is automatically inserted to allow for sampling the analog input. The SARS line goes high at the end of this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).
4. The data out (DO) line now comes out of TRI-STATE and provides a leading zero.
5. During the conversion the output of the SAR comparator indicates whether the analog input is greater than (high) or less than (low) a series of successive voltages generated internally from a ratioed capacitor array (first 5 bits) and a resistor ladder (last 3 bits). After each comparison the comparator's output is shipped to the DO line on the falling edge of CLK. This data is the result of the conversion being shifted out (with the MSB first) and can be read by the processor immediately.
6. After 8 clock periods the conversion is completed. The SARS line returns low to indicate this ½ clock cycle later.
7. The stored data in the successive approximation register is loaded into an internal shift register. If the programmer prefers the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. On the ADC08138 the $\overline{SE}$ line is brought out and if held high the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low the data is clocked out LSB first. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. The ADC08131 is an exception in that its data is only output in MSB first format.
8. All internal registers are cleared when the $\overline{CS}$ line is high and the t_{SELECT} requirement is met. See Figure 18. If another conversion is desired $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only “looked-at” during the MUX addressing interval while the DO line is still in a high impedance state.

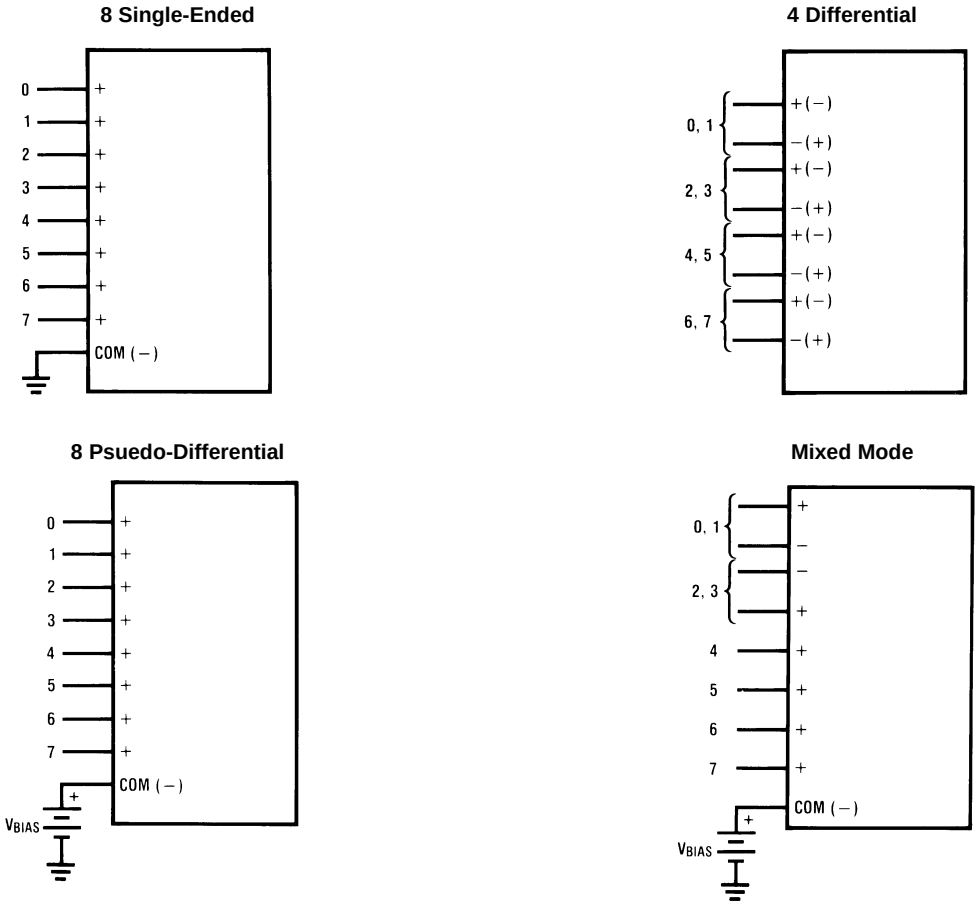


Figure 24. Analog Input Multiplexer Options for the ADC08138

REFERENCE CONSIDERATIONS

The V_{REF}IN pin on these converters is the top of a resistor divider string and capacitor array used for the successive approximation conversion. The voltage applied to this reference input defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$ over which the 256 possible output codes apply). The reference source must be capable of driving the reference input resistance, which can be as low as 1.3 kΩ.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference input must be biased with a stable voltage source. The ADC08134 and the ADC08138 provide the output of a 2.5V band-gap reference at V_{REF}OUT. This voltage does not vary appreciably with temperature, supply voltage, or load current (see Reference Timing under Electrical Characteristics) and can be tied directly to V_{REF}IN for an analog input span of 0V to 2.5V. This output can also be used to bias external circuits and can therefore be used as the reference in ratiometric applications. Bypassing V_{REF}OUT with a 100 µF capacitor is recommended.

For the ADC08131, the output of the on-board reference is internally tied to the reference input. Consequently, the analog input span for this device is set at 0V to 2.5V. The pin V_{REF}C is provided for bypassing purposes and biasing external circuits as suggested above.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Converter Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals V_{REF}/256).

Reference Examples

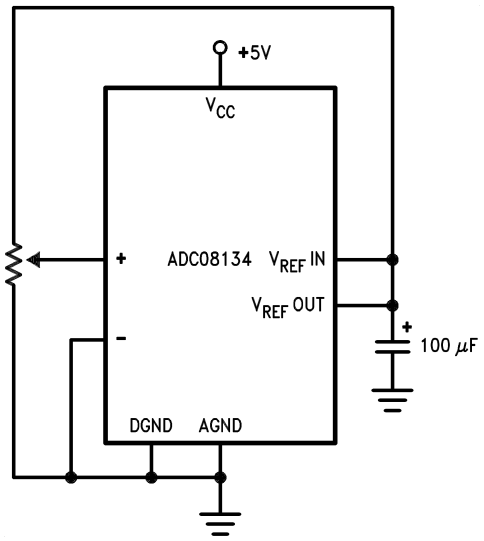


Figure 25. Ratiometric

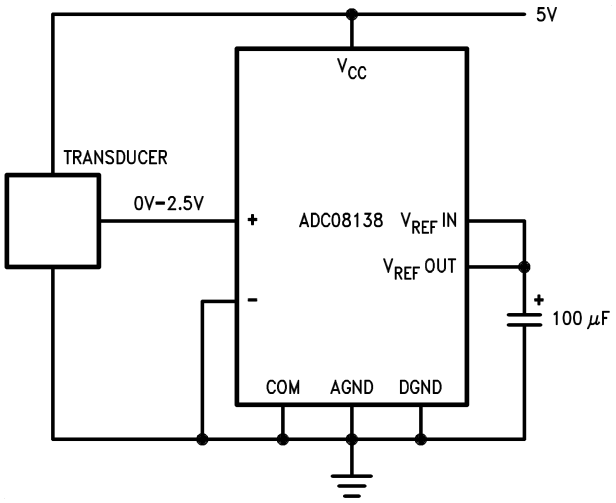


Figure 26. Absolute

THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM}) \left(\frac{0.5}{f_{CLK}}\right) \quad (1)$$

where

- f_{CM} is the frequency of the common-mode signal
- V_{PEAK} is its peak voltage value
- f_{CLK} is the A/D clock frequency

For a 60Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Source resistance limitation is important with regard to the DC leakage currents of the input multiplexer. While operating near or at maximum speed bypass capacitors should not be used if the source resistance is greater than 1kΩ. The worst-case leakage current of ±1µA over temperature will create a 1mV input error with a 1kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

OPTIONAL ADJUSTMENTS

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for V_{REF} = 5.000V_{DC}).

Full Scale

A full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF}IN input for a digital output code which is just changing from 1111 1110 to 1111 1111 (See Figure 31). This is possible only with the ADC08134 and ADC08138. (The reference is internally connected to V_{REF}IN of the ADC08131).

Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN} (−) voltage applied] by forcing a voltage to the V_{IN} (+) input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right] \quad (2)$$

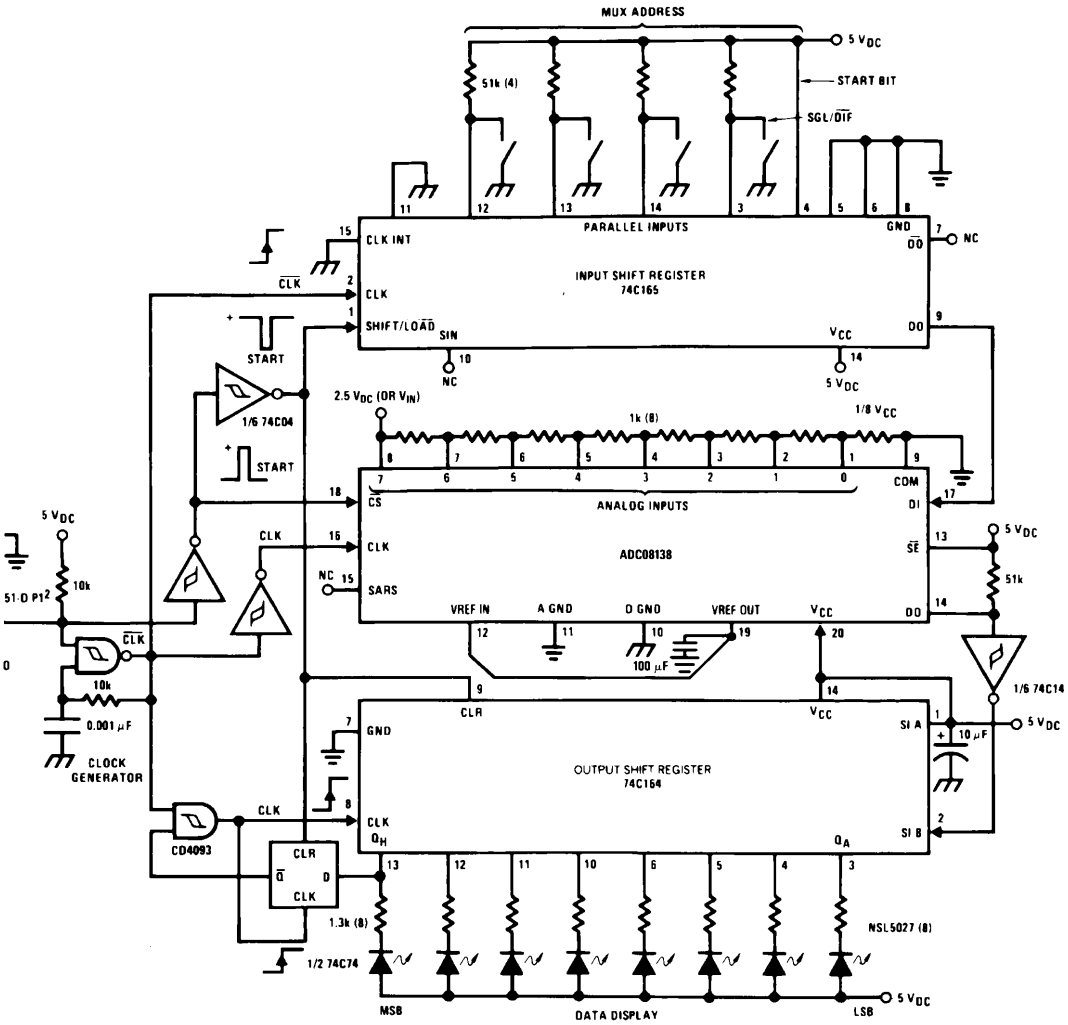
where

- V_{MAX} = the high end of the analog input range
- V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The V_{REF}IN (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

APPLICATIONS



*Pinouts shown for ADC08138.
For all other products tie to pin functions as shown.

Figure 27. A "Stand-Alone" Hook-Up for ADC08138 Evaluation

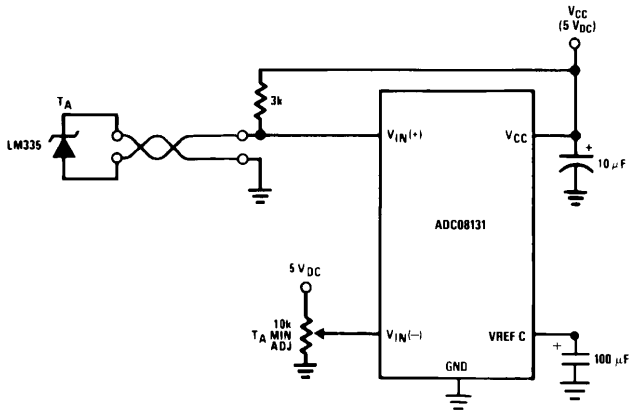
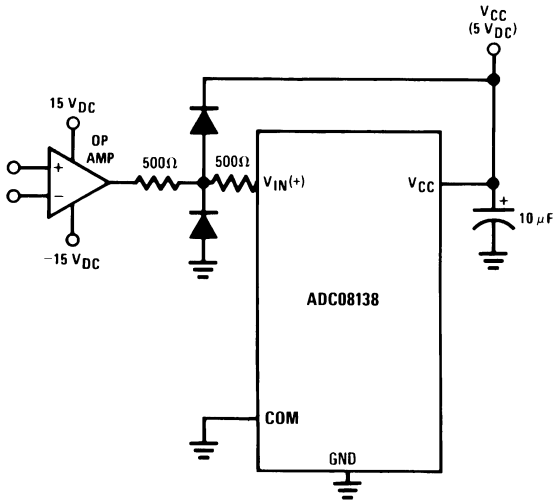
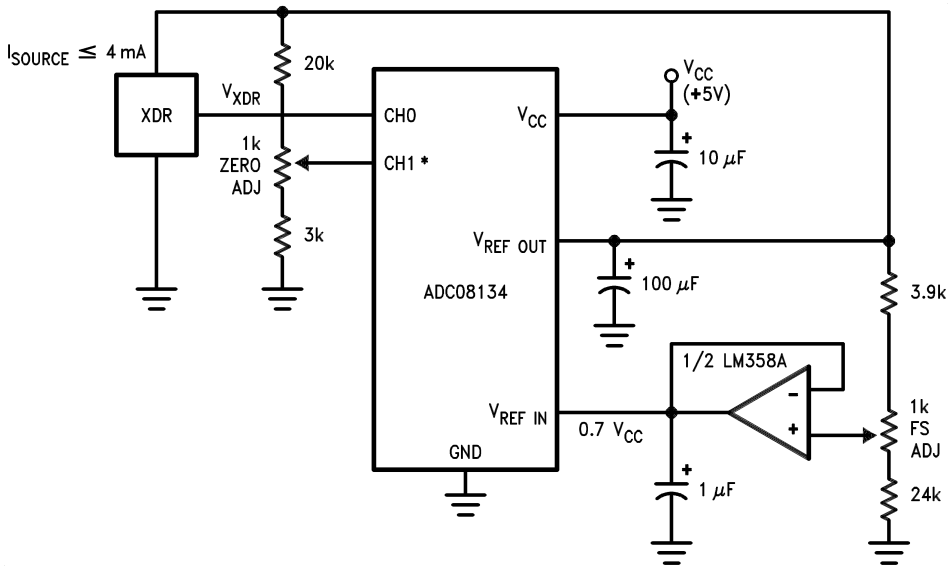


Figure 28. Low-Cost Remote Temperature Sensor



Diodes are 1N914

Figure 29. Protecting the Input



*$V_{IN}(-) = 0.15\ V_{REF}$
15% of $V_{REF} \leq V_{XDR} \leq 85\%$ of V_{REF}

Figure 30. Operating with Ratiometric Transducers

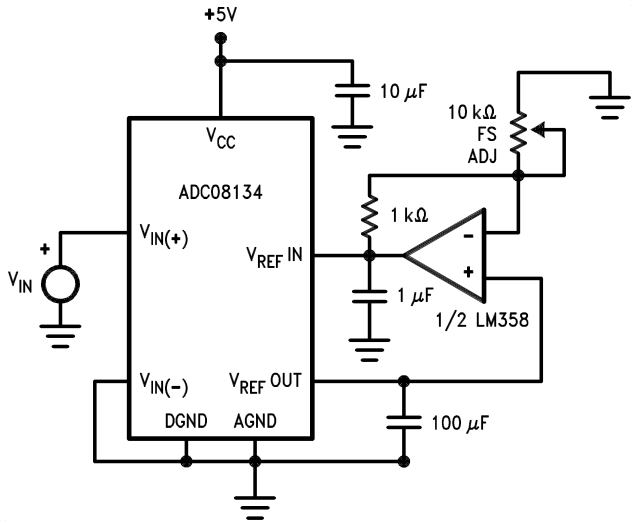


Figure 31. Span Adjust; 0V ≤ V_{IN} ≤ 3V

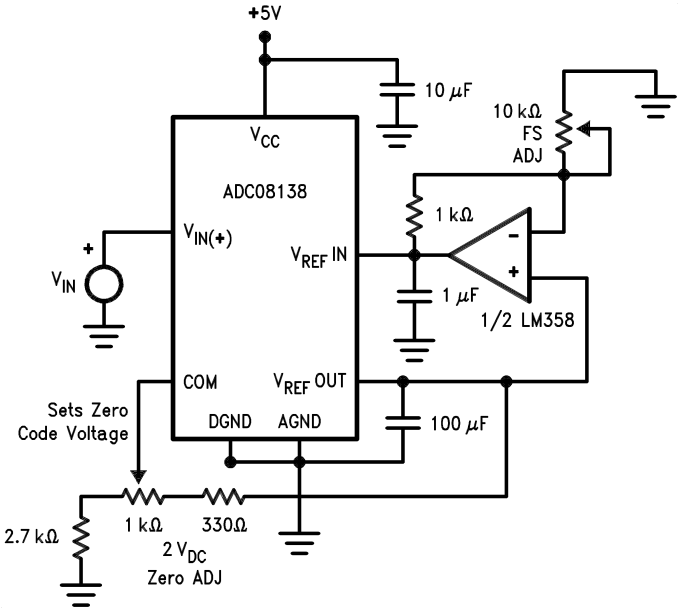


Figure 32. Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	19

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