

# SN74LVC2G53 Single-Pole Double-Throw (SPDT) Analog Switch 2:1 Analog Multiplexer/Demultiplexer

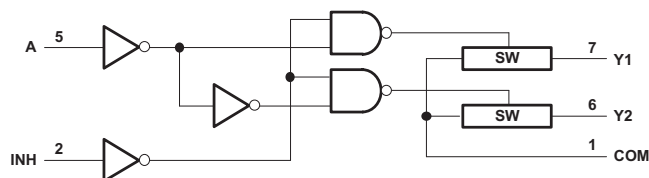
## 1 Features

- Available in the Texas Instruments NanoFree™ Package
- 1.65-V to 5.5-V  $V_{CC}$  Operation
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5 ns ( $V_{CC} = 3$  V,  $C_L = 50$  pF)
- Low ON-State Resistance, Typically 6.5  $\Omega$  ( $V_{CC} = 4.5$  V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## 2 Applications

- Wireless Devices
- Audio and Video Signal Routing
- Portable Computing
- Wearable Devices
- Signal Gating, Chopping, Modulation or Demodulation (Modem)
- Signal Multiplexing for Analog-to-Digital and Digital-to-Analog Conversion Systems

### Logic Diagram



NOTE: For simplicity, the test conditions shown in [Figure 1](#) through [Figure 4](#) and [Figure 6](#) through [Figure 10](#) are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

## 3 Description

This single 2:1 analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G53 device can handle both analog and digital signals. This device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

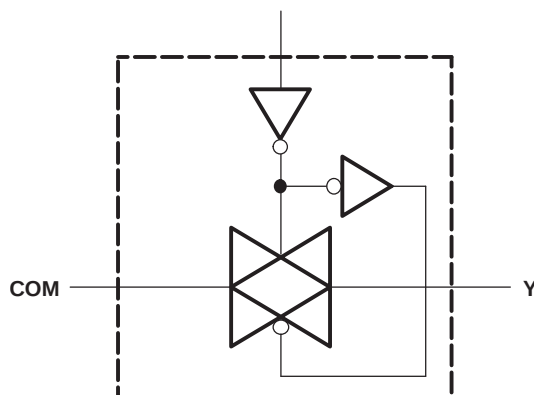
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

### Device Information<sup>(1)</sup>

| PART NUMBER    | PACKAGE   | BODY SIZE (NOM)   |
|----------------|-----------|-------------------|
| SN74LVC2G53DCT | SM8 (8)   | 2.95 mm × 2.80 mm |
| SN74LVC2G53DCU | VSSOP (8) | 2.30 mm × 2.00 mm |
| SN74LVC2G53YZP | DSBGA (8) | 1.91 mm × 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Logic Diagram, Each Switch (SW)



## Table of Contents

|                                                  |           |                                                                  |           |
|--------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                          | <b>1</b>  | 8.2 Functional Block Diagram .....                               | <b>15</b> |
| <b>2 Applications</b> .....                      | <b>1</b>  | 8.3 Feature Description .....                                    | <b>15</b> |
| <b>3 Description</b> .....                       | <b>1</b>  | 8.4 Device Functional Modes .....                                | <b>15</b> |
| <b>4 Revision History</b> .....                  | <b>2</b>  | <b>9 Application and Implementation</b> .....                    | <b>16</b> |
| <b>5 Pin Configuration and Functions</b> .....   | <b>3</b>  | 9.1 Application Information .....                                | <b>16</b> |
| <b>6 Specifications</b> .....                    | <b>4</b>  | 9.2 Typical Application .....                                    | <b>16</b> |
| 6.1 Absolute Maximum Ratings .....               | <b>4</b>  | <b>10 Power Supply Recommendations</b> .....                     | <b>17</b> |
| 6.2 ESD Ratings .....                            | <b>4</b>  | <b>11 Layout</b> .....                                           | <b>18</b> |
| 6.3 Recommended Operating Conditions .....       | <b>4</b>  | 11.1 Layout Guidelines .....                                     | <b>18</b> |
| 6.4 Thermal Information .....                    | <b>5</b>  | 11.2 Layout Example .....                                        | <b>18</b> |
| 6.5 Electrical Characteristics .....             | <b>5</b>  | <b>12 Device and Documentation Support</b> .....                 | <b>19</b> |
| 6.6 Switching Characteristics .....              | <b>6</b>  | 12.1 Documentation Support .....                                 | <b>19</b> |
| 6.7 Analog Switch Characteristics .....          | <b>6</b>  | 12.2 Receiving Notification of Documentation Updates .....       | <b>19</b> |
| 6.8 Operating Characteristics .....              | <b>7</b>  | 12.3 Community Resources .....                                   | <b>19</b> |
| 6.9 Typical Characteristics .....                | <b>8</b>  | 12.4 Trademarks .....                                            | <b>19</b> |
| <b>7 Parameter Measurement Information</b> ..... | <b>9</b>  | 12.5 Electrostatic Discharge Caution .....                       | <b>19</b> |
| <b>8 Detailed Description</b> .....              | <b>15</b> | 12.6 Glossary .....                                              | <b>19</b> |
| 8.1 Overview .....                               | <b>15</b> | <b>13 Mechanical, Packaging, and Orderable Information</b> ..... | <b>19</b> |

## 4 Revision History

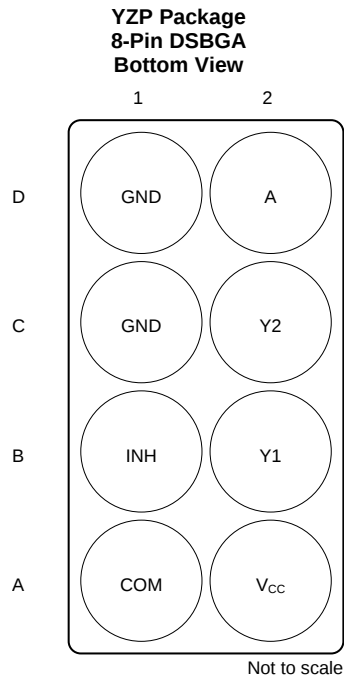
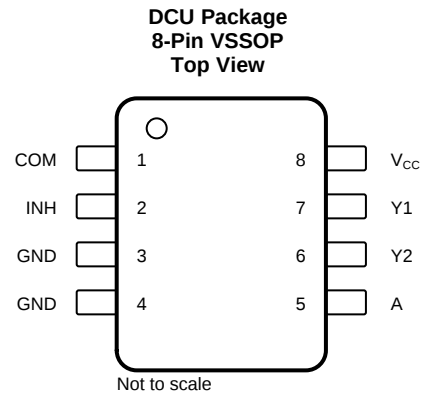
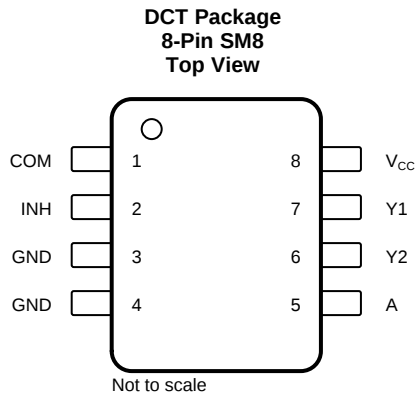
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision P (October 2016) to Revision Q | Page     |
|------------------------------------------------------|----------|
| • Changed the <i>Thermal Information</i> table ..... | <b>5</b> |

| Changes from Revision O (December 2015) to Revision P                        | Page      |
|------------------------------------------------------------------------------|-----------|
| • Added DSBGA package in <i>Pin Functions</i> table .....                    | <b>3</b>  |
| • Added <i>Receiving Notification of Documentation Updates</i> section ..... | <b>19</b> |

| Changes from Revision N (January 2014) to Revision O                                                                                                                                                                                                                                                                                                                                                                                                 | Page     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| • Added <i>Applications</i> section, <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. .... | <b>1</b> |
| • Moved T <sub>stg</sub> to <i>Absolute Maximum Ratings</i> table .....                                                                                                                                                                                                                                                                                                                                                                              | <b>4</b> |

## 5 Pin Configuration and Functions



See [Mechanical, Packaging, and Orderable Information](#) for dimensions.

### Pin Functions

| PIN             |            |       | I/O | DESCRIPTION                         |
|-----------------|------------|-------|-----|-------------------------------------|
| NAME            | SM8, VSSOP | DSBGA |     |                                     |
| A               | 5          | D2    | I   | Controls the switch                 |
| COM             | 1          | A1    | I/O | Bidirectional signal to be switched |
| GND             | 3          | C1    | —   | Ground pin                          |
| GND             | 4          | D1    | —   | Ground pin                          |
| INH             | 2          | B1    | I   | Enables or disables the switch      |
| V <sub>CC</sub> | 8          | A2    | —   | Power pin                           |
| Y2              | 6          | C2    | I/O | Bidirectional signal to be switched |
| Y1              | 7          | B2    | I/O | Bidirectional signal to be switched |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                   | MIN                                                        | MAX                   | UNIT |
|------------------|---------------------------------------------------|------------------------------------------------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage <sup>(2)</sup>                     | −0.5                                                       | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage <sup>(2)(3)</sup>                   | −0.5                                                       | 6.5                   | V    |
| V <sub>I/O</sub> | Switch I/O voltage <sup>(2)(3)(4)</sup>           | −0.5                                                       | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Control input clamp current                       | V <sub>I</sub> < 0                                         | −50                   | mA   |
| I <sub>I/O</sub> | I/O port diode current                            | V <sub>I/O</sub> < 0 or V <sub>I/O</sub> > V <sub>CC</sub> | ±50                   | mA   |
| I <sub>T</sub>   | ON-state switch current                           | V <sub>I/O</sub> = 0 to V <sub>CC</sub>                    | ±50                   | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |                                                            | ±100                  | mA   |
| T <sub>J</sub>   | Junction temperature                              |                                                            | 150                   | °C   |
| T <sub>stg</sub> | Storage temperature                               | −65                                                        | 150                   | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) This value is limited to 5.5 V maximum.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

See note<sup>(1)</sup>.

|                  |                                         | MIN                                | MAX                    | UNIT |
|------------------|-----------------------------------------|------------------------------------|------------------------|------|
| V <sub>CC</sub>  | Supply voltage                          | 1.65                               | 5.5                    | V    |
| V <sub>I/O</sub> | I/O port voltage                        | 0                                  | V <sub>CC</sub>        | V    |
| V <sub>IH</sub>  | High-level input voltage, control input | V <sub>CC</sub> = 1.65 V to 1.95 V | V <sub>CC</sub> × 0.65 | V    |
|                  |                                         | V <sub>CC</sub> = 2.3 V to 2.7 V   | V <sub>CC</sub> × 0.7  |      |
|                  |                                         | V <sub>CC</sub> = 3 V to 3.6 V     | V <sub>CC</sub> × 0.7  |      |
|                  |                                         | V <sub>CC</sub> = 4.5 V to 5.5 V   | V <sub>CC</sub> × 0.7  |      |
| V <sub>IL</sub>  | Low-level input voltage, control input  | V <sub>CC</sub> = 1.65 V to 1.95 V | V <sub>CC</sub> × 0.35 | V    |
|                  |                                         | V <sub>CC</sub> = 2.3 V to 2.7 V   | V <sub>CC</sub> × 0.3  |      |
|                  |                                         | V <sub>CC</sub> = 3 V to 3.6 V     | V <sub>CC</sub> × 0.3  |      |
|                  |                                         | V <sub>CC</sub> = 4.5 V to 5.5 V   | V <sub>CC</sub> × 0.3  |      |
| V <sub>I</sub>   | Control input voltage                   | 0                                  | 5.5                    | V    |
| Δt/Δv            | Input transition rise and fall time     | V <sub>CC</sub> = 1.65 V to 1.95 V | 20                     | ns/V |
|                  |                                         | V <sub>CC</sub> = 2.3 V to 2.7 V   | 20                     |      |
|                  |                                         | V <sub>CC</sub> = 3 V to 3.6 V     | 10                     |      |
|                  |                                         | V <sub>CC</sub> = 4.5 V to 5.5 V   | 10                     |      |
| T <sub>A</sub>   | Operating free-air temperature          | −40                                | 85                     | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                                       | SN74LVC2G53 |             |             | UNIT |
|-------------------------------|-------------------------------------------------------|-------------|-------------|-------------|------|
|                               |                                                       | DCT (SM8)   | DCU (VSSOP) | YZP (DSBGA) |      |
|                               |                                                       | 8 PINS      | 8 PINS      | 8 PINS      |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance <sup>(2)</sup> | 185.9       | 288.9       | 98.3        | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance             | 116.3       | 99.6        | 1.1         | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance                  | 98.4        | 207.3       | 27.6        | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter            | 41.6        | 22.4        | 0.6         | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter          | 97.3        | 205.7       | 27.4        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       |                                                    | TEST CONDITIONS                                                                                                             |               | V <sub>CC</sub> | MIN | TYP <sup>(1)</sup> | MAX             | UNIT     |
|-----------------|----------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|---------------|-----------------|-----|--------------------|-----------------|----------|
| $r_{on}$        | ON-state switch resistance                         | $V_I = V_{CC}$ or GND,<br>$V_{INH} = V_{IL}$<br>(see <a href="#">Figure 2</a><br>and <a href="#">Figure 1</a> )             | $I_S = 4$ mA  | 1.65 V          |     | 13                 | 30              | $\Omega$ |
|                 |                                                    |                                                                                                                             | $I_S = 8$ mA  | 2.3 V           |     | 10                 | 20              |          |
|                 |                                                    |                                                                                                                             | $I_S = 24$ mA | 3 V             |     | 8.5                | 17              |          |
|                 |                                                    |                                                                                                                             | $I_S = 32$ mA | 4.5 V           |     | 6.5                | 13              |          |
| $r_{on(p)}$     | Peak ON-state resistance                           | $V_I = V_{CC}$ to GND,<br>$V_{INH} = V_{IL}$<br>(see <a href="#">Figure 2</a><br>and <a href="#">Figure 1</a> )             | $I_S = 4$ mA  | 1.65 V          |     | 86.5               | 120             | $\Omega$ |
|                 |                                                    |                                                                                                                             | $I_S = 8$ mA  | 2.3 V           |     | 23                 | 30              |          |
|                 |                                                    |                                                                                                                             | $I_S = 24$ mA | 3 V             |     | 13                 | 20              |          |
|                 |                                                    |                                                                                                                             | $I_S = 32$ mA | 4.5 V           |     | 8                  | 15              |          |
| $\Delta r_{on}$ | Difference of ON-state resistance between switches | $V_I = V_{CC}$ to GND,<br>$V_C = V_{IH}$<br>(see <a href="#">Figure 2</a><br>and <a href="#">Figure 1</a> )                 | $I_S = 4$ mA  | 1.65 V          |     |                    | 7               | $\Omega$ |
|                 |                                                    |                                                                                                                             | $I_S = 8$ mA  | 2.3 V           |     |                    | 5               |          |
|                 |                                                    |                                                                                                                             | $I_S = 24$ mA | 3 V             |     |                    | 3               |          |
|                 |                                                    |                                                                                                                             | $I_S = 32$ mA | 4.5 V           |     |                    | 2               |          |
| $I_{S(off)}$    | OFF-state switch leakage current                   | $V_I = V_{CC}$ and $V_O =$ GND or<br>$V_I =$ GND and $V_O = V_{CC}$ ,<br>$V_{INH} = V_{IH}$ (see <a href="#">Figure 3</a> ) |               | 5.5 V           |     | $\pm 1$            | $\pm 0.1^{(1)}$ | $\mu A$  |
| $I_{S(on)}$     | ON-state switch leakage current                    | $V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ ,<br>$V_O =$ Open (see <a href="#">Figure 4</a> )                                 |               | 5.5 V           |     | $\pm 1$            | $\pm 0.1^{(1)}$ | $\mu A$  |
| $I_I$           | Control input current                              | $V_C = V_{CC}$ or GND                                                                                                       |               | 5.5 V           |     | $\pm 1$            | $\pm 0.1^{(1)}$ | $\mu A$  |
| $I_{CC}$        | Supply current                                     | $V_C = V_{CC}$ or GND                                                                                                       |               | 5.5 V           |     |                    | 1               | $\mu A$  |
| $\Delta I_{CC}$ | Supply-current change                              | $V_C = V_{CC} - 0.6$ V                                                                                                      |               | 5.5 V           |     |                    | 500             | $\mu A$  |
| $C_{ic}$        | Control input capacitance                          |                                                                                                                             |               | 5 V             |     | 3.5                |                 | pF       |
| $C_{io(off)}$   | Switch input/output capacitance                    | Y                                                                                                                           |               | 5 V             |     | 6.5                |                 | pF       |
|                 |                                                    | COM                                                                                                                         |               |                 |     | 10                 |                 |          |
| $C_{io(on)}$    | Switch input/output capacitance                    |                                                                                                                             |               | 5 V             |     | 19.5               |                 | pF       |

(1)  $T_A = 25^\circ C$

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

| PARAMETER       | FROM (INPUT) | TO (OUTPUT) | V <sub>CC</sub>                           | MIN | MAX  | UNIT |
|-----------------|--------------|-------------|-------------------------------------------|-----|------|------|
| $t_{pd}^{(1)}$  | COM or Y     | Y or COM    | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | 2    | ns   |
|                 |              |             | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  |     | 1.2  |      |
|                 |              |             | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  |     | 0.8  |      |
|                 |              |             | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$    |     | 0.6  |      |
| $t_{en}^{(2)}$  | INH          | COM or Y    | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | 3.3 | 9    | ns   |
|                 |              |             | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  | 2.5 | 6.1  |      |
|                 |              |             | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  | 2.2 | 5.4  |      |
|                 |              |             | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$    | 1.8 | 4.5  |      |
| $t_{dis}^{(3)}$ | INH          | COM or Y    | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | 3.2 | 10.9 | ns   |
|                 |              |             | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  | 2.3 | 8.3  |      |
|                 |              |             | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  | 2.3 | 8.1  |      |
|                 |              |             | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$    | 1.6 | 8    |      |
| $t_{en}^{(2)}$  | A            | COM or Y    | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | 2.9 | 10.3 | ns   |
|                 |              |             | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  | 2.1 | 7.2  |      |
|                 |              |             | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  | 1.9 | 5.8  |      |
|                 |              |             | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$    | 1.3 | 5.4  |      |
| $t_{dis}^{(3)}$ | A            | COM or Y    | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | 2.1 | 2.1  | ns   |
|                 |              |             | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  | 1.4 | 7.9  |      |
|                 |              |             | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  | 1.1 | 7.2  |      |
|                 |              |             | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$    | 1   | 5    |      |

- (1)  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ . The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- (2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- (3)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

## 6.7 Analog Switch Characteristics

T<sub>A</sub> = 25°C

| PARAMETER                                   | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS                                                                                       | V <sub>CC</sub> | TYP  | UNIT |
|---------------------------------------------|--------------|-------------|-------------------------------------------------------------------------------------------------------|-----------------|------|------|
| Frequency response (switch on)              | COM or Y     | Y or COM    | $C_L = 50\text{ pF}$ , $R_L = 600\ \Omega$ ,<br>$f_{in} = \text{sine wave}$<br>(see Figure 6)         | 1.65 V          | 35   | MHz  |
|                                             |              |             |                                                                                                       | 2.3 V           | 120  |      |
|                                             |              |             |                                                                                                       | 3 V             | 190  |      |
|                                             |              |             |                                                                                                       | 4.5 V           | 215  |      |
|                                             |              |             | $C_L = 5\text{ pF}$ , $R_L = 50\ \Omega$ ,<br>$f_{in} = \text{sine wave}$<br>(see Figure 6)           | 1.65 V          | >300 |      |
|                                             |              |             |                                                                                                       | 2.3 V           | >300 |      |
|                                             |              |             |                                                                                                       | 3 V             | >300 |      |
|                                             |              |             |                                                                                                       | 4.5 V           | >300 |      |
| Crosstalk <sup>(1)</sup> (between switches) | COM or Y     | Y or COM    | $C_L = 50\text{ pF}$ , $R_L = 600\ \Omega$ ,<br>$f_{in} = 1\text{ MHz}$ (sine wave)<br>(see Figure 7) | 1.65 V          | –58  | dB   |
|                                             |              |             |                                                                                                       | 2.3 V           | –58  |      |
|                                             |              |             |                                                                                                       | 3 V             | –58  |      |
|                                             |              |             |                                                                                                       | 4.5 V           | –58  |      |
|                                             |              |             | $C_L = 5\text{ pF}$ , $R_L = 50\ \Omega$ ,<br>$f_{in} = 1\text{ MHz}$ (sine wave)<br>(see Figure 7)   | 1.65 V          | –42  |      |
|                                             |              |             |                                                                                                       | 2.3 V           | –42  |      |
|                                             |              |             |                                                                                                       | 3 V             | –42  |      |
|                                             |              |             |                                                                                                       | 4.5 V           | –42  |      |

- (1) Adjust  $f_{in}$  voltage to obtain 0 dBm at input.

## Analog Switch Characteristics (continued)

 $T_A = 25^\circ\text{C}$ 

| PARAMETER                                     | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                                                                                                                | V <sub>CC</sub> | TYP    | UNIT |
|-----------------------------------------------|-----------------|----------------|--------------------------------------------------------------------------------------------------------------------------------|-----------------|--------|------|
| Crosstalk<br>(control input to signal output) | INH             | COM or Y       | $C_L = 50\text{ pF}$ , $R_L = 600\ \Omega$ ,<br>$f_{in} = 1\text{ MHz}$ (square wave)<br>(see <a href="#">Figure 8</a> )       | 1.65 V          | 35     | mV   |
|                                               |                 |                |                                                                                                                                | 2.3 V           | 50     |      |
|                                               |                 |                |                                                                                                                                | 3 V             | 70     |      |
|                                               |                 |                |                                                                                                                                | 4.5 V           | 100    |      |
| Feedthrough attenuation<br>(switch off)       | COM or Y        | Y or COM       | $C_L = 50\text{ pF}$ , $R_L = 600\ \Omega$ ,<br>$f_{in} = 1\text{ MHz}$ (sine wave)<br>(see <a href="#">Figure 9</a> )         | 1.65 V          | –60    | dB   |
|                                               |                 |                |                                                                                                                                | 2.3 V           | –60    |      |
|                                               |                 |                |                                                                                                                                | 3 V             | –60    |      |
|                                               |                 |                |                                                                                                                                | 4.5 V           | –60    |      |
|                                               |                 |                | $C_L = 5\text{ pF}$ , $R_L = 50\ \Omega$ ,<br>$f_{in} = 1\text{ MHz}$ (sine wave)<br>(see <a href="#">Figure 9</a> )           | 1.65 V          | –50    |      |
|                                               |                 |                |                                                                                                                                | 2.3 V           | –50    |      |
|                                               |                 |                |                                                                                                                                | 3 V             | –50    |      |
|                                               |                 |                |                                                                                                                                | 4.5 V           | –50    |      |
| Sine-wave distortion                          | COM or Y        | Y or COM       | $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$ ,<br>$f_{in} = 1\text{ kHz}$ (sine wave)<br>(see <a href="#">Figure 10</a> )  | 1.65 V          | 0.1%   |      |
|                                               |                 |                |                                                                                                                                | 2.3 V           | 0.025% |      |
|                                               |                 |                |                                                                                                                                | 3 V             | 0.015% |      |
|                                               |                 |                |                                                                                                                                | 4.5 V           | 0.01%  |      |
|                                               |                 |                | $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$ ,<br>$f_{in} = 10\text{ kHz}$ (sine wave)<br>(see <a href="#">Figure 10</a> ) | 1.65 V          | 0.15%  |      |
|                                               |                 |                |                                                                                                                                | 2.3 V           | 0.025% |      |
|                                               |                 |                |                                                                                                                                | 3 V             | 0.015% |      |
|                                               |                 |                |                                                                                                                                | 4.5 V           | 0.01%  |      |

## 6.8 Operating Characteristics

 $T_A = 25^\circ\text{C}$ 

| PARAMETER                                     | TEST CONDITIONS                            | V <sub>CC</sub>         | TYP | UNIT |
|-----------------------------------------------|--------------------------------------------|-------------------------|-----|------|
| C <sub>pd</sub> Power dissipation capacitance | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | $V_{CC} = 1.8\text{ V}$ | 9   | pF   |
|                                               |                                            | $V_{CC} = 2.5\text{ V}$ | 10  |      |
|                                               |                                            | $V_{CC} = 3.3\text{ V}$ | 10  |      |
|                                               |                                            | $V_{CC} = 5\text{ V}$   | 12  |      |

## 6.9 Typical Characteristics

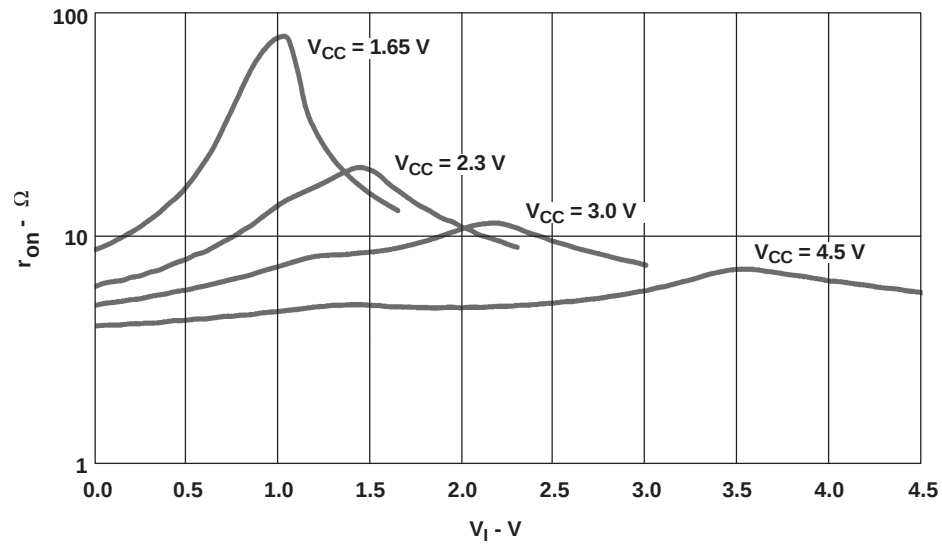
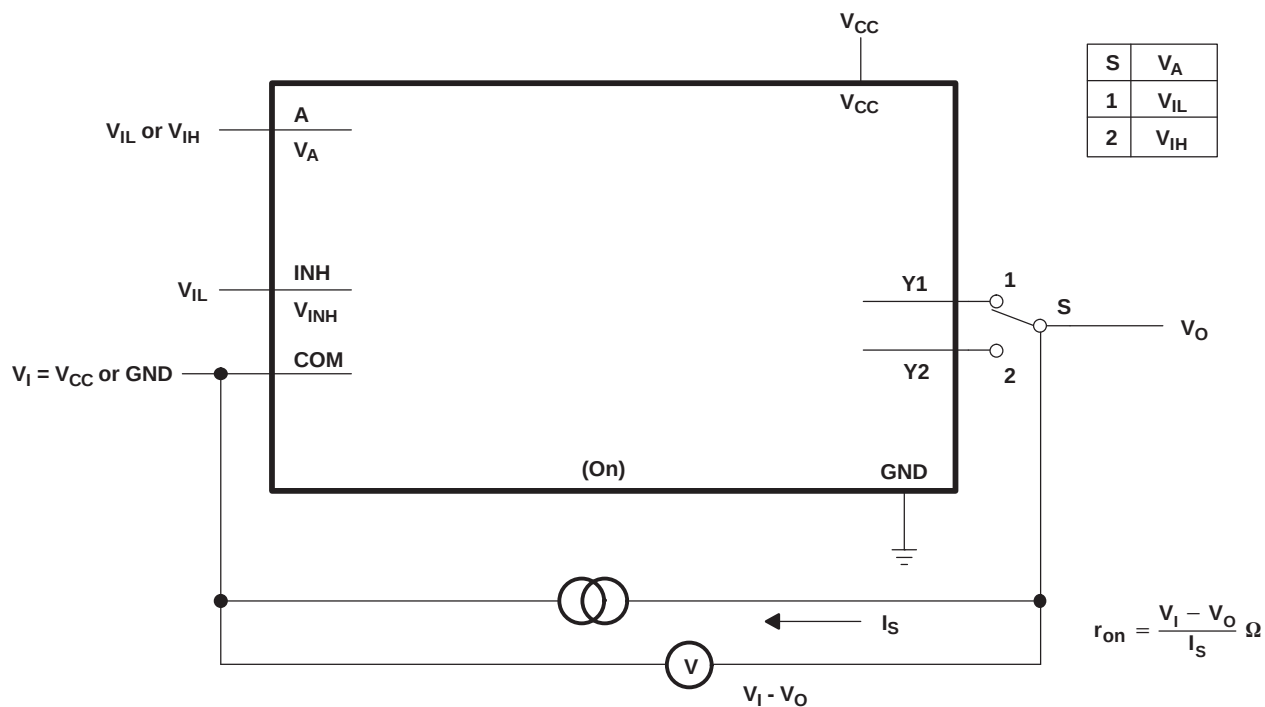
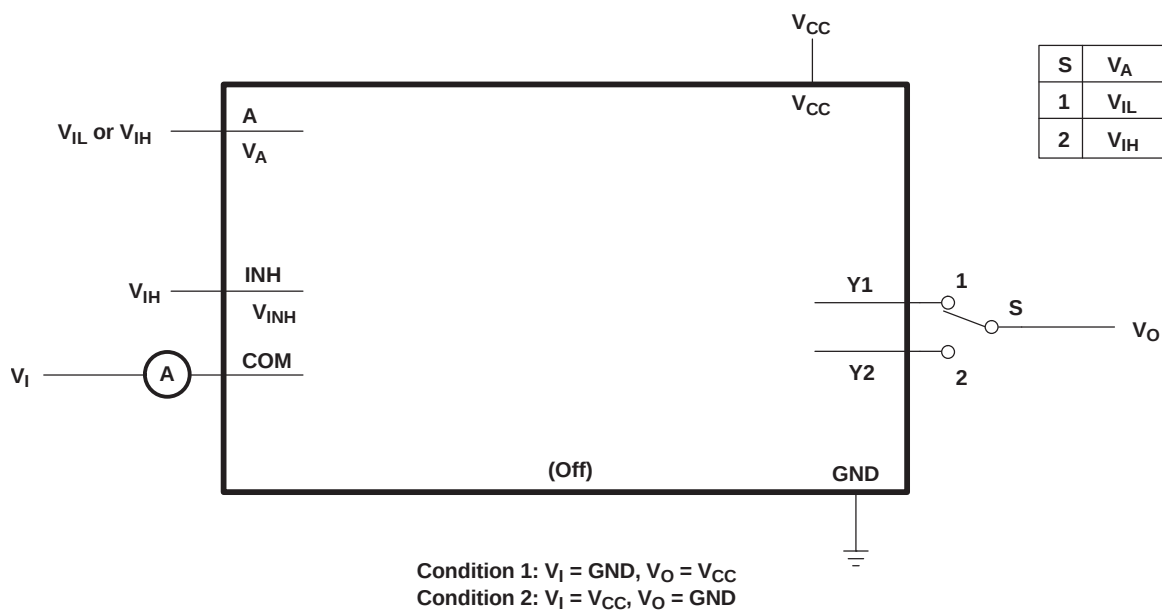


Figure 1. Typical  $r_{on}$  as a Function of Input Voltage ( $V_I$ ) for  $V_I = 0$  to  $V_{CC}$

## 7 Parameter Measurement Information

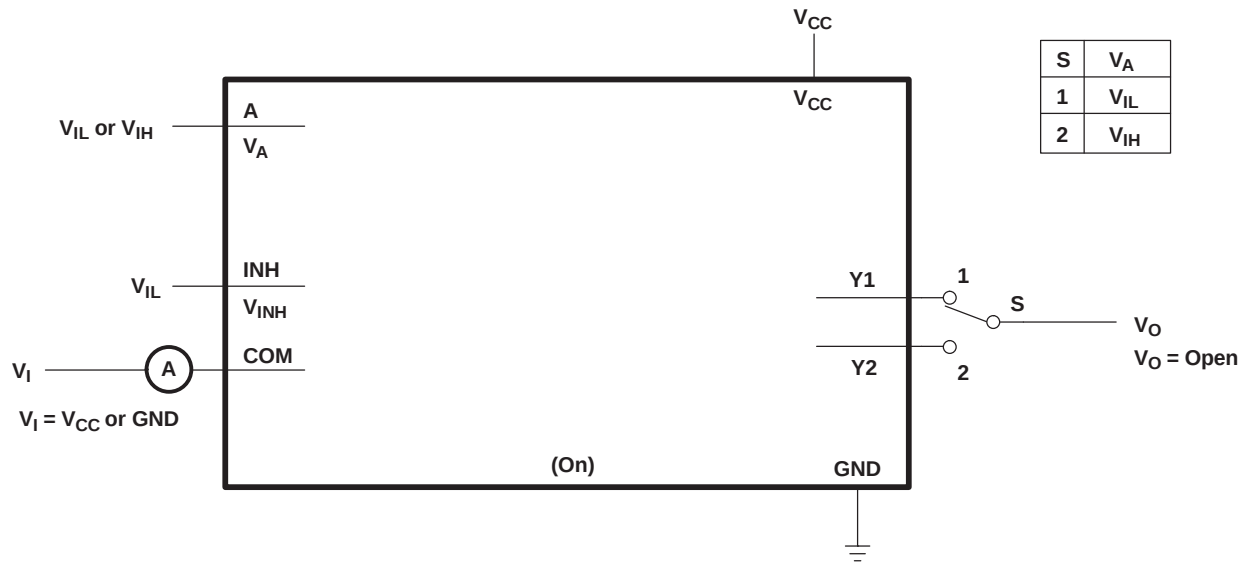


**Figure 2. ON-State Resistance Test Circuit**



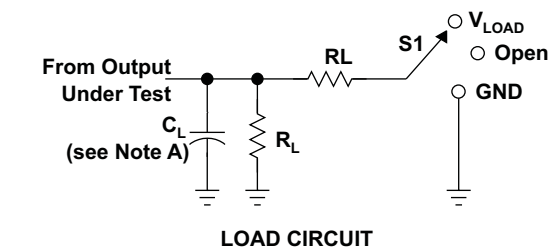
**Figure 3. OFF-State Switch Leakage-Current Test Circuit**

**Parameter Measurement Information (continued)**



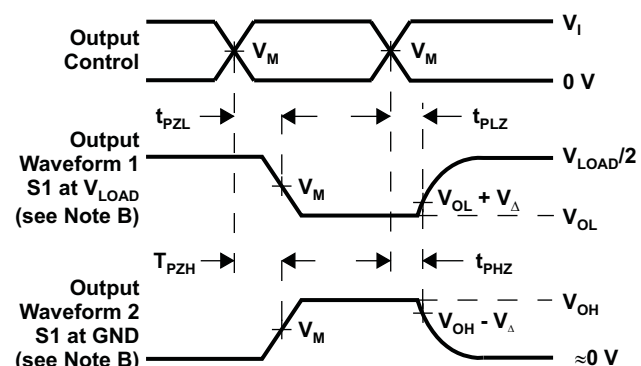
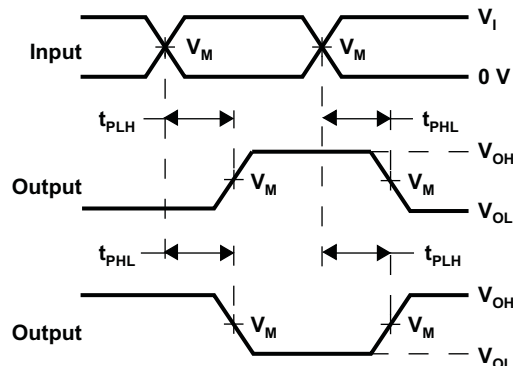
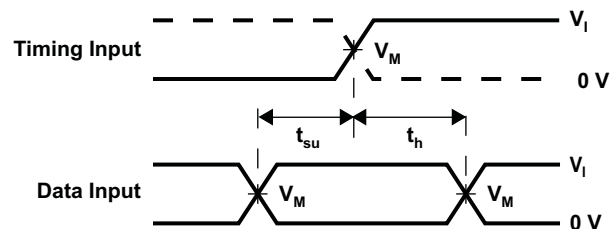
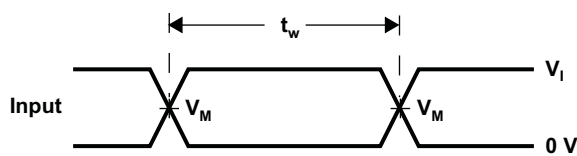
**Figure 4. ON-State Switch Leakage-Current Test Circuit**

## Parameter Measurement Information (continued)



| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

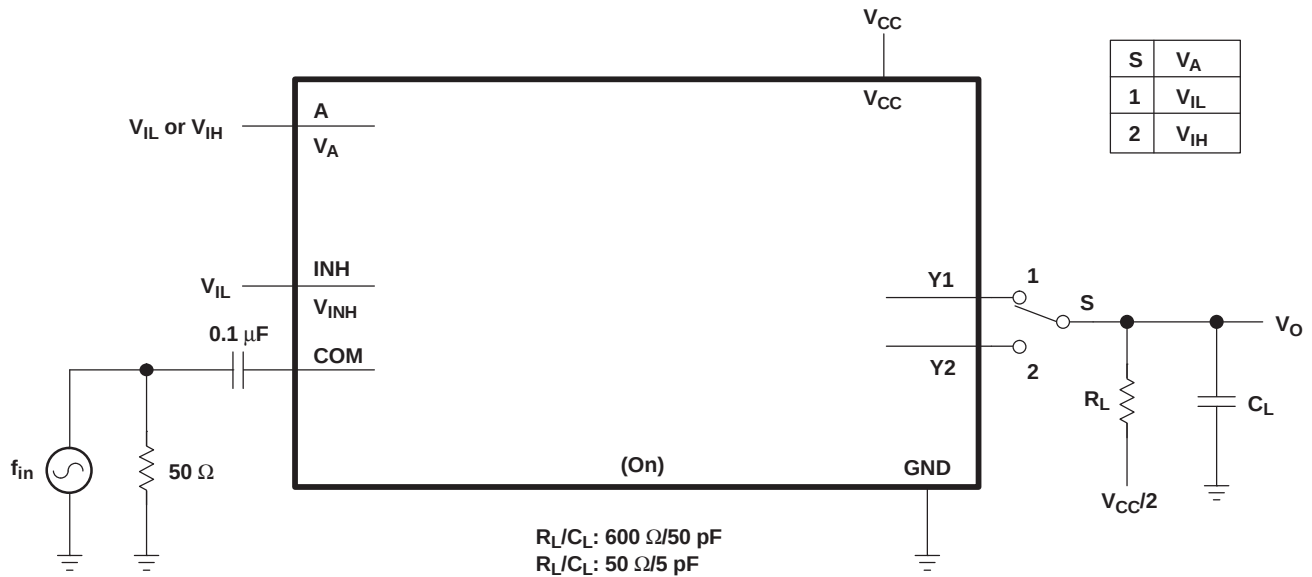
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



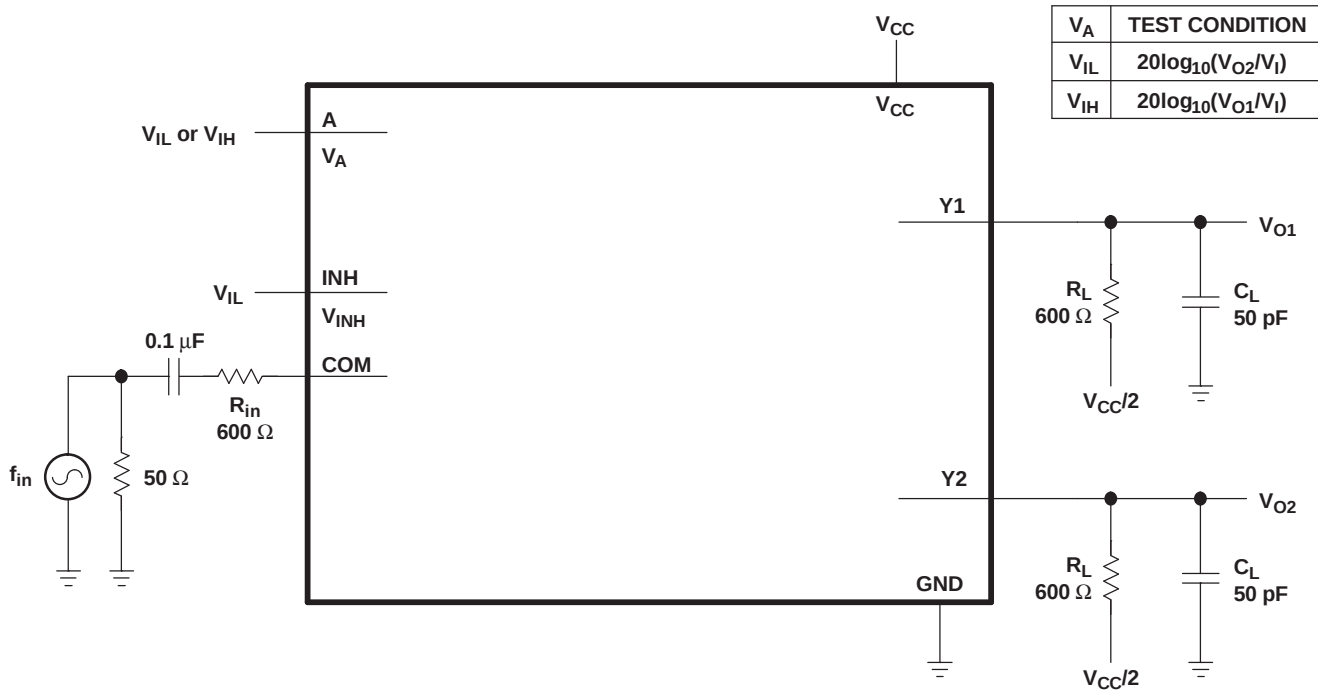
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

**Parameter Measurement Information (continued)**

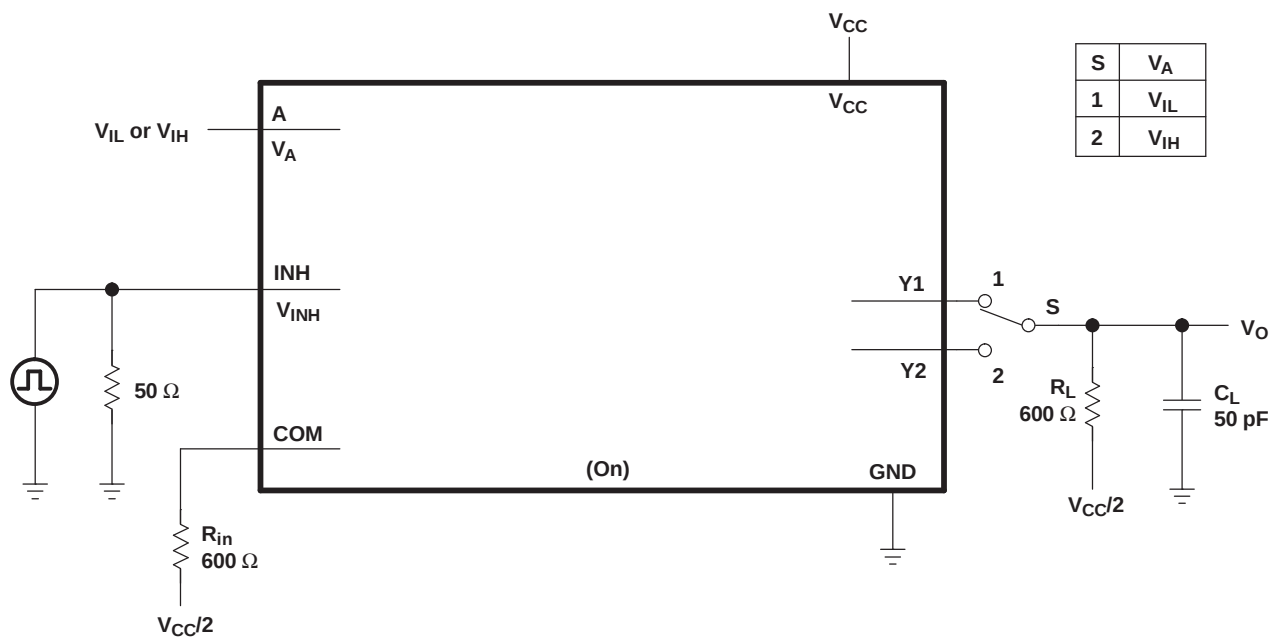


**Figure 6. Frequency Response (Switch On)**

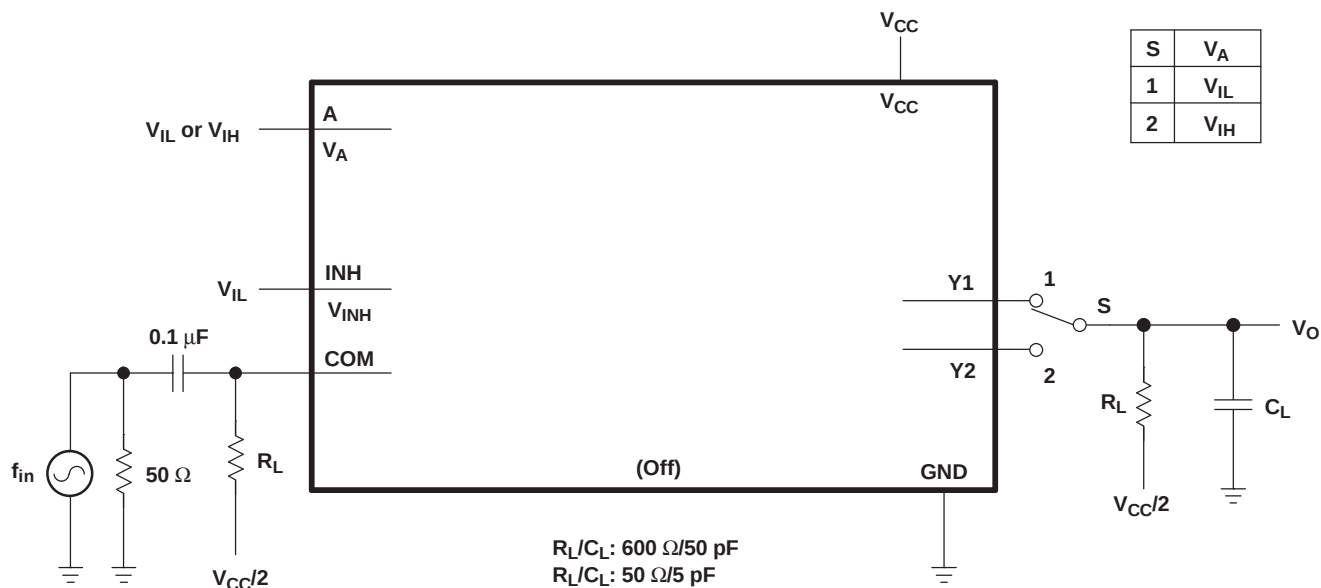


**Figure 7. Crosstalk (Between Switches)**

## Parameter Measurement Information (continued)

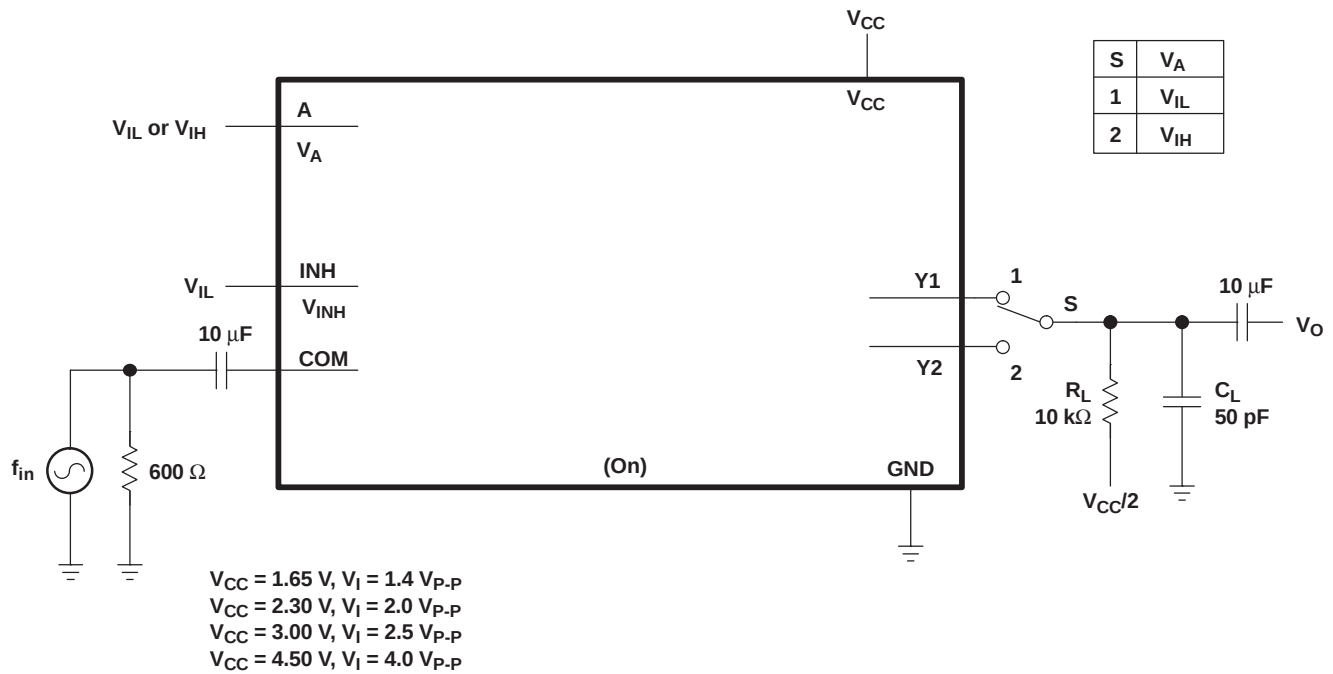


**Figure 8. Crosstalk (Control Input, Switch Output)**



**Figure 9. Feedthrough (Switch Off)**

**Parameter Measurement Information (continued)**



**Figure 10. Sine-Wave Distortion**

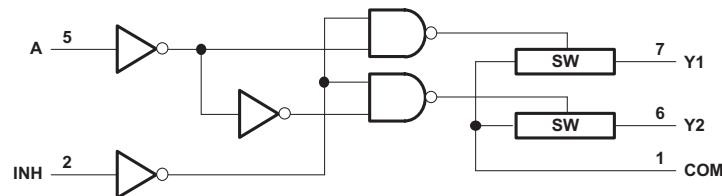
## 8 Detailed Description

### 8.1 Overview

This dual analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

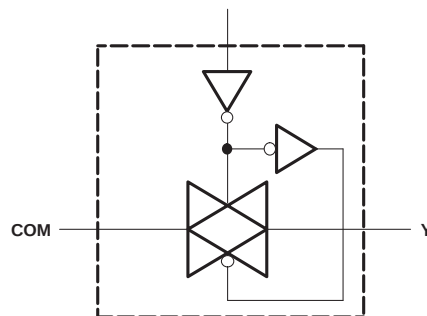
The SN74LVC2G53 device can handle both analog and digital signals. This device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

### 8.2 Functional Block Diagram



NOTE: For simplicity, the test conditions shown in Figure 1 through Figure 4 and Figure 6 through Figure 10 are for the demultiplexer configuration. Signals can be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

**Figure 11. Logic Diagram**



**Figure 12. Logic Diagram, Each Switch (SW)**

### 8.3 Feature Description

A high-level voltage applied to INH disables the switches. When INH is low, signals can pass from A to Y or Y to A. Low ON-resistance of 6.5  $\Omega$  at 4.5-V  $V_{CC}$  is ideal for analog signal conditioning systems. The control signals can accept voltages up to 5.5 V without  $V_{CC}$  connected in the system. Combination of lower  $t_{pd}$  of 0.8 ns at 3.3 V and low enable and disable time make this part suitable for high-speed signal switching applications.

### 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC2G53.

**Table 1. Function Table**

| CONTROL INPUTS |   | ON CHANNEL |
|----------------|---|------------|
| INH            | A |            |
| L              | L | Y1         |
| L              | H | Y2         |
| H              | X | None       |

## 9 Application and Implementation

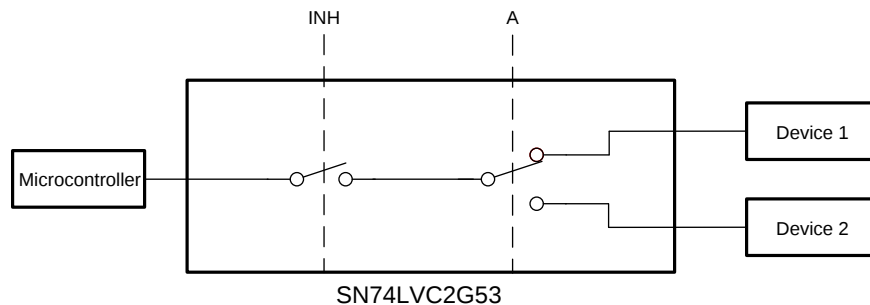
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LVC2G53 can be used in any situation where an SPDT switch is required in an application. This switch helps to select one of two signals of which signals can be either digital or analog.

### 9.2 Typical Application



**Figure 13. Typical Application Schematic**

#### 9.2.1 Design Requirements

The SN74LVC2G53 allows on/off control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and  $V_{CC}$  for optimal operation.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta v$  in the [Recommended Operating Conditions](#) table.
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Recommended Operating Conditions](#) table.
  - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommended Output Conditions:
  - Load currents should not exceed  $\pm 50$  mA.
3. Frequency Selection Criterion:
  - Maximum frequency tested is 150 MHz.
  - Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in [Layout](#).

## Typical Application (continued)

### 9.2.3 Application Curve

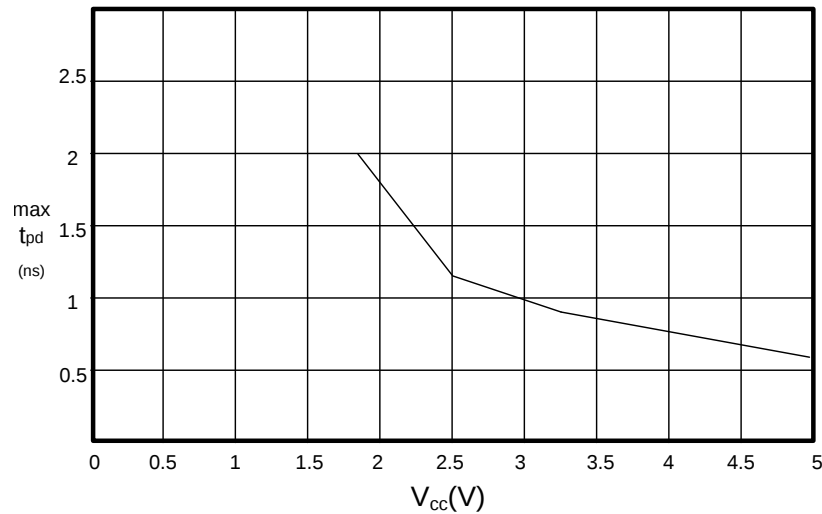


Figure 14. t<sub>pd</sub> vs V<sub>CC</sub>

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Absolute Maximum Ratings](#).

Each V<sub>CC</sub> terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V<sub>CC</sub>, then a 0.01-μF or 0.022-μF capacitor is recommended for each V<sub>CC</sub> because the V<sub>CC</sub> pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V<sub>CC</sub> and V<sub>DD</sub>, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

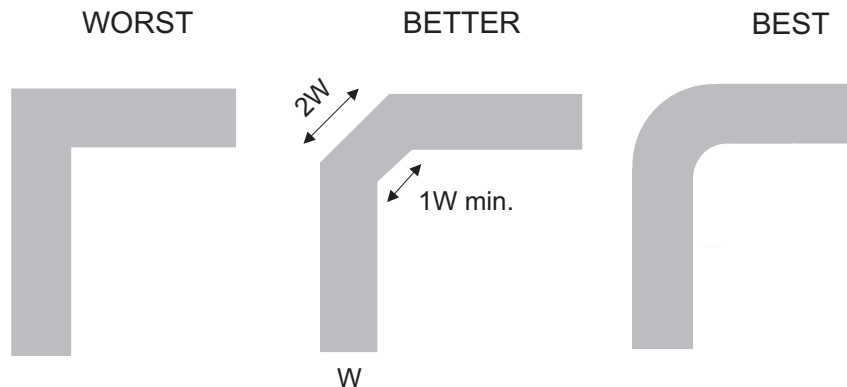
### 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection.

#### NOTE

Not all PCB traces can be straight, and so they will have to turn corners. [Figure 15](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

### 11.2 Layout Example



**Figure 15. Trace Example**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)    |
|-----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------|
| <a href="#">SN74LVC2G53DCT3</a>   | Obsolete      | Production           | SSOP (DCT)   8  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | C53<br>Z               |
| <a href="#">SN74LVC2G53DCTR</a>   | Active        | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | C53<br>Z               |
| SN74LVC2G53DCTR.A                 | Active        | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | C53<br>Z               |
| SN74LVC2G53DCTR.B                 | Active        | Production           | SSOP (DCT)   8  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | C53<br>Z               |
| <a href="#">SN74LVC2G53DCUR</a>   | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | (53, C53Q, C53R)<br>CZ |
| SN74LVC2G53DCUR.A                 | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | (53, C53Q, C53R)<br>CZ |
| SN74LVC2G53DCUR.B                 | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | (53, C53Q, C53R)<br>CZ |
| <a href="#">SN74LVC2G53DCURG4</a> | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | C53R                   |
| SN74LVC2G53DCURG4.B               | Active        | Production           | VSSOP (DCU)   8 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | C53R                   |
| <a href="#">SN74LVC2G53DCUT</a>   | Obsolete      | Production           | VSSOP (DCU)   8 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | (53, C53Q, C53R)<br>CZ |
| <a href="#">SN74LVC2G53DCUTG4</a> | Active        | Production           | VSSOP (DCU)   8 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -            | C53R                   |
| SN74LVC2G53DCUTG4.B               | Active        | Production           | VSSOP (DCU)   8 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | C53R                   |
| <a href="#">SN74LVC2G53YZPR</a>   | Active        | Production           | DSBGA (YZP)   8 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | C4N                    |
| SN74LVC2G53YZPR.B                 | Active        | Production           | DSBGA (YZP)   8 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | C4N                    |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC2G53DCTR   | SSOP         | DCT             | 8    | 3000 | 180.0              | 13.0               | 3.35    | 4.5     | 1.55    | 4.0     | 12.0   | Q3            |
| SN74LVC2G53DCUR   | VSSOP        | DCU             | 8    | 3000 | 178.0              | 9.0                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G53DCURG4 | VSSOP        | DCU             | 8    | 3000 | 180.0              | 8.4                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G53DCUTG4 | VSSOP        | DCU             | 8    | 250  | 180.0              | 8.4                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G53YZPR   | DSBGA        | YZP             | 8    | 3000 | 178.0              | 9.2                | 1.02    | 2.02    | 0.63    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC2G53DCTR   | SSOP         | DCT             | 8    | 3000 | 182.0       | 182.0      | 20.0        |
| SN74LVC2G53DCUR   | VSSOP        | DCU             | 8    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC2G53DCURG4 | VSSOP        | DCU             | 8    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74LVC2G53DCUTG4 | VSSOP        | DCU             | 8    | 250  | 202.0       | 201.0      | 28.0        |
| SN74LVC2G53YZPR   | DSBGA        | YZP             | 8    | 3000 | 220.0       | 220.0      | 35.0        |

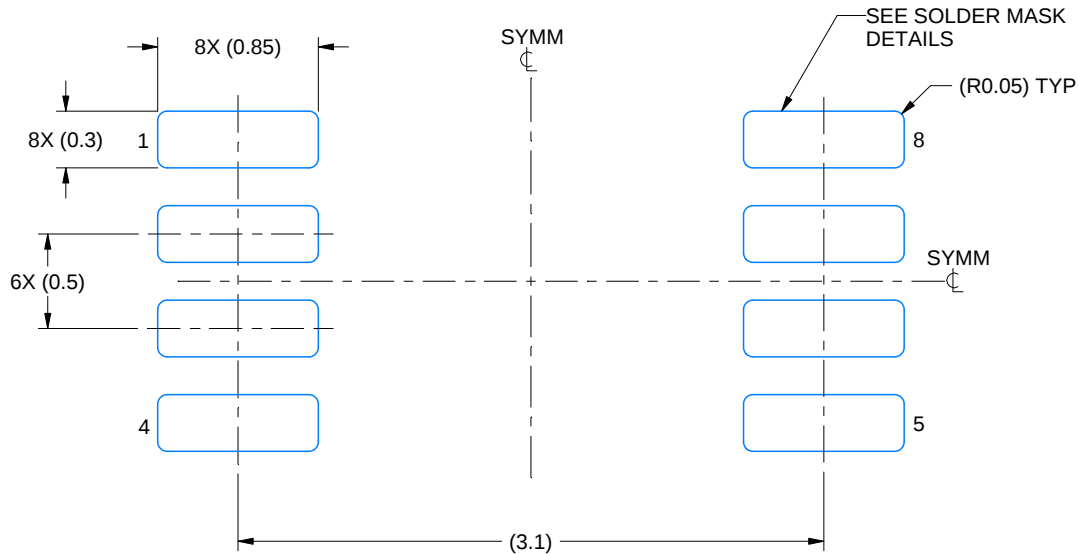


# EXAMPLE BOARD LAYOUT

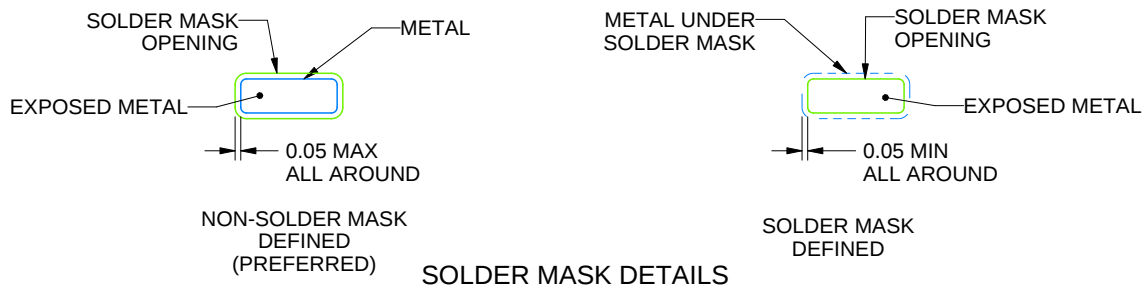
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

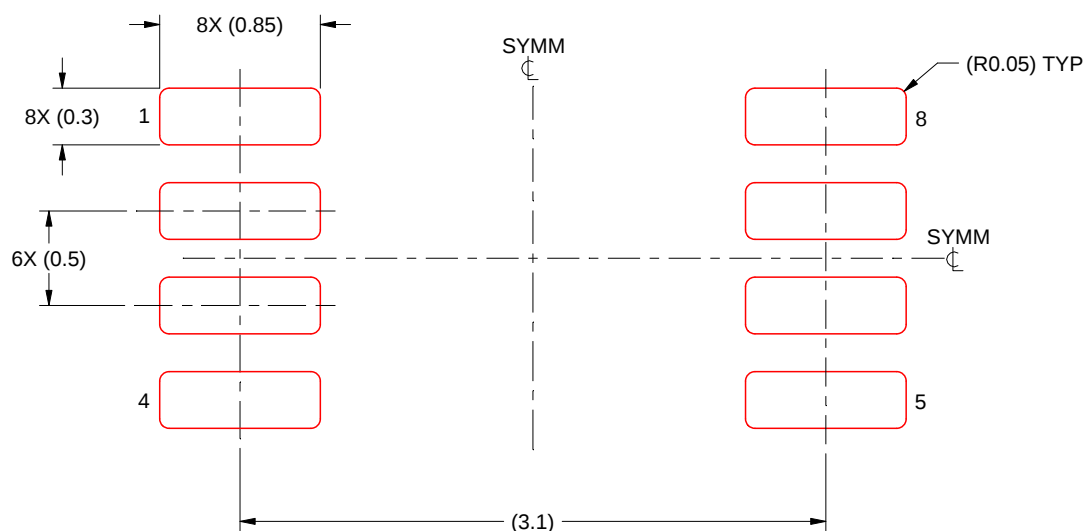
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

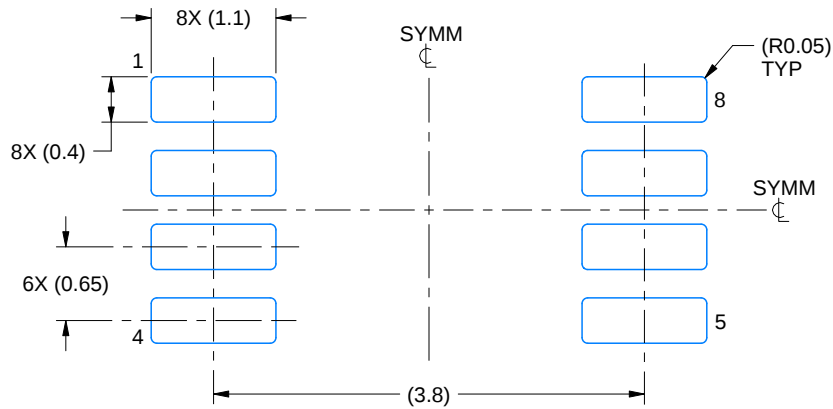


# EXAMPLE BOARD LAYOUT

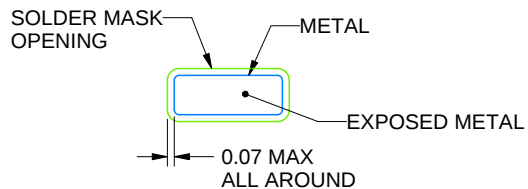
DCT0008A

SSOP - 1.3 mm max height

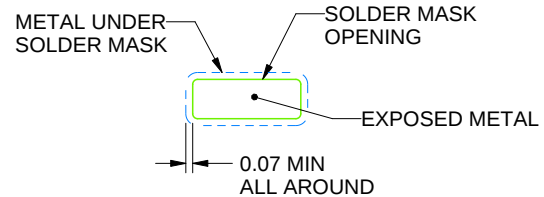
SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

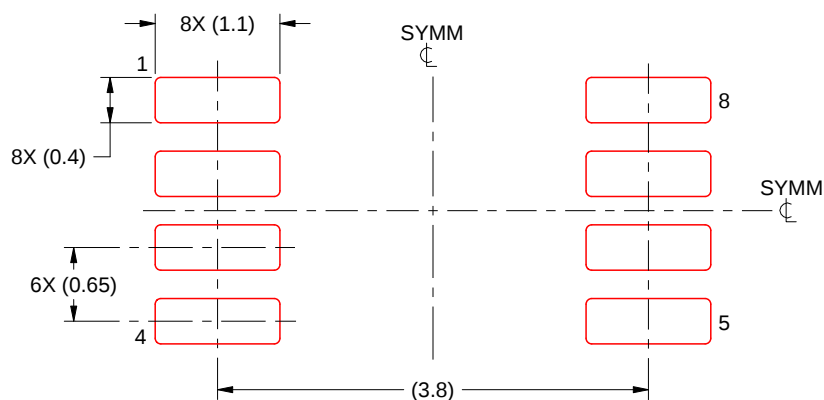
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



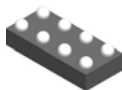
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

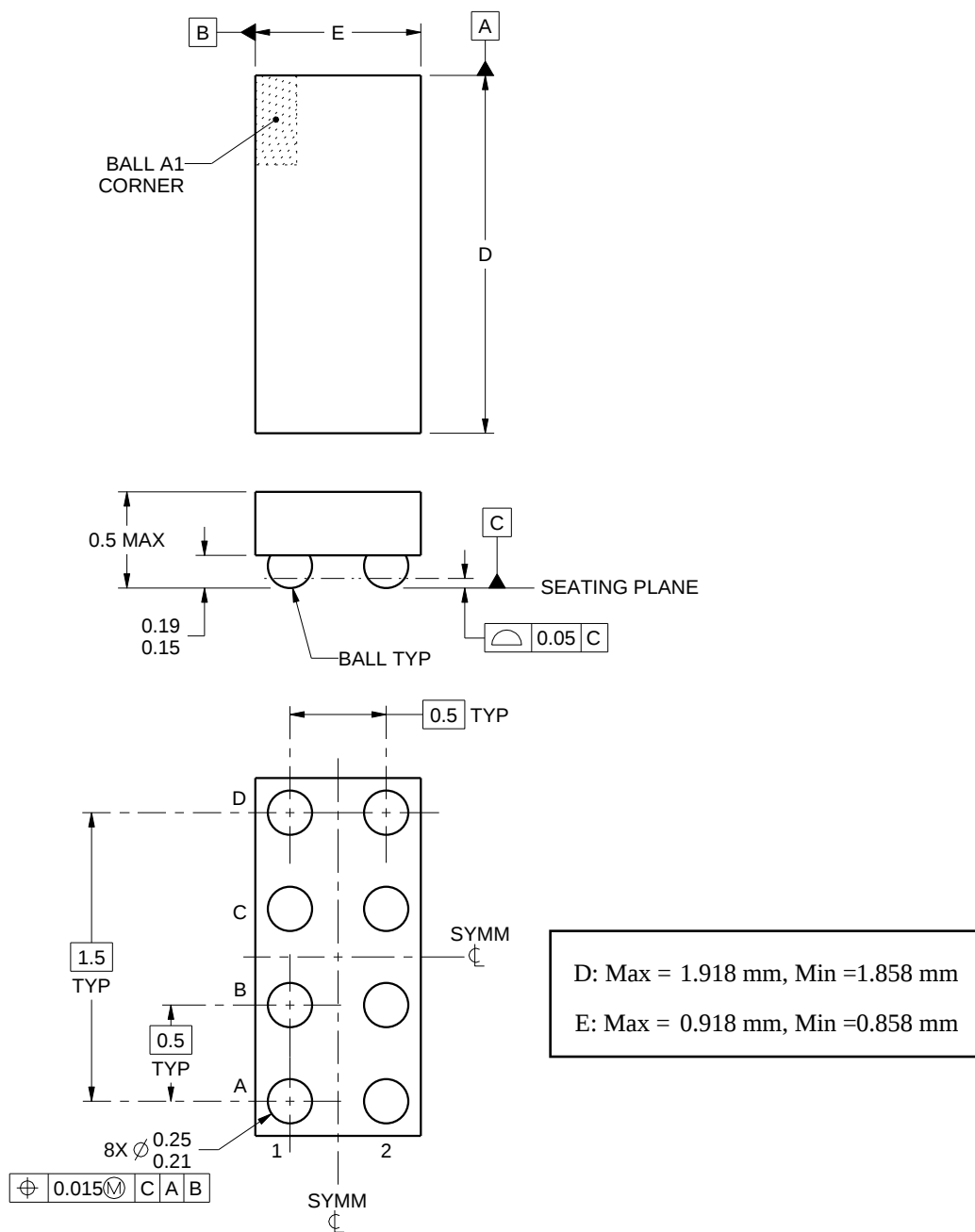
YZP0008



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

## NOTES:

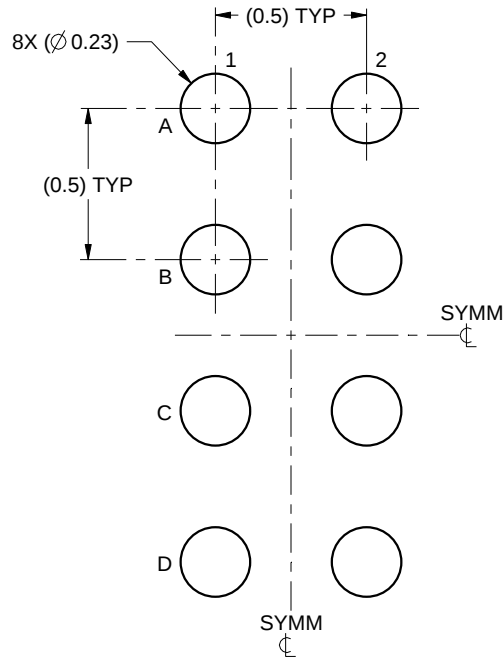
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

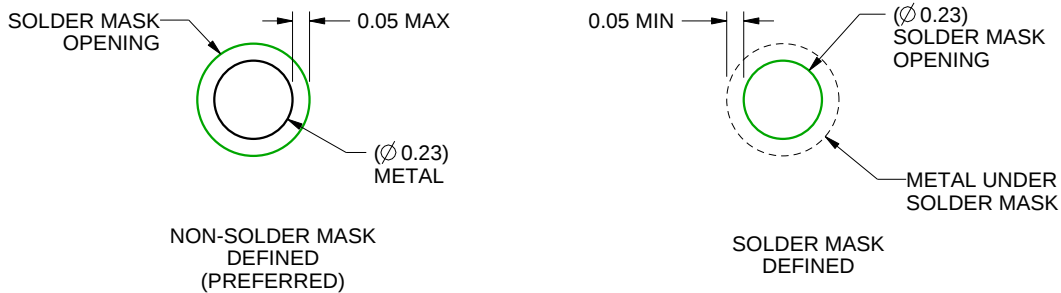
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

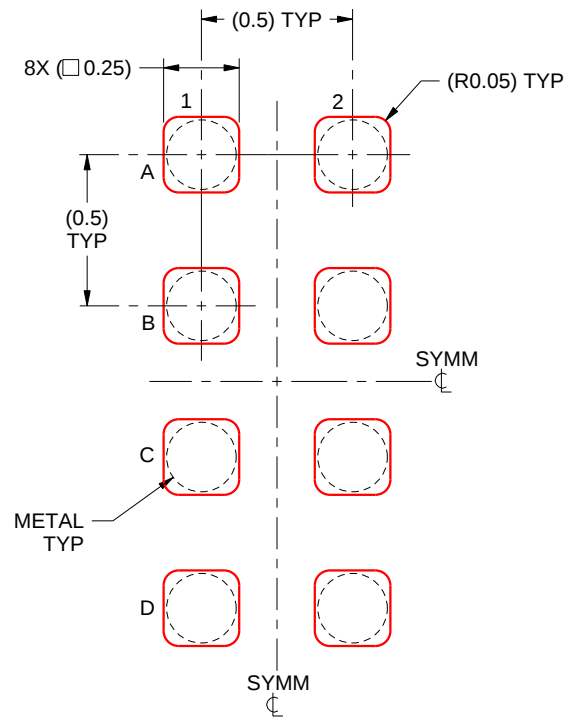
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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