TMS27128
131,072-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

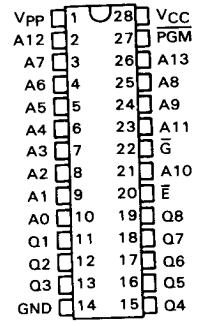
OCTOBER 1983 – REVISED JANUARY 1984

- **16,384 X 8 Organization**
- **Single +5-V Power Supply**
- **Pin Compatible with TMS2764 EPROM**
- **All Inputs and Outputs Are TTL Compatible**
- **Max Access/Min Cycle Time:**

TMS27128-25	250 ns
TMS27128-30	300 ns
TMS27128-45	450 ns

- **Low Active Current – 100 mA (Maximum)**
- **JEDEC Approved Pinout**
- **Fast Programming Algorithm**

TMS27128 . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Addresses
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	+5-V Power Supply
V_{PP}	+21-V Power Supply

description

The TMS27128 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 131,072 bits organized as 16,384 words of 8-bit length. The TMS27128 only requires a single 5-volt power supply. The TMS27128-25 provides an access time of 250 ns, which is compatible with high-speed microprocessors.

The TMS27128 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable/Power Down ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS27128 has a standby mode that reduces the maximum power dissipation from 525 mW to 210 mW when the device is placed on standby.

This EPROM is supplied in a 28-pin dual-in-line ceramic package (JL suffix). It is pin compatible with the TMS2764 EPROM and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMs27128 are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	X
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IL} or V_{IH}

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read

The dual control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 100 mA to 40 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

erasure

Before programming, the TMS27128 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 mW/cm^2 UV lamp will erase the device in approximately 20 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27128, the window should be covered with an opaque label.

fast programming

Note that the application of a voltage in excess of 22 V to V_{PP} may damage the TMS27128.

After erasure, logic "0's" are programmed into the desired locations. Programming consists of the following sequence of events. With the level on V_{PP} equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied, if correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at V_{CC} = 6.0 V and V_{PP} = 21.0 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V. A flowchart of the fast programming routine is shown in Figure 1.

multiple device programming

Several TMS27128's can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS27128's connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

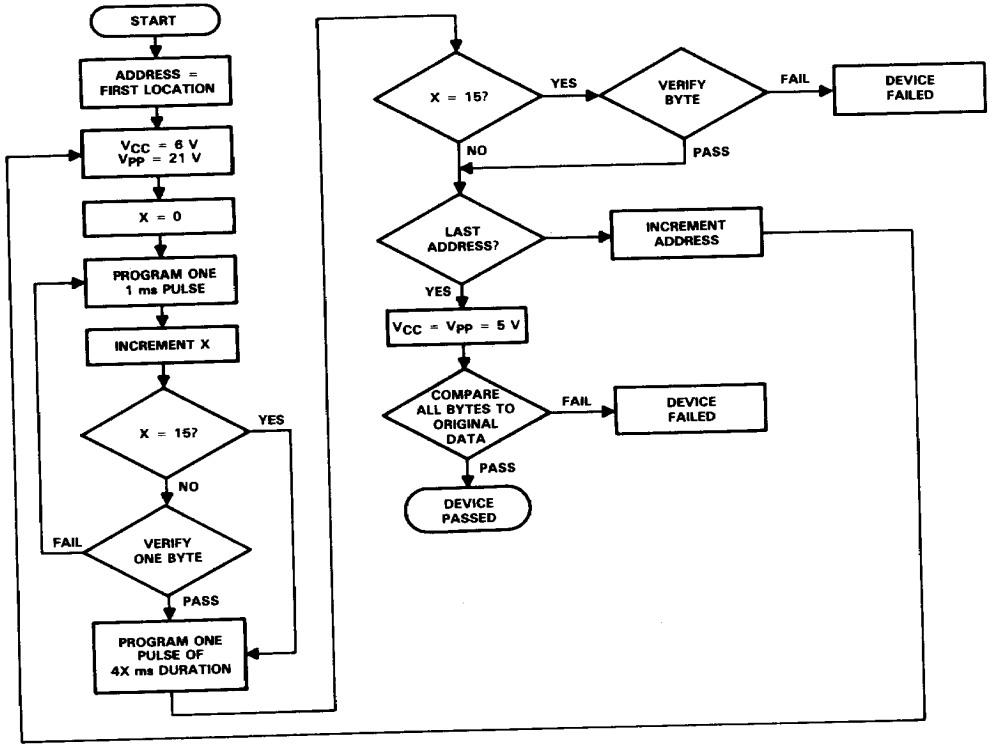

FIGURE 1 – FAST PROGRAMMING FLOWCHART

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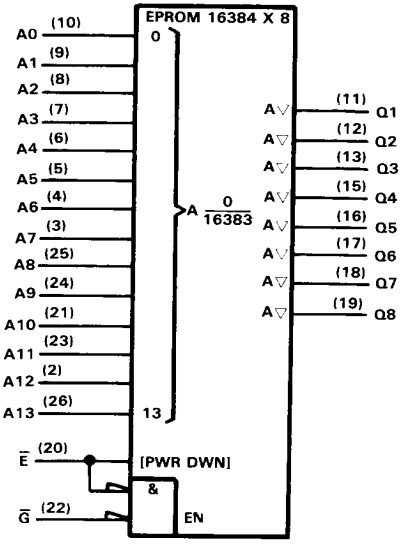
logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.6 V to 7 V
Supply voltage, V_{PP}	−0.6 V to 22 V
All input voltage	−0.6 V to 7 V
Output voltage	−0.6 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS27128			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{PP}		V_{CC}		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL} (see Note 1)	−0.1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 1: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V			±10	μA
I_{PP1}	V_{PP} supply current (read)	V_{PP} = 5.25 V			5	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{E}$ and $\overline{PGM}$ at V_{IL}			50	mA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}			40	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}			100	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V		4	6	pF
C_o	Output capacitance	V_O = 0 V		8	12	pF

† Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range, C_L = 100 pF, 1 Series 74 TTL load (see note 2 and figure 2)

PARAMETER		TMS27128-25		TMS27128-30		TMS27128-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		250		300		450	ns
$t_{a(E)}$	Access time from E		250		300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		100		120		150	ns
$t_{dis(G)}$‡	Output disable time from $\overline{G}$	0	60	0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first	0		0		0		ns

NOTE 2: For switching characteristics and timing measurements, input timing reference levels are 0.8 V and 2 V; output timing reference levels are 0.8 V and 2 V.

‡ Value calculated from 0.5 volt delta to measured output level; $t_{dis(G)}$ is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first. Refer to read cycle timing diagram.

recommended conditions for fast programming routine, T_A = 25°C (see note 2 and fast programming cycle timing diagram)

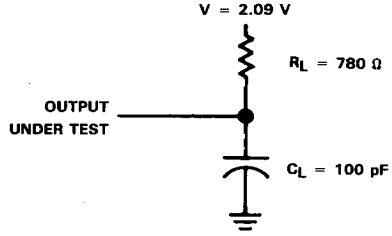
PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	5.75	6	6.25	V
V_{PP}	Supply voltage (see Note 4)	20.5	21	21.5	V
$t_{w(IPGM)}$	$\overline{PGM}$ initial program pulse duration (see Note 5)	0.95	1	1.05	ms
$t_{w(FPGM)}$	$\overline{PGM}$ final pulse duration (see Note 6)	3.8		63	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs

fast programming characteristics, T_A = 25°C (see note 2 and fast programming cycle timing diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{dis(G)FP}$	Output disable time from $\overline{G}$ (see Note 7)	C_L = 100 pF	0		130	ns
$t_{en(G)FP}$	Output enable time from $\overline{G}$	1 Series 74 TTL load			150	

NOTES:
2. For all switching characteristics and timing measurements, input timing reference levels are 0.8 V and 2 V; output timing reference levels are 0.8 V and 2 V.
3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
4. When programming the TMS27128, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.
5. The initial program pulse duration tolerance is 1 ms ± 5%.
6. The length of the Final pulse will vary from 3.8 ms to 63 ms depending on the number of initial pulse applications (X).
7. This parameter is only sampled and is not 100% tested.

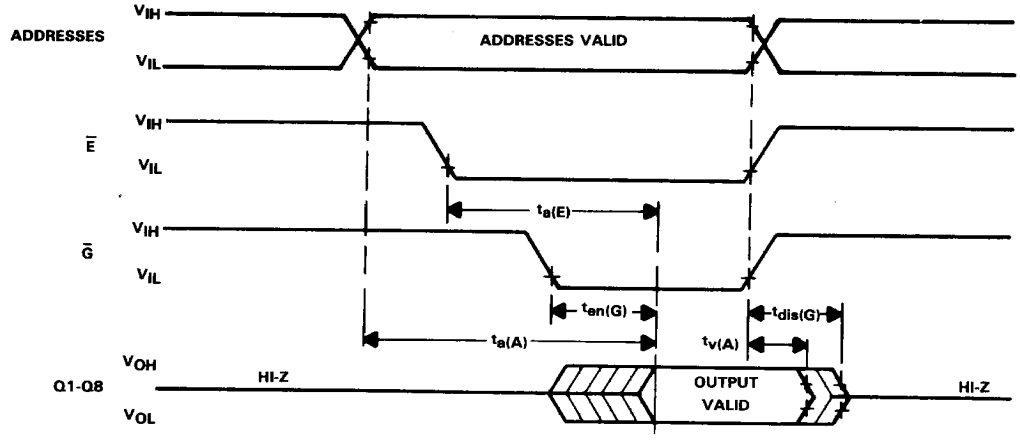
PARAMETER MEASUREMENT INFORMATION



NOTE: $t_f \leq 20$ ns and $t_r \leq 20$ ns.

FIGURE 2 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



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fast program cycle timing