64-Position OTP Digital Potentiometer

AD5273

FEATURES

64 Positions
OTP (One-Time-Programmable)[1] Set-and-Forget Resistance Setting
1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ End-to-End Terminal Resistance
Compact SOT-23-8 Standard Package
Ultralow Power: I_{DD} = 5 μA Max
Fast Settling Time: t_S = 5 μs Typ in Power-Up
I²C® Compatible Digital Interface
Computer Software[2] Replaces μC in Factory Programming Applications
Wide Temperature Range: –40°C to +105°C
5 V Programming Voltage
Low Operating Voltage: 2.7 V to 5.5 V
OTP Validation Check Function

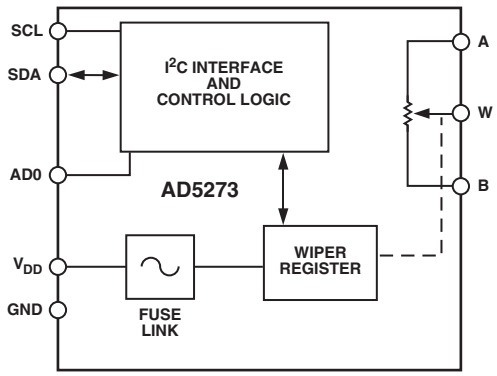
APPLICATIONS

Systems Calibrations
Electronics Level Settings
Mechanical Trimmers Replacement in New Designs
Automotive Electronics Adjustments
Transducer Circuits Adjustments
Programmable Filters up to 6 MHz BW[3]

GENERAL DESCRIPTION

The AD5273 is a 64-position, one-time-programmable (OTP) digital potentiometer[4] that employs fuse link technology to achieve the permanent program setting. This device performs the same electronic adjustment function as most mechanical trimmers and variable resistors. It allows unlimited adjustments before permanently setting the resistance values. The AD5273 is programmed using a 2-wire, I²C compatible digital control. During the write mode, a fuse blow command is executed after the final value is determined, thereby freezing the wiper position at a given setting (analogous to placing epoxy on a mechanical trimmer). When this permanent setting is achieved, the value will not change, regardless of the supply variations or environmental stresses under normal operating conditions. To verify the success of permanent programming, Analog Devices patterned the OTP validation such that the fuse status can be discerned from two validation bits in the read mode.

FUNCTIONAL BLOCK DIAGRAM



In addition, for applications that program the AD5273 at the factory, Analog Devices offers device programming software[2] running on Windows NT®, 2000, and XP operating systems. This software application effectively replaces any external I²C controllers, which in turn enhances users' systems' time-to-market.

The AD5273 is available in 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ resistances, in a compact SOT-23 8-lead standard package, and operates from –40°C to +105°C.

Along with its unique OTP feature, the AD5273 lends itself well to general digital potentiometer applications due to its effective resolution, array resistance options, small footprint, and low cost.

An AD5273 evaluation kit and software are available. The kit includes the connector and cable that can be converted for further factory programming applications.

For applications that require dynamic adjustment of resistance settings with nonvolatile EEMEM, users should refer to the AD523x and AD525x families of nonvolatile memory digital potentiometers.

NOTES
[1] One-Time-Programmable—Unlimited adjustments before permanent setting.
[2] ADI cannot guarantee the software to be 100% compatible in all systems due to the wide variations in computer configurations.
[3] Applies to 1 kΩ parts only.
[4] The terms digital potentiometer, VR, and RDAC are used interchangeably.

REV. A

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AD5273–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS 1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = 2.7 V to 5.5 V, $V_A \le V_{DD}$, V_B = 0 V, –40°C < T_A < +105°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resolution	N				6	Bits
Resistor Differential NL[2]	R-DNL					
(10 kΩ, 50 kΩ, 100 kΩ)		R_{WB}, V_A = NC	–0.5	+0.05	+0.5	LSB
(1 kΩ)		R_{WB}, V_A = NC	–1	+0.25	+1	LSB
Resistor Nonlinearity[2]	R-INL					LSB
(10 kΩ, 50 kΩ, 100 kΩ)		R_{WB}, V_A = NC	–0.5	+0.10	+0.5	LSB
(1 kΩ)		R_{WB}, V_A = NC	–5	+2	+5	LSB
Nominal Resistance Tolerance[3]	ΔR_{AB}	T_A = 25°C				
(10 kΩ, 50 kΩ, 100 kΩ)			–30		+30	%
Nominal Resistance (1 kΩ)	R_{AB}		0.8	1.2	1.6	kΩ
Rheostat Mode Temperature Coefficient[4]	$\Delta R_{WB}/\Delta T$	Wiper = No Connect		300		ppm/°C
Wiper Resistance	R_W	$I_W = V_{DD}/R$, V_{DD} = 3 V or 5 V		60	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[5]	DNL		–0.5	+0.1	+0.5	LSB
Integral Nonlinearity[5]	INL		–0.5		+0.5	LSB
Voltage Divider[4]						
Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x20		10		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x3F	–1		0	LSB
(10 kΩ, 50 kΩ, 100 kΩ)			–1		0	LSB
(1 kΩ)			–6		0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	–6		0	LSB
(10 kΩ, 50 kΩ, 100 kΩ)			0		1	LSB
(1 kΩ)			0		5	LSB
RESISTOR TERMINALS						
Voltage Range[6]	$V_{A, B, W}$		0		V_{DD}	V
Capacitance[7] A, B	$C_{A, B}$	f = 5 MHz, Measured to GND, Code = 0x20			25	pF
Capacitance[7] W	C_W	f = 1 MHz, Measured to GND, Code = 0x20			55	pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{LOGIC} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{LOGIC} = 3 V			0.6	V
Output Logic High (SDO)	V_{IH}		4.9			V
Output Logic Low (SDO)	V_{IL}				0.4	V
Input Logic Current	I_{IL}	V_{IN} = 0 V or 5 V		0.01	1	µA
Input Capacitance[7]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Power Supply[8]	V_{DD_OTP}	T_A = 25°C	5		6	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		0.1	5	µA
OTP Supply Current[9]	I_{DD_OTP}	T_A = 25°C	100			mA
Power Dissipation[10]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V		0.2	0.3	mW
Power Supply Sensitivity	PSRR	R_{AB} = 1 kΩ	–0.3		+0.3	%/%
	PSRR	R_{AB} = 10 kΩ, 50 kΩ, 100 kΩ	–0.05		+0.05	%/%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS[7, 11, 12]						
Bandwidth –3 dB	BW_1 kΩ	R_{AB} = 1 kΩ, Code = 0x20		6000		kHz
	BW_10 kΩ	R_{AB} = 10 kΩ, Code = 0x20		600		kHz
	BW_50 kΩ	R_{AB} = 50 kΩ, Code = 0x20		110		kHz
	BW_100 kΩ	R_{AB} = 100 kΩ, Code = 0x20		60		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, R_{AB} = 1 kΩ, V_B = 0 V, f = 1 kHz		0.014		%
Adjustment Settling Time	t_{S1}	V_A = 5 V ± 1 LSB Error Band, V_B = 0, Measured at V_W		5		µs
OTP Settling Time[13]	t_{S_OTP}	V_A = 5 V ± 1 LSB Error Band, V_B = 0, Measured at V_W		400		ms
Power-Up Settling Time – Post Fuses Blown	t_{S2}	V_A = 5 V ± 1 LSB Error Band, V_B = 0, Measured at V_W		5		µs
Resistor Noise Voltage	e_{N_WB}	R_{AB} = 1 kΩ, f = 1 kHz, Code = 0x20		3		nV/√Hz
		R_{AB} = 20 kΩ, f = 1 kHz, Code = 0x20		13		nV/√Hz
		R_{AB} = 50 kΩ, f = 1 kHz, Code = 0x20		20		nV/√Hz
		R_{AB} = 100 kΩ, f = 1 kHz, Code = 0x20		28		nV/√Hz
INTERFACE TIMING CHARACTERISTICS (applies to all parts[7, 12, 14])						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD;\,STA}$ Hold Time (repeated START)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;\,STA}$ Setup Time for START Condition	t_5		0.6			µs
$t_{HD;\,DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;\,DAT}$ Data Setup Time	t_7		0.1			µs
t_F Fall Time of Both SDA and SCL Signals	t_8				0.3	µs
t_R Rise Time of Both SDA and SCL Signals	t_9				0.3	µs
$t_{SU;\,STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

NOTES

[1] Typicals represent average readings at 25°C, V_{DD} = 5 V, and V_{SS} = 0 V.

[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

[3] V_{AB} = V_{DD}, Wiper (V_W) = No Connect.

[4] $\Delta R_{WB}/\Delta T = \Delta R_{WA}/\Delta T$. Temperature coefficient is code dependent; see the Typical Performance Characteristics.

[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

[6] Resistor terminals A, B, and W have no limitations on polarity with respect to each other.

[7] Guaranteed by design and not subject to production test.

[8] Different from operating power supply, power supply for OTP is used one time only.

[9] Different from operating current, supply current for OTP lasts approximately 400 ms for the one time it is needed.

[10] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[11] Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

[12] All dynamic characteristics use V_{DD} = 5 V.

[13] Different from settling time after fuses are blown. The OTP settling time occurs once only.

[14] See Figure 1 for location of measured values.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V, +6.5 V
V_A, V_B, V_W to GND . . . . . GND, V_{DD}
A–B, A–W, B–W
  Intermittent[2] . . . . . ±20 mA
  Continuous . . . . . ±2 mA
Digital Input and Output Voltage to GND . . . . . 0 V, V_{DD}
Operating Temperature Range . . . . . –40°C to +105°C
Maximum Junction Temperature ($T_{J\ MAX}$) . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
  Vapor Phase (60 sec) . . . . . 215°C
  Infrared (15 sec) . . . . . 220°C
Thermal Resistance[3] θ_{JA}, SOT-23 . . . . . 230°C/W

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[3] Package Power Dissipation = $(T_{J\ MAX} - T_A)/\theta_{JA}$.

ORDERING GUIDE

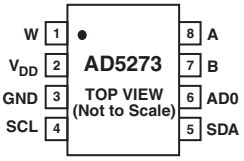
Model	Resistance R_{AB} (kΩ)	Package Code	Package Description	Full Container Quantities	Branding
AD5273BRJ1-REEL7	1	RJ	SOT-23-8	3000	DYA
AD5273BRJ10-REEL7	10	RJ	SOT-23-8	3000	DYB
AD5273BRJ50-REEL7	50	RJ	SOT-23-8	3000	DYC
AD5273BRJ100-REEL7	100	RJ	SOT-23-8	3000	DYD
AD5273BRJ1-R2	1	RJ	SOT-23-8	250	DYA
AD5273BRJ10-R2	10	RJ	SOT-23-8	250	DYB
AD5273BRJ50-R2	50	RJ	SOT-23-8	250	DYC
AD5273BRJ100-R2	100	RJ	SOT-23-8	250	DYD
AD5273EVAL	*	NA	NA	*	NA

*Users should order samples additionally as the evaluation kit comes with a socket but does not include the parts.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5273 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

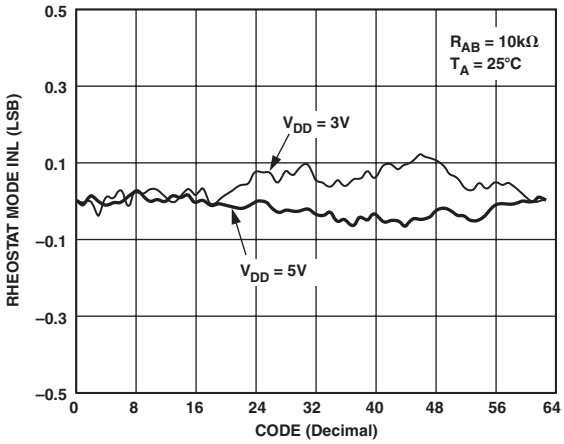
PIN CONFIGURATION



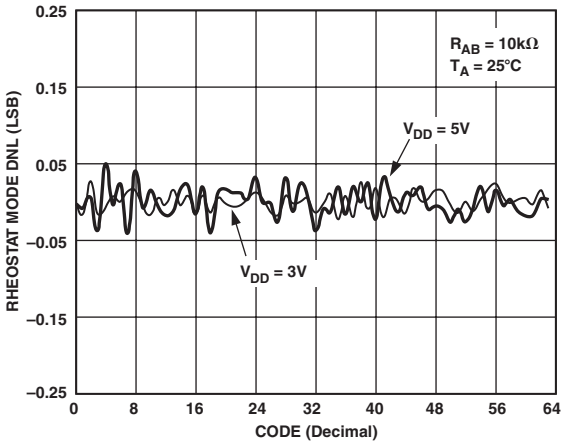
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	W	Wiper Terminal W.
2	V_{DD}	Positive Power Supply. Specified for non-OTP operation from 2.7 V to 5.5 V. For OTP programming, V_{DD} needs to be a minimum of 5 V.
3	GND	Common Ground.
4	SCL	Serial Clock Input. Requires pull-up resistor.
5	SDA	Serial Data Input/Output. Requires pull-up resistor.
6	AD0	I^2C Device Address Bit. Allows maximum of two AD5273s to be addressed.
7	B	Resistor Terminal B.
8	A	Resistor Terminal A.

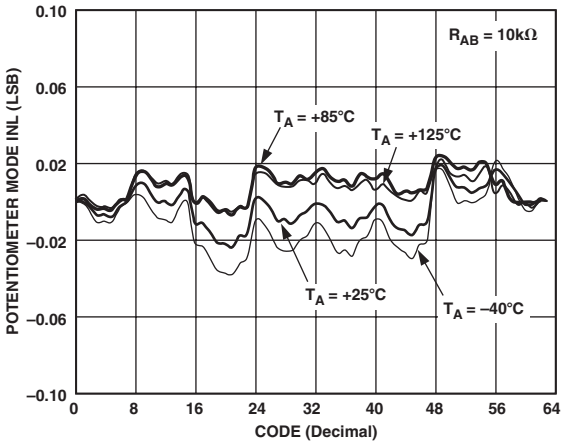
AD5273–Typical Performance Characteristics



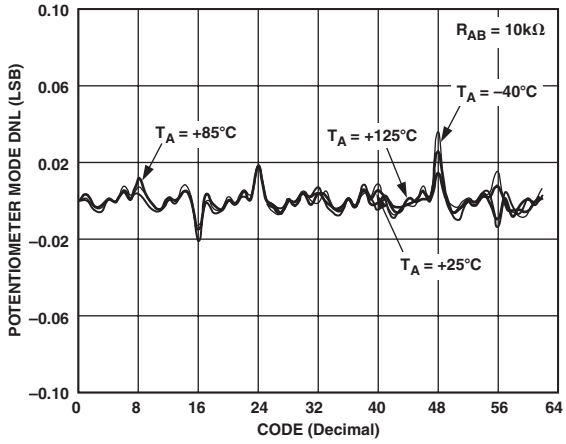
TPC 1. R_{INL} vs. Code vs. Supply Voltages



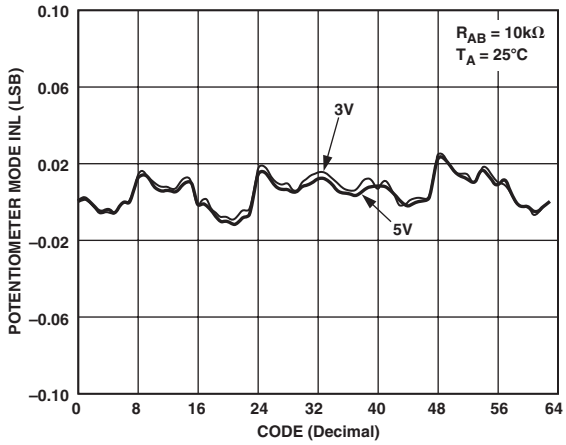
TPC 2. R_{DNL} vs. Code vs. Supply Voltages



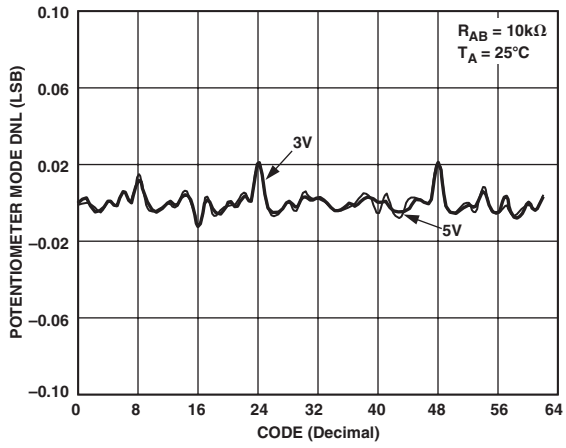
TPC 3. INL vs. Code vs. Temperature



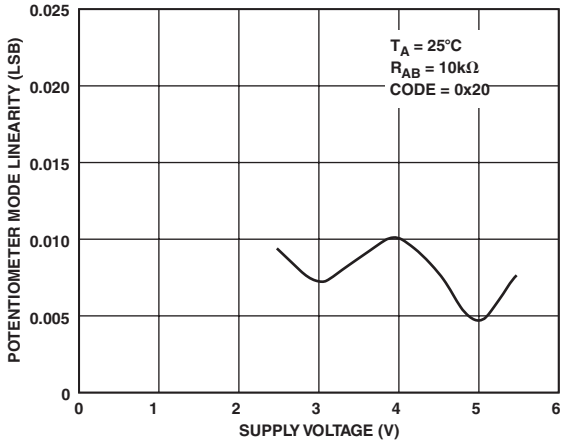
TPC 4. DNL vs. Code vs. Temperature



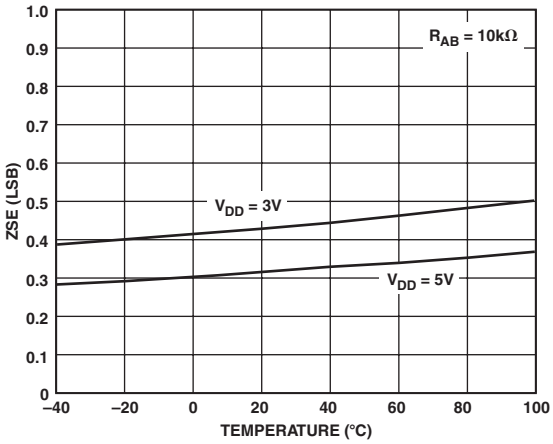
TPC 5. INL vs. Code vs. Supply Voltages



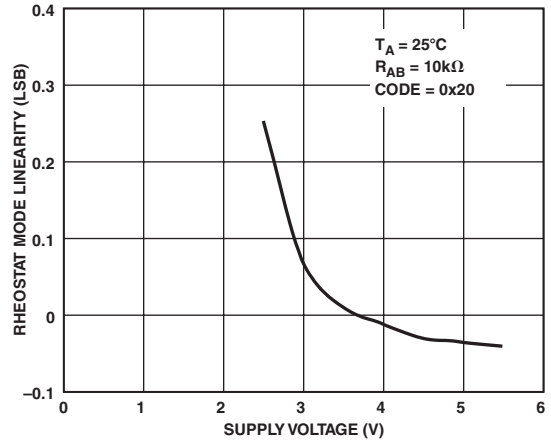
TPC 6. DNL vs. Code vs. Supply Voltages



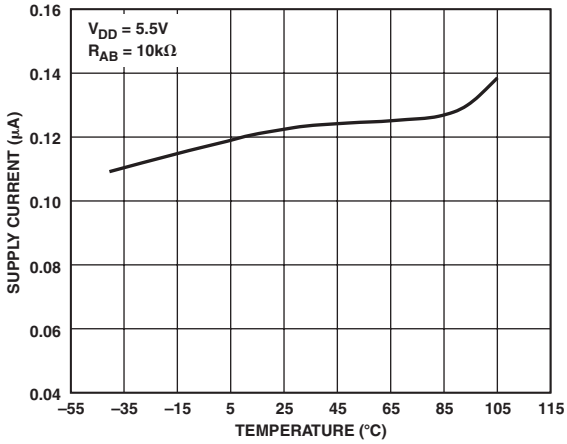
TPC 7. INL Oversupply Voltage



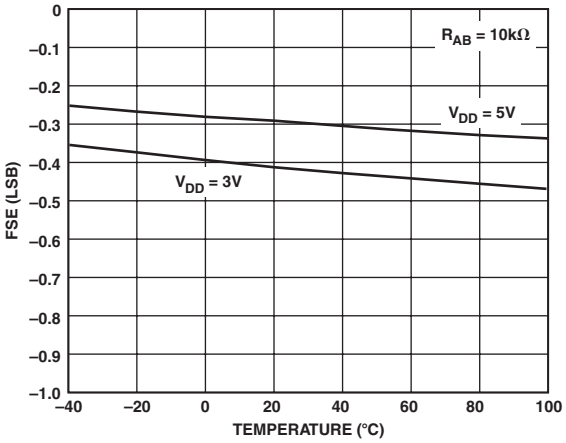
TPC 10. Zero-Scale Error



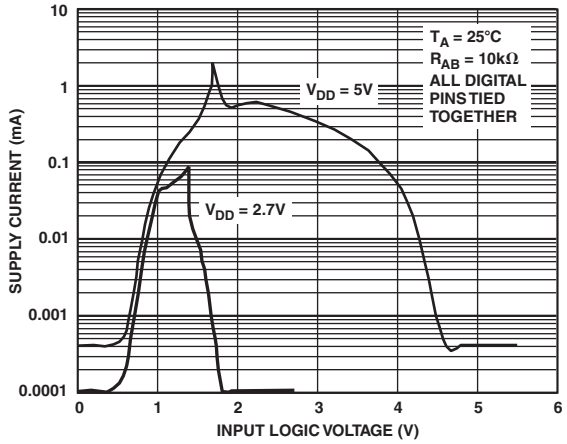
TPC 8. R_{INL} Oversupply Voltage



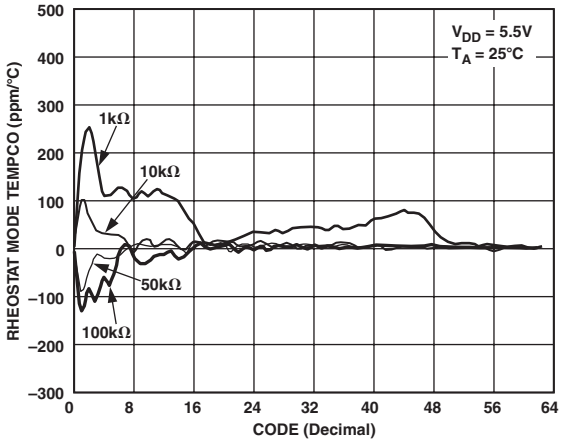
TPC 11. Supply Current vs. Temperature



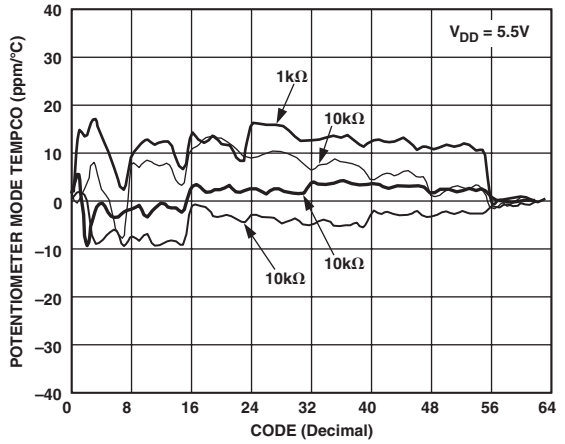
TPC 9. Full-Scale Error



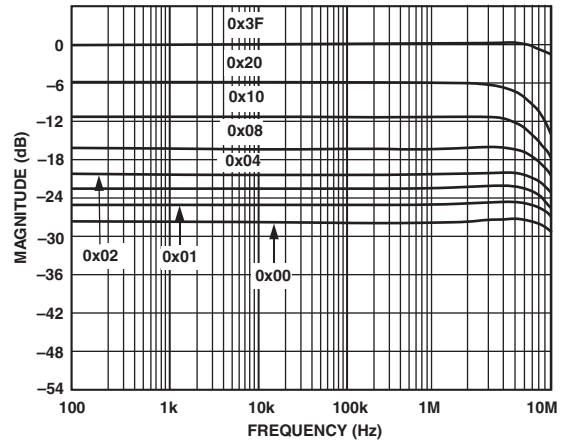
TPC 12. Supply Current vs. Digital Input Voltage



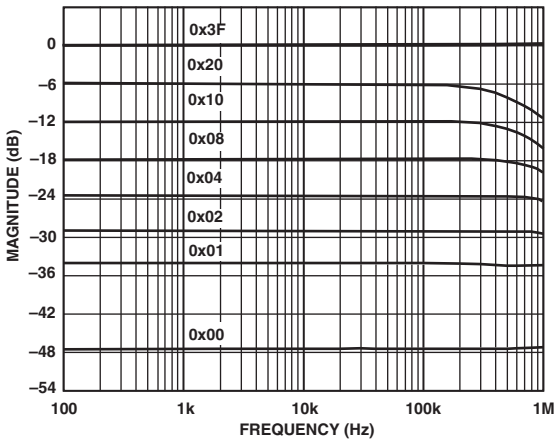
TPC 13. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code



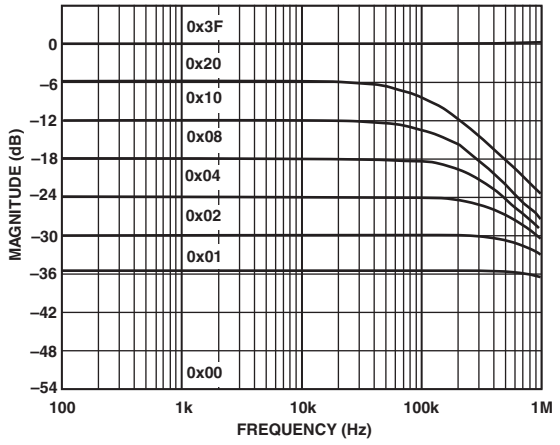
TPC 14. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code



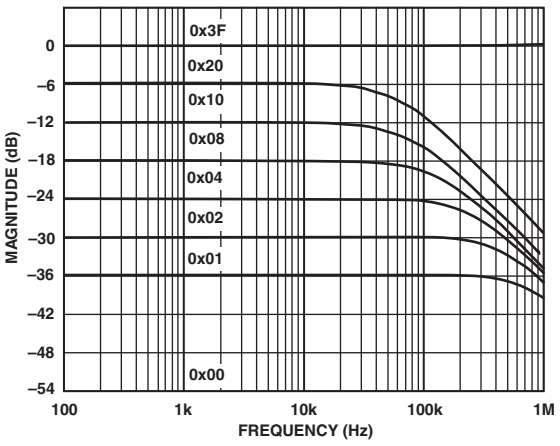
TPC 15. Gain vs. Frequency vs. Code, R_{AB} = 1 kΩ



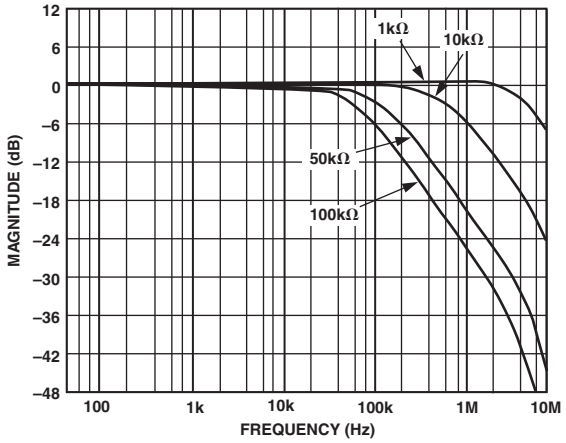
TPC 16. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ



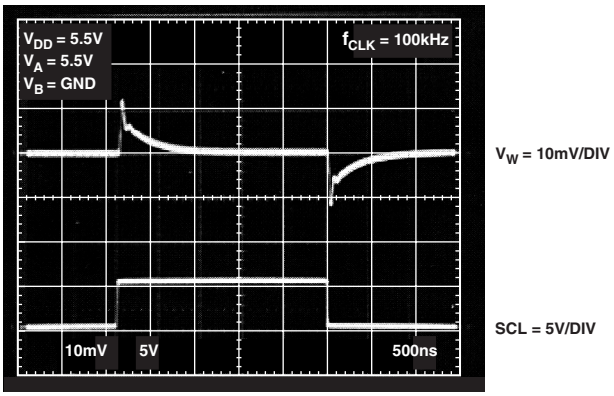
TPC 17. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ



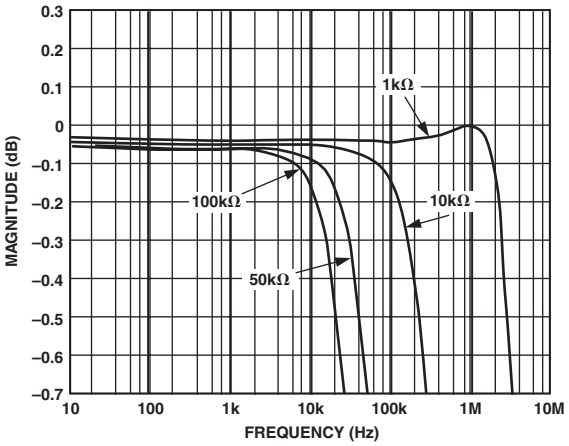
TPC 18. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ



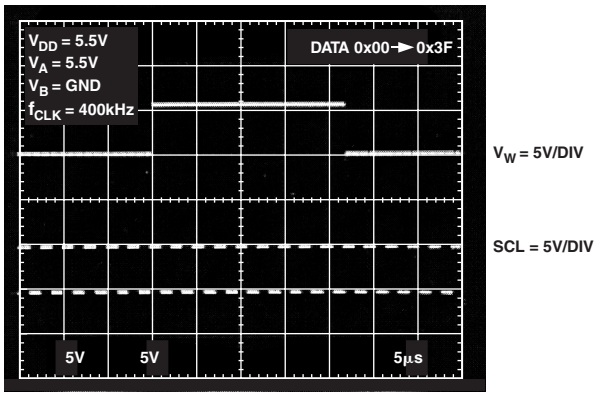
TPC 19. –3 dB Bandwidth



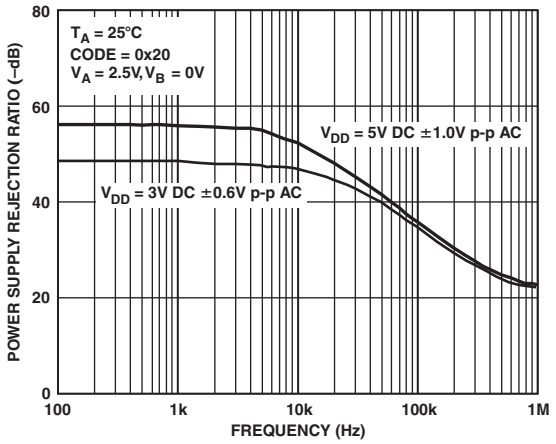
TPC 22. Digital Feedthrough vs. Time



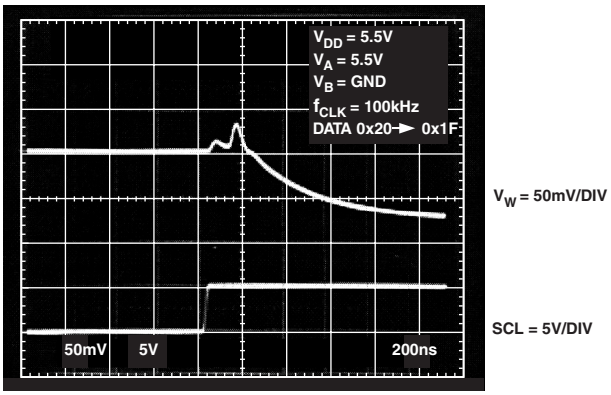
TPC 20. Normalized Gain Flatness vs. Frequency



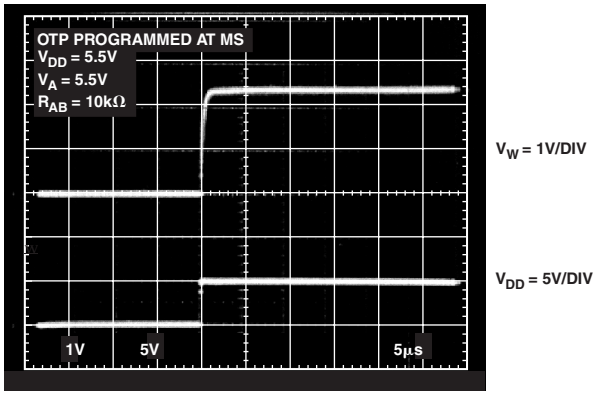
TPC 23. Large Settling Time



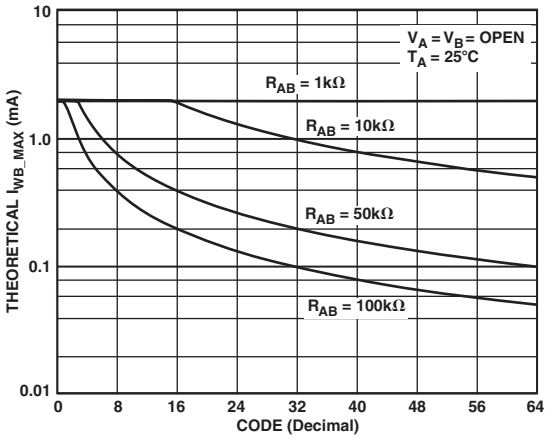
TPC 21. PSRR vs. Frequency



TPC 24. Midscale Glitch Energy



TPC 25. Power-Up Settling Time after Fuses Blown



TPC 26. I_{WB_MAX} vs. Code

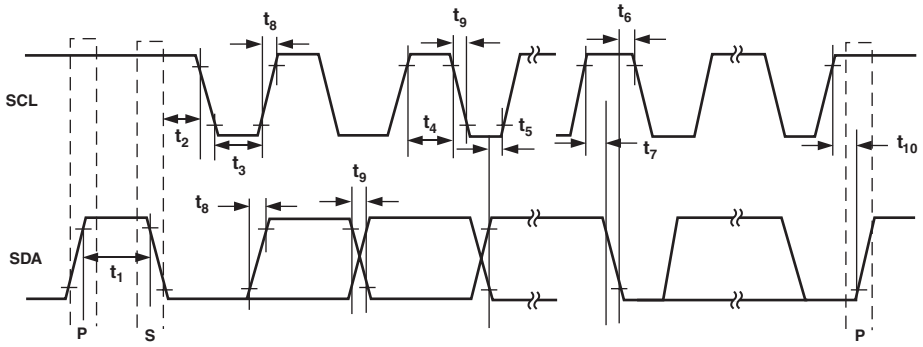


Figure 1. Interface Timing Diagram

Table I. SDA Write Mode Bit Format

S	0	1	0	1	1	0	AD0	0	A	T	X	X	X	X	X	X	X	A	X	X	D5	D4	D3	D2	D1	D0	A	P
	SLAVE ADDRESS BYTE									INSTRUCTION BYTE									DATA BYTE									

Table II. SDA Read Mode Bit Format

S	0	1	0	1	1	0	AD0	1	A	E1	E0	D5	D4	D3	D2	D1	D0	A	P
	SLAVE ADDRESS BYTE									DATA BYTE									

SDA BIT DEFINITIONS AND DESCRIPTIONS

S = Start Condition.

P = Stop Condition.

A = Acknowledge.

X = Don't Care.

T = OTP Programming Bit. Logic 1 programs wiper position permanently.

D5, D4, D3, D2, D1, D0 = Data Bits.

E1, E0 = OTP Validation Bits.

0, 0 = Ready to Program.

0, 1 = Test Fuse not Blown Successfully. (Check Setup.)

1, 0 = Fatal Error. Retry.

1, 1 = Programmed Successfully. No further adjustments possible.

AD0 = I^2C Device Address Bit. Allows maximum of two AD5273s to be addressed.

THEORY OF OPERATION

The AD5273 is a one-time-programmable (OTP), set-and-forget, 6-bit digital potentiometer. It comprises six data fuses, which control the address decoder for programming the RDAC, one user mode test fuse for checking setup error, and one programming lock fuse for disabling any further programming once the data fuses are programmed correctly.

One-Time-Programming (OTP)

The AD5273 has an internal power-on preset that places the wiper in the midscale during power-on. After the wiper is adjusted to the desired position, the wiper setting can be permanently programmed by setting the T bit, MSB of the instruction byte, to 1 along with the proper coding. Refer to Table I.

The one-time program control circuit has two validation bits, E1 and E0, that can be read back in the read mode for checking the programming status. Table III shows the validation status.

Table III. Validation Status

E1	E0	Status
0	0	Ready for Programming.
0	1	Test Fuse Not Blown Successfully (for Setup Checking).
1	0	Fatal Error. Some fuses are not blown. Retry.
1	1	Successful. No further programming is possible.

The detailed programming sequence is explained further as follows. When the OTP T bit is set, the internal clock is enabled. The program will attempt to blow a test fuse. The operation stops if this fuse is not blown successfully. The validation bits, E1 and E0, show 01, and the users should check the setup. If the test fuse is blown successfully, the data fuses will be programmed next. The six data fuses will be programmed in six clock cycles. The output of the fuses is compared with the code stored in the DAC register. If they do not match, E1 and E0 = 10 is issued as a fatal error and the operation stops. Users may retry with the same code. If the output and the stored code match, the programming lock fuse will be blown so that no further programming is possible. In the meantime, E1 and E0 will issue 11, indicating the lock fuse is blown successfully. All the fuse latches are enabled at power-on from this point on. Figure 2 shows a detailed functional block diagram.

DETERMINING THE VARIABLE RESISTANCE AND VOLTAGE*

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The final two or three digits of the part number determine the nominal resistance value, e.g., 1 kΩ = 1, 10 kΩ = 10, 50 kΩ = 50, and 100 kΩ = 100. The nominal resistance (R_{AB}) of the RDAC has 64 contact points accessed by the wiper terminal, plus the B terminal contact. The 6-bit data in the RDAC latch is decoded to select one of the 64 possible settings. Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Since there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between terminals W and B. The second connection is the first tap point and corresponds to 219 Ω (R_{WB} = R_{AB}/63 + R_W = 159 + 60) for data 0x01. The third connection is the next tap point, representing 378 Ω (159 × 2 + 60) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10060 Ω [R_{AB} + R_W]. Figure 3 shows a simplified diagram of the equivalent RDAC circuit. The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{63} \times R_{AB} + R_W \quad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 6-bit RDAC register.

R_{AB} is the nominal end-to-end resistance.

R_W is the wiper resistance contributed by the on resistance of the internal switch.

Again, if R_{AB} is 10 kΩ and terminal A is opened, the following output resistance values R_{WB} will be set for the following RDAC latch codes:

D (Dec)	R_{WB} (Ω)	Output State
63	10060	Full-Scale (R_{AB} + R_W)
32	5139	Midscale
1	219	1 LSB
0	60	Zero-Scale (Wiper Contact Resistance)

*Applies to potentiometer mode only.

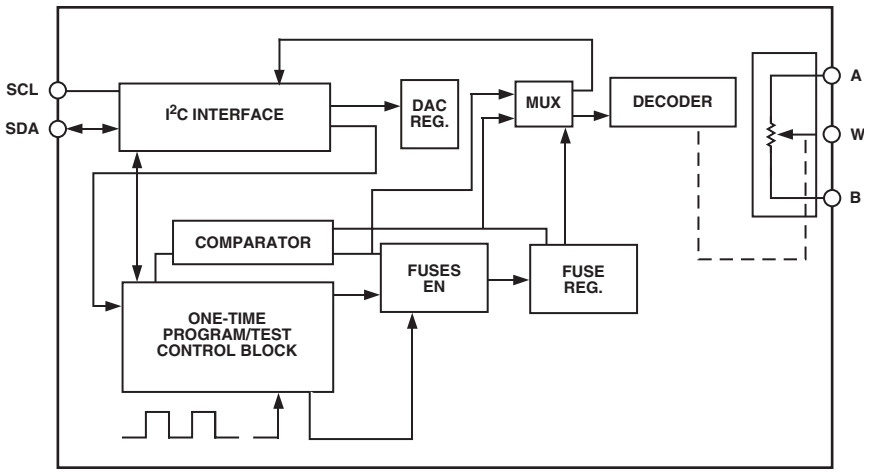


Figure 2. Detailed Functional Block Diagram

Note that in the zero-scale condition, a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. When these terminals are used, terminal B can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{63 - D}{63} \times R_{AB} + R_W \quad (2)$$

For R_{AB} equals 10 kΩ and terminal B is opened, the following output resistance R_{WA} will be set for the following RDAC latch codes:

D (Dec)	R_{WA} (Ω)	Output State
63	60	Full-Scale
32	4980	Midscale
1	9901	1 LSB
0	10060	Zero-Scale

The typical distribution of the nominal resistance R_{AB} from channel to channel matches within ±1%. Device-to-device matching is process lot dependent and can have a ±30% variation.

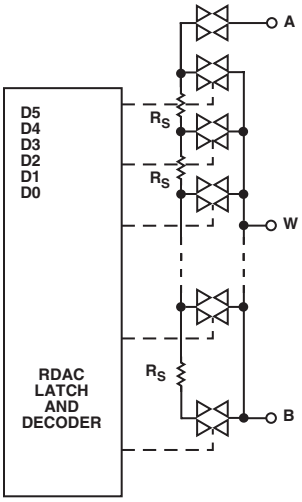


Figure 3. Equivalent RDAC Circuit

Voltage Output Operation

Similar to the D/A converter, the digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A to be proportional to the input voltage at A–B. Unlike the polarity of V_{DD}, which must be positive, voltage across A–B, W–A, and W–B can be at either polarity as long as the voltage across them is ≤ $|V_{DD}|$.

If ignoring the effect of the wiper resistance for approximation, connecting terminal A to 5 V and terminal B to ground produces an output voltage at the wiper-to-B starting at 0 V up to 5 V. Each LSB of voltage is equal to the voltage applied across terminal A–B, divided by the 63 position of the potentiometer divider as

$$V_W(D) = \frac{D}{63} V_A \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation overtemperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not on the absolute values. Therefore, the temperature drift reduces to 10 ppm/°C.

ESD PROTECTION

All digital inputs are protected with a series input resistor and the parallel Zener ESD structures shown in Figures 4a and 4b. This applies to digital input pins SDA and SCL.

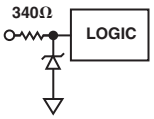


Figure 4a. ESD Protection of Digital Pins

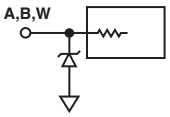


Figure 4b. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The V_{DD} of AD5273 defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} will be clamped by the internal forward-biased diodes (see Figure 5).

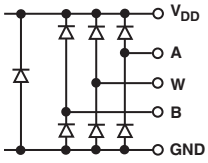


Figure 5. Maximum Terminal Voltages Set by V_{DD}

POWER-UP SEQUENCE

Since there are ESD protection diodes that limit the voltage compliance at terminals A, B, and W (Figure 5), it is important to power V_{DD} first before applying any voltage to terminals A, B, and W. Otherwise, the diode will be forward-biased such that V_{DD} will be powered unintentionally and may affect the rest of the users' circuits. The ideal power-up sequence is GND, V_{DD}, digital inputs, and $V_{A/B/W}$. The order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}.

POWER SUPPLY CONSIDERATIONS

AD5273 employs fuse link technology, which requires an adequate current density to blow the internal fuses to achieve a given setting. As a result, the power supply, either an on-board linear regulator or rack-mount power supply, must be rated at 5 V with less than ±5% tolerance. The supply should be able to handle 100 mA of transient current and lasts about 400 ms during the one-time programming. A low ESR 1 μF to 10 μF tantalum or electrolytic

bypass capacitor should be applied to V_{DD} to minimize the transient disturbances during the programming as shown in Figure 6a. Once the programming is completed, the supply voltage can be reduced to 2.7 V with a supply current that reduces to less than 1 μA.

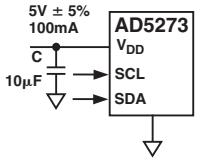


Figure 6a. OTP Power Supply Requirement

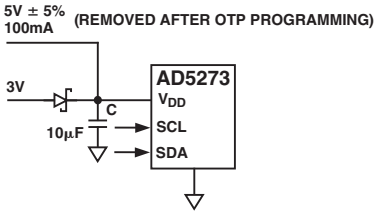


Figure 6b. External Power Supply Applied for Programming

For users who have an on-board 3 V supply for portable applications, a separate 5 V supply must be applied one time in the factory for programming, and a low VF Schottky diode should be designed with the AD5273 to isolate the supply voltages. Once the programming is done, the 5 V supply can be removed with V_{DD} maintained at 2.7 V for minimum operation. Figure 6b shows one such implementation.

CONTROLLING THE AD5273

There are two ways of controlling the AD5273. Users can either program the device with computer software or with external I^2C controllers.

Software Programming

Due to the advantage of the one-time-programmable feature, most systems using the AD5273 will program the devices in the factory before shipping them to the end users. As a result, ADI offers device programming software that can be implemented in the factory on computers running Windows NT, 2000, and XP platforms. The software, which can be downloaded from the AD5273 product folder at www.analog.com, is an executable file that does not require any programming languages or user programming skills. Figure 7 shows the software interface.

Write

The AD5273 starts at midscale after power-up prior to any OTP programming. To increment or decrement the resistance, the user may simply move the scrollbar on the left. Once the desired setting is found, the user can press the Program Permanent button to lock the setting permanently. To write any specific values, the user should use the bit pattern control in the upper screen and press the Run button. The format of writing data to the device is shown in Table I. Once the desired setting is found, the user can turn the T bit to 1 and press the Run button to program the setting permanently.

Read

To read the validation bits and data out from the device, the user can simply press the Read button. The user can also set the bit pattern in the upper screen and press the Run button. The format of reading data out from the device is shown in Table II.

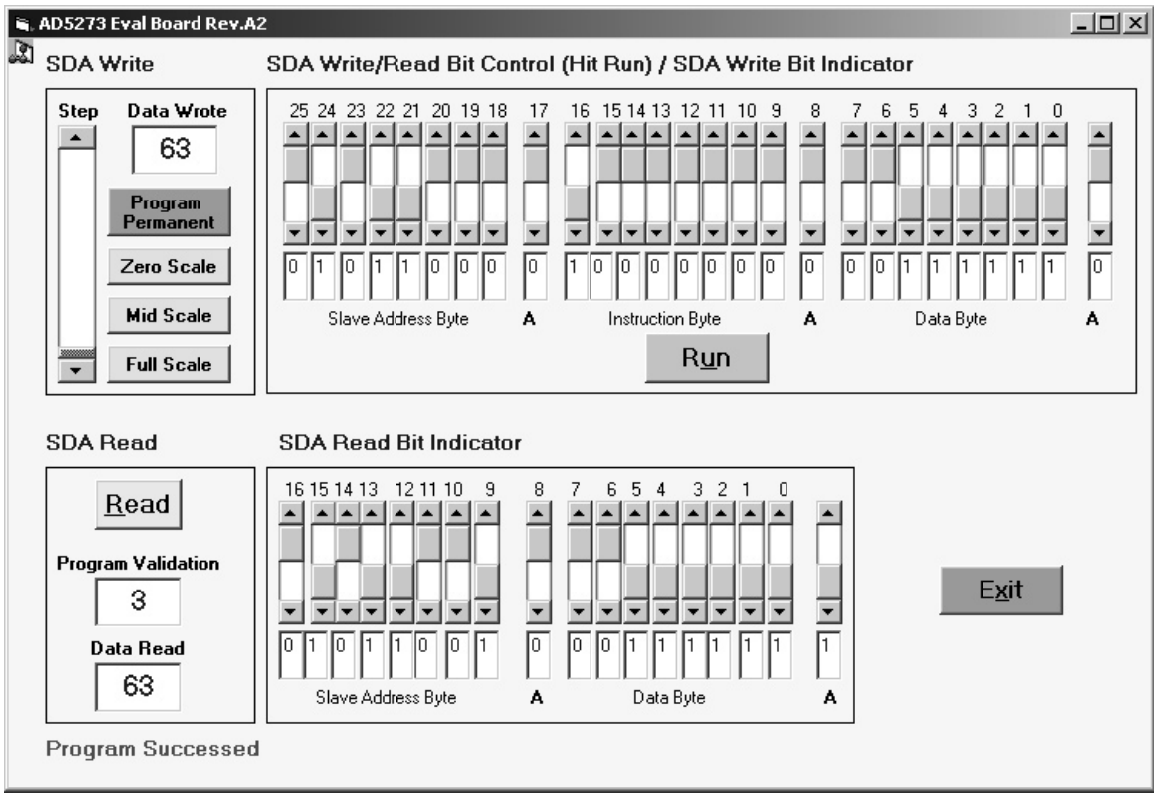


Figure 7. Computer Software

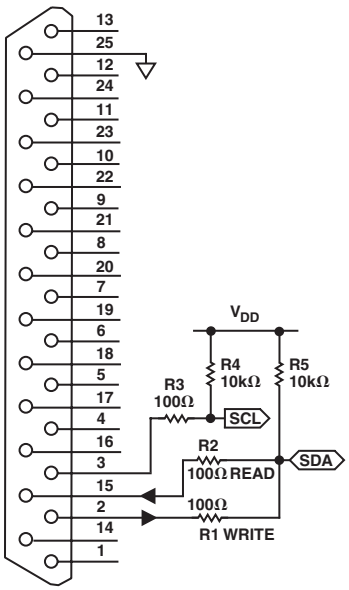


Figure 8. Parallel Port Connection. Pin 2 = SDA_write, Pin 3 = SCL, Pin 15 = SDA_read, and Pin 25 = DGND.

In both read and write operations, the program generates the I^2C digital signals through the parallel port LPT1 Pins 2, 3, 15, and 25 for SDA_write, SCL, SDA_read, and DGND, respectively, to control the device (see Figure 8).

To apply the device programming software in the factory, users may lay out the AD5273 SCL and SDA pads on the PCB such that the programming signals can be communicated to and from the parallel port. Figure 9 shows a recommended AD5273 PCB layout into which pogo pins can be inserted for factory programming. 100 Ω resistors should also be put in series to the SCL and SDA pins to prevent damaging the PC parallel port. Pull-up resistors on SCL and SDA are also required.

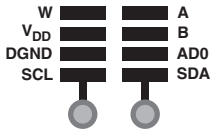


Figure 9. Recommended AD5273 PCB Layout. The SCL and SDA pads allow pogo pins to be inserted so that signals can communicate through the parallel port for programming. Refer to Figure 8.

For users who do not use the software solution, the AD5273 can be controlled via an I^2C compatible serial bus and is connected to this bus as a slave device. Referring to Figures 10a, 10b, and 11, the 2-wire I^2C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when SDA goes from high to low while SCL is high (Figure 10a). The following byte is the slave address byte, which consists of the six MSBs as slave address defined as 010110. The next bit is AD0; it is an I^2C device address bit. Depending on the states of their AD0 bits, two AD5273s can be addressed on the same bus (see Figure 12). The last LSB is the R/$\overline{W}$ bit, which determines whether data will be read from or written to the slave device.

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register.
2. A write operation contains one more instruction byte than the read operation. The instruction byte in the write mode follows the slave address byte. The MSB of the instruction byte labeled T is the one-time programming bit. After acknowledging the instruction byte, the last byte in the write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 10a).
3. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (slight difference with the write mode, there are eight data bits followed by a no acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL as shown in Figure 11.
4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In the write mode, the master will pull the SDA line high during the 10th clock pulse to establish a stop condition (see Figures 10a and 10b). In the read mode, the master will issue a no acknowledge for the ninth clock pulse, i.e., the SDA line remains high. The master will then bring the SDA line low before the 10th clock pulse, which goes high to establish a stop condition (see Figure 11).

A repeated write function gives the user flexibility to update the RDAC output a number of times, except after permanent programming, after addressing and instructing the part only once. During the write cycle, each data byte will update the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output will update after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte will update the output of the selected slave device. If different instructions are needed, the write mode has to be started again with a new slave address, instruction, and data bytes. Similarly, a repeated read function of the RDAC is also allowed.

I²C Controller Programming

Write Bit Pattern Illustrations

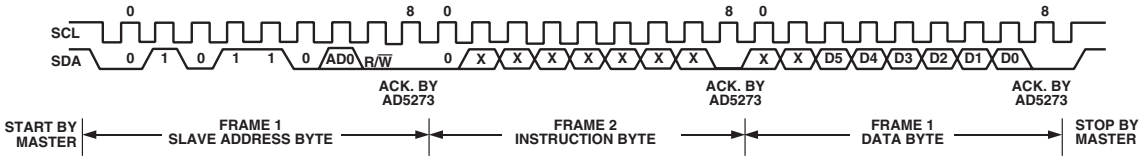


Figure 10a. Writing to the RDAC Register

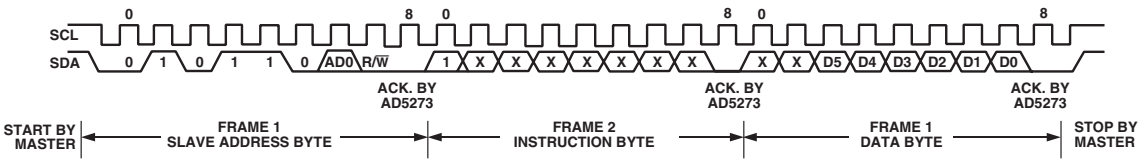


Figure 10b. Activating One-Time Programming

Read Bit Pattern Illustration

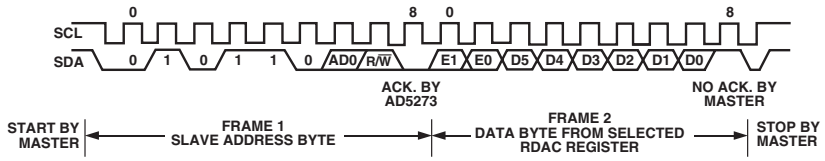


Figure 11. Reading Data from the RDAC Register

CONTROLLING TWO DEVICES ON ONE BUS

Figure 12 shows two AD5273 devices on the same serial bus. Each has a different slave address since the state of each AD0 pin is different. This allows each device to operate independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C compatible interface.

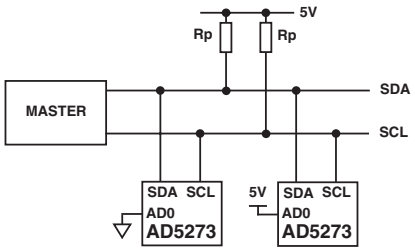


Figure 12. Two AD5273 Devices on One Bus

APPLICATIONS

Programmable Voltage Reference

For voltage divider mode operation, as shown in Figure 13, it is common to buffer the output of the digital potentiometer unless the load is much larger than R_{WB}. Not only does the buffer serve the purpose of impedance conversion, it also allows a heavier load to be driven.

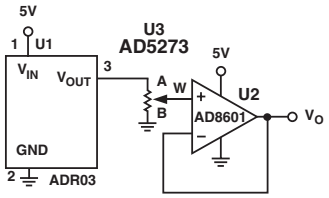


Figure 13. Programmable Voltage Reference

Programmable Voltage Source with Boosted Output

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 14).

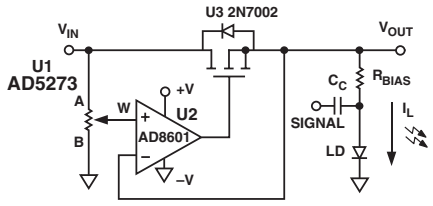


Figure 14. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-Ch FET N_1. N_1 power handling must be adequate to dissipate $(V_{IN} - V_{OUT}) \times I_L$ power. This circuit can source a maximum of 100 mA with a 5 V supply. For precision applications, a voltage reference, such as the ADR421, ADR03, or ADR370, can be applied at the A terminal of the digital potentiometer.

Programmable Current Source

A programmable current source can be implemented with the circuit shown in Figure 15. The load current is simply the voltage across terminals B-to-W of the AD5273 divided by R_S. Notice that at zero-scale, the A terminal of the AD5273 will be at –2.048 V, which makes the wiper voltage clamped at ground potential. Dependent on the load, Equation 5 is therefore valid only at certain codes. For example, when the compliance voltage V_L equals half of the V_{REF}, the current can be programmed from midscale to full-scale of the AD5273.

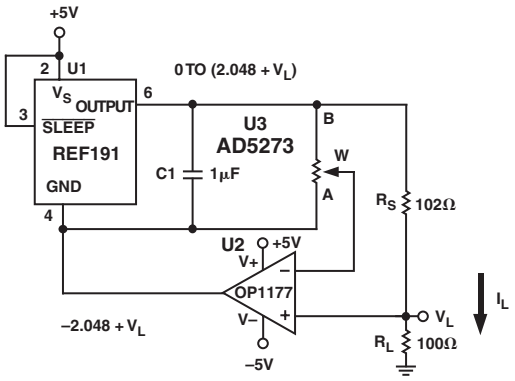


Figure 15. Programmable Current Source

$$I_L = \frac{(V_{REF} \times D)/64}{R_S} \Big| 32 \le D \le 63 \quad (5)$$

Gain Control Compensation

As shown in Figure 16, the digital potentiometers are commonly used in gain controls or sensor transimpedance amplifier signal conditioning applications.

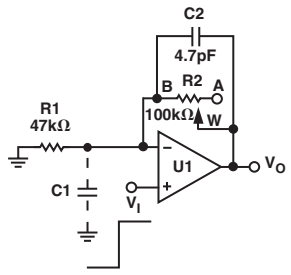


Figure 16. Typical Noninverting Gain Amplifier

In both applications, one of the digital potentiometer terminals is connected to the op amp inverting node with finite terminal capacitance C1. It introduces a zero for the 1 β_o term with 20 dB/dec, whereas a typical op amp GBP has –20 dB/dec characteristics. A large R2 and finite C1 can cause this zero's frequency to fall well below the crossover frequency. Thus the rate of closure becomes 40 dB/dec and the system has 0° phase margin at the crossover frequency. The output may ring, or in the worst case, oscillate when the input is a step function. Similarly, it is also likely to ring when switching between two gain values because this is equivalent to a step change at the input. To reduce the effect of C1, users should also configure B or A rather than W terminal at the inverting node.

Depending on the op amp GBP, reducing the feedback resistor may extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor C2 to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2. This is not an option because of the variation of R2. As a result, one may use the relationship above and scale C2 as if R2 were at its maximum value. Doing so may overcompensate by slowing down the settling time when R2 is set at low values. As a result, C2 should be found empirically for a given application. In general, C2 in the range of a few picofarads to no more than a few tenths of a picofarad is adequate for the compensation.

There is also a W terminal capacitance connected to the output (not shown); its effect on stability is less significant so that the compensation may not be necessary unless the op amp is driving a large capacitive load.

Programmable Low-Pass Filter

In A/D conversion applications, it is common to include an anti-aliasing filter to band-limit the sampling signal. To minimize various system redesigns, users can use two 1 kΩ AD5273s to construct a generic second order Sallen Key low-pass filter. Since the AD5273 is a single-supply device, the input must be dc offset when an ac signal is applied to avoid clipping at ground. This is illustrated in Figure 17. The design equations are

$$\frac{V_O}{V_I} = \frac{\omega_O^{\,2}}{S^2 + \frac{\omega_O}{Q}S + \omega_O^{\,2}} \quad (6)$$

$$\omega_o = \sqrt{\frac{1}{R1R2C1C2}} \quad (7)$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \quad (8)$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where $Q = 0.707$, let $C1$ be twice the size of $C2$ and let $R1 = R2$. As a result, $R1$ and $R2$ can be adjusted to the same setting to achieve the desirable bandwidth.

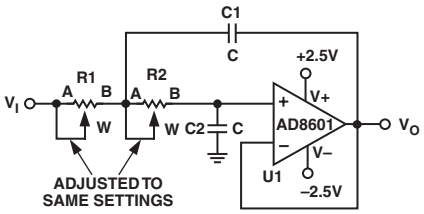


Figure 17. Sallen Key Low-Pass Filter

Level Shift for Different Voltages Operation

When users need to interface a 2.5 V controller with the AD5273, a proper voltage level shift must be employed so that the digital potentiometer can be read from or written to the controller; Figure 18 shows one of the implementations. M1 and M2 should be low threshold N-Ch power MOSFETs, such as the FDV301N.

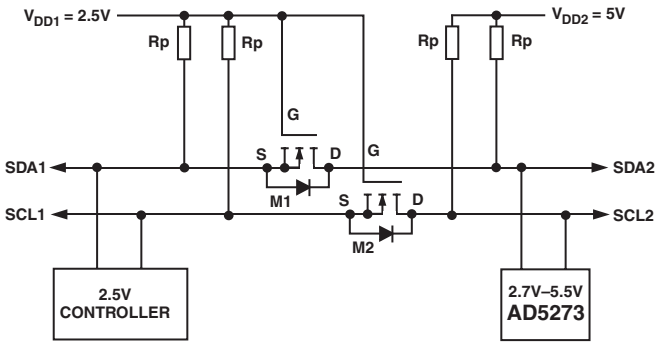


Figure 18. Level Shift for Different Voltage Operation

Resistance Scaling

The AD5273 offers 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ nominal resistances. For users who need to optimize the resolution with an arbitrary full-range resistance, the following techniques can be the solutions. Applicable only to the voltage divider mode, by paralleling a discrete resistor as shown in Figure 19, a proportionately lower voltage appears at terminal A–B. This translates into a finer degree of precision because the step size at terminal W will be smaller. The voltage can be found as

$$V_W(D) = \frac{(R_{AB} \,||\, R2)}{R3 + R_{AB} \,||\, R2} \times \frac{D}{256} \times V_{DD} \quad (9)$$

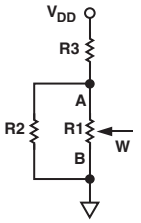


Figure 19. Lowering the Nominal Resistance

Figure 19 shows that the digital potentiometer changes steps linearly. On the other hand, log taper adjustment is usually preferred in applications like volume control. Figure 20 shows another way of resistance scaling. In this circuit, the smaller the R2 with respect to R_{AB}, the more it behaves like the pseudo log taper characteristic. The wiper voltage is simply

$$V_W(D) = \frac{(R_{WB}(D) \,||\, R2)}{R_{WA}(D) + R_{WB}(D) \,||\, R2} \times V_I \quad (10)$$

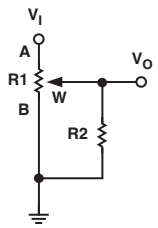


Figure 20. Resistor Scaling with Log Adjustment Characteristics

Resolution Enhancement

Borrowing from ADI's patented RDAC segmentation technique, users can configure three AD5273s to double the resolution (see Figure 21). First, U3 must be paralleled with a discrete resistor R_P that is chosen to be equal to a step resistance ($R_P = R_{AB}/64$). Adjusting U1 and U2 together forms the coarse 6-bit adjustment, and adjusting U3 alone forms the finer 6-bit adjustment. As a result, the effective resolution becomes 12-bit.

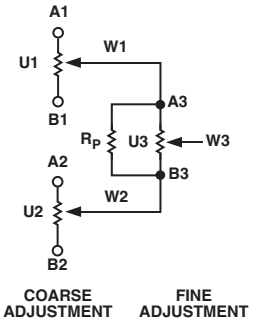


Figure 21. Double the Resolution in Rheostat Mode Operation

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the digital potentiometers. Configured as a potentiometer divider, the –3 dB bandwidth of the AD5273 (1 kΩ resistor) measures 6 MHz at half scale. TPCs 15 to 18 provide the large signal BODE plot characteristics of the four available resistor versions 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. Figure 22 shows a parasitic simulation model. The code following Figure 22 provides a macro model net list for the 1 kΩ device.

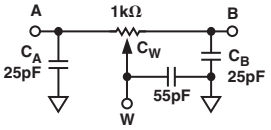


Figure 22. Circuit Simulation Model for RDAC = 1 kΩ

Macro Model Net List for RDAC

```
.PARAM D = 63, RDAC = 1E3
*
.SUBCKT DPOT (A,W,B)
*
CA      A      0      25E-12
RWA     A      W      {(1-D/63)*RDAC+60}
CW      W      0      55E-12
RWB     W      B      {D/63*RDAC+60}
CB      B      0      25E-12
*
.ENDS DPOT
```

EVALUATION BOARD

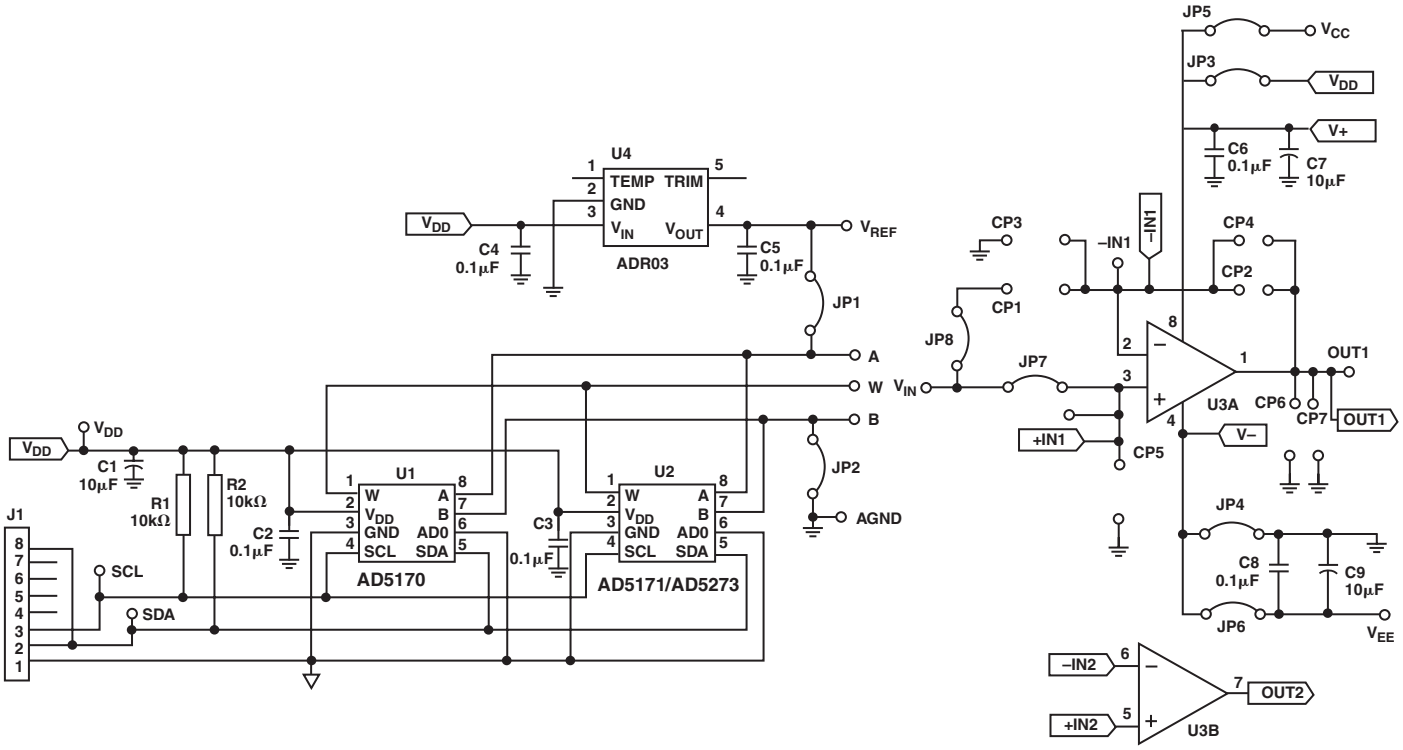


Figure 23. Evaluation Board Schematic

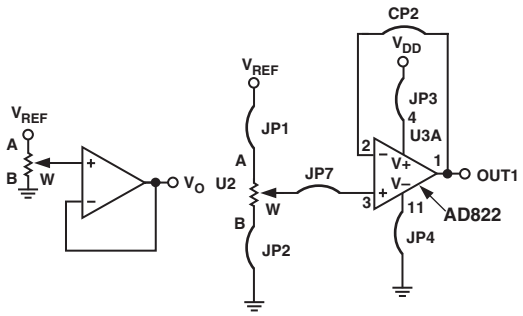


Figure 24. One of the Possible Configurations: Programmable Voltage Reference

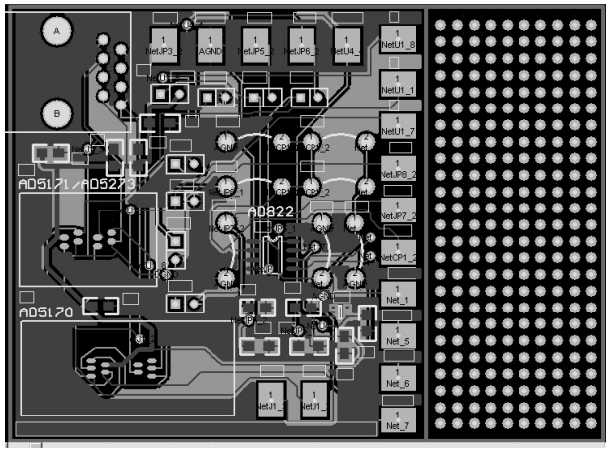


Figure 25. Evaluation Board

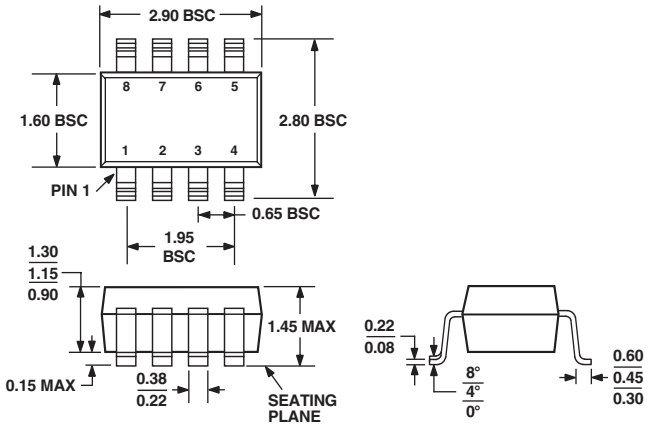
Digital Potentiometer Family Selection Guide*

Part No.	No. of VRs per Package	Terminal Voltage Range (V)	Interface Data Control	Nominal Resistance (kΩ)	Resolution (No. of Wiper Positions)	Power Supply Current (I_{DD}) (μA)	Packages	Comments
AD5201	1	±3, +5.5	3-wire	10, 50	33	40	MSOP-10	Full AC Specs, Dual Supply, Power-On Reset, Low Cost
AD5220	1	5.5	UP/DOWN	10, 50, 100	128	40	PDIP, SOIC-8, MSOP-8	No Rollover, Power-On Reset
AD7376	1	±15, +28	3-wire	10, 50, 100, 1000	128	100	PDIP-14, SOIC-16, TSSOP-14	Single +28 V or Dual ±15 V Supply Operation
AD5200	1	±3, +5.5	3-wire	10, 50	256	40	MSOP-10	Full AC Specs, Dual Supply, Power-On Reset
AD8400	1	5.5	3-wire	1, 10, 50, 100	256	5	SOIC-8	Full AC Specs
AD5260	1	±5, +15	3-wire	20, 50, 200	256	60	TSSOP-14	+5 V to +15 V or ±5 V Operation, TC < 50 ppm/°C
AD5280	1	±5, +15	2-wire	20, 50, 200	256	60	TSSOP-14	+5 V to +15 V or ±5 V Operation, TC < 50 ppm/°C
AD5241	1	±3, +5.5	2-wire	10, 100, 1000	256	50	SOIC-14, TSSOP-14	I^2C Compatible, TC < 50 ppm/°C
AD5231	1	±2.75, +5.5	3-wire	10, 50, 100	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5222	2	±3, +5.5	UP/DOWN	10, 50, 100, 1000	128	80	SOIC-14, TSSOP-14	No Rollover, Stereo, Power-On Reset, TC < 50 ppm/°C
AD8402	2	5.5	3-wire	1, 10, 50, 100	256	5	PDIP, SOIC-14, TSSOP-14	Full AC Specs, nA Shutdown Current
AD5207	2	±3, +5.5	3-wire	10, 50, 100	256	40	TSSOP-14	Full AC Specs, Dual Supply, Power-On Reset, SDO
AD5232	2	±2.75, +5.5	3-wire	10, 50, 100	256	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5235	2	±2.75, +5.5	3-wire	25, 250	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, TC < 50 ppm/°C
AD5242	2	±3, +5.5	2-wire	10, 100, 1000	256	50	SOIC-16, TSSOP-16	I^2C Compatible, TC < 50 ppm/°C
AD5262	2	±5, +15	3-wire	20, 50, 200	256	60	TSSOP-16	+5 V to +15 V or ±5 V Operation, TC < 50 ppm/°C
AD5282	2	±5, +15	3-wire	20, 50, 200	256	60	TSSOP-16	+5 V to +15 V or ±5 V Operation, TC < 50 ppm/°C
AD5203	4	5.5	3-wire	10, 100	64	5	PDIP, SOIC-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5233	4	±2.75, +5.5	3-wire	10, 50, 100	64	20	TSSOP-24	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5204	4	±3, +5.5	3-wire	10, 50, 100	256	60	PDIP, SOIC-24, TSSOP-24	Full AC Specs, Dual Supply, Power-On Reset
AD8403	4	5.5	3-wire	1, 10, 50, 100	256	5	PDIP, SOIC-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5206	6	±3, +5.5	3-wire	10, 50, 100	256	60	PDIP, SOIC-24, TSSOP-24	Full AC Specs, Dual Supply, Power-On Reset

*For the most current information on digital potentiometers, check the website at: www.analog.com/digitalpotentiometers.

OUTLINE DIMENSIONS

8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178BA

C03224–0–6/03(0)

Revision History

Location	Page
6/03—Data Sheet changed from REV. 0 to REV. A.	
Change to SPECIFICATIONS	2
Change to POWER SUPPLY CONSIDERATIONS section	12
Updated OUTLINE DIMENSIONS	20