

***KVR533D2D8F4/1G***  
***1GB 128M x 72-Bit PC2-4200***  
***CL4 ECC 240-Pin FBDIMM***

## **Description:**

This document describes ValueRAM's 1GB (128M x 72-bit) PC2-4200 CL4 SDRAM (Synchronous DRAM) "fully buffered" ECC "dual rank" memory module. This module is based on eighteen 64M x 8-bit 533MHz DDR2 FBGA components. The module also includes an AMB device (Advanced Memory Buffer). The electrical and mechanical specifications are as follows:

## **Feature:**

- FBDIMM Module: 240-pin
- JEDEC Standard: R/C B
- Memory Organization: 2 rank of x8 devices
- DDR2 DRAM Interface: SSTL\_18
- DDR2 Speed Grade: 533 Mbps
- CAS Latency: 4-4-4
- Module Bandwidth: 4.2 GB/s
- FBDIMM Channel Peak Throughput: 6.4 GB/s
- DRAM: VDD = VDDQ = 1.8V
- AMB: VCC = VCCFBD = 1.5V
- EEPROM: VDDSPD = 3.3V (typical)
- Heat Spreader: AMB-only heat sink
- PCB Height: 30.35mm, double-side
- RoHS Compliant

## DDR2 240-pin FBDIMM Pinout:

| Pin # | Front Side      | Pin # | Back Side       | Pin # | Front Side      | Pin # | Back Side       | Pin # | Front Side      | Pin # | Back Side       | Pin # | Front Side      | Pin # | Back Side       |
|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|
| 1     | V <sub>DD</sub> | 121   | V <sub>DD</sub> | 31    | PN3             | 151   | SN3             | 61    | PN9             | 181   | SN9             | 91    | PS9             | 211   | SS9             |
| 2     | V <sub>DD</sub> | 122   | V <sub>DD</sub> | 32    | PN3             | 152   | SN3             | 62    | V <sub>SS</sub> | 182   | V <sub>SS</sub> | 92    | V <sub>SS</sub> | 212   | V <sub>SS</sub> |
| 3     | V <sub>DD</sub> | 123   | V <sub>DD</sub> | 33    | V <sub>SS</sub> | 153   | V <sub>SS</sub> | 63    | PN10            | 183   | SN10            | 93    | PS5             | 213   | SS5             |
| 4     | V <sub>SS</sub> | 124   | V <sub>SS</sub> | 34    | PN4             | 154   | SN4             | 64    | PN10            | 184   | SN10            | 94    | PS5             | 214   | SS5             |
| 5     | V <sub>DD</sub> | 125   | V <sub>DD</sub> | 35    | PN4             | 155   | SN4             | 65    | V <sub>SS</sub> | 185   | V <sub>SS</sub> | 95    | V <sub>SS</sub> | 215   | V <sub>SS</sub> |
| 6     | V <sub>DD</sub> | 126   | V <sub>DD</sub> | 36    | V <sub>SS</sub> | 156   | V <sub>SS</sub> | 66    | PN11            | 186   | SN11            | 96    | PS6             | 216   | SS6             |
| 7     | V <sub>DD</sub> | 127   | V <sub>DD</sub> | 37    | PN5             | 157   | SN5             | 67    | PN11            | 187   | SN11            | 97    | PS6             | 217   | SS6             |
| 8     | V <sub>SS</sub> | 128   | V <sub>SS</sub> | 38    | PN5             | 158   | SN5             | 68    | V <sub>SS</sub> | 188   | V <sub>SS</sub> | 98    | V <sub>SS</sub> | 218   | V <sub>SS</sub> |
| 9     | V <sub>CC</sub> | 129   | V <sub>CC</sub> | 39    | V <sub>SS</sub> | 159   | V <sub>SS</sub> | KEY   |                 |       |                 | 99    | PS7             | 219   | SS7             |
| 10    | V <sub>CC</sub> | 130   | V <sub>CC</sub> | 40    | PN13            | 160   | SN13            | 69    | V <sub>SS</sub> | 189   | V <sub>SS</sub> | 100   | PS7             | 220   | SS7             |
| 11    | V <sub>SS</sub> | 131   | V <sub>SS</sub> | 41    | PN13            | 161   | SN13            | 70    | PS0             | 190   | SS0             | 101   | V <sub>SS</sub> | 221   | V <sub>SS</sub> |
| 12    | V <sub>CC</sub> | 132   | V <sub>CC</sub> | 42    | V <sub>SS</sub> | 162   | V <sub>SS</sub> | 71    | PS0             | 191   | SS0             | 102   | PS8             | 222   | SS8             |
| 13    | V <sub>CC</sub> | 133   | V <sub>CC</sub> | 43    | V <sub>SS</sub> | 163   | V <sub>SS</sub> | 72    | V <sub>SS</sub> | 192   | V <sub>SS</sub> | 103   | PS8             | 223   | SS8             |
| 14    | V <sub>SS</sub> | 134   | V <sub>SS</sub> | 44    | RFU*            | 164   | RFU*            | 73    | PS1             | 193   | SS1             | 104   | V <sub>SS</sub> | 224   | V <sub>SS</sub> |
| 15    | V <sub>TT</sub> | 135   | V <sub>TT</sub> | 45    | RFU*            | 165   | RFU*            | 74    | PS1             | 194   | SS1             | 105   | RFU**           | 225   | RFU**           |
| 16    | VID1            | 136   | VID0            | 46    | V <sub>SS</sub> | 166   | V <sub>SS</sub> | 75    | V <sub>SS</sub> | 195   | V <sub>SS</sub> | 106   | RFU**           | 226   | RFU**           |
| 17    | RESET           | 137   | DNU/M_Test      | 47    | V <sub>SS</sub> | 167   | V <sub>SS</sub> | 76    | PS2             | 196   | SS2             | 107   | V <sub>SS</sub> | 227   | V <sub>SS</sub> |
| 18    | V <sub>SS</sub> | 138   | V <sub>SS</sub> | 48    | PN12            | 168   | SN12            | 77    | PS2             | 197   | SS2             | 108   | V <sub>DD</sub> | 228   | SCK             |
| 19    | RFU**           | 139   | RFU**           | 49    | PN12            | 169   | SN12            | 78    | V <sub>SS</sub> | 198   | V <sub>SS</sub> | 109   | V <sub>DD</sub> | 229   | SCK             |
| 20    | RFU**           | 140   | RFU**           | 50    | V <sub>SS</sub> | 170   | V <sub>SS</sub> | 79    | PS3             | 199   | SS3             | 110   | V <sub>SS</sub> | 230   | V <sub>SS</sub> |
| 21    | V <sub>SS</sub> | 141   | V <sub>SS</sub> | 51    | PN6             | 171   | SN6             | 80    | PS3             | 200   | SS3             | 111   | V <sub>DD</sub> | 231   | V <sub>DD</sub> |
| 22    | PN0             | 142   | SN0             | 52    | PN6             | 172   | SN6             | 81    | V <sub>SS</sub> | 201   | V <sub>SS</sub> | 112   | V <sub>DD</sub> | 232   | V <sub>DD</sub> |
| 23    | PN0             | 143   | SN0             | 53    | V <sub>SS</sub> | 173   | V <sub>SS</sub> | 82    | PS4             | 202   | SS4             | 113   | V <sub>DD</sub> | 233   | V <sub>DD</sub> |
| 24    | V <sub>SS</sub> | 144   | V <sub>SS</sub> | 54    | PN7             | 174   | SN7             | 83    | PS4             | 203   | SS4             | 114   | V <sub>SS</sub> | 234   | V <sub>SS</sub> |
| 25    | PN1             | 145   | SN1             | 55    | PN7             | 175   | SN7             | 84    | V <sub>SS</sub> | 204   | V <sub>SS</sub> | 115   | V <sub>DD</sub> | 235   | V <sub>DD</sub> |
| 26    | PN1             | 146   | SN1             | 56    | V <sub>SS</sub> | 176   | V <sub>SS</sub> | 85    | V <sub>SS</sub> | 205   | V <sub>SS</sub> | 116   | V <sub>DD</sub> | 236   | V <sub>DD</sub> |
| 27    | V <sub>SS</sub> | 147   | V <sub>SS</sub> | 57    | PN8             | 177   | SN8             | 86    | RFU*            | 206   | RFU*            | 117   | V <sub>TT</sub> | 237   | V <sub>TT</sub> |
| 28    | PN2             | 148   | SN2             | 58    | PN8             | 178   | SN8             | 87    | RFU*            | 207   | RFU*            | 118   | SA2             | 238   | VDDSPD          |
| 29    | PN2             | 149   | SN2             | 59    | V <sub>SS</sub> | 179   | V <sub>SS</sub> | 88    | V <sub>SS</sub> | 208   | V <sub>SS</sub> | 119   | SDA             | 239   | SA0             |
| 30    | V <sub>SS</sub> | 150   | V <sub>SS</sub> | 60    | PN9             | 180   | SN9             | 89    | V <sub>SS</sub> | 209   | V <sub>SS</sub> | 120   | SCL             | 240   | SA1             |
|       |                 |       |                 |       |                 |       |                 | 90    | PS9             | 210   | SS9             |       |                 |       |                 |

RFU = Reserved Future Use.

\* These pin positions are reserved for forwarded clocks to be used in future module implementations

\*\* These pin positions are reserved for future architecture flexibility

1) The following signals are CRC bits and thus appear out of the normal sequence: PN12/PN12, SN12/SN12, PN13/PN13, SN13/SN13, PS9/PS9, SS9/SS9

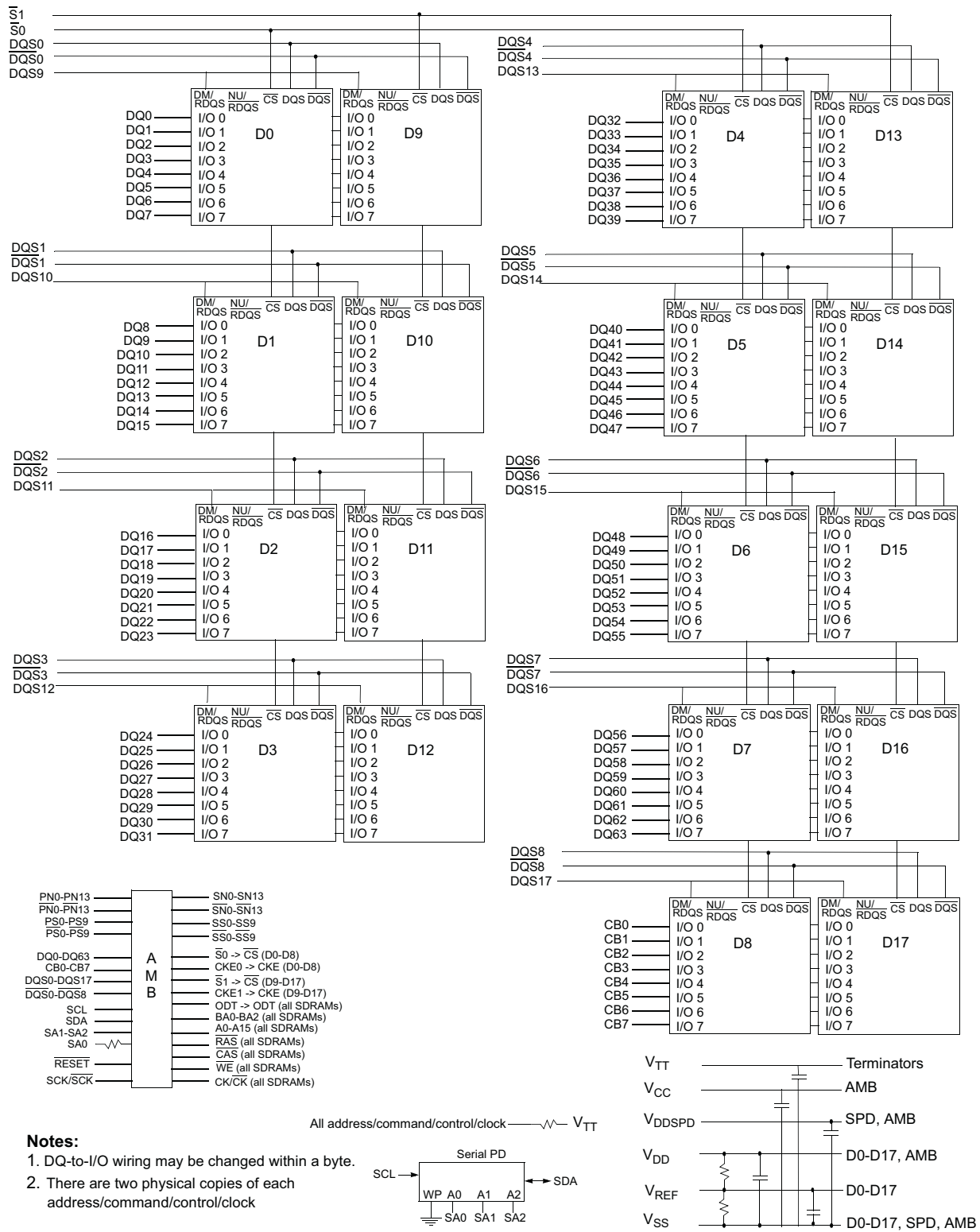
## DIMM Connector Pin Description:

| Pin Name                     | Pin Description                                                                                                                                                                                                                                                                                                                                                                                  | Count |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| SCK                          | System Clock Input, positive line <sup>1</sup>                                                                                                                                                                                                                                                                                                                                                   | 1     |
| $\overline{\text{SCK}}$      | System Clock Input, negative line <sup>1</sup>                                                                                                                                                                                                                                                                                                                                                   | 1     |
| PN[13:0]                     | Primary Northbound Data, positive lines                                                                                                                                                                                                                                                                                                                                                          | 14    |
| $\overline{\text{PN}}[13:0]$ | Primary Northbound Data, negative lines                                                                                                                                                                                                                                                                                                                                                          | 14    |
| PS[9:0]                      | Primary Southbound Data, positive lines                                                                                                                                                                                                                                                                                                                                                          | 10    |
| $\overline{\text{PS}}[9:0]$  | Primary Southbound Data, negative lines                                                                                                                                                                                                                                                                                                                                                          | 10    |
| SN[13:0]                     | Secondary Northbound Data, positive lines                                                                                                                                                                                                                                                                                                                                                        | 14    |
| $\overline{\text{SN}}[13:0]$ | Secondary Northbound Data, negative lines                                                                                                                                                                                                                                                                                                                                                        | 14    |
| SS[9:0]                      | Secondary Southbound Data, positive lines                                                                                                                                                                                                                                                                                                                                                        | 10    |
| $\overline{\text{SS}}[9:0]$  | Secondary Southbound Data, negative lines                                                                                                                                                                                                                                                                                                                                                        | 10    |
| SCL                          | Serial Presence Detect (SPD) Clock Input                                                                                                                                                                                                                                                                                                                                                         | 1     |
| SDA                          | SPD Data Input / Output                                                                                                                                                                                                                                                                                                                                                                          | 1     |
| SA[2:0]                      | SPD Address Inputs, also used to select the DIMM number in the AMB                                                                                                                                                                                                                                                                                                                               | 3     |
| VID[1:0]                     | Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs<br>VID[0] is $V_{DD}$ value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is $V_{CC}$ value: OPEN = 1.5 V, GND = 1.2 V                                                                                                                                                                                                       | 2     |
| $\overline{\text{RESET}}$    | AMB reset signal                                                                                                                                                                                                                                                                                                                                                                                 | 1     |
| RFU                          | Reserved for Future Use <sup>2</sup>                                                                                                                                                                                                                                                                                                                                                             | 16    |
| $V_{CC}$                     | AMB Core Power and AMB Channel Interface Power (1.5 Volt)                                                                                                                                                                                                                                                                                                                                        | 8     |
| $V_{DD}$                     | DRAM Power and AMB DRAM I/O Power (1.8 Volt)                                                                                                                                                                                                                                                                                                                                                     | 24    |
| $V_{TT}$                     | DRAM Address/Command/Clock Termination Power ( $V_{DD}/2$ )                                                                                                                                                                                                                                                                                                                                      | 4     |
| $V_{DDSPD}$                  | SPD Power                                                                                                                                                                                                                                                                                                                                                                                        | 1     |
| $V_{SS}$                     | Ground                                                                                                                                                                                                                                                                                                                                                                                           | 80    |
| DNU/M_Test                   | The DNU/M_Test pin provides an external connection on R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.<br>1 | 1     |
|                              | Total                                                                                                                                                                                                                                                                                                                                                                                            | 240   |

1. System Clock Signals SCK and  $\overline{\text{SCK}}$  switch at one half the DRAM CK/ $\overline{\text{CK}}$  frequency

2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility

## Functional Block Diagram:



## Architecture:

### Advanced Memory Buffer Pin Description:

| Pin Name                                                    | Pin Description                                                                                                               | Count      |
|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|------------|
| <b>FB-DIMM Channel Signals</b>                              |                                                                                                                               | <b>99</b>  |
| SCK                                                         | System Clock Input, positive line                                                                                             | 1          |
| $\overline{\text{SCK}}$                                     | System Clock Input, negative line                                                                                             | 1          |
| PN[13:0]                                                    | Primary Northbound Data, positive lines                                                                                       | 14         |
| $\overline{\text{PN}}[13:0]$                                | Primary Northbound Data, negative lines                                                                                       | 14         |
| PS[9:0]                                                     | Primary Southbound Data, positive lines                                                                                       | 10         |
| $\overline{\text{PS}}[9:0]$                                 | Primary Southbound Data, negative lines                                                                                       | 10         |
| SN[13:0]                                                    | Secondary Northbound Data, positive lines                                                                                     | 14         |
| $\overline{\text{SN}}[13:0]$                                | Secondary Northbound Data, negative lines                                                                                     | 14         |
| SS[9:0]                                                     | Secondary Southbound Data, positive lines                                                                                     | 10         |
| $\overline{\text{SS}}[9:0]$                                 | Secondary Southbound Data, negative lines                                                                                     | 10         |
| FBDRES                                                      | To an external precision calibration resistor connected to Vcc                                                                | 1          |
| <b>DDR2 Interface Signals</b>                               |                                                                                                                               | <b>175</b> |
| DQS[8:0]                                                    | Data Strobes, positive lines                                                                                                  | 9          |
| $\overline{\text{DQS}}[8:0]$                                | Data Strobes, negative lines                                                                                                  | 9          |
| DQS[17:9]/DM[8:0]                                           | Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.                               | 9          |
| $\overline{\text{DQS}}[17:9]$                               | Data Strobes (x4 DRAM only), negative lines                                                                                   | 9          |
| DQ[63:0]                                                    | Data                                                                                                                          | 64         |
| CB[7:0]                                                     | Checkbits                                                                                                                     | 8          |
| A[15:0]A, A[15:0]B                                          | Addresses. A10 is part of the pre-charge command                                                                              | 32         |
| BA[2:0]A, BA[2:0]B                                          | Bank Addresses                                                                                                                | 6          |
| $\overline{\text{RASA}}$ , $\overline{\text{RASB}}$         | Part of command, with $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , and $\overline{\text{CS}}[1:0]$ .                    | 2          |
| $\overline{\text{CASA}}$ , $\overline{\text{CASB}}$         | Part of command, with $\overline{\text{RAS}}$ , $\overline{\text{WE}}$ , and $\overline{\text{CS}}[1:0]$ .                    | 2          |
| $\overline{\text{WEA}}$ , $\overline{\text{WEB}}$           | Part of command, with $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , and $\overline{\text{CS}}[1:0]$ .                   | 2          |
| ODTA, ODTB                                                  | On-die Termination Enable                                                                                                     | 2          |
| CKE[1:0]A, CKE[1:0]B                                        | Clock Enable (one per rank)                                                                                                   | 4          |
| $\overline{\text{CS}}[1:0]A$ , $\overline{\text{CS}}[1:0]B$ | Chip Select (one per rank)                                                                                                    | 4          |
| CLK[3:0]                                                    | CLK[1:0] used on 9 and 18 device DIMMs, CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use. | 4          |
| $\overline{\text{CLK}}[3:0]$                                | Negative lines for CLK[3:0]                                                                                                   | 4          |
| DDRC_C14                                                    | DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18.                                                                | 1          |
| DDRC_B18                                                    | DDR Compensation: Resistor connected to common return pin DDRC_C14                                                            | 1          |
| DDRC_C18                                                    | DDR Compensation: Resistor connected to common return pin DDRC_C14                                                            | 1          |
| DDRC_B12                                                    | DDR Compensation: Resistor connected to V <sub>SS</sub>                                                                       | 1          |
| DDRC_C12                                                    | DDR Compensation: Resistor connected to V <sub>DD</sub>                                                                       | 1          |

## Advanced Memory Buffer Pin Description:

| SPD Bus Interface Signals |                                                                                                        | 5          |
|---------------------------|--------------------------------------------------------------------------------------------------------|------------|
| SCL                       | Serial Presence Detect (SPD) Clock Input                                                               | 1          |
| SDA                       | SPD Data Input / Output                                                                                | 1          |
| SA[2:0]                   | SPD Address Inputs, also used to select the DIMM number in the AMB                                     | 3          |
| Miscellaneous Signals     |                                                                                                        | 163        |
| PLLTSTO                   | PLL Clock Observability Output                                                                         | 1          |
| VCCAPLL                   | Analog VCC for the PLL. Tied with low pass filter to VCC.                                              | 1          |
| VSSAPLL                   | Analog VSS for the PLL. Tied to ground on the AMB die. Do not tie to ground on the DIMM.               | 1          |
| TEST_pin#                 | Leave floating on the DIMM                                                                             | 6          |
| TESTLO_pin#               | Tie to ground on the DIMM <sup>2</sup>                                                                 | 5          |
| BFUNC                     | Tie to ground to set functionality as "buffer on DIMM."                                                | 1          |
| $\overline{\text{RESET}}$ | AMB reset signal                                                                                       | 1          |
| NC                        | No connect. Many NC are connected to VDD on the DIMM, to lower the impedance of the VDD power islands. | 129        |
| RFU                       | Reserved for Future Use                                                                                | 18         |
| Power/Ground Signals      |                                                                                                        | 213        |
| V <sub>CC</sub>           | AMB Core Power (1.5 Volt)                                                                              | 24         |
| V <sub>CCFBD</sub>        | AMB Channel I/O Power (1.5 Volt)                                                                       | 8          |
| V <sub>DD</sub>           | AMB DRAM I/O Power (1.8 Volt)                                                                          | 24         |
| V <sub>DDSPD</sub>        | SPD Power (3.3 Volt)                                                                                   | 1          |
| V <sub>SS</sub>           | Ground                                                                                                 | 156        |
| <b>Total</b>              |                                                                                                        | <b>655</b> |

1. System Clock Signals SCK and  $\overline{\text{SCK}}$  switch at one half the DRAM CK/ $\overline{\text{CK}}$  frequency.

2. TESTLO\_AB20 and TESTLO\_AC20 should be configured for debug purposes on prototype DIMMs: each pin should have a zero ohm resistor pulldown to ground, and an unpopulated resistor pullup to VCC. These resistors can be replaced on production DIMMs with a direct connection to ground.

## Package Dimensions:

