

# Graphics Video Sync Adder/Extractor

MAX9539/MAX9540

## General Description

The MAX9539/MAX9540 chipset provides a 3-wire (RGB) interface for 5-wire (RGBHV) video by adding and extracting the H, V, and composite sync from the graphics video signals. This chipset eliminates the problem of sync-to-video timing (skew errors) in a 5-wire interface, while reducing the number of channels required to transport video signals.

The MAX9539 mixes the H and V sync signals and adds them to create a 3-wire interface from a 5-wire (RGBHV) input. The MAX9540 recovers the H and V sync signals to create a 5-wire (RGBHV) interface from the 3-wire input. The MAX9540 also provides a composite sync output.

The chipset includes the MAX9539 sync adder and the MAX9540 sync extractor with 180MHz large-signal bandwidths to address display resolutions up to 1600 x 1200 at 85Hz for VGA-to-UXGA applications. Both devices feature a DC restore function, which virtually eliminates any changes in black level. The chipset uses a proprietary H and V sync addition/extraction scheme (true sync) to minimize skew errors.

The MAX9539/MAX9540 are available in 28-pin TSSOP packages and are specified over the extended -40°C to +85°C temperature range.

## Applications

Enterprise Class (Blade) Servers  
Laptop PCs  
Web Appliances  
Keyboard-Video-Mouse (KVM)

## Features

- ◆ 3-Wire RBG to 5-Wire RBGHV Interface
- ◆ Supports VGA-to-UXGA Resolution
- ◆ Low Offset Voltage ( $\pm 1\text{mV}$ )
- ◆ 180MHz Large-Signal Bandwidth

## Ordering Information

PART	PIN-PACKAGE	PKG CODE	DESCRIPTION
MAX9539EUI+*	28 TSSOP	U28-3	Sync Adder
MAX9539EUI	28 TSSOP	U28-3	Sync Adder
MAX9540EUI+*	28 TSSOP	U28-3	Sync Extractor
MAX9540EUI	28 TSSOP	U28-3	Sync Extractor

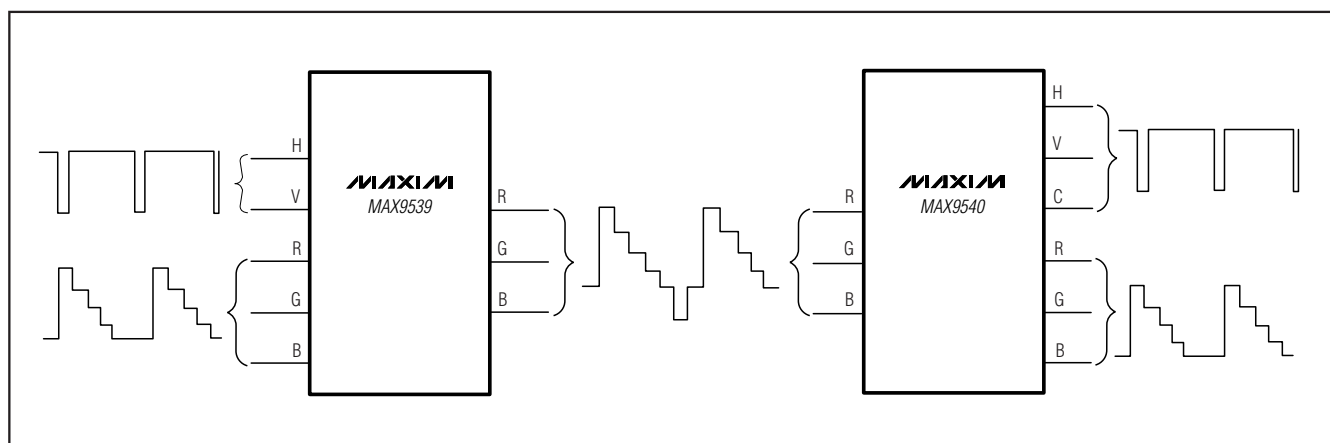
**Note:** All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes lead-free package.

\*Future product—contact factory for availability.

Pin Configurations appear at end of data sheet.

## Chipset Diagram



# Graphics Video Sync Adder/Extractor

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$  to GND ..... -0.3V to +6V  
 $V_{EE}$  to GND ..... -6V to +0.3V  
 $IN_R, IN_G, IN_B, REST_R, REST_G,$   
 $REST_B$  ..... ( $V_{EE} - 0.3V$ ) to ( $V_{CC} + 0.3V$ )  
 $OUT_R, OUT_G, OUT_B$  Short Circuit  
to GND (Note 1) ..... Continuous  
 $OUT_R, OUT_G, OUT_B$  Short Circuit to  
 $V_{CC}$  ..... 5s  
MAX9539:  
HSYNC, VSYNC, SP\_H, SP\_V ..... -0.3V to ( $V_{CC} + 0.3V$ )  
MAX9540:  
HSYNC, CSYNC, VSYNC Short Circuit to GND ..... Continuous  
HSYNC, CSYNC, VSYNC Short Circuit to  $V_{CC}$  ..... 1min  
SP\_C, SP\_V, SP\_H ..... -0.3V to ( $V_{CC} + 0.3V$ )

Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
28-Pin TSSOP (U28-3) Single-Layer Board  
(derate 13mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 1039mW  
28-Pin TSSOP (U28-3) Multilayer Board  
(derate 14.3mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 1143mW  
Operating Temperature .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
Junction Temperature .....  $+150^\circ\text{C}$   
Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
Lead Temperature (soldering, 10s) .....  $+300^\circ\text{C}$

**Note 1:** Continuous power dissipation rating must also be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## MAX9539 DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +5V$ ,  $V_{EE} = -5V$ , GND = 0V,  $R_L = 150\Omega$  to GND,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise specified. Typical values are at  $T_A = +25^\circ\text{C}$ .) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{CC}$	Guaranteed by PSRR test	4.5		5.5	V
	$V_{EE}$	Guaranteed by PSRR test	-5.5		-4.5	
Quiescent Supply Current	$I_{CC}$	$R_L = \infty$		61	90	mA
	$I_{EE}$	$R_L = \infty$		55	75	
Input Voltage Range	$V_{IN}$	Inferred from voltage gain test	0		1	V
DC-Restore Input Voltage Range	$\Delta V_{IN\_RESTORE}$	Inferred from output DC-Restore Rejection Ratio test	-0.30		+0.30	V
DC-Restore Rejection Ratio	DCRR ( $\Delta V_{OS} / \Delta V_{IN\_RESTORE}$ )	$V_{IN\_RESTORE} = -0.3V$ to $+0.3V$	28	50		dB
Input Bias Current	$I_B$			$\pm 2$	$\pm 30$	$\mu\text{A}$
Input Resistance	$R_{IN}$			400		$k\Omega$
Output Sync Amplitude	$V_{SYNC}$	H or V sync is active	-2.65	-2.35	-2.05	V
Output Offset Voltage	$V_{OS}$	$\Delta V_{IN\_RESTORE} = 0V$ , $T_A = +25^\circ\text{C}$ (Note 4)		$\pm 1$	$\pm 8$	mV
Temperature Coefficient of Output Offset Voltage	$TCV_{OS}$ ( $\Delta V_{OS} / \Delta T_A$ )	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		-24		$\mu\text{V}/^\circ\text{C}$
Voltage Gain	G	$V_{IN} = 0$ to $+1V$	+1.95	+2	+2.05	V/V
Gain Matching	$\Delta G$	R to G to B		$\pm 1$	$\pm 2$	%
Gain Linearity				0.02		%
Power-Supply Rejection Ratio	PSRR $\Delta V_{OS} / \Delta(V_{CC} - V_{EE})$	$V_{CC}, V_{EE} = \pm 4.5V$ to $\pm 5.5V$	50	70		dB

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## MAX9539 DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +5V$ ,  $V_{EE} = -5V$ ,  $GND = 0V$ ,  $R_L = 150\Omega$  to  $GND$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise specified. Typical values are at  $T_A = +25^\circ C$ .) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>HSYNC, VSYNC INPUTS</b>						
High Input Voltage	$V_{IH}$		2			V
Low Input Voltage	$V_{IL}$				0.8	V
High Input Current	$I_{IH}$	$V_I = 5V$		10	60	$\mu A$
Low Input Current	$I_{IL}$	$V_I = 0V$		2.5		$\mu A$
<b>SP_H, SP_V INPUTS</b>						
High Input Voltage	$V_{IH}$		2			V
Low Input Voltage	$V_{IL}$				0.8	V
High Input Current	$I_{IH}$	$V_I = 5V$		0.1	20	$\mu A$
Low Input Current	$I_{IL}$	$V_I = 0V$		1	20	$\mu A$
<b>REST_R, REST_B, REST_G INPUTS</b>						
Hold-Mode Droop Current	$I_{DROOP}$			$\pm 2$		nA

## MAX9539 AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +5V$ ,  $V_{EE} = -5V$ ,  $GND = 0V$ ,  $R_L = 150\Omega$  to  $GND$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise specified. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Large-Signal Bandwidth	LSBW	$V_{OUT} = 2V_{P-P}$		180		MHz
Slew Rate	SR	$V_{OUT} = 2V_{P-P}$		900		V/ $\mu s$
Channel-to-Channel Crosstalk	$X_{TALK}$	$V_{OUT} = 2V_{P-P}$ at 10MHz		-60		dB
Settling Time	$t_S$	$V_{OUT} = 2V_{P-P}$ to 0.1%		15		ns
Input Voltage-Noise Density	$e_n$	$f = 100kHz$		30		nV/ $\sqrt{Hz}$
Input Current-Noise Density	$i_n$	$f = 100kHz$		12		pA/ $\sqrt{Hz}$
Sync Timing Delay	$t_D$	H sync only (Note 5)		-20		ns
Channel-to-Channel Sync Timing Skew	$\Delta(t_D)$	H sync only (Note 5)		1		ns
Sync Edge Jitter	$t_{JITTER}$			200		psp-p
Line Droop		$f = 50kHz$		0.01		%
Field Tilt		$f = 60Hz$		0.04		%
Sync Frequency Range	$f_H$	H sync		15 to 150		kHz
	$f_V$	V sync		40 to 100		Hz

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## MAX9540 DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +5V$ ,  $V_{EE} = -5V$ ,  $GND = 0V$ ,  $R_L = 150\Omega$  to  $GND$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise specified. Typical values are at  $T_A = +25^\circ C$ .) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	$V_{CC}$	Guaranteed by PSRR test	4.5		5.5	V
	$V_{EE}$	Guaranteed by PSRR test	-5.5		-4.5	
Quiescent Supply Current	$I_{CC}$	$R_L = \infty$		61	90	mA
	$I_{EE}$	$R_L = \infty$		54	75	
Input Voltage Range	$V_{IN}$	Inferred from voltage gain test	0		1	V
DC-Restore Input Voltage Range	$\Delta V_{IN\_RESTORE}$	Inferred from DC-Restore Rejection Ratio test	-0.30		+0.30	V
DC-Restore Rejection Ratio	DCRR ( $\Delta V_{OS} / \Delta V_{IN\_RESTORE}$ )	$V_{IN\_RESTORE} = -0.3V$ to $+0.3V$	28	50		dB
Input Bias Current	$I_B$			$\pm 2$	$\pm 30$	$\mu A$
Input Resistance	$R_{IN}$			400		$k\Omega$
Output Black Level	$V_{BLACK}$	H or V sync is active: $V_{IN} < -1V$		$\pm 1$	$\pm 16$	mV
Output Offset Voltage	$V_{OS}$	$\Delta V_{IN\_RESTORE} = 0V$ , $T_A = +25^\circ C$ (Note 4)		$\pm 1$	$\pm 8$	mV
Temperature Coefficient of Output Offset Voltage	$TCV_{OS}$ ( $\Delta V_{OS} / \Delta T_A$ )	$T_A = -40^\circ C$ to $+85^\circ C$		-24		$\mu V/^\circ C$
Voltage Gain	$G$	$V_{IN} = 0$ to $+1V$	+1.95	+2	+2.05	V/V
Gain Matching	$\Delta G$	R to G to B		$\pm 1$	$\pm 2$	%
Gain Linearity				0.02		%
Power-Supply Rejection Ratio	PSRR $\Delta V_{OS} / \Delta(V_{CC} - V_{EE})$	$V_{CC}, V_{EE} = \pm 4.5V$ to $\pm 5.5V$	50	70		dB
<b>SP_H, SP_V, SP_C INPUTS</b>						
High Input Voltage	$V_{IH}$		2			V
Low Input Voltage	$V_{IL}$				0.8	V
High Input Current	$I_{IH}$	$V_I = 5V$		0.01	20	$\mu A$
Low Input Current	$I_{IL}$	$V_I = 0V$		1	20	$\mu A$
<b>REST_R, REST_G, REST_B INPUTS</b>						
Hold-Mode Droop Current	$I_{DROOP}$			$\pm 2$		nA
<b>HSYNC, VSYNC, CSYNC OUTPUTS</b>						
High Voltage Level	$V_{OH}$	$I_{OH}(\text{source}) = +8mA$	2.4			V
Low Voltage Level	$V_{OL}$	$I_{OL}(\text{sink}) = -8mA$			0.5	V

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## MAX9540 AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +5V$ ,  $V_{EE} = -5V$ ,  $GND = 0V$ ,  $R_L = 150\Omega$  to  $GND$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise specified. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Large-Signal Bandwidth	LSBW	$V_{OUT} = 2V_{P-P}$		180		MHz
Slew Rate	SR	$V_{OUT} = 2V_{P-P}$		900		V/ $\mu s$
Channel-to-Channel Crosstalk	X-TALK	$V_{OUT} = 2V_{P-P}$ at 10MHz	-60			dB
Settling Time	$t_S$	$V_{OUT} = 2V_{P-P}$ to 0.1%		15		ns
Input Voltage-Noise Density	$e_n$	$f = 100kHz$		30		nV/ $\sqrt{Hz}$
Input Current-Noise Density	$i_n$	$f = 100kHz$		12		pA/ $\sqrt{Hz}$
Sync Timing Delay	$t_D$	H sync only (Note 5)	-10			ns
Sync Timing Skew	$\Delta(t_D)$	H sync only (Note 5)		1		ns
Sync Edge Jitter	$t_{JITTER}$			200		psp-p
Line Droop		$f = 50kHz$		0.01		%
Field Tilt		$f = 60Hz$		0.04		%
Sync Frequency Range	$f_H$	H sync		15 to 150		kHz
	$f_V$	V sync		40 to 100		Hz

**Note 2:** All devices are 100% production tested at  $T_A = +25^\circ C$ . Specifications over temperature limits are guaranteed by design.

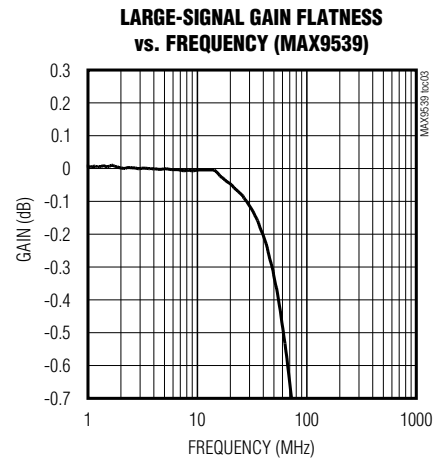
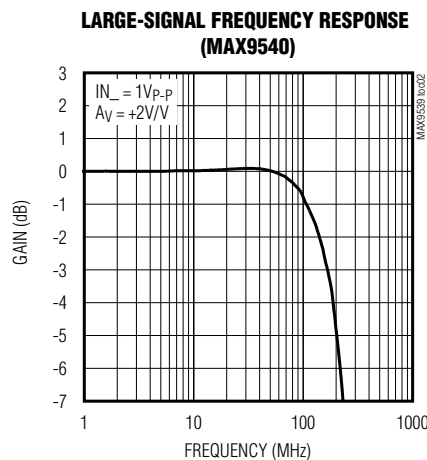
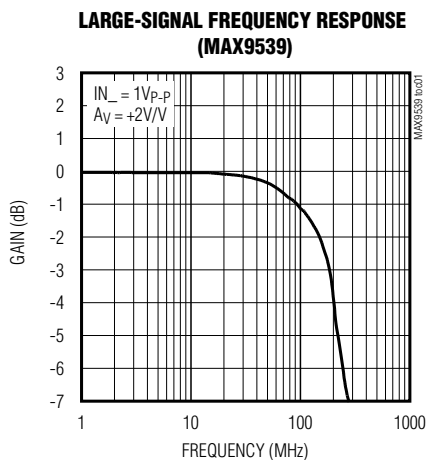
**Note 3:** DC restore is not active. HSYNC and VSYNC are not applied. REST\_R, REST\_G, and REST\_B are grounded.

**Note 4:** DC restore is active. REST\_R, REST\_G, and REST\_B are bypassed with 1nF to ground.

**Note 5:** The sync timing error is measured as follows: The input signals are measured from the falling edge of H sync/V sync to the start of active video, called  $t_1$ . The output signal is then measured from the falling edge of H sync/V sync to the start of active video, called  $t_2$ . All measurements are at the 50% points as shown in Figure 1.

## Typical Operating Characteristics

( $T_A = +25^\circ C$ ,  $V_{CC} = +5V$ ,  $V_{EE} = -5V$ ,  $GND = 0V$ ,  $R_L = 150\Omega$  to  $GND$ , unless otherwise noted.)

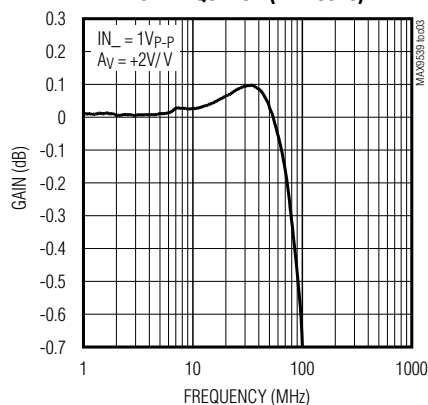


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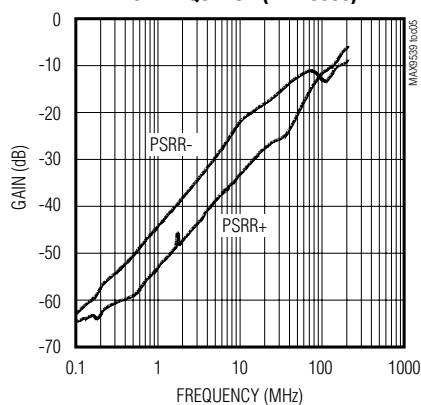
## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$ ,  $V_{EE} = -5\text{V}$ ,  $\text{GND} = 0\text{V}$ ,  $R_L = 150\Omega$  to GND, unless otherwise noted.)

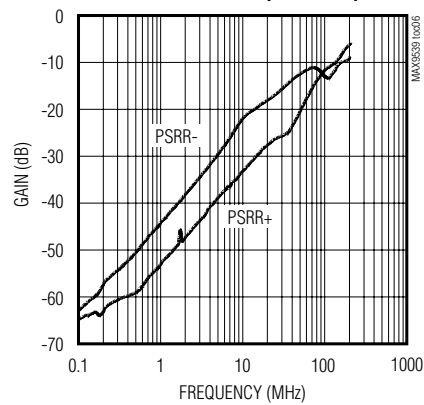
**LARGE-SIGNAL GAIN FLATNESS  
vs. FREQUENCY (MAX9540)**



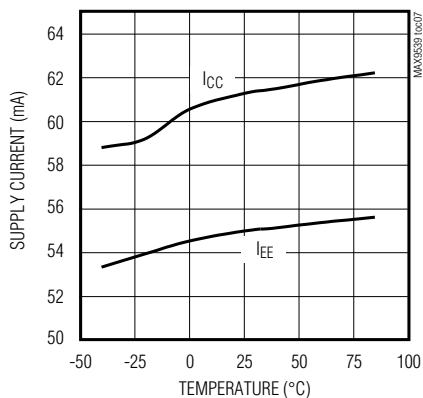
**POWER-SUPPLY REJECTION RATIO  
vs. FREQUENCY (MAX9539)**



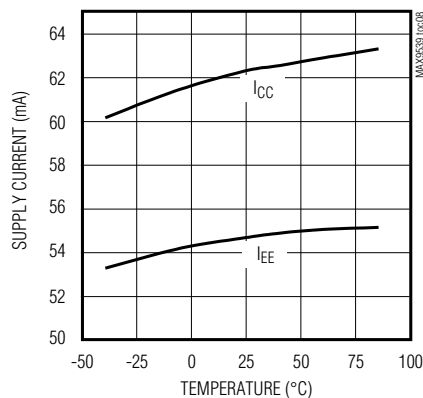
**POWER-SUPPLY REJECTION RATIO  
vs. FREQUENCY (MAX9540)**



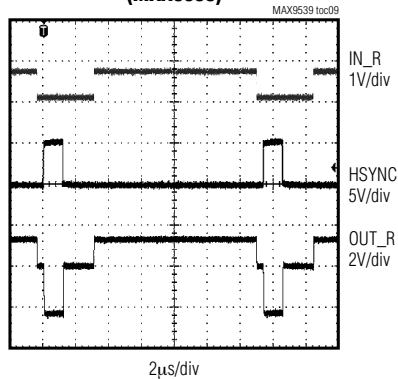
**SUPPLY CURRENT  
vs. TEMPERATURE (MAX9539)**



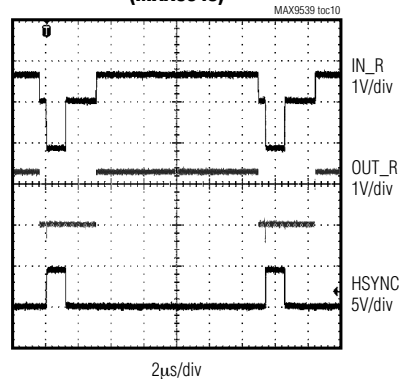
**SUPPLY CURRENT  
vs. TEMPERATURE (MAX9540)**



**OUTPUT vs. INPUT  
(MAX9539)**



**OUTPUT vs. INPUT  
(MAX9540)**



# Graphics Video Sync Adder/Extractor

## MAX9539 Pin Description

PIN	NAME	FUNCTION
1	IN_R	Red Video Input
2, 7, 12	GND	Ground
3	REST_R	Red DC Restore. Connect a 1nF capacitor from REST_R to GND.
4, 9, 10, 14, 15, 20, 21, 22, 25	N.C.	No Connection. Not internally connected.
5	I.C.	Internally Connected. For best performance, connect this pin to GND.
6	IN_G	Green Video Input
8	REST_G	Green DC Restore. Connect a 1nF capacitor from REST_G to GND.
11	IN_B	Blue Video Input
13	REST_B	Blue DC Restore. Connect a 1nF capacitor from REST_B to GND.
16	VSYNC	Vertical Sync Input
17	SP_V	Vertical Sync Polarity Input
18	OUT_B	Blue Output with Vertical Sync
19	VEE	Negative Power-Supply Input. Bypass with a 0.1 $\mu$ F capacitor to GND.
23	OUT_G	Green Output with Composite Sync.
24	VCC	Positive Power-Supply Input. Bypass with a 0.1 $\mu$ F capacitor to GND.
26	HSYNC	Horizontal Sync Input
27	SP_H	Horizontal Sync Polarity Input
28	OUT_R	Red Output with Horizontal Sync

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# Graphics Video Sync Adder/Extractor

## MAX9540 Pin Description

PIN	NAME	FUNCTION
1	IN_R	Red Video Input with Horizontal Sync
2, 7, 12	GND	Ground
3	REST_R	Red DC Restore. Connect a 1nF capacitor from REST_R to GND.
4, 9, 10, 14, 15, 20, 25	N.C.	No Connection. Not internally connected.
5	I.C.	Internally Connected. For best performance, connect this pin to GND.
6	IN_G	Green Video Input with Composite Sync
8	REST_G	Green DC Restore. Connect a 1nF capacitor from REST_G to GND.
11	IN_B	Blue Video Input with Vertical Sync
13	REST_B	Blue DC Restore. Connect a 1nF capacitor from REST_B to GND.
16	VSYNC	Vertical Sync Output
17	SP_V	Vertical Sync Polarity Input
18	OUT_B	Blue Video Output
19	VEE	Negative Power-Supply Input. Bypass with a 0.1 $\mu$ F capacitor to GND.
21	CSYNC	Composite Sync Output
22	SP_C	Composite Sync Polarity Input
23	OUT_G	Green Video Output
24	VCC	Positive Power-Supply Input. Bypass with a 0.1 $\mu$ F capacitor to GND.
26	HSYNC	Horizontal Sync Output
27	SP_H	Horizontal Sync Polarity Input
28	OUT_R	Red Video Output

## Detailed Description

The MAX9539/MAX9540 chipset provides a 3-wire (RGB) interface for 5-wire (RGBHV) video by adding and extracting the H, V, and composite sync from the graphics video signals. This chipset eliminates the problem of sync-to-video timing (skew errors) in a 5-wire interface, while reducing the number of channels required when transporting video signals.

The MAX9539 mixes the H and V sync signals and adds them to create a 3-wire interface from a 5-wire (RGBHV) input. The MAX9540 recovers the H and V sync signals to create a 5-wire (RGBHV) interface from the 3-wire input. The MAX9540 also provides a composite sync output.

The chipset includes the MAX9539 sync adder and the MAX9540 sync extractor with 180MHz large-signal bandwidths to address display resolutions up to 1600 x 1200 at 85Hz for VGA-to-UXGA applications. Both devices feature a DC-restore function, which virtually eliminates any changes in black level. The chipset uses a proprietary H and V sync addition/extraction scheme (true sync) to minimize skew errors.

## MAX9539 Sync Adder

The MAX9539 mixes the H and V sync signals and adds them to create a 3-wire interface from a 5-wire (RGBHV) input. Sync signals are added to the input video signals. Horizontal sync is added to red video, vertical sync is added to blue video, and composite sync is added to green video. Composite sync is the XOR function between H sync and V sync and is internally generated by the MAX9539. The sync level of the video outputs is -2.4V. The DC-restore function removes any DC offset ( $\Delta V_{IN\_RESTORE}$ ) in the RGB video inputs and sets the output black level to 0V at the back porch of the H sync. Therefore, the output black level is set to 0V at the beginning of every line.

Figure 2 illustrates the functionality of the MAX9539. In this example, the sync signals are of positive polarity.

## MAX9540 Sync Extractor

The MAX9540 recovers the H and V sync signals to create a 5-wire (RGBHV) interface from the 3-wire input. The output video signals are obtained by removing the sync pulses of the input video. The sync outputs correspond to the sync pulses of the input video: horizontal sync is

# Graphics Video Sync Adder/Extractor

obtained from the red input, vertical sync is obtained from the blue input, and composite sync is obtained from the green input. Like the MAX9539, the DC-restore function removes any DC offset in the RGB video inputs and sets the output black levels to 0V. This happens at the back porch (trailing edge) of the sync pulse.

Figure 3 illustrates the functionality of the MAX9540. In this example, the sync signals are of positive polarity.

## DC Restore

The MAX9539/MAX9540 DC-restore function removes the input signal DC level and restores 0V for the black level of the output video signal. 1nF restore capacitors are needed for the sample-and-hold circuitry at REST\_R, REST\_G, and REST\_B. A value less than 0.5nF can cause AC instability in the sample-and-hold circuitry. A value higher than 2nF increases the settling time of the sample-and-hold circuitry, shifting the output black level from 0V.

## Sync Polarity

Sync polarity refers to the idle state and pulse amplitude of the sync pulse. A sync pulse that idles low and pulses high is referred to as a positive sync pulse. A sync pulse that idles high and pulses low is referred to as a negative sync pulse as seen in Figure 4. To accommodate positive and negative sync input signals, the MAX9539/MAX9540 have vertical and horizontal sync polarity inputs (SP\_V and SP\_H). Drive SP\_V or SP\_H high for positive sync polarity. Drive SP\_V or SP\_H low for negative sync polarity. The MAX9540 also has a composite polarity input (SP\_C). Drive SP\_C high for positive sync polarity or drive SP\_C low for negative sync polarity (Table 1).

## Layout and Power-Supply Bypassing

The MAX9539/MAX9540 have an extremely high bandwidth and require careful board layout. For best performance use constant-impedance microstrip or stripline techniques.

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible. With multilayer boards, locate the ground plane on a layer that incorporates no signal or power traces.

Observe the following guidelines when designing the board regardless of whether or not a constant-impedance board is used.

- 1) Do not use wire-wrap boards or breadboards.

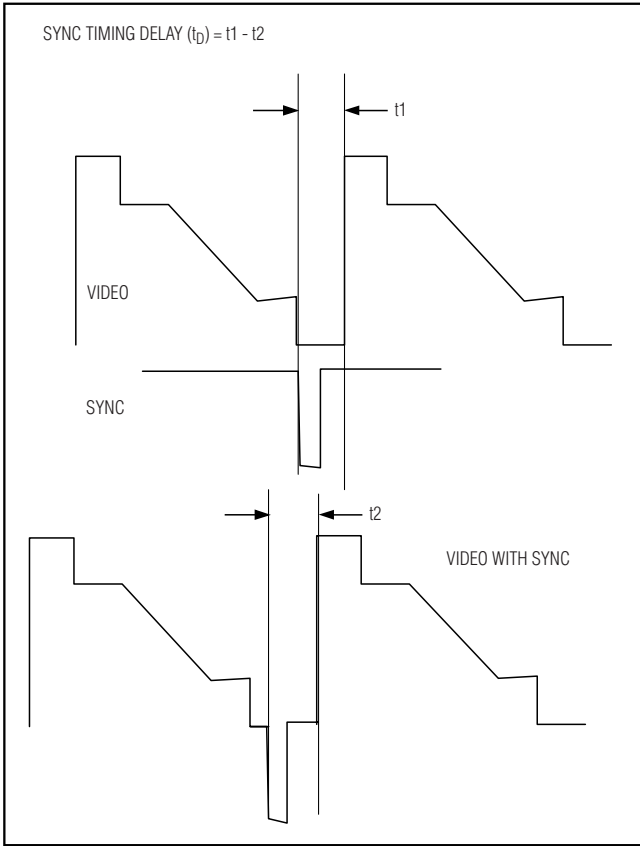


Figure 1. Sync Timing Delay ( $t_D$ ) =  $t_1 - t_2$

Table 1. Sync Polarity Table

INPUT LOGIC VALUE	SP_V	SP_H	SP_C (MAX9540)
1	Positive sync	Positive sync	Positive sync
0	Negative sync	Negative sync	Negative sync

- 2) Do not use IC sockets; they increase parasitic capacitance and inductance.
- 3) Keep lines as short and as straight as possible. Do not make 90° turns; round all corners.
- 4) Observe high-frequency bypassing techniques to maintain the amplifier's accuracy and stability.
- 5) Use surface-mount components. They generally have shorter bodies and lower parasitic reactance, yielding better high-frequency performance than through-hole components.

# Graphics Video Sync Adder/Extractor

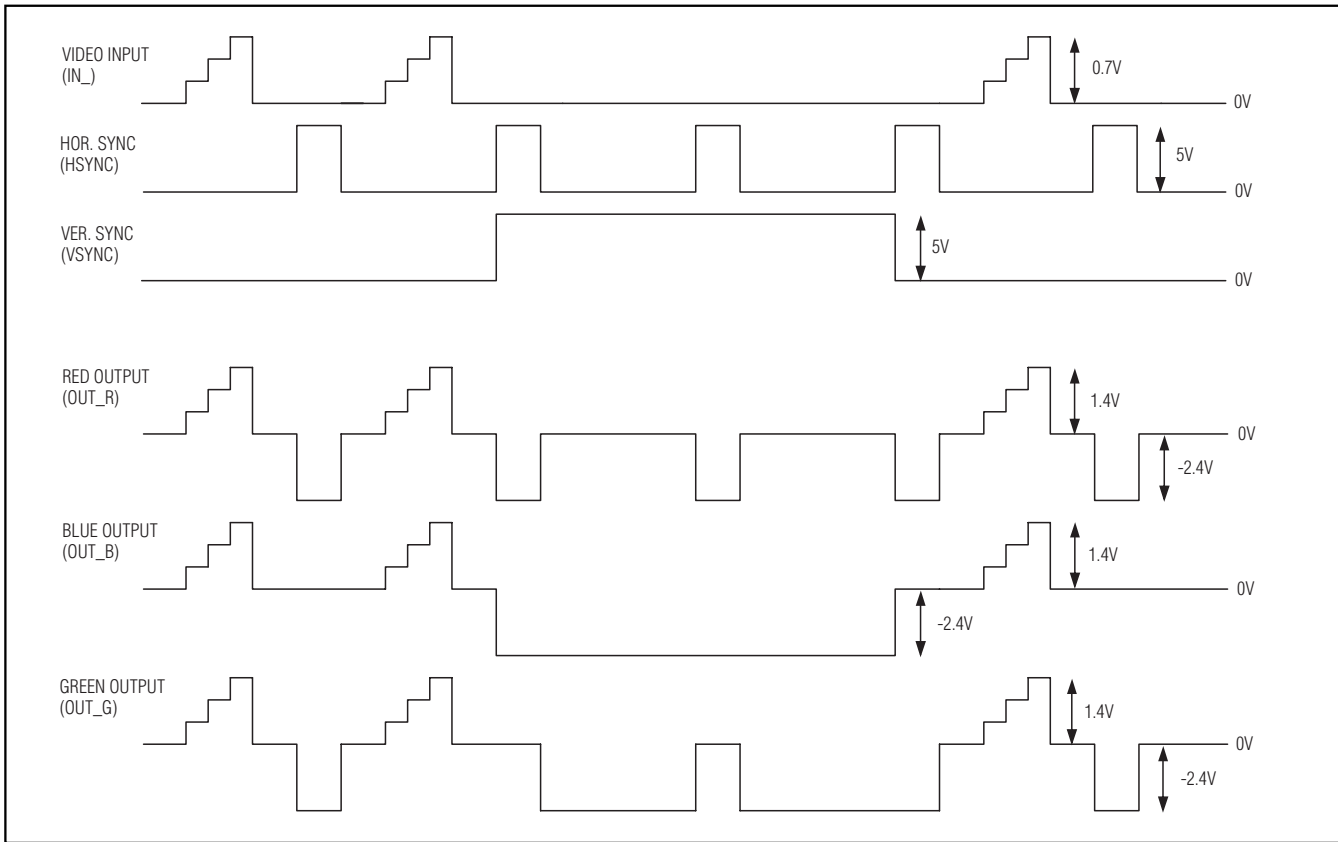


Figure 2. MAX9539 Input and Output Functionality

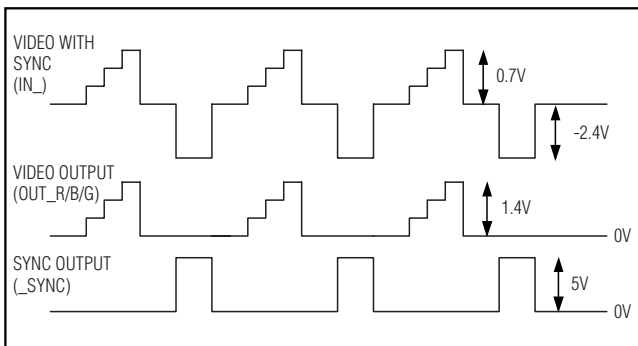


Figure 3. MAX9540 Input and Output Functionality

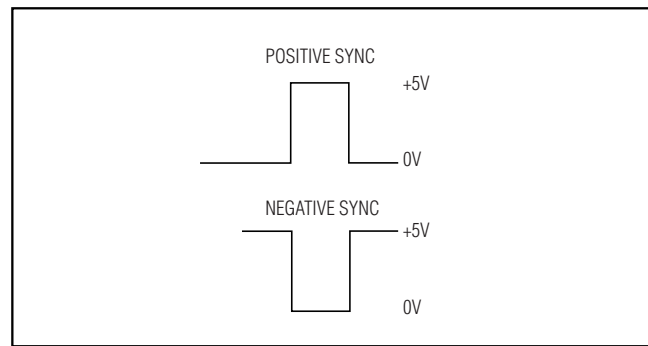


Figure 4. Sync Pulse Polarity

The bypass capacitors should include a 0.1 $\mu$ F ceramic surface-mount capacitor between each supply pin and the ground plane, located as close to the package as possible. Optionally, place a 10 $\mu$ F tantalum capacitor at the power-supply pins' points of entry to the PC board to ensure the integrity of incoming supplies. The power-supply trace should lead directly from the tanta-

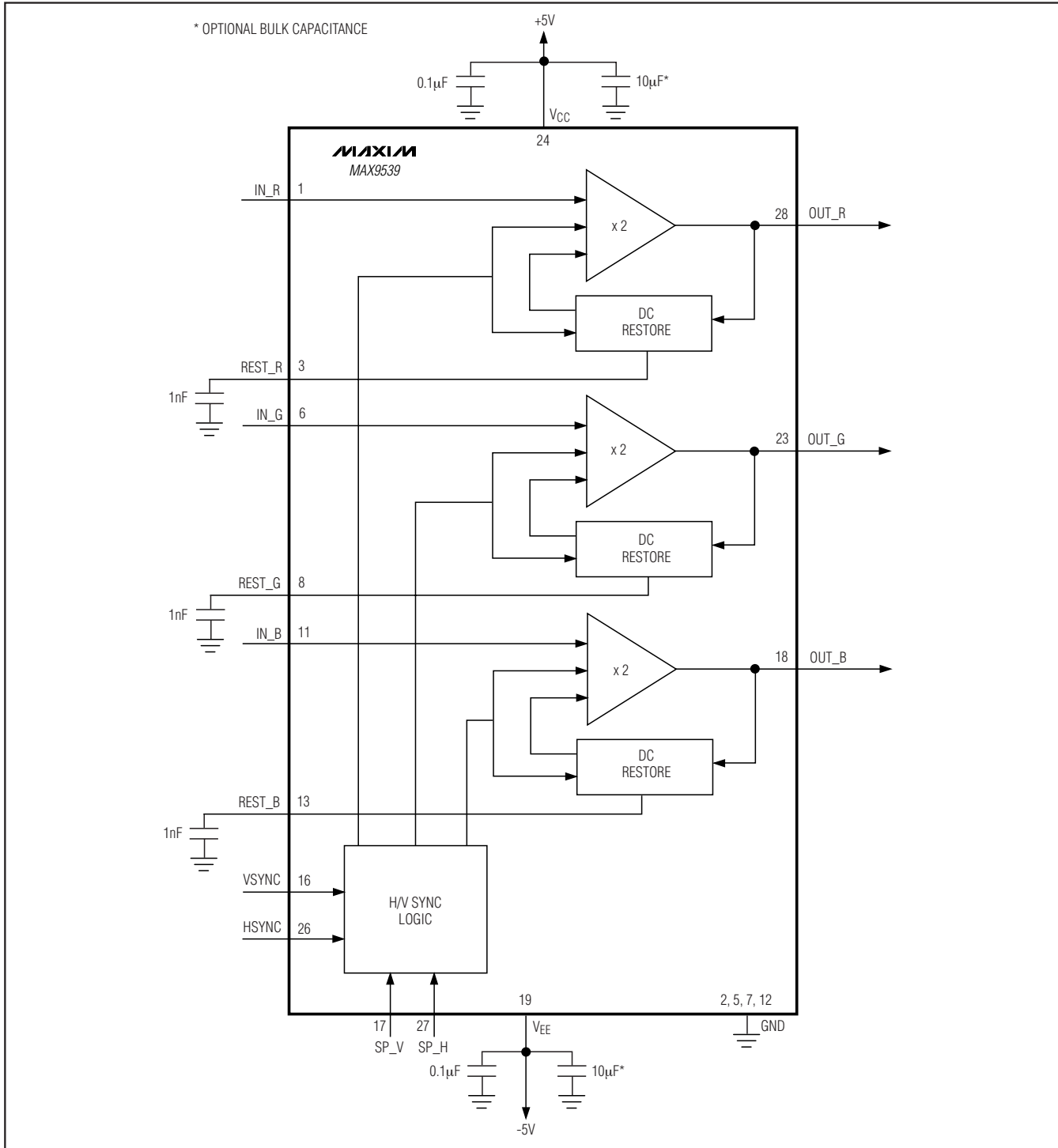
lum capacitor to the VCC and VEE pins. To minimize parasitic inductance, keep PC traces short and use surface-mount components.

Use surface-mount resistors for input termination and output back termination. Place the termination resistors as close to the IC as possible.

# Graphics Video Sync Adder/Extractor

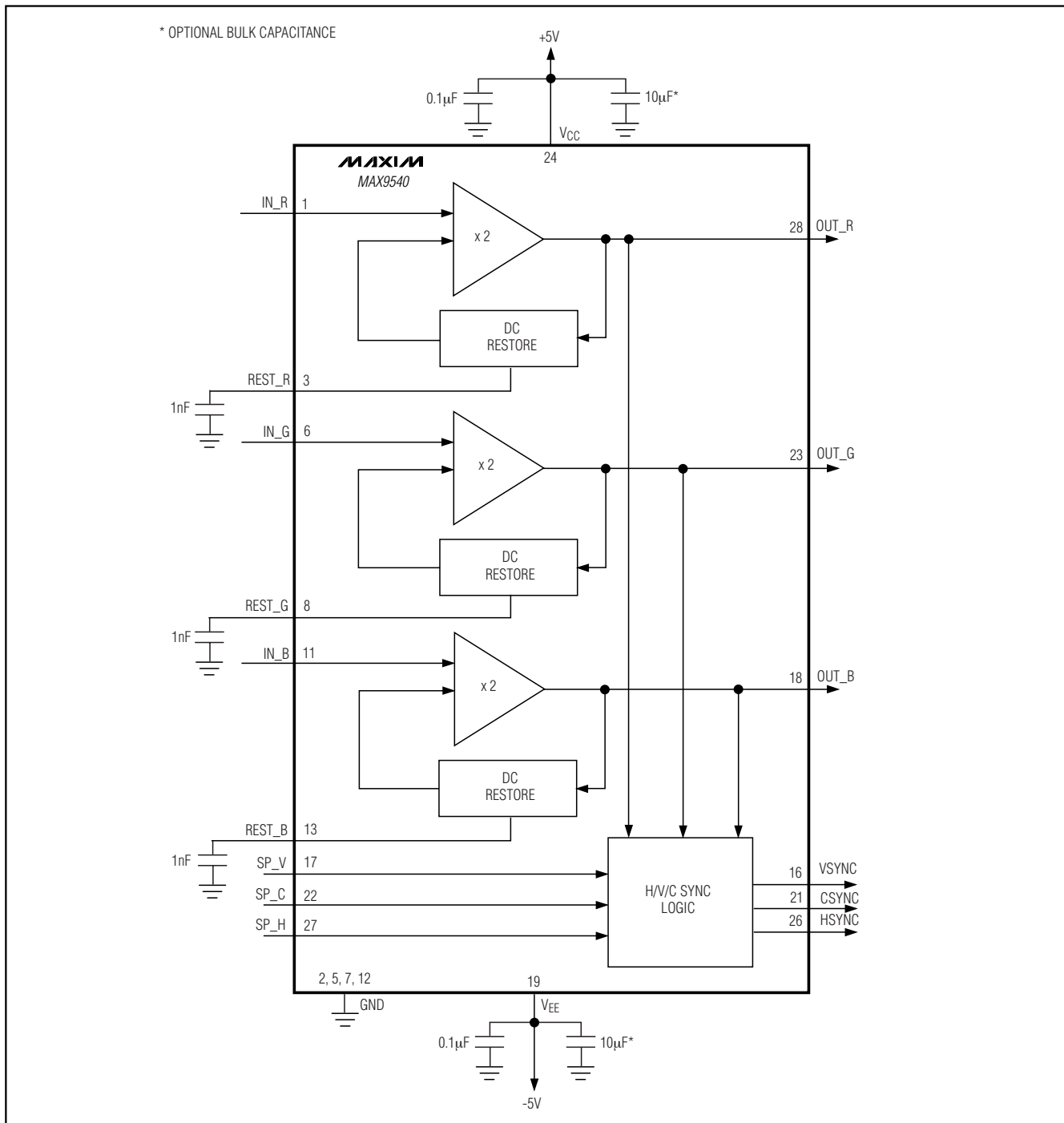
## Functional Diagrams

MAX9539/MAX9540



# Graphics Video Sync Adder/Extractor

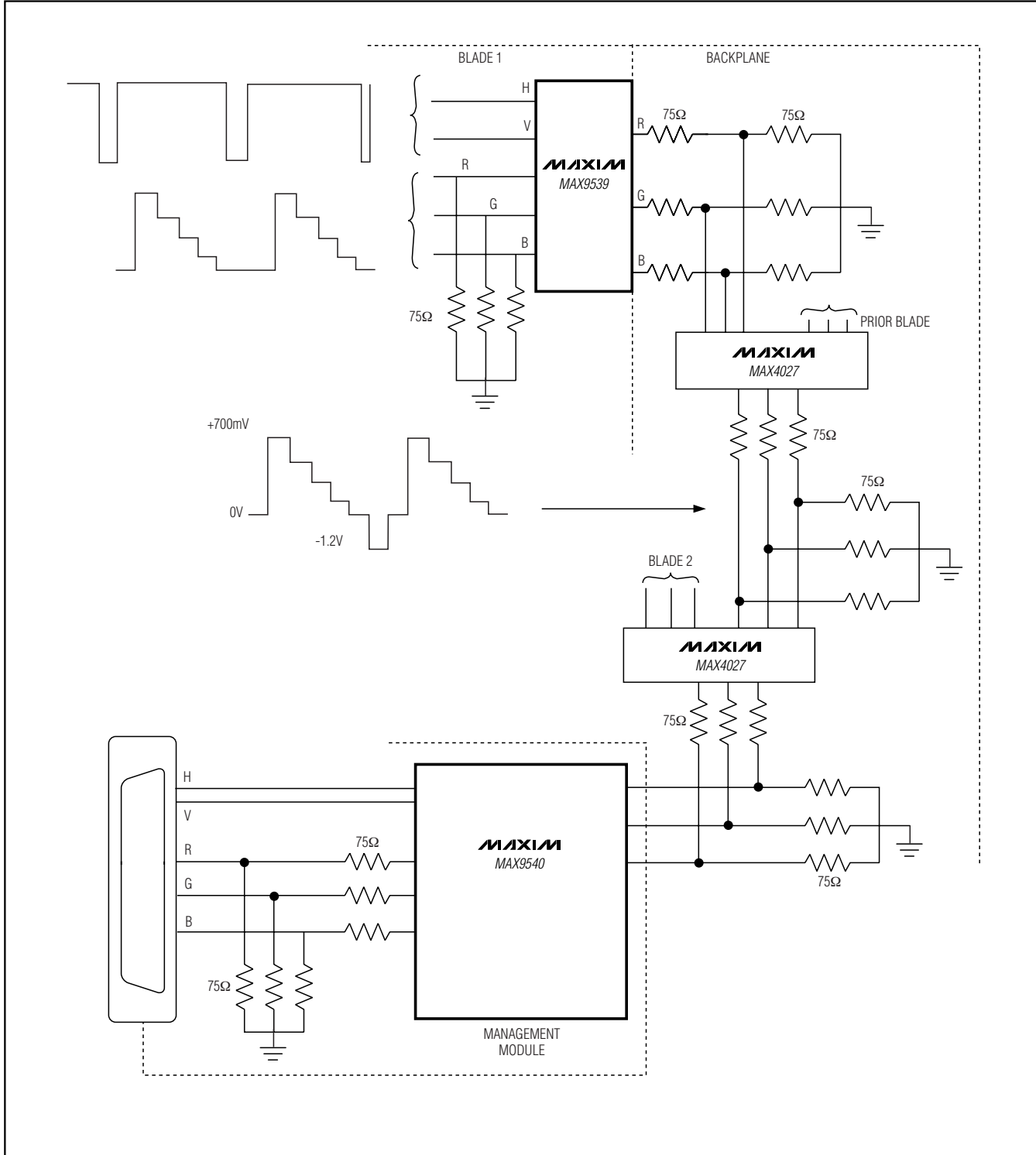
## Functional Diagrams (continued)



# Graphics Video Sync Adder/Extractor

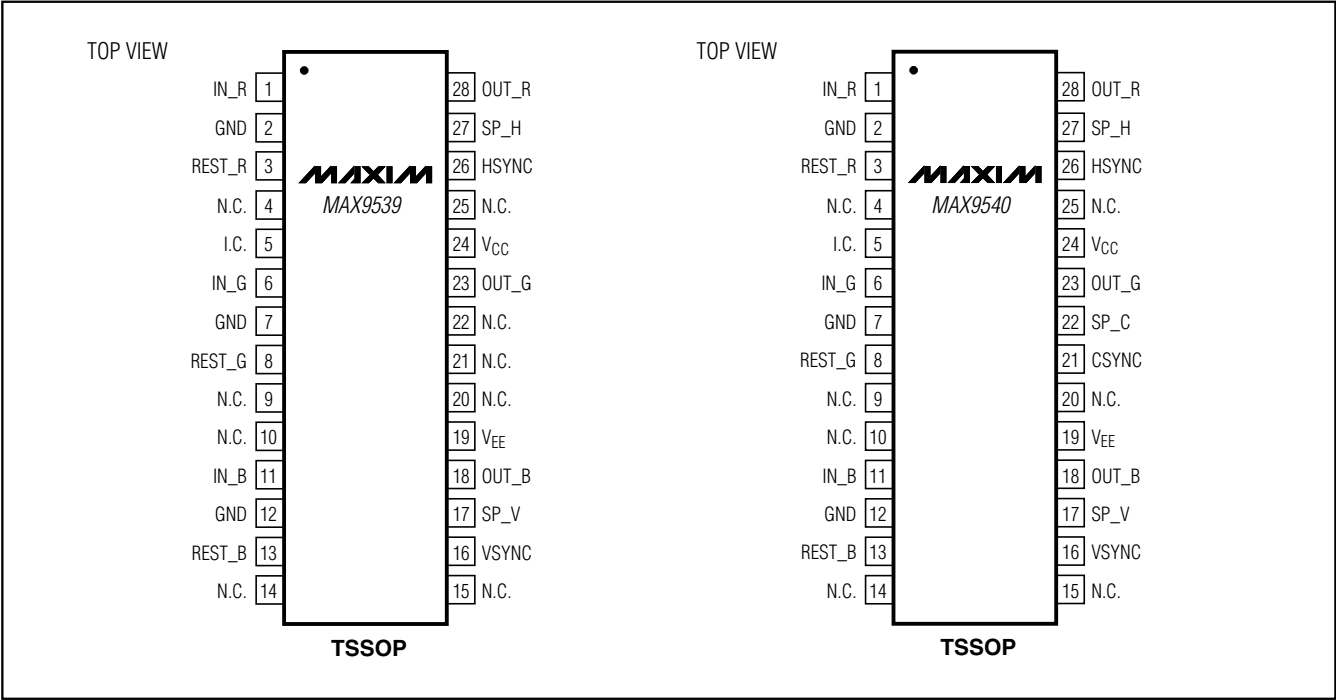
## Typical Application Diagram

MAX9539/MAX9540



# Graphics Video Sync Adder/Extractor

## Pin Configurations



## Chip Information

PROCESS: Bipolar

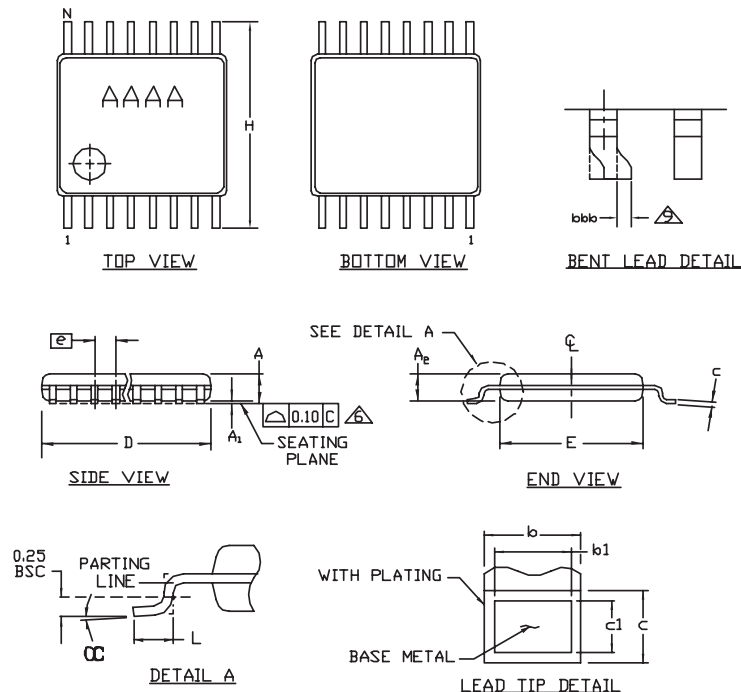
# Graphics Video Sync Adder/Extractor

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX9539/MAX9540

TSSOP4.40mm EPS



	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		.043
A <sub>1</sub>	0.05	0.15	.002	.006
A <sub>e</sub>	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b <sub>1</sub>	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c <sub>1</sub>	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	.065 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bb	0.10 MAX			

JEDEC MO-153	N	PKG. CODES	VARIATIONS			
			MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D U14-1; U14-2	4.90	5.10	.193	.201
AB	16	D U16-1; U16-2	4.90	5.10	.193	.201
AC	20	D U20-2; U20-3	6.40	6.60	.252	.260
AD	24	D U24-1	7.70	7.90	.303	.311
AE	28	D U28-1; U28-2; U28-3	9.60	9.80	.378	.386

### NOTES

1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.

-DRAWING NOT TO SCALE-

 <b>DALLAS</b> SEMICONDUCTOR			
TITLE PACKAGE OUTLINE, TSSOP 4.40mm BODY			
APPROVAL	DOCUMENT CONTROL NO. 21-0066	REV. I	1 / 1

## Revision History

Pages changed at Rev 2: 1, 2, 4, 15

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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