

Fully integrated microstepping motor driver using the L6470

Data brief

Features

- Voltage range from 8 V to 45 V
- Phase current up to 3 A_{r.m.s.}
- SPI with daisy-chain feature
- Socket for external resonator or crystal
- SW input
- Thermal resistance junction-to-ambient of 40 °C/W (typical)
- Suitable to be used in combination with STEVAL-PCC009V2

Description

The EVAL6470 demonstration board is a fully integrated microstepping motor driver. In combination with the STEVAL-PCC009V2 communication board and the dSPIN Evaluation Software, the board allows the engineer to investigate all the features of the L6470 device.

In particular, the board can be used to check the voltage mode driving and to regulate the L6470 parameters in order to fit the application requirements.

Two or more EVAL6470 can be driven by a single communication board making the demonstration board suitable for the evaluation of L6470 in multi-motor applications.



1 Board description

Figure 1. EVAL6470 demonstration board jumper and connector locations

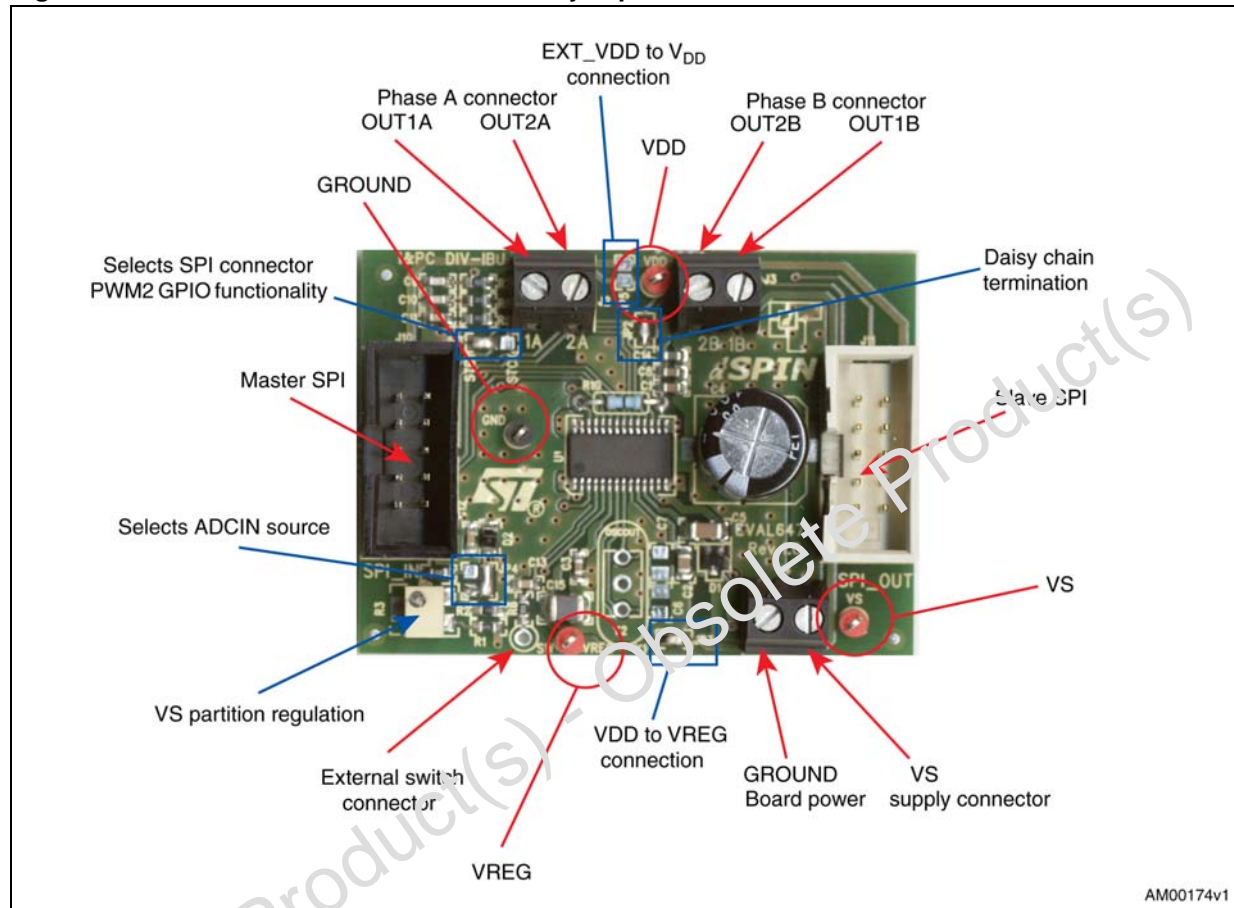


Table 1. EVAL6470: jumper and connector description

Name	Type	Function
J4	Power supply	Board power supply
J2	Power outputs	Bridge A outputs
J3	Power outputs	Bridge B outputs
J10	SPI connector	Master SPI connector
J11	SPI connector	Slave SPI connector
SW	NM test point	External switch connector
VS	Test point	Motor supply voltage
V _{REG}	Test point	Internal 3 V regulator output
V _{DD}	Test point	Logic interface voltage
GND	Test point	Ground
JP7	Jumper	Selects SPI connector PWM2 GPIO functionality
JP2	Jumper	Daisy chain termination
JP5	Jumper	EXT_VDD (SPI connector) to V _{DD} connection
JP3	Jumper	V _{DD} to V _{REG} connection
JP4	Jumper	Selects ADCIN source

Table 2. EVAL6470: master SPI connector pinout (J10)

Pin number	Description
1	L6470 BUSY open drain output
2	L6470 FLAG open drain output
3	Ground
4	EXT_VDD (can be used as external logic power supply)
5	SPI <i>master in, slave out</i> signal (connected to L6470 SDO output through daisy chain termination jumper JP2)
6	SPI serial clock signal (connected to L6470 CK input)
7	SPI <i>master out, slave in</i> signal (connected to L6470 SDI input)
8	SPI slave select signal (connected to L6470 CS input)
9	PWM1 input
10	PWM2 input

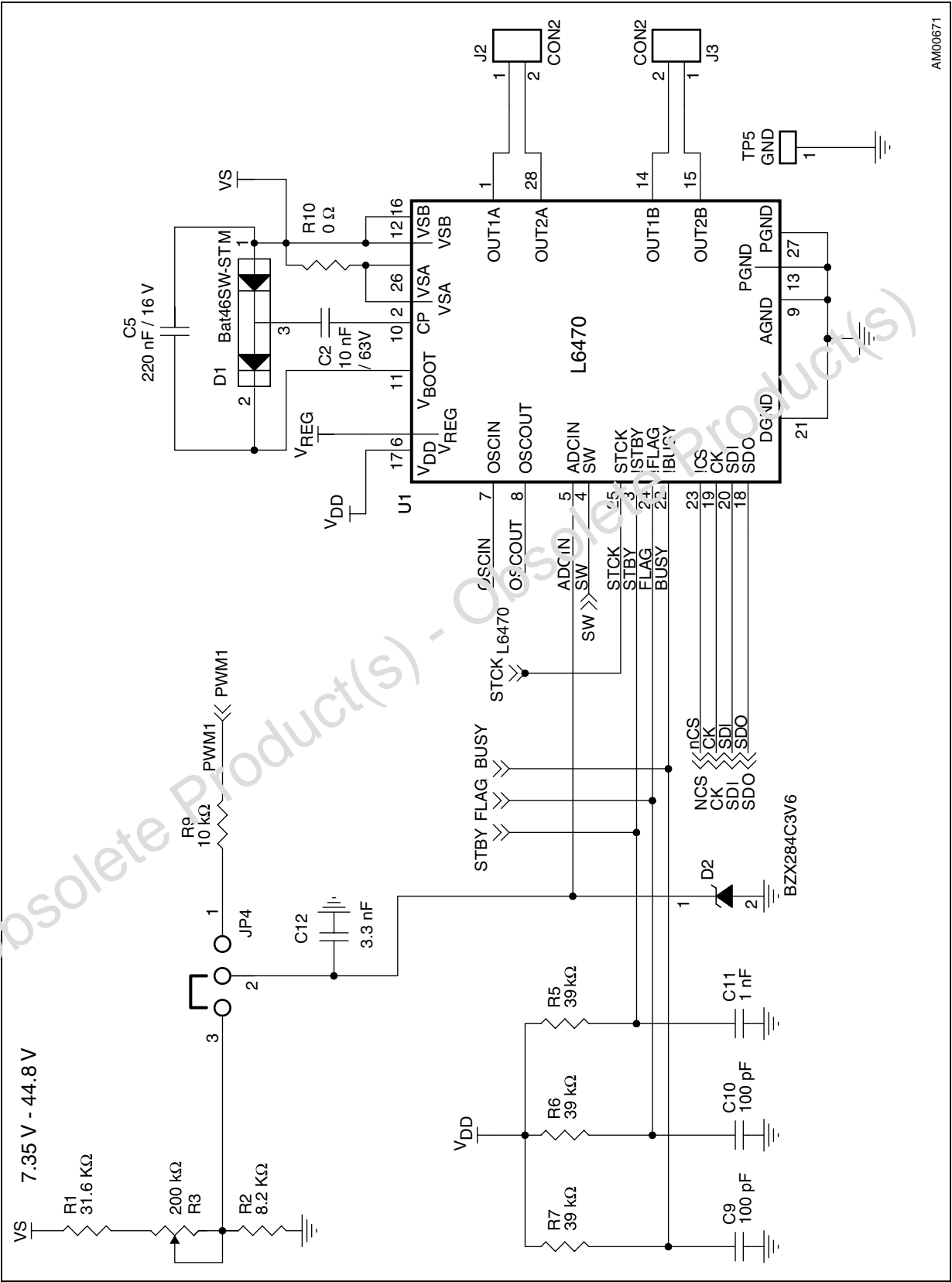
Table 3. EVAL6470: slave SPI connector pinout (J11)

Pin number	Description
1	L6470 BUSY open drain output
2	L6470 FLAG open drain output
3	Ground
4	EXT_VDD (can be used as external logic power supply)
5	SPI <i>master in, slave out</i> signal (connected to pin 5 of J10)
6	SPI serial clock signal (connected to L6470 CK input)
7	SPI <i>master out, slave in</i> signal (connected to L6470 SDO output)
8	SPI slave select signal (connected to L6470 CS input)
9	PWM1 input
10	PWM2 input

Table 4. EVAL6470: electrical specification (recommended values)

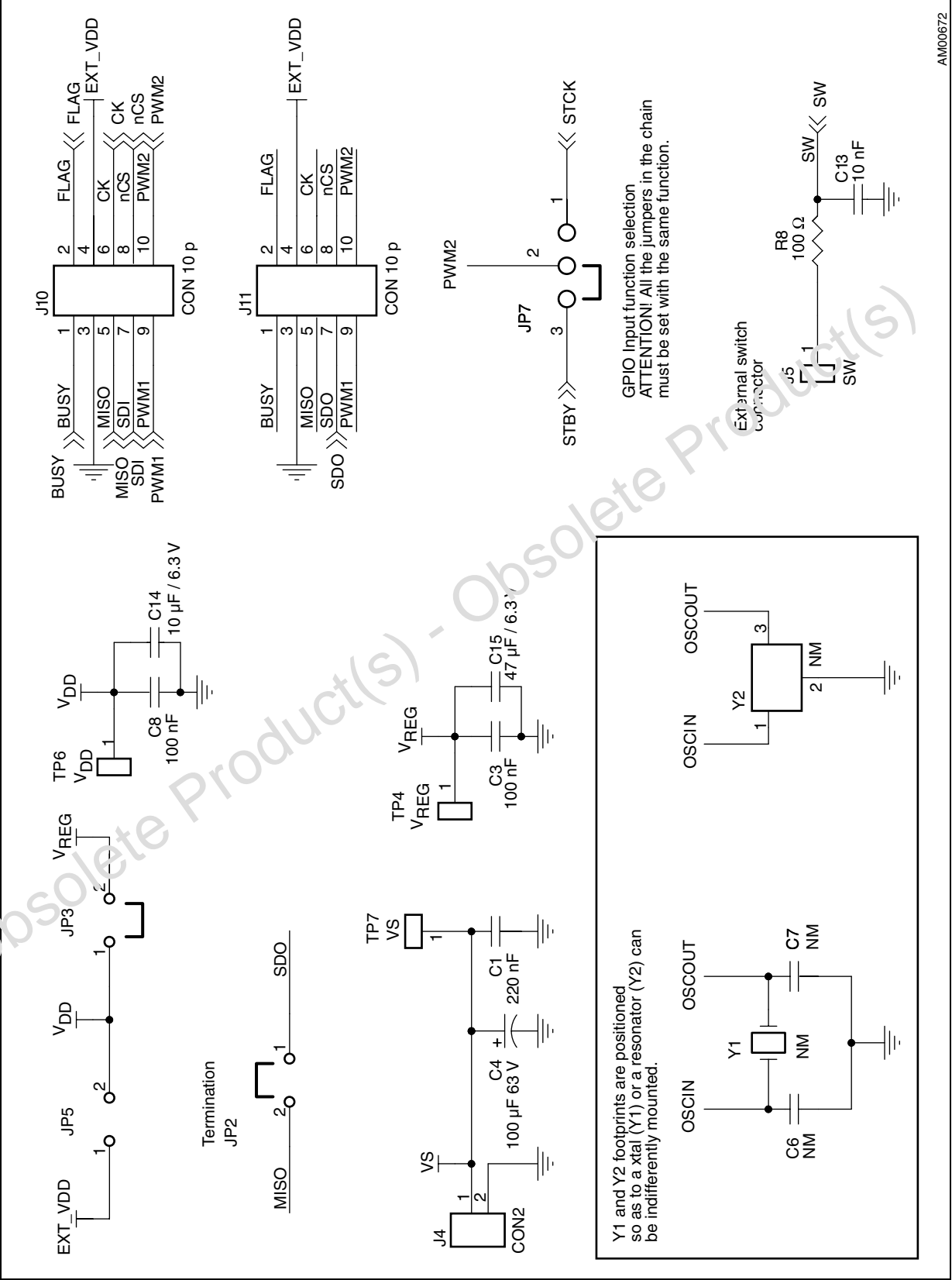
Parameter	Value
Supply voltage range (V_S)	8 to 45 V
Output current rating	Up to 3 A _{rms}
Logic supply voltage (V_{REG})	3.3 V (when externally supplied)
Logic interface voltage (V_{DD})	3.3 V or 5 V (when externally supplied)
Logic inputs voltage range	0 to +5 V
Operating temperature range	−25 to +125 °C
L6470H thermal resistance junction-to-ambient	40 °C/W

Figure 2. EVAL6470 schematic - part 1



AM00671

Figure 3. EVAL6470 schematic - part 2



AM00672

Table 5. EVAL6470: component list

Part reference	Part value	Part description
C1	100 nF	50 V ceramic capacitor
C2	10 nF	63 V ceramic capacitor
C3, C8	100 nF	Ceramic capacitor
C4	100 μ F	63 V electrolytic capacitor
C5	220 nF	16 V ceramic capacitor
C6, C7	NM	Ceramic capacitor
C9, C10	100 pF	Ceramic capacitor
C11	1 nF	Ceramic capacitor
C12	3.3 nF	Ceramic capacitor
C13	10 nF	Ceramic capacitor
C14	10 μ F	6.3 V ceramic capacitor
C15	47 μ F	6.3 V ceramic capacitor
D1	BAT46SW	Low drop diode couple
D2	BZX284C3V6	3.6 V Zener diode
JP2, JP3		Jumper 2 x 1
JP5		Jumper 2 x 1
JP4		Jumper 3 x 1
JP7		Jumper 3 x 1
J2, J3, J4		Connector
J5	NM	Strip pin
J10		Vertical 5 x 2 male connector
J11		Vertical 5 x 2 male connector
R1	31.6 k Ω	Resistor 1%
R2	8.2 k Ω	Resistor 1%
R5, R6, R7	39 k Ω	Resistor 1%
R9	10 k Ω	Resistor 1%
R3	200 k Ω	Trimmer
R8	100 Ω	Resistor 1%
R10	0 Ω	Resistor 1/8 W
TP5		Test point
TP4, TP6		Test point
U1	L6470H	L6470 dSPIN
Y1	NM	Crystal
Y2	NM	Ceramic resonator

Figure 4. EVAL6470 layout (top layer)

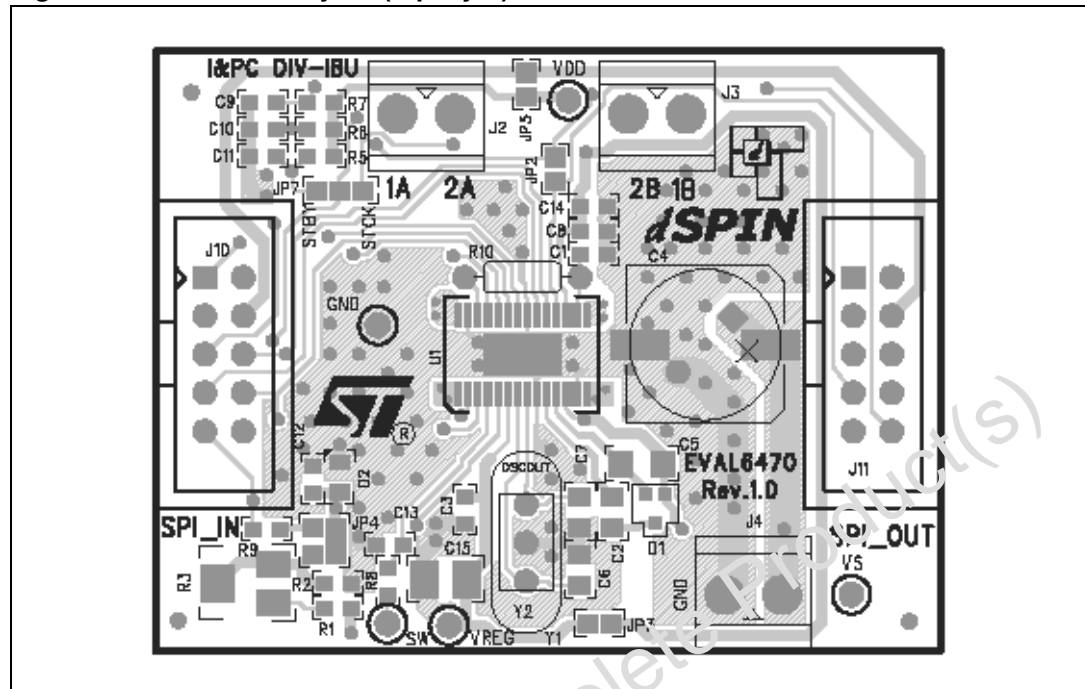
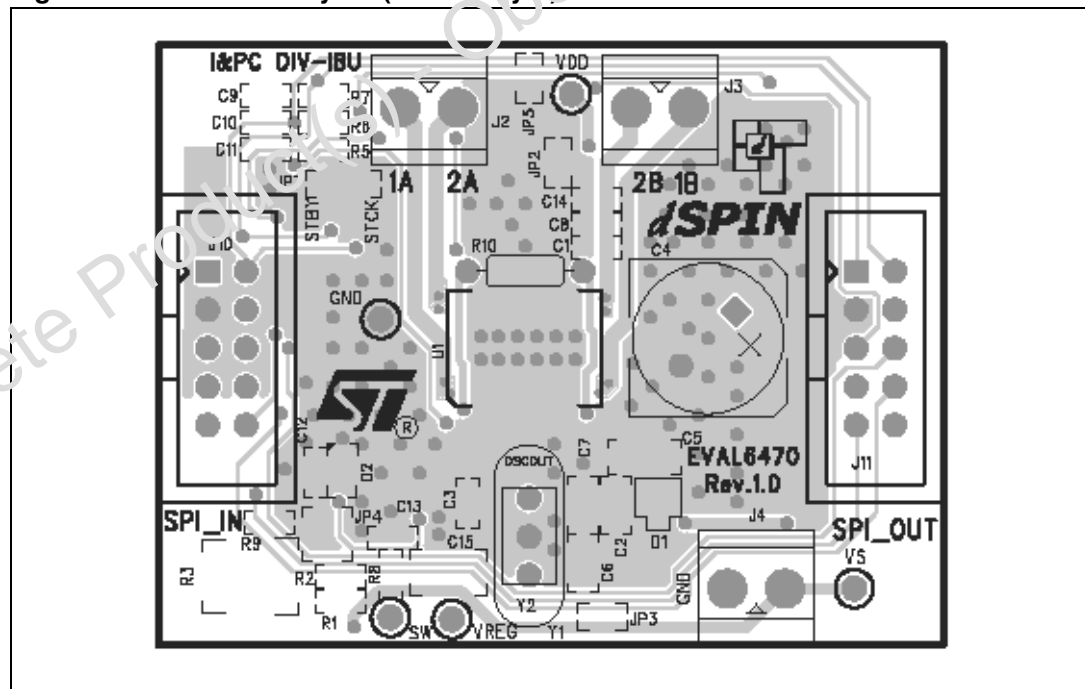


Figure 5. EVAL6470 layout (bottom layer)



2 Connection to IBU universal interface board

The EVAL6470 should be connected to the interface board (STEVAL-PCC009V2 or STEVAL-PCC009V1), and the following steps performed:

1. Connect the interface board to the PC through the USB cable
2. If requested, install interface board drivers
3. Verify interface board operation (check if operation LED diode is turned on)
4. Connect the interface board 10-pin connector to the EVAL6470 J10 connector (SPI_IN) through the 10-pole flat cable
5. Connect motor phases to the EVAL6470 J2 and J3 connectors
6. Connect the power supply (8 V to 45 V) to the EVAL6470 J4 connector
7. Start the dSPIN Evaluation tool.

2.1 Daisy-chain mode

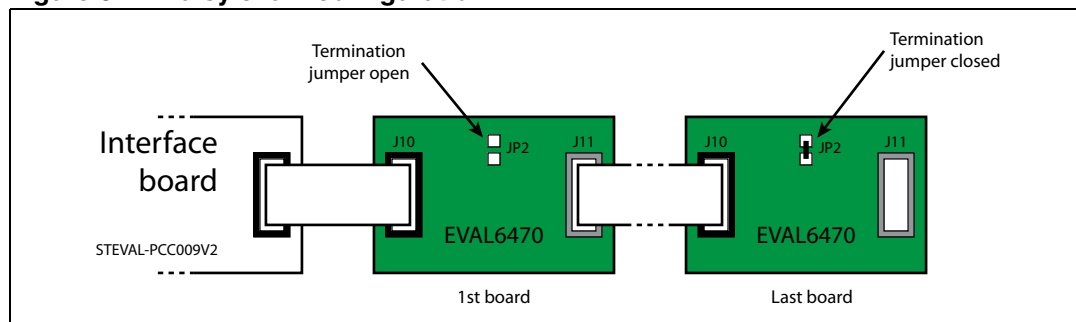
More EVAL6470 boards can be connected in daisy chain mode. This way you can control up to eight motors using a single communication board (STEVAL-PCC009V2 only).

To drive two or more boards in daisy chain configuration:

1. Connect the interface board to the PC through the USB cable
2. If requested, install the interface board drivers
3. Verify interface board operation (check if the operation LED diode is turned on)
4. Connect the interface board 10-pin connector to the first EVAL6470 J10 connector (SPI_IN) through the 10-pole flat cable
5. Open the JP2 jumper of EVAL6470
6. Connect the J11 connector (SPI_OUT) of the previous EVAL6470 to the J10 connector (SPI_IN) of the next one through the 10-pole flat cable
7. Repeat point 5 and 6 for all the others board of the chain but the last one.
8. Check the JP2 jumpers of EVAL6470 boards: all the jumpers but the last one should be opened
9. Check the JP7 jumpers of EVAL6470 boards: all the jumpers should be in the same configuration (STCK or STBY)

Caution: Increasing the number of devices connected in chain could degrade SPI communication performances. If communication issues are founded, try to reduce SPI clock speed.

Figure 6. Daisy chain configuration



3 Revision history

Table 6. Document revision history

Date	Revision	Changes
22-Mar-2010	1	Initial release.

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