

CYPRESS
SEMICONDUCTOR

T-46-23-12

CY7C132/CY7C136
CY7C142/CY7C1462048 x 8 Dual-Port
Static RAM

SRAMS

Features

- 0.8-micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- MASTER CY7C132/CY7C136 easily expands data bus width to 16 or more bits using SLAVE CY7C142/CY7C146
- **BUSY** output flag on CY7C132/CY7C136; **BUSY** input on CY7C142/CY7C146
- **INT** flag for port-to-port communication (52-pin LCC/PLCC versions)

Functional Description

The CY7C132/CY7C136/CY7C142/CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMS. Two ports are provided permitting independent access to any location in memory. The CY7C132/CY7C136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

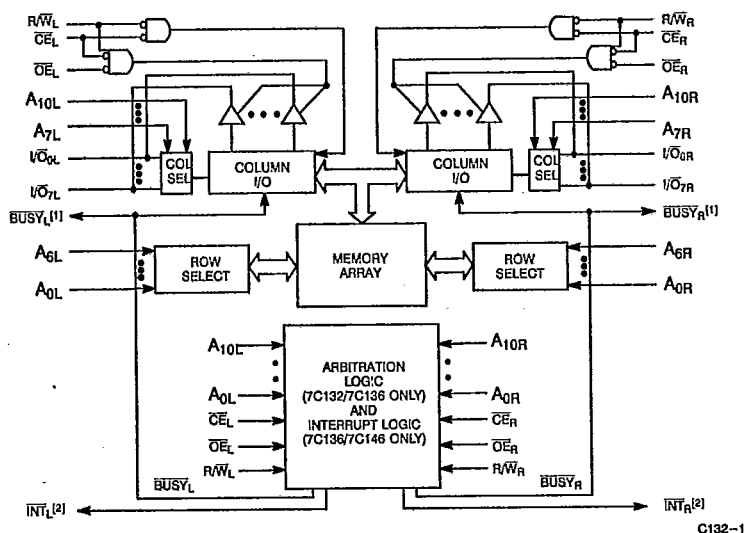
Each port has independent control pins; chip enable ($\overline{CE}$), write enable ($\overline{R/W}$), and

output enable ($\overline{OE}$). **BUSY** flags are provided on each port. In addition, an interrupt flag (**INT**) is provided on each port of the 52-pin LCC and PLCC versions. **BUSY** signals that the port is trying to access the same location currently being accessed by the other port. On the LCC/PLCC versions, **INT** is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C132/CY7C142 are available in both 48-pin DIP and 48-pin LCC. The CY7C136/CY7C146 are available in both 52-pin LCC and 52-pin PLCC.

Logic Block Diagram



Pin Configuration

DIP Top View			
$\overline{CE}_L$	1	48	V_{CC}
$\overline{R/W}_L$	2	47	$\overline{CE}_R$
BUSY _L	3	46	$\overline{R/W}_R$
A_{10L}	4	45	BUSY _R
$\overline{OE}_L$	5	44	A_{10R}
A_{0L}	6	43	$\overline{OE}_R$
A_{1L}	7	42	A_{0R}
A_{2L}	8	41	A_{1R}
A_{3L}	9	40	A_{2R}
A_{4L}	10	39	A_{3R}
A_{5L}	11	38	A_{4R}
A_{6L}	12	37	A_{5R}
A_{7L}	13	36	A_{6R}
A_{8L}	14	35	A_{7R}
A_{9L}	15	34	A_{8R}
V_{O0L}	16	33	A_{9R}
V_{O1L}	17	32	V_{O7R}
V_{O2L}	18	31	V_{O6R}
V_{O3L}	19	30	V_{O5R}
V_{O4L}	20	29	V_{O4R}
V_{O5L}	21	28	V_{O3R}
V_{O6L}	22	27	V_{O2R}
V_{O7L}	23	26	V_{O1R}
GND	24	25	V_{O0R}

C132-2

Notes:

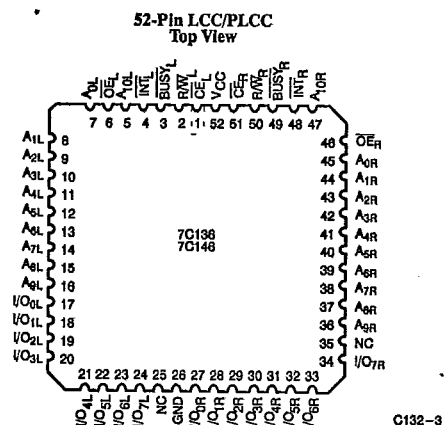
1. CY7C132/CY7C136 (Master): **BUSY** is open drain output and requires pull-up resistor.
CY7C142/CY7C146 (Slave): **BUSY** is input.
2. Open drain outputs; pull-up resistor required.



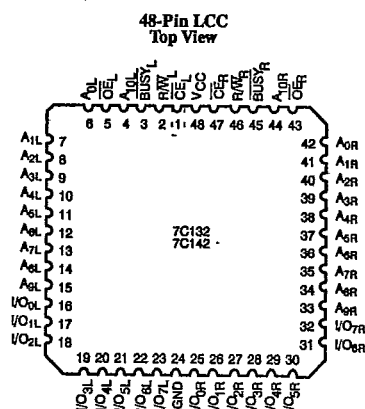
T-46-23-12

CY7C132/CY7C136
CY7C142/CY7C146

Pin Configurations (continued)



C132-3



C132-4

Selection Guide

		7C132-25 ^[3] 7C136-25 7C142-25 7C146-25	7C132-30 7C136-30 7C142-30 7C146-30	7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C

Ambient Temperature with
Power Applied - 55°C to +125°CSupply Voltage to Ground Potential
(Pin 48 to Pin 24) - 0.5V to +7.0VDC Voltage Applied to Outputs
in High Z State - 0.5V to +7.0V

DC Input Voltage - 3.5V to +7.0V

Output Current into Outputs (Low) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	- 40°C to +85°C	5V ± 10%
Military ^[4]	- 55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available in LCC and PLCC packages only.

4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range^[5]

Parameter	Description	Test Conditions	7C13225, 30 ^[3] 7C136-25,30 7C142-25,30 7C146-25,30		7C132-35 7C136-35 7C142-35 7C146-35		7C132-45,55 7C136-45,55 7C142-45,55 7C146-45,55		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 4.0 mA		0.4		0.4		0.4	V
		I _{OL} = 16.0 mA ^[7]		0.5		0.5		0.5	V
V _{IH}	Input HIGH Voltage		2.2		2.2		2.2		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[8]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	CE = V _{IL} , Outputs Open, f = f _{MAX} ^[6]	Com'l	170		120		90	mA
			Mil			170		120	mA
I _{SB1}	Standby Current Both Ports, TTL Inputs	CE _L and CE _R ≥ V _{IH} , f = f _{MAX} ^[6]	Com'l	65		45		35	mA
			Mil			65		45	mA
I _{SB2}	Standby Current One Port, TTL Inputs	CE _L or CE _R ≥ V _{IH} , Active Port Outputs Open, f = f _{MAX} ^[6]	Com'l	115		90		75	mA
			Mil			115		90	mA
I _{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports CE _L and CE _R ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0	Com'l	15		15		15	mA
			Mil			15		15	mA
I _{SB4}	Standby Current One Port, CMOS Inputs	One Port CE _L or CE _R ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, Active Port Outputs Open, f = f _{MAX} ^[6]	Com'l	105		85		70	mA
			Mil			105		85	mA

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Capacitance^[9]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	15	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

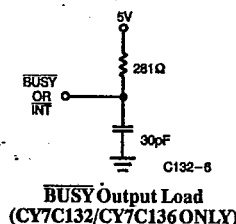
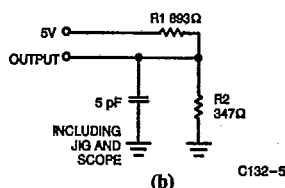
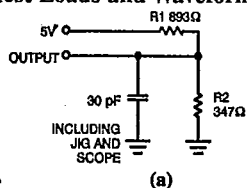
- See the last page of this specification for Group A subgroup testing information.
- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{RC} and using AC Test Waveforms input levels of GND to 3V.
- BUSY and INT pins only.
- Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
- AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.



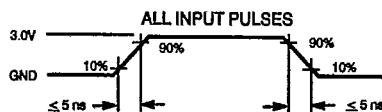
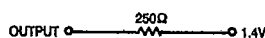
T-46-23-12

CY7C132/CY7C136
CY7C142/CY7C146

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range^[5,10]

Parameters	Description	7C132-25 ^[3]		7C132-30		7C132-35		7C132-45		7C132-55		Units
		7C136-25	7C136-30	7C136-35	7C136-45	7C136-55						
		7C142-25	7C142-30	7C142-35	7C142-45	7C142-55						
		7C146-25	7C146-30	7C146-35	7C146-45	7C146-55						
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	25		30		35		45		55		ns
t _{AA}	Address to Data Valid ^[11]		25		30		35		45		55	ns
t _{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t _{ACE}	CE LOW to Data Valid ^[11]		25		30		35		45		55	ns
t _{DOE}	OE LOW to Data Valid ^[11]		15		20		20		25		25	ns
t _{LZOE}	OE LOW to Low Z	3		3		3		3		3		ns
t _{HZOE}	OE HIGH to High Z ^[12]		15		15		20		20		25	ns
t _{LZCE}	CE LOW to Low Z ^[13]	5		5		5		5		5		ns
t _{HZCE}	CE HIGH to High Z ^[12,13]		15		15		20		20		25	ns
t _{PU}	CE LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	CE HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE ^[14]												
t _{WC}	Write Cycle Time	25		30		35		45		55		ns
t _{SCE}	CE LOW to Write End	20		25		30		35		40		ns
t _{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t _{HA}	Address Hold from Write End	2		2		2		2		2		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	R/W Pulse Width	15		25		25		30		30		ns
t _{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE}	R/W LOW to High Z		15		15		20		20		25	ns
t _{LZWE}	R/W HIGH to Low Z	0		0		0		0		0		ns



T-46-23-12

CY7C132/CY7C136
CY7C142/CY7C146

Switching Characteristics Over the Operating Range^[5,10] (continued)

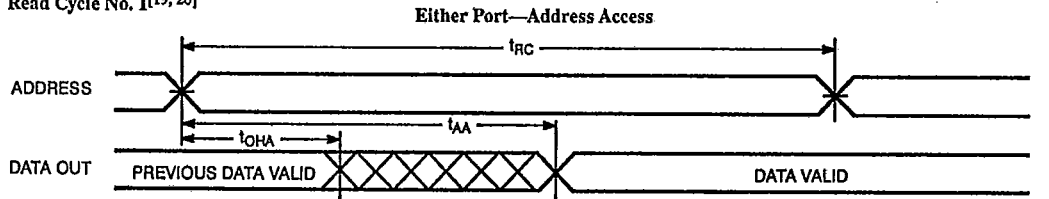
Parameters	Description	7C132-25 ^[3]		7C132-30		7C132-35		7C132-45		7C132-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
tBLA	BUSY LOW from Address Match		20		20		20		25		30	ns
tBHA	BUSY HIGH from Address Mismatch ^[15]		20		20		20		25		30	ns
tBLC	BUSY LOW from CE LOW		20		20		20		25		30	ns
tBHC	BUSY HIGH from CE HIGH ^[15]		20		20		20		25		30	ns
tPS	Port Set Up for Priority	5		5		5		5		5		ns
tWB ^[16]	R/W LOW after BUSY LOW	0		0		0		0		0		ns
tWH	R/W HIGH after BUSY HIGH	20		30		30		35		35		ns
tBDD	BUSY HIGH to Valid Data		25		30		35		45		45	ns
tDDD	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
tWDD	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING ^[18]												
tWINS	R/W to INTERRUPT Set Time		25		25		25		35		45	ns
tEINS	CE to INTERRUPT Set Time		25		25		25		35		45	ns
tINS	Address to INTERRUPT Set Time		25		25		25		35		45	ns
tOINR	OE to INTERRUPT Reset Time ^[15]		25		25		25		35		45	ns
tEINR	CE to INTERRUPT Reset Time ^[15]		25		25		25		35		45	ns
tINR	Address to INTERRUPT Reset Time ^[15]		25		25		25		35		45	ns

- Notes:
15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C142/CY7C146 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
- A. BUSY on Port B goes HIGH.
 - B. Port B's address toggled.
 - C. CE for Port B is toggled.
 - D. R/W for Port B is toggled during valid read.

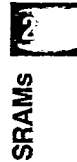
18. 52-pin LCC/PLCC versions only.
19. R/W is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. If $\overline{OE}$ is LOW during a R/W controlled write cycle, the write pulse width must be the larger of tp_{WE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD} .
23. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in a high-impedance state.

Switching Waveforms

Read Cycle No. 1^[19, 20]



C132-7





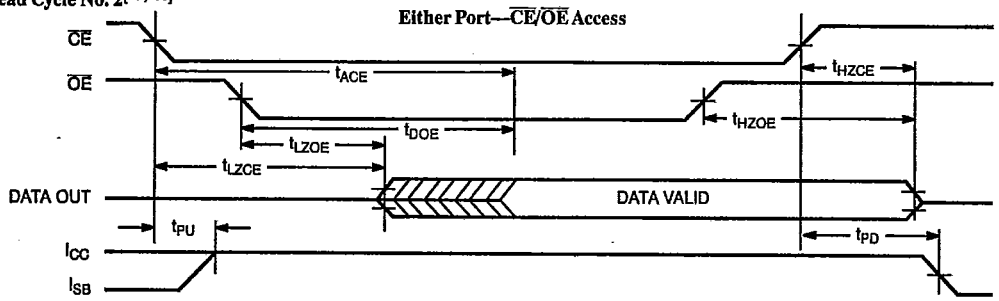
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CY7C132/CY7C136
CY7C142/CY7C146

Switching Waveforms (continued)

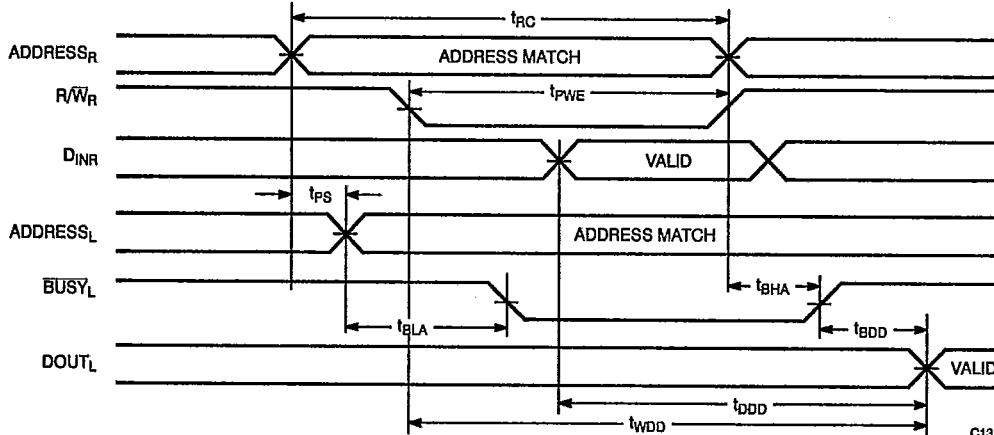
Read Cycle No. 2^[19, 21]



C132-8

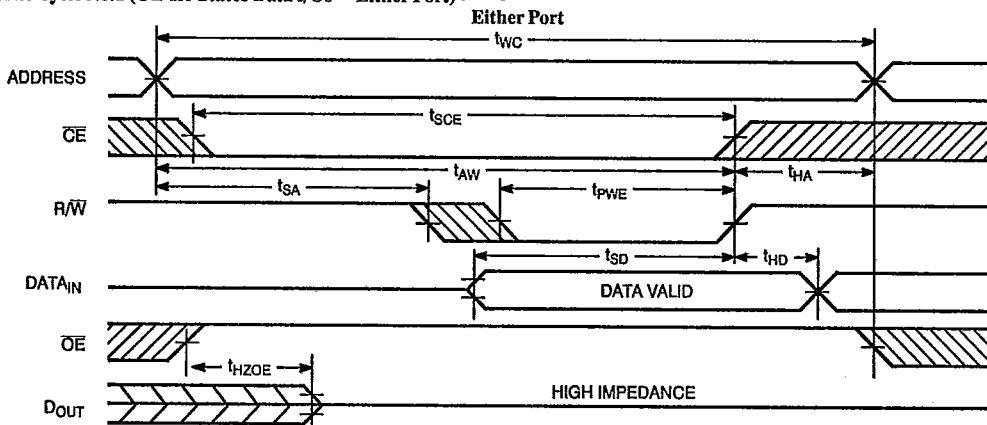
Read Cycle No. 3

Read with $\overline{\text{BUSY}}$ Master: CY7C132 and 7C136^[20]



C132-9

Write Cycle No.1 ($\overline{\text{OE}}$ Tri-States Data I/Os - Either Port) ^[14, 22]



C132-10

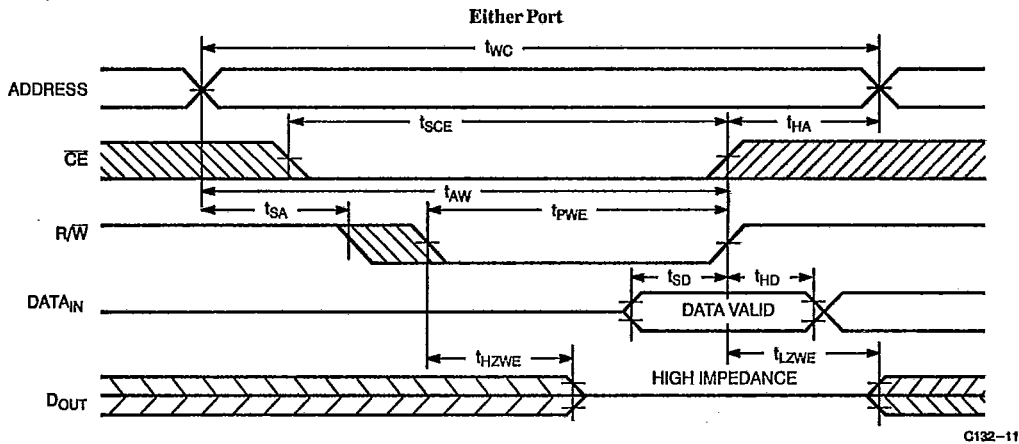


CY7C132/CY7C136
CY7C142/CY7C146

Switching Waveforms (continued)

T-46-23-12

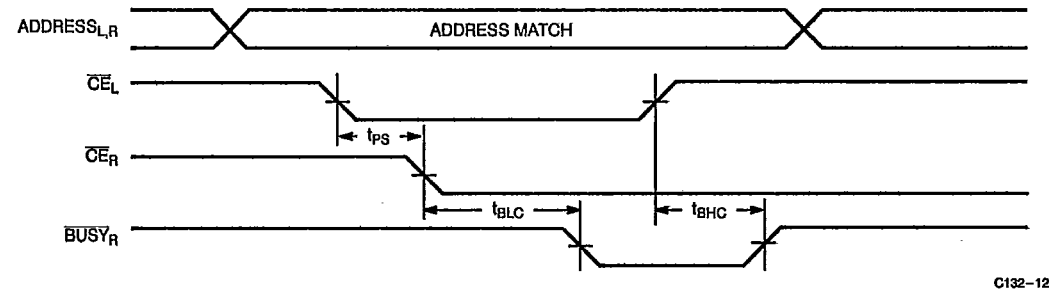
Write Cycle No. 2 (R/W Tri-States Data I/Os – Either Port)^[14,23]



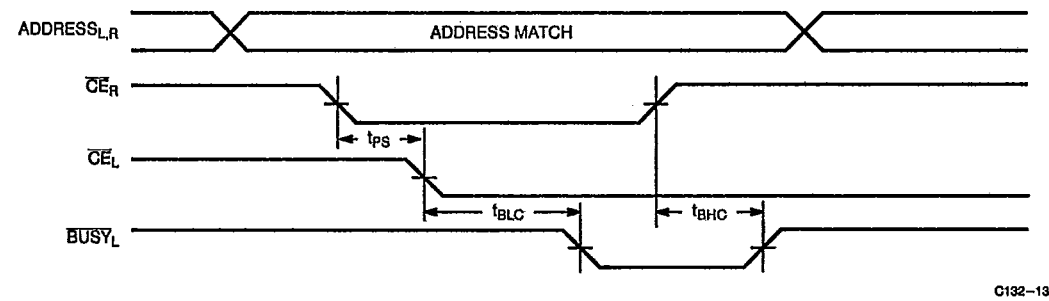
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Busy Timing Diagram No. 1 (CE Arbitration)

CE_L Valid First:



CE_R Valid First:



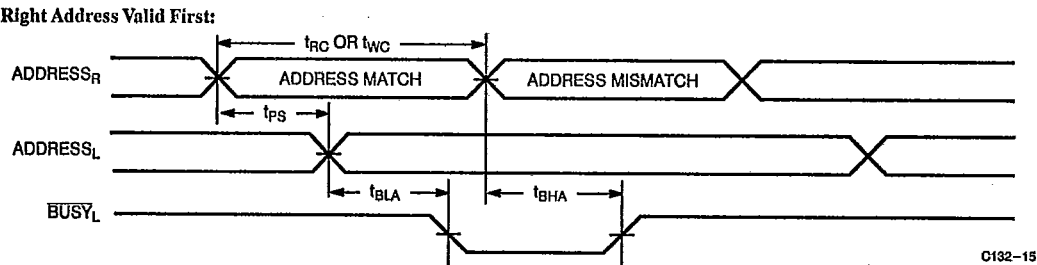
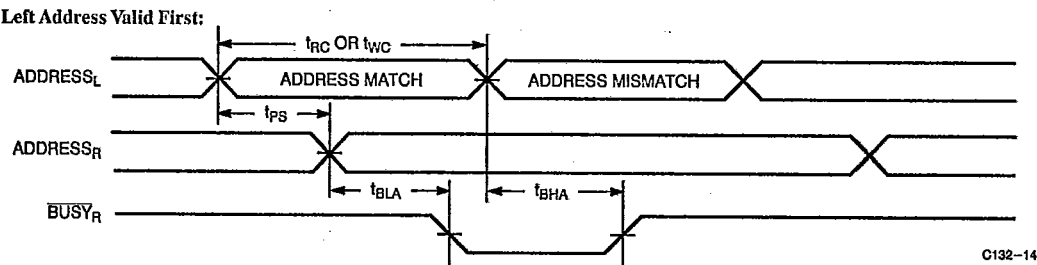


CY7C132/CY7C136
CY7C142/CY7C146

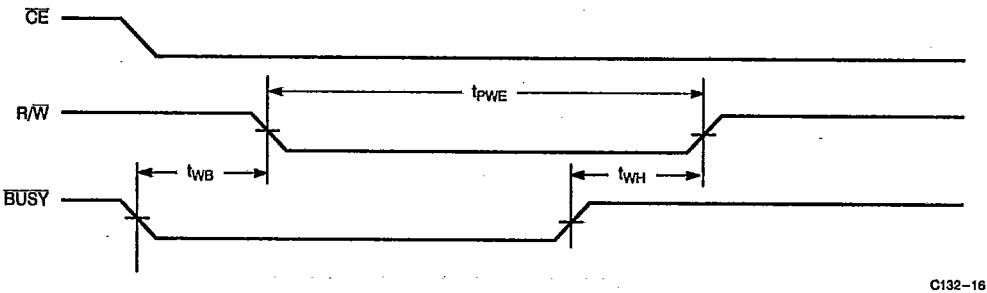
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

T-46-23-12



Busy Timing Diagram No. 3 (Write with $\overline{\text{BUSY}}$, Slave: CY7C142/CY7C146)





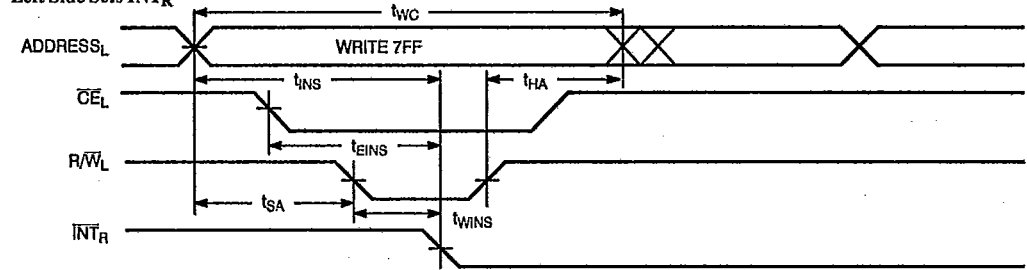
CY7C132/CY7C136
CY7C142/CY7C146

Switching Waveforms (continued)

T-46-23-12

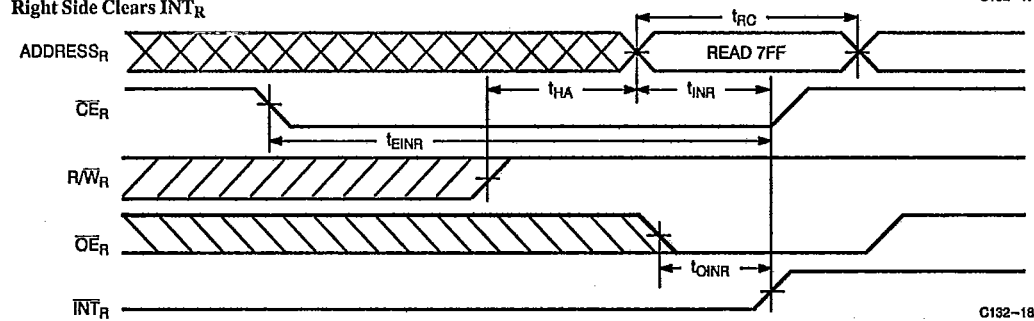
Interrupt Timing Diagrams^[18]

Left Side Sets $\overline{INT}_R$

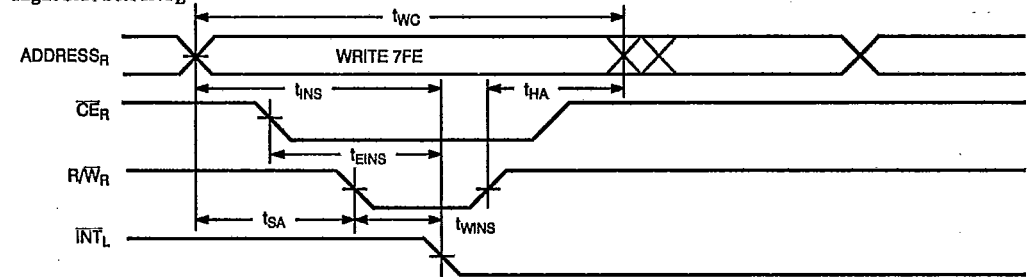


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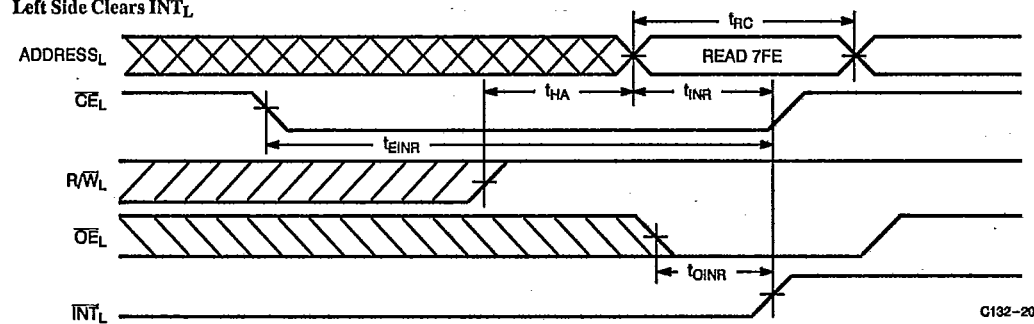
Right Side Clears $\overline{INT}_R$



Right Side Sets $\overline{INT}_L$



Left Side Clears $\overline{INT}_L$

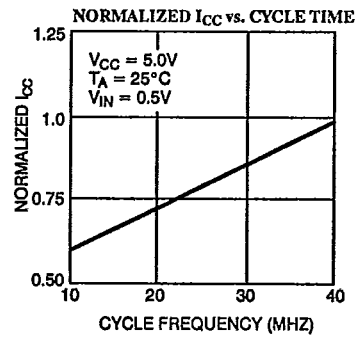
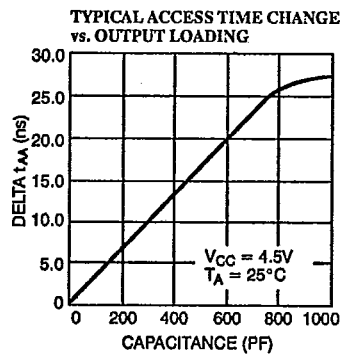
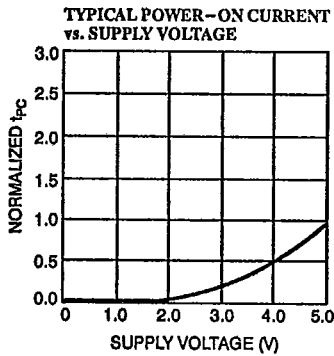
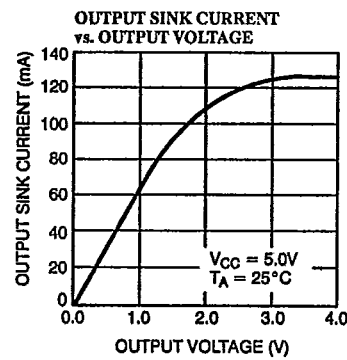
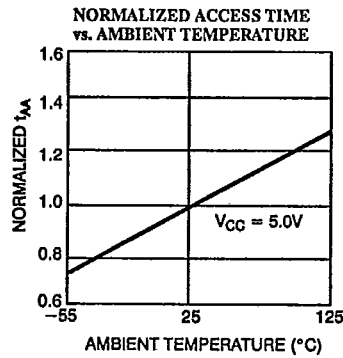
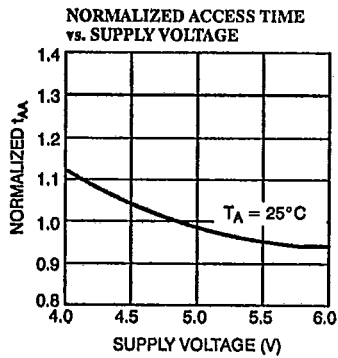
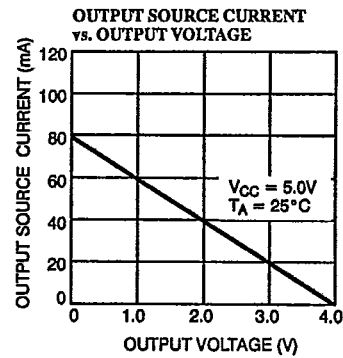
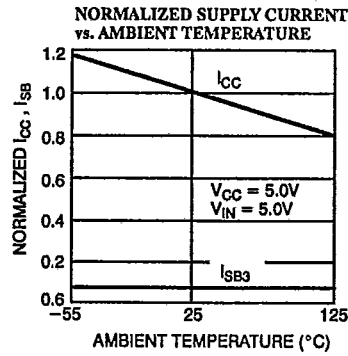
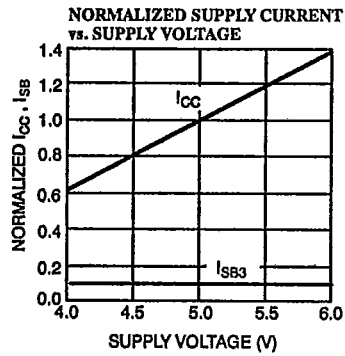




CY7C132/CY7C136
CY7C142/CY7C146

Typical DC and AC Characteristics

T-46-23-12





CY7C132/CY7C136
CY7C142/CY7C146

Ordering Information

T-46-23-12

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C132-25LC	L68	Commercial
30	CY7C132-30DC	D26	Commercial
	CY7C132-30LC	L68	
	CY7C132-30PC	P25	
	CY7C132-30DI	D26	Industrial
	CY7C132-30PI	P25	
35	CY7C132-35DC	D26	Commercial
	CY7C132-35LC	L68	
	CY7C132-35PC	P25	
	CY7C132-35DI	D26	Industrial
	CY7C132-35PI	P25	
	CY7C132-35DMB	D26	Military
	CY7C132-35FMB	F78	
	CY7C132-35LMB	L68	
45	CY7C132-45DC	D26	Commercial
	CY7C132-45LC	L68	
	CY7C132-45PC	P25	
	CY7C132-45DI	D26	Industrial
	CY7C132-45PI	P25	
	CY7C132-45DMB	D26	Military
	CY7C132-45FMB	F78	
	CY7C132-45LMB	L68	
55	CY7C132-55DC	D26	Commercial
	CY7C132-55LC	L68	
	CY7C132-55PC	P25	
	CY7C132-55DI	D26	Industrial
	CY7C132-55PI	P25	
	CY7C132-55DMB	D26	Military
	CY7C132-55FMB	F78	
	CY7C132-55LMB	L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C136-25JC	J69	Commercial
	CY7C136-25LC	L69	
30	CY7C136-30JC	J69	Commercial
	CY7C136-30LC	L69	
	CY7C136-30JI	J69	Industrial
35	CY7C136-35JC	J69	Commercial
	CY7C136-35LC	L69	
	CY7C136-35JI	J69	Industrial
	CY7C136-35LMB	L69	
45	CY7C136-45JC	J69	Commercial
	CY7C136-45LC	L69	
	CY7C136-45JI	J69	Industrial
	CY7C136-45LMB	L69	
55	CY7C136-55JC	J69	Commercial
	CY7C136-55LC	L69	
	CY7C136-55JI	J69	Industrial
	CY7C136-55LMB	L69	

SRAMS



T-46-23-12

CY7C132/CY7C136
CY7C142/CY7C146

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C142-25LC	L68	Commercial
30	CY7C142-30DC	D26	Commercial
	CY7C142-30LC	L68	
	CY7C142-30PC	P25	
	CY7C142-30DI	D26	Industrial
	CY7C142-30PI	P25	
35	CY7C142-35DC	D26	Commercial
	CY7C142-35LC	L68	
	CY7C142-35PC	P25	
	CY7C142-35DI	D26	Industrial
	CY7C142-35PI	P25	
	CY7C142-35DMB	D26	Military
	CY7C142-35FMB	F78	
	CY7C142-35LMB	L68	
45	CY7C142-45DC	D26	Commercial
	CY7C142-45LC	L68	
	CY7C142-45PC	P25	
	CY7C142-45DI	D26	Industrial
	CY7C142-45PI	P25	
	CY7C142-45DMB	D26	Military
	CY7C142-45FMB	F78	
	CY7C142-45LMB	L68	
55	CY7C142-55DC	D26	Commercial
	CY7C142-55LC	L68	
	CY7C142-55PC	P25	
	CY7C142-55DI	D26	Industrial
	CY7C142-55PI	P25	
	CY7C142-55DMB	D26	Military
	CY7C142-55FMB	F78	
	CY7C142-55LMB	L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C146-25JC	J69	Commercial
	CY7C146-25LC	L69	
30	CY7C146-30JC	J69	Commercial
	CY7C146-30LC	L69	
	CY7C146-30JI	J69	Industrial
35	CY7C146-35JC	J69	Commercial
	CY7C146-35LC	L69	
	CY7C146-35JI	J69	Industrial
	CY7C146-35LMB	L69	Military
45	CY7C146-45JC	J69	Commercial
	CY7C146-45LC	L69	
	CY7C146-45JI	J69	Industrial
	CY7C146-45LMB	L69	Military
55	CY7C146-55JC	J69	Commercial
	CY7C146-55LC	L69	
	CY7C146-55JI	J69	Industrial
	CY7C146-55LMB	L69	Military



MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
VOH	1, 2, 3
VOL	1, 2, 3
VIH	1, 2, 3
VIL Max.	1, 2, 3
IIX	1, 2, 3
IOZ	1, 2, 3
ICC	1, 2, 3
ISB1	1, 2, 3
ISB2	1, 2, 3
ISB3	1, 2, 3
ISB4	1, 2, 3



Switching Characteristics

Parameters	Subgroups
READ CYCLE	
tRC	7, 8, 9, 10, 11
tAA	7, 8, 9, 10, 11
tACE	7, 8, 9, 10, 11
tDOE	7, 8, 9, 10, 11
WRITE CYCLE	
tWC	7, 8, 9, 10, 11
tSCE	7, 8, 9, 10, 11
tAW	7, 8, 9, 10, 11
tHA	7, 8, 9, 10, 11
tSA	7, 8, 9, 10, 11
tPWE	7, 8, 9, 10, 11
tSD	7, 8, 9, 10, 11
tHD	7, 8, 9, 10, 11

Parameters	Subgroups
BUSY/INTERRUPT TIMING	
tBLA	7, 8, 9, 10, 11
tBHA	7, 8, 9, 10, 11
tBLC	7, 8, 9, 10, 11
tBHC	7, 8, 9, 10, 11
tps	7, 8, 9, 10, 11
tWINS	7, 8, 9, 10, 11
tEINS	7, 8, 9, 10, 11
tINS	7, 8, 9, 10, 11
tOINR	7, 8, 9, 10, 11
tEINR	7, 8, 9, 10, 11
tINR	7, 8, 9, 10, 11
BUSY TIMING	
tWB ^[24]	7, 8, 9, 10, 11
tWH	7, 8, 9, 10, 11
tBDD	7, 8, 9, 10, 11

Note:
24. CY7C142/CY7C146 only.
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