MC1600 Series (-30°C to +85°C)

The requirement for digital systems with ever higher performance has increased the need for high-speed integrated circuits. The industry has recognized that the only economical way to obtain high operating system speed is through the use of emitter-coupled logic. Motorola offers a state-of-the-art, emitter-coupled logic family with sub-nanosecond propagation delays – MECL III.

MECL III circuit design is similar to that used in the popular MECL 10,000 family. In the MECL III line, as well as MECL 10,000, advanced processing techniques are employed and the capability for driving low-impedance terminated lines is provided. MECL III is recommended for new designs.

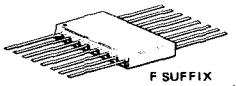
2

GENERAL FEATURES

- Gate Switching Speeds of 1.0 ns typical
- Capability of Driving Terminated Lines with Impedance as Low as 50 Ohms
- Flip-Flop Toggle Rate Greater Than 500 MHz
- Operation with Unused Inputs Left Open
- Multilayer Metalization for economy
- New Packages with Improved Electrical and Thermal Characteristics
- Compatibility with MECL 10,000 Series
- Counting Speeds to above 1 GHz

P SUFFIX
PLASTIC PACKAGE
CASE 646

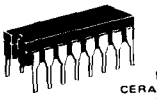
L SUFFIX
CERAMIC PACKAGE
CASE 632



F SUFFIX
CERAMIC PACKAGE
CASE 650

P SUFFIX
PLASTIC PACKAGE
CASE 648

F SUFFIX
CERAMIC PACKAGE
CASE 607



L SUFFIX
CERAMIC PACKAGE
CASE 620

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C unless otherwise noted.)

Function	Type ① -30° to +85°C	Loading Factor # Each Output	Propagation Delay 50-ohm Load ns typ	Power Dissipation (No Load) mW typ/pkg	Case
Voltage Controlled Oscillator	MC1648	–	*225 MHz typ	150	607,632,646
Dual A/D Comparator	MC1650	70	3.5	275	620,650
Dual A/D Comparator	MC1651	70	3.0	275	620,650
Binary Counter	MC1654	70	*325 MHz typ	750 ⌐⌐⌐	620
Voltage-Controlled Multivibrator	MC1658	70	*150 MHz typ	125	620,648,650
Dual 4-Input OR/NOR Gate	MC1660	70	1.1	120	620,650
Quad 2-Input NOR Gate	MC1662	70	1.1	240	620,650
Quad 2-Input OR Gate	MC1664	70	1.1	240	620,650
Dual Clocked R-S Flip-Flop	MC1666	70	1.8	220	620,650
Dual Clocked Latch	MC1668	70	1.8	220	620,650
Master-Slave Type D Flip-Flop	MC1670	70	*350 MHz typ	220	620,650
Triple 2-Input Exclusive OR Gate	MC1672	70	1.3	220	620,650
Triple 2-Input Exclusive NOR Gate	MC1674	70	1.3	220	620,650
Bi-Quinary Counter	MC1678	70	*350 MHz typ	750 ⌐⌐⌐	620
Dual 4-5-Input OR/NOR Gate	MC1688	70	0.8	125	650
UHF Prescaler Type D Flip-Flop	MC1690	70	*500 MHz min	200	620,650
Quad Line Receiver	MC1692	70	1.1	220	620,650
4-Bit Shift Register	MC1694	70	*325 MHz typ	750 ⌐⌐⌐	620
1 GHz Divide-By-Ten Counter	MC1696	–	*1 GHz min	650	650

① L suffix denotes Dual In-Line Ceramic Package, F suffix denotes Ceramic Flat Package, P suffix denotes Dual In-Line Plastic Package. (i.e., MC1600L = Ceramic Dual In-Line Package, MC1600F = Ceramic Flat Package, MC1600P = Plastic Dual In-Line Package).

⌐⌐⌐ Requires Heat Sink – IERC-LIC-214A2WCB or equivalent.

*Toggle Frequency

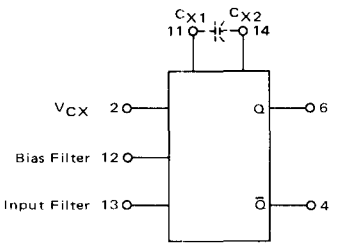
#DC Loading Factors are based on:

1. Full load output current, I_L = -25 mAdc max
2. Maximum input current, I_{in} = 350 μAdc

2

MULTIVIBRATOR

MC1658
Voltage-Controlled Multivibrator

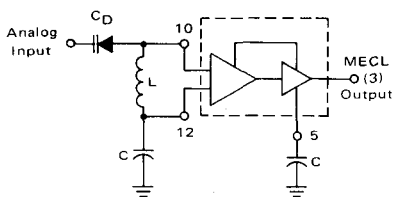


V_{CC1} = Pin 1
V_{CC2} = Pin 5
V_{EE} = Pin 6

Operating Frequency = 150 MHz typ
P_D = 125 mW typ/pkg

OSCILLATOR

MC1648
Emitter Coupled Oscillator



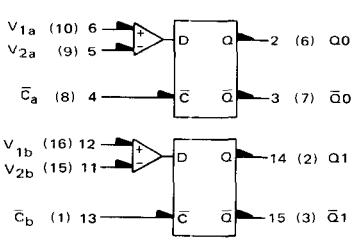
V_{CC} = Pins 1, 14
V_{EE} = Pins 7, 8

Operating Frequency = 225 MHz typ
P_D = 150 mW typ/pkg
(+5.0 Vdc Supply)

L, C, C_D are external components.
C_D is a varactor diode.

COMPARATOR

MC1650
MC1651
Dual A/D Comparator

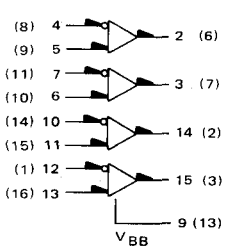


t_{pd} = 3.5 ns typ (MC1650)
3.0 ns typ (MC1651)
P_D = 330 mW typ/pkg (No load)

V_{CC} = +5.0 V = Pin 7,10 - (11), (14)
V_{EE} = -5.2 V = Pin 8 (12)
Gnd = Pin 1, 16 (4) (5)

RECEIVER

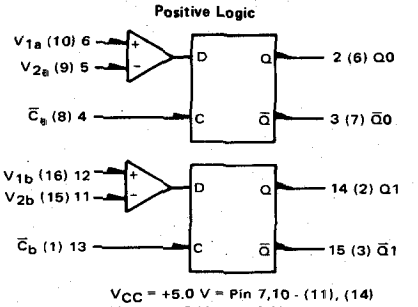
MC1692
Quad Line Receiver



t_{pd} = 0.9 ns typ (510-ohm load)
1.1 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No load)

DUAL A/D COMPARATOR

MC1650 • MC1651



V_{CC} = +5.0 V = Pin 7,10 - (11), (14)
V_{EE} = -5.2 V = Pin 8 (12)
Gnd = Pin 1,16 (4) (5)

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (MC1650)
  = 3.0 ns typ (MC1651)
- Input Slew Rate = 350 V/μs (MC1650)
  = 500 V/μs (MC1651)
- Differential Input Voltage:
  -5.0 V to +5.0 V (-30°C to +85°C)
- Common Mode Range:
  -3.0 V to +2.5 V (-30°C to +85°C) (MC1651)
  -2.5 V to +3.0 V (-30°C to +85°C) (MC1650)
- Resolution: ≤20 mV (-30°C to +85°C)
- Drives 50 Ω lines

Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC-1651 is a lower impedance option, with higher input slew rate and higher speed capability.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$) operate from MECL III or MECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

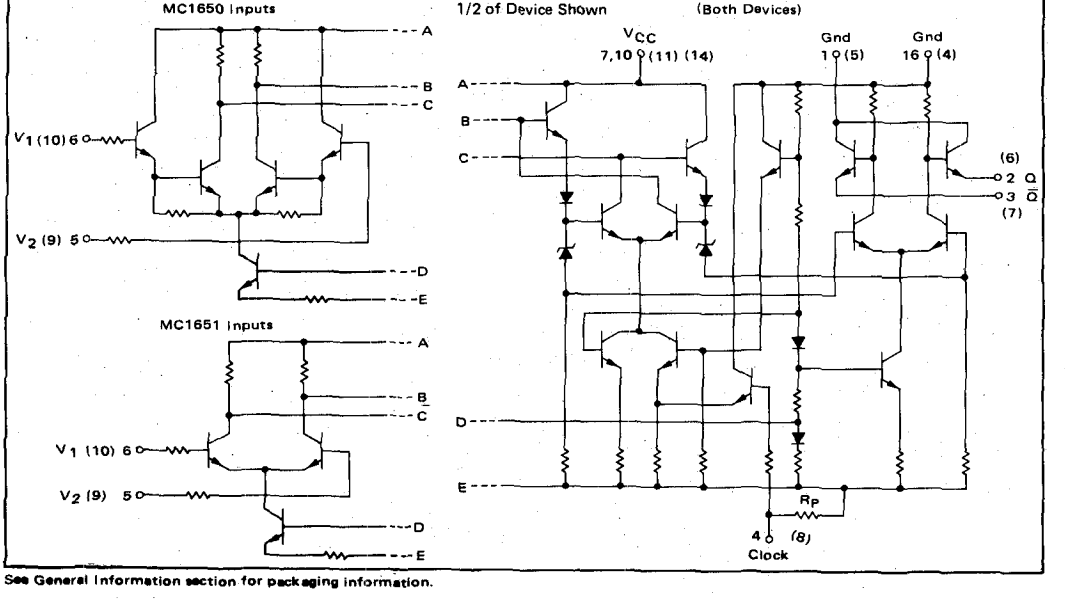
Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 3 and 6.

TRUTH TABLE

$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

CIRCUIT SCHEMATIC

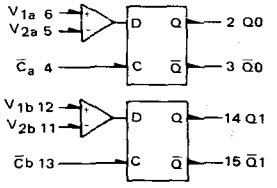


See General Information section for packaging information.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

POSITIVE LOGIC



L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

Characteristic	Symbol	Pin Under Test	MC1650L/1651L Test Limits ① -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
Power Supply Drain Current																						
Positive	I_{CC}	7,10	–	–	–	25*	–	–	mAdc	–	4,13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Negative	I_E	8	–	–	–	55*	–	–	mAdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Input Current	I_{in}																					
MC1650		6	–	–	–	10	–	–	μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
MC1651		6	–	–	–	40	–	–	μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
Input Leakage Current	I_R																					
MC1650		6	–	–	–	7	–	–	μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
MC1651		6	–	–	–	10	–	–	μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
Input Clock Current	$I_{in}H$	4	–	–	–	350	–	–	μAdc	4	13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
	$I_{in}L$	4	–	–	0.5	–	–	–	μAdc	–	13	–	–	6,12	–	–	–	–	–	7,10	4,8	1,5,11,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
		2												–	5,11	–	–	–	–			1,6,12,16
		2												–	–	6,12	5,11	–	–			1,16
		2												–	–	–	–	5,11	6,12			1,16
		3												–	6,12	–	–	–	–			1,5,11,16
		3												5,11	–	–	–	–	–			1,6,12,16
		3												–	–	5,11	6,12	–	–			1,16
		3												–	–	–	–	6,12	5,11			1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13	–	–	–	–	6,12	–	–	–	–	7,10	8	1,5,11,16
		2												5,11	–	–	–	–	–			1,6,12,16
		2												–	–	5,11	6,12	–	–			1,16
		2												–	–	–	–	6,12	5,11			1,16
		3												6,12	–	–	–	–	–			1,5,11,16
		3												–	5,11	–	–	–	–			1,6,12,16
		3												–	–	6,12	5,11	–	–			1,16
		3												–	–	–	–	5,11	6,12			1,16
Logic "1" Threshold Voltage ②	V_{OHA}	1	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
		2		–		–		–		–		–	4	–	6	–	–	–	–			
		3		–		–		–		–		4	–	–	6	–	–	–	–			
		4		–		–		–		–		–	4	6	–	–	–	–	–			
Logic "0" Threshold Voltage ②	V_{OLA}	1	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
		2	–		–		–			–		–	4	–	6	–	–	–	–			
		3	–		–		–			–		4	–	–	6	–	–	–	–			
		4	–		–		–			–		–	4	6	–	–	–	–	–			

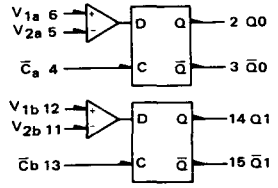
NOTES: ① All data is for ½ MC1650 or MC1651, except data marked (*) which refers to the entire package.
② These tests done in order indicated. See Figure 4.
③ Maximum Power Supply Voltages (beyond which device life may be impaired):
$|V_{EE}| + |V_{CC}| \leq 12$ Vdc.

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
MC1650	+3.000	+2.980	-2.500	-2.480
MC1651	+2.500	+2.480	-3.000	-2.980

SWITCHING TIMES

POSITIVE LOGIC



L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts)							
	V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	
-30°C	+2.000	See Note ④		+1.040	+2.00	+7.00	-3.20	See Figure 2
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20	
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20	

Characteristic	Symbol	Pin Under Test	MC1650L/1651L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	P1	P2	P3	P4
Switching Times Propagation Delay (50% to 50%) V-Input to Output	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{6+2+}	2								–	5	–					–	6	–	–
	t_{6+2+}	2								–	–	5					–	–	6	–
	t_{6+3-}	3								5	–	–					6	–	–	–
	t_{6+3-}	3								–	5	–					–	6	–	–
	t_{6+3-}	3								–	–	5					–	–	6	–
	t_{6-2-}	2								5	–	–					6	–	–	–
	t_{6-2-}	2								–	5	–					–	6	–	–
	t_{6-2-}	2								–	–	5					–	–	6	–
	t_{6-3+}	3								5	–	–					6	–	–	–
	t_{6-3+}	3								–	5	–					–	6	–	–
	t_{6-3+}	3								–	–	5					–	–	6	–
Clock to Output ②	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
	t_{4+2-}	2								6	–	–	–				5	–	–	
	t_{4+3+}	3								6	–	–	–				5	–	–	
	t_{4+3-}	3								5	–	–	–				6	–	–	
Clock Enable Time ③	t_{setup}	6	–	–	2.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Clock Aperture Time ③	t_{ap}	6	–	–	1.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Rise Time (10% to 90%)	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
Fall Time (10% to 90%)	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–

NOTES: ① Maximum Power Supply Voltages (beyond which device life may be impaired:
$|V_{CC}| + |V_{EE}| \leq 12$ Vdc.

② Unused clock inputs may be tied to ground.

③ See Figure 8.

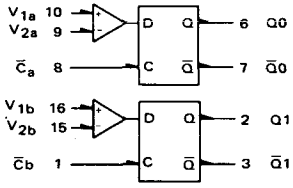
④

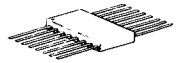
All Temperatures	V_{R2}	V_{R3}
MC1650	+4.900	-0.400
MC1651	+4.400	-0.900

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

POSITIVE LOGIC





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts)											
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

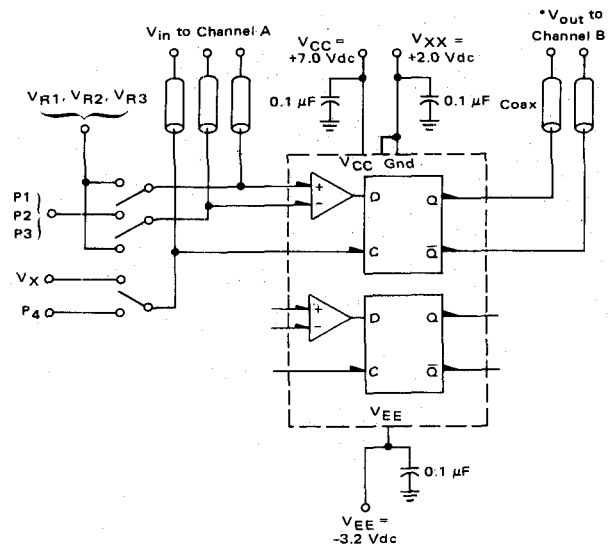
Characteristic	Symbol	Pin Under Test	MC1650F/1651F Test Limits ① -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
Power Supply Drain Current																						
Positive	I_{CC}	11,14	–	–	–	25*	–	–	mAdc	–	1,8	–	–	10,16	–	–	–	–	–	11,14	12	4,5,9,15
Negative	I_E	12	–	–	–	55*	–	–	mAdc	1,8	–	–	–	10,16	–	–	–	–	–	11,14	12	4,5,9,15
Input Current	I_{in}																					
MC1650		10	–	–	–	10	–	–	μAdc	8	1	–	–	16	–	10	–	–	–	11,14	12	4,5,9,15
MC1651		10	–	–	–	40	–	–	μAdc	8	1	–	–	16	–	10	–	–	–	11,14	12	4,5,9,15
Input Leakage Current	I_R																					
MC1650		10	–	–	–	7	–	–	μAdc	8	1	–	–	16	–	–	–	10	–	11,14	12	4,5,9,15
MC1651		10	–	–	–	10	–	–	μAdc	8	1	–	–	16	–	–	–	10	–	11,14	12	4,5,9,15
Input Clock Current	I_{inH}	8	–	–	–	350	–	–	μAdc	8	1	–	–	10,16	–	–	–	–	–	11,14	12	4,5,9,15
	I_{inL}	8	–	–	0.5	–	–	–	μAdc	–	1	–	–	10,16	–	–	–	–	–	11,14	8,12	4,5,9,15
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	1,8	–	–	–	10,16	–	–	–	–	–	11,14	12	4,5,9,15
		6									–	–	–	–	9,15	–	–	–	–			4,5,10,16
		6									–	–	–	–	–	10,16	9,15	–	–			4,5
		6									–	–	–	–	–	–	–	9,15	10,16			4,5
		7									–	–	–	–	10,16	–	–	–	–			4,5,9,15
		7									–	–	–	9,15	–	–	–	–	–			4,5,10,16
		7									–	–	–	–	–	9,15	10,16	–	–			4,5
		7									–	–	–	–	–	–	–	10,16	9,15			4,5
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	1,8	–	–	–	–	10,16	–	–	–	–	11,14	12	4,5,9,15
		6									–	–	–	9,15	–	–	–	–	–			4,5,10,16
		6									–	–	–	–	–	9,15	10,16	–	–			4,5
		6									–	–	–	–	–	–	–	10,16	9,15			4,5
		7									–	–	–	10,16	–	–	–	–	–			1,5,11,16
		7									–	–	–	–	9,15	–	–	–	–			1,6,12,16
		7									–	–	–	–	–	10,16	9,15	–	–			1,16
		7									–	–	–	–	–	–	–	9,11	10,16			1,16
Logic "1" Threshold Voltage ②	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	1	8	–	10	–	–	–	–	–	11,14	12	4,5,9
		6		–		–		–		–		–	8	–	10	–	–	–	–			
		7		–		–		–		–		8	–	–	10	–	–	–	–			
		7		–		–		–		–		–	8	10	–	–	–	–	–			
Logic "0" Threshold Voltage ②	V_{OLA}	7	–	-1.630	–	-1.600	–	-1.555	Vdc	–	1	8	–	10	–	–	–	–	–	11,14	12	4,5,9
		7	–		–		–			–		–	8	–	10	–	–	–	–			
		6	–		–		–			–		8	–	–	10	–	–	–	–			
		6	–		–		–			–		–	8	10	–	–	–	–	–			

NOTES: ① All data is for ½ MC1650 or MC1651, except data marked (*) which refers to the entire package.
② These tests done in order indicated. See Figure 4.
③ Maximum Power Supply Voltages (beyond which device life may be impaired):
$|V_{EE}| + |V_{CC}| \leq 12$ Vdc.

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
MC1650	+3.000	+2.980	-2.500	-2.480
MC1651	+2.500	+2.480	-3.000	-2.980

FIGURE 1 – SWITCHING TIME TEST CIRCUIT @ 25°C



50-ohm termination to ground located in each scope channel input
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

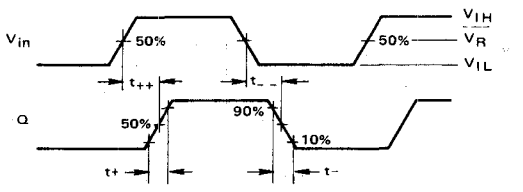
*Complement of output under test should always be loaded with 50-ohms to ground.

4

FIGURE 2 – SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output



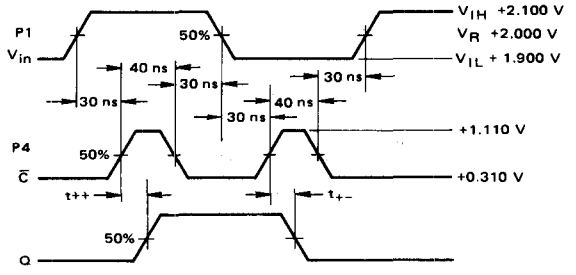
Test pulses: $t_+, t_- = 1.5 \pm 0.2$ ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle
V_{IH} is applied to $\overline{C}$ during tests.

4

TEST PULSE LEVELS

	Pulse 1		Pulse 2		Pulse 3	
	MC1650	MC1651	MC1650	MC1651	MC1650	MC1651
V_{IH}	+2.100 V	+2.100 V	+5.000 V	+4.500 V	-0.300 V	-0.800 V
V_R	+2.000 V	+2.000 V	+4.900 V	+4.400 V	-0.400 V	-0.900 V
V_{IL}	+1.900 V	+1.900 V	+4.800 V	+4.300 V	-0.500 V	-1.000 V

Clock to Output



P4: $t_+, t_- = 1.5 \pm 0.2$ ns.

FIGURE 3 – PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE

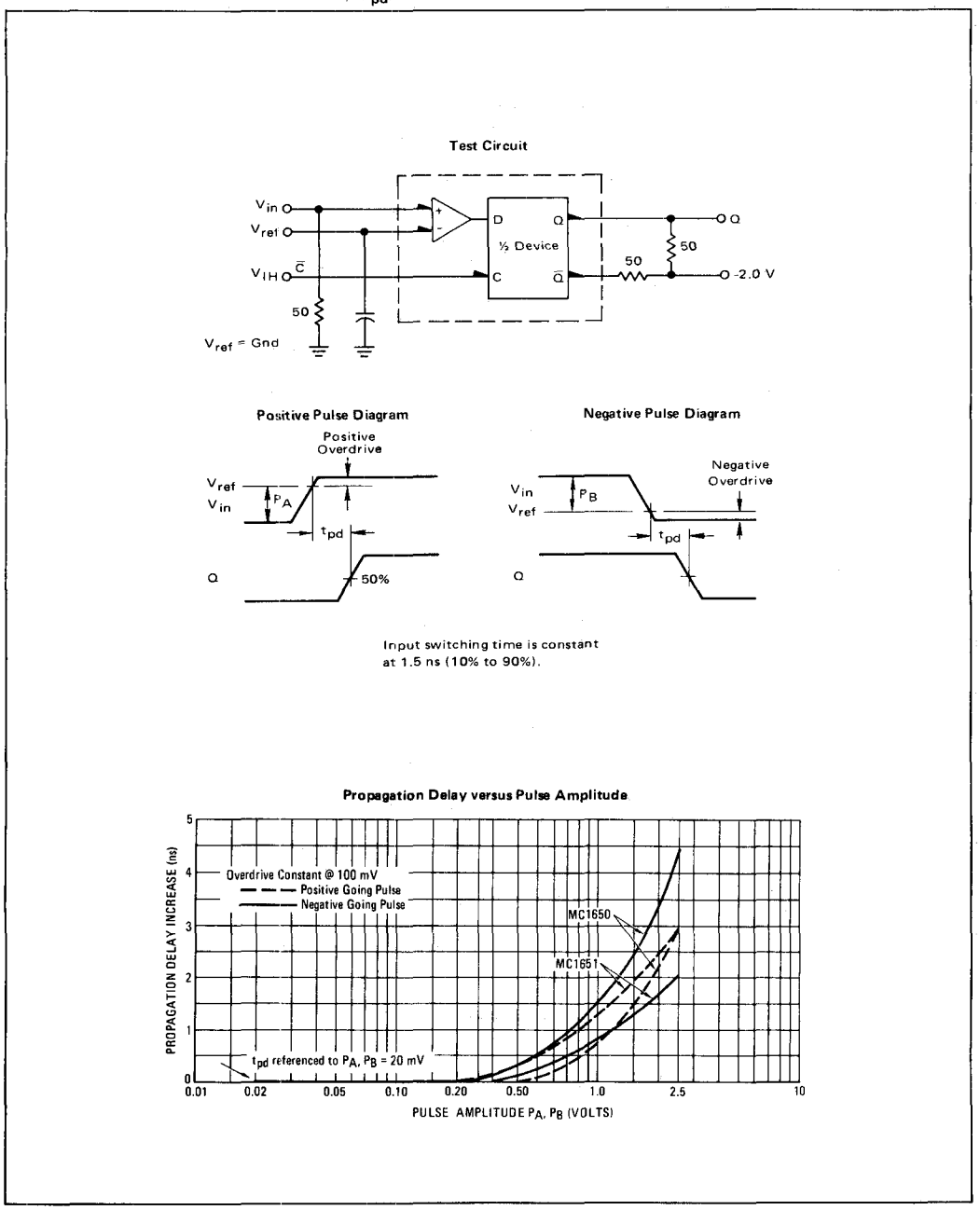


FIGURE 3 (continued)

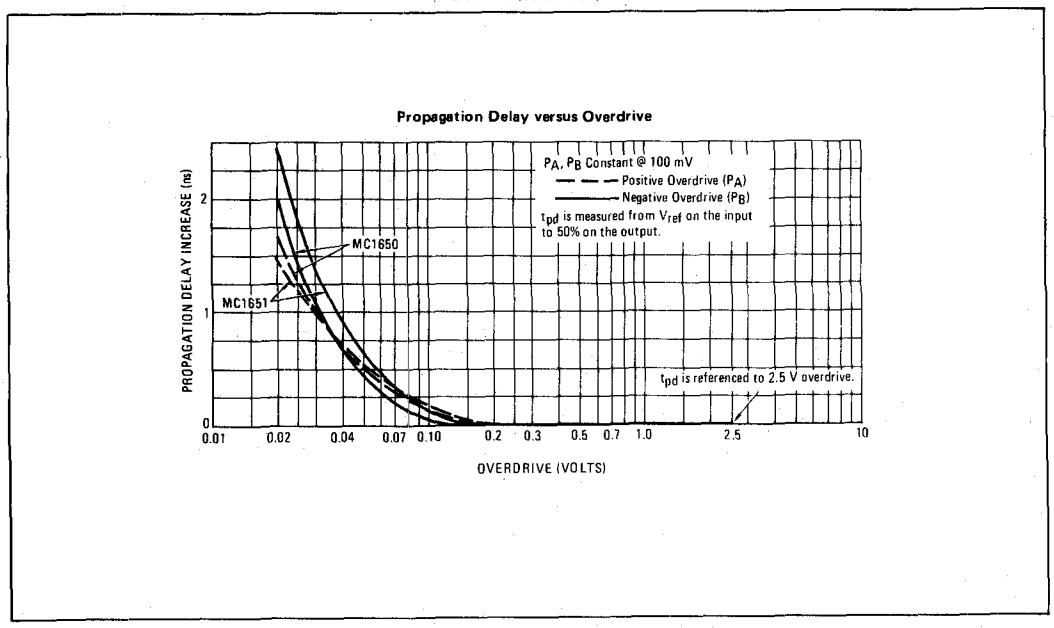


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FIGURE 4 – LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

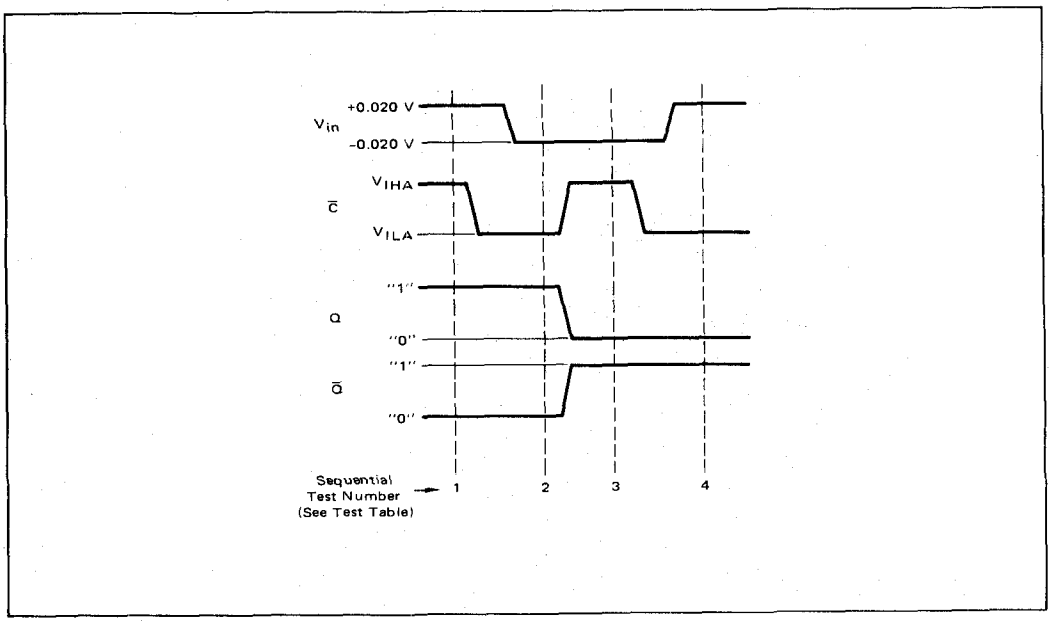
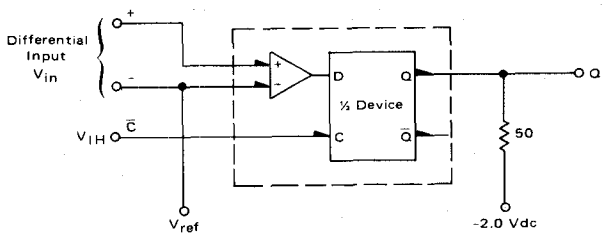


FIGURE 5 – TRANSFER CHARACTERISTICS (Q versus V_{in})

Test Configuration



$-2.5\ Vdc \leqslant V_{ref} \leqslant +2.5\ Vdc$

Typical Transfer Curves

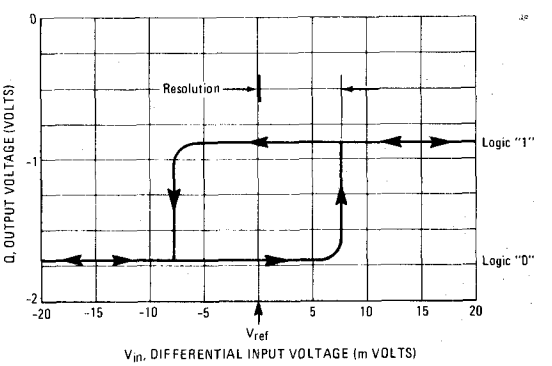


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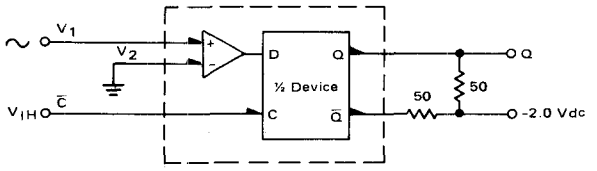
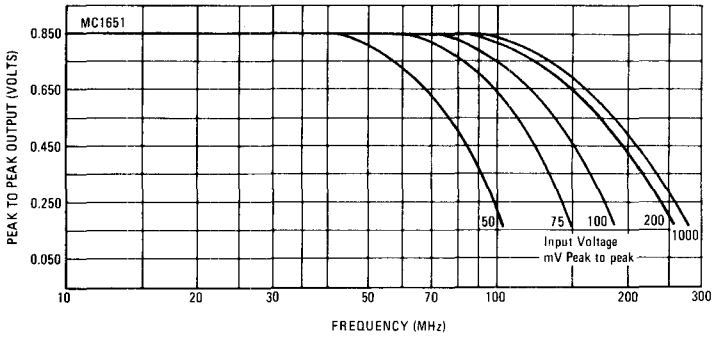
FIGURE 6 – OUTPUT VOLTAGE SWING versus FREQUENCY

(A) Test Circuit



(B) Typical Output Logic Swing versus Frequency



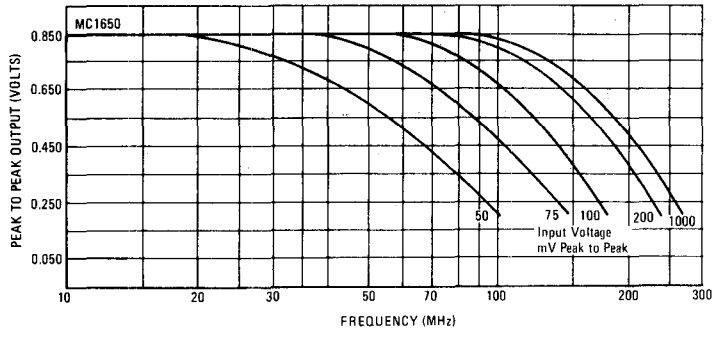
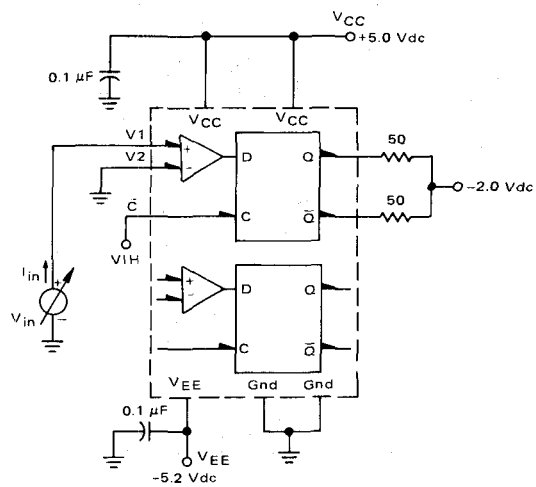
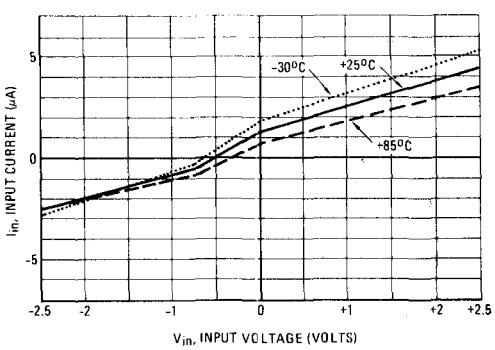


FIGURE 7 – INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT



Typical MC1650 (Complementary Input Grounded)



Typical MC1651 (Complementary Input Grounded)

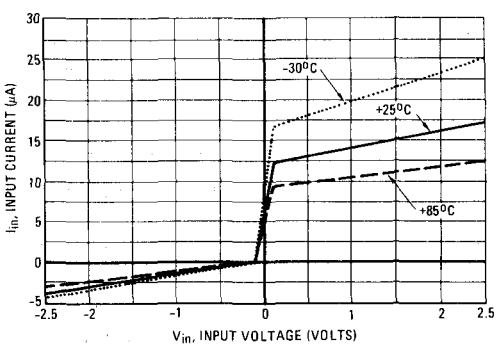
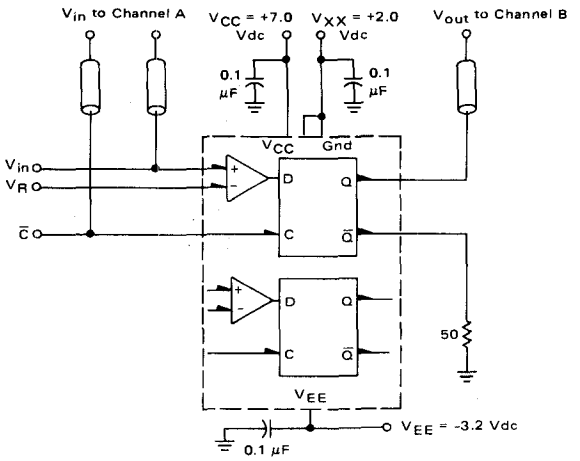


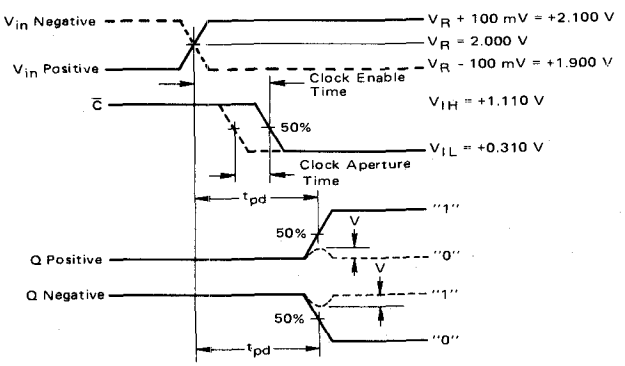
FIGURE 8 – CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case



——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

– – – – – Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.