HIGH SPEED PWM CONTROLLER

FEATURES

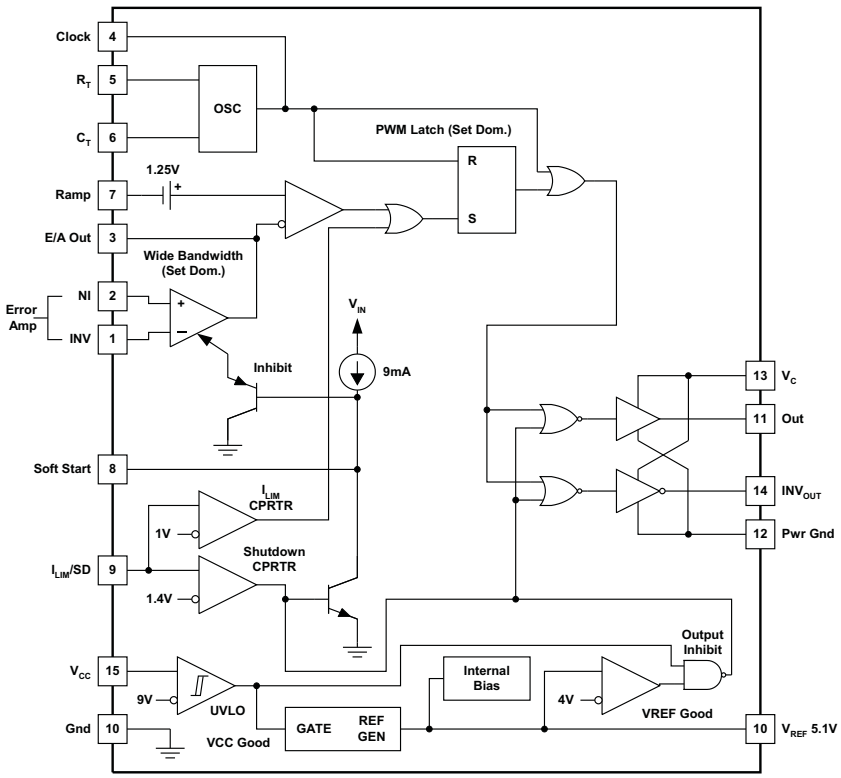
- **Complementary Outputs**
- **Practical Operation Switching Frequencies to 1 MHz**
- **50-ns Propagation Delay to Output**
- **High Current Dual Totem Pole Outputs (1.5 A Peak)**
- **Wide Bandwidth Error Amplifier**
- **Fully Latched Logic With Double Pulse Suppression**
- **Pulse-by-Pulse Current Limiting**
- **Soft Start/Maximum Duty Cycle Control**
- **Under-Voltage Lockout with Hysteresis**
- **Low Start Up Current (1.1 mA)**
- **Trimmed Bandgap Reference (5.1 V ± 1%)**

DESCRIPTION

The UC1824 family of PWM control devices is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1-V threshold, a TTL compatible shutdown port, and a soft-start pin which doubles as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800 mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

BLOCK DIAGRAM



DESCRIPTION (CONTINUED)

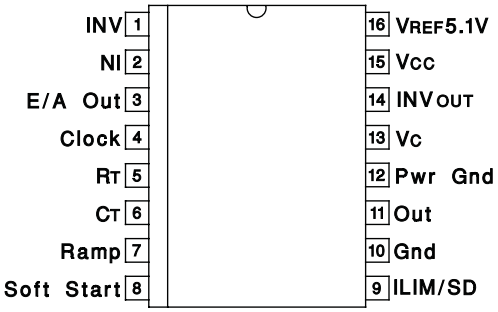
These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

ABSOLUTE MAXIMUM RATINGS(1)(2)

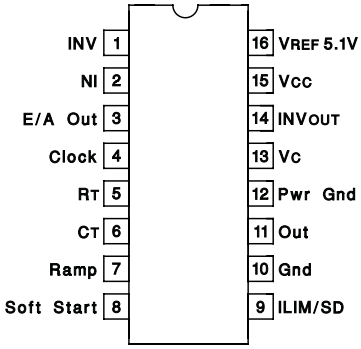
		VALUE	UNIT
Supply voltage (pins 13, 15)		30	V
Output current, source or sink (pins 11, 14)			
	DC	0.5	A
	Pulse (0.5 ms)	2	
Analog inputs			
	(Pins 1, 2, 7)	–0.3 TO 7	V
	(Pin 8, 9)	–0.3 TO 6	
Clock output current (pin 4)		–5	mA
Error amplifier output current (pin 3)		5	
Soft start sink current (pin 8)		20	
Oscillator charging current (pin 5)		–5	
Power dissipation		1	W
Storage temperature range		–65 to 150	°C
Lead temperature (soldering, 10 seconds)		300	

(1) All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.
(2) Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

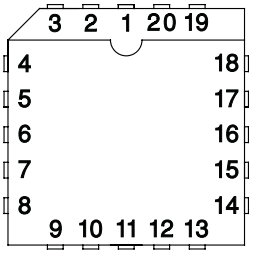
SOIC-16
DW PACKAGE
(TOP VIEW)



DIL-16
J OR N PACKAGE
(TOP VIEW)



PLCC-20 AND LCC-20
Q AND L PACKAGES
(TOP VIEW)



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
R_T	7
C_T	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out	14
Pwr Gnd	15
N/C	16
V_C	17
INV_{OUT}	18
V_{CC}	19
V_{REF} 5.1V	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for, R_T = 3.65k, C_T = 1 nF, V_{CC} = 15 V, –55°C < T_A < 125°C for the UC1824, –40°C < T_A < 85°C for the UC2824, and 0°C < T_A < 70°C for the UC3824, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1824 UC2824			UC3824			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output voltage	T_J = 25°C, I_O = 1 mA	5.05	5.10	5.15	5	5.10	5.20	V
Line regulation	10 V < V_{CC} < 30 V		2	20		2	20	mV mV
Load regulation	1 mA < I_O < 10 mA		5	20		5	20	
Temperature stability(1)	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total output variation(1)	Line, Load, Temperature	5		5.20	4.95		5.25	V
Output noise voltage(1)	10 Hz < f < 10 kHz		50			50		µV
long term stability(1)	T_J = 125°C, 1000 hrs.		5	25		5	25	mV
Short circuit current	V_{REF} = 0 V	–15	–50	–100	–15	–50	–100	mA
Oscillator Section								
Initial accuracy(1)	T_J = 25°C	360	400	440	360	400	440	kHz
Voltage stability(1)	10 V < V_{CC} < 30 V		0.2%	2%		0.2%	2%	
Temperature stability(1)	T_{MIN} < T_A < T_{MAX}		5%			5%		
Total variation(1)	Line, Temperature	340		460	340		460	kHz
Clock out high		3.9	4.5		3.9	4.5		V
Clock out low			2.3	2.9		2.3	2.9	
Ramp peak(1)		2.6	2.8	3	2.6	2.8	3	
Ramp valley(1)		0.7	1	1.25	0.7	1	1.25	
Ramp valley to peak(1)		1.6	1.8	2	1.6	1.8	2	
Error Amplifier Section								
Input offset voltage				10			15	mV
Input bias current			0.6	3		0.6	3	µA
Input offset current			0.1	1		0.1	1	µA
Open loop gain	1 V < V_O < 4 V	60	95		60	95		dB
CMRR	1.5 V < V_{CM} < 5.5 V	75	95		75	95		
PSRR	10 V < V_{CC} < 30 V	85	110		85	110		
Output sink current	$V_{PIN\ 3}$ = 1 V	1	2.5		1	2.5		mA
Output source current	$V_{PIN\ 3}$ = 4 V	–0.5	–1.3		–0.5	–1.3		
Output high voltage	$I_{PIN\ 3}$ = –0.5 mA	4	4.7	5	4	4.7	5	V
Output low voltage	$I_{PIN\ 3}$ = 1 mA	0	0.5	1	0	0.5	1	
Unity gain bandwidth(1)		3	5.5		3	5.5		MHz
Slew rate(1)		6	12		6	12		V/µs
PWM Comparator Section								
Pin 7 bias current	$V_{PIN\ 7}$ = 0 V		–1	–5		–1	–5	µA
Duty cycle range		0		80	0		85	%
Pin 3 zero dc threshold	$V_{PIN\ 7}$ = 0 V	1.1	1.25		1.1	1.25		V
Delay to output(1)			50	80		50	80	ns
Soft-Start Section								
Charge current	$V_{PIN\ 8}$ = 0.5 V	3	9	20	3	9	20	µA
Discharge current	$V_{PIN\ 8}$ = 1 V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 bias current	0 < $V_{PIN\ 9}$ < 4 V			15			10	µA

(1) This parameter not 100% tested in production but guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for, R_T = 3.65k, C_T = 1 nF, V_{CC} = 15 V, –55°C < T_A < 125°C for the UC1824, –40°C < T_A < 85°C for the UC2824, and 0°C < T_A < 70°C for the UC3824, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1824 UC2824			UC3824			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Current limit threshold		0.9	1	1.1	0.9	1	1.1	V
Shutdown threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to output			50	80		50	80	ns
Output Section								
Output low level	I_{OUT} = 20 mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200 mA		1.2	2.2		1.2	2.2	V
Output high level	I_{OUT} = –20 mA	13	13.5		13	13.5		V
	I_{OUT} = –200 mA	12	13		12	13		V
Collector leakage	V_C = 30 V		100	500		10	500	µA
Rise/fall time(2)	CL = 1 nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current Section								
Start up current	V_{CC} = 8 V		1.1	2.5		1.1	2.5	mA
ICC	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0 V; $V_{PIN\ 2}$ = 1 V		22	33		22	33	mA

(2) This parameter not 100% tested in production but guaranteed by design.

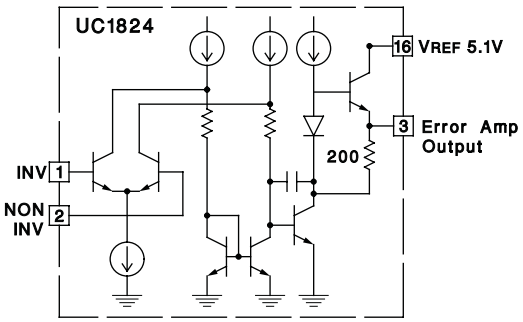
UC1824 Printed Circuit Board Layout Considerations

High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1824 follow these rules:

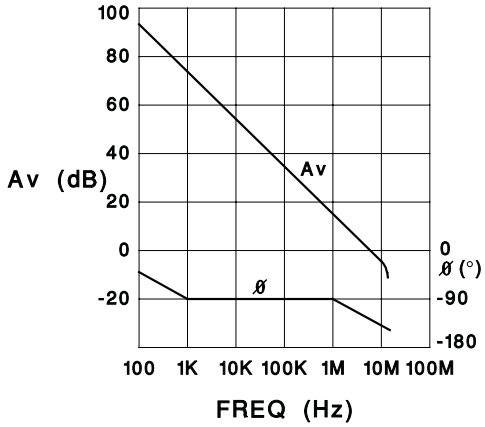
1. Use a ground plane.
2. Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1-A Schottky diode at the output pin serves this purpose.
3. Bypass V_{CC}, V_C, and V_{REF}. Use 0.1-µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane.
4. Treat the timing capacitor, C_T, like a bypass capacitor.

Error Amplifier Circuit

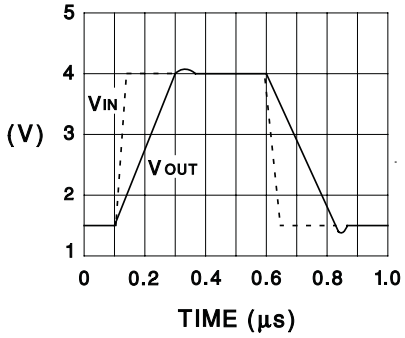
Simplified Schematic



Open Loop Frequency Response

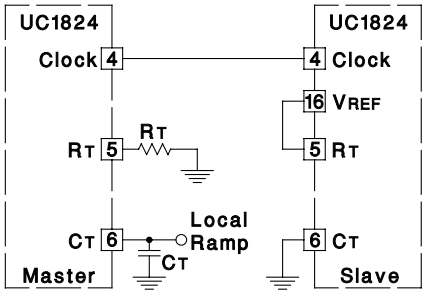


Unity Gain Slew Rate

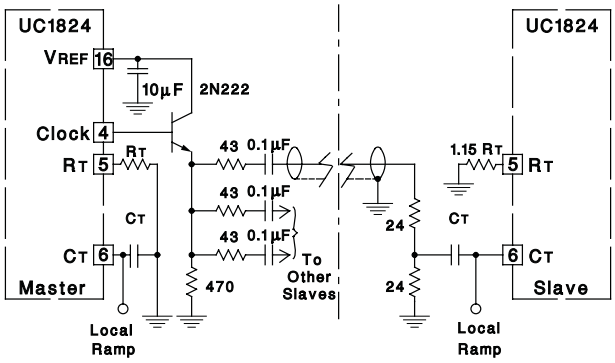


Synchronized Operation

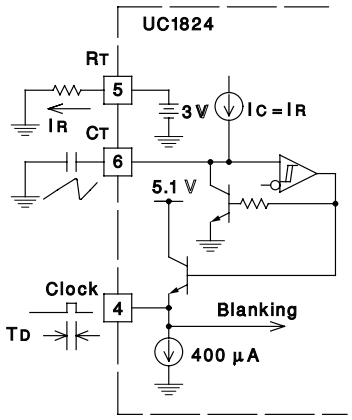
Two Units in Close Proximity



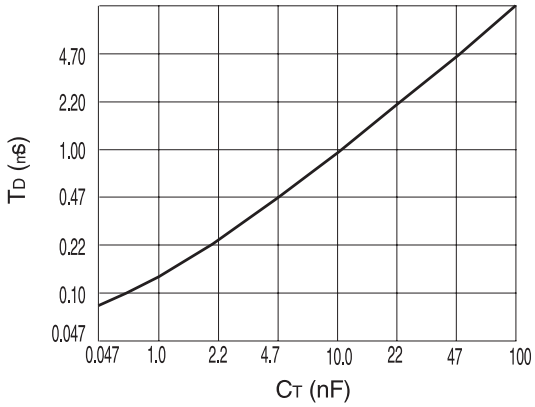
Generalized Synchronization



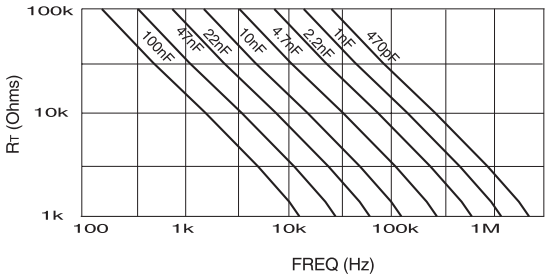
Oscillator Circuit



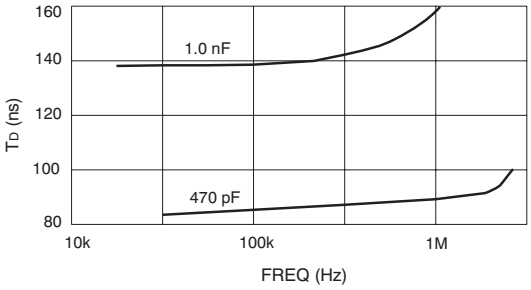
Primary Output Deadtime vs C_T ($3k \le R_T \le 100k$)



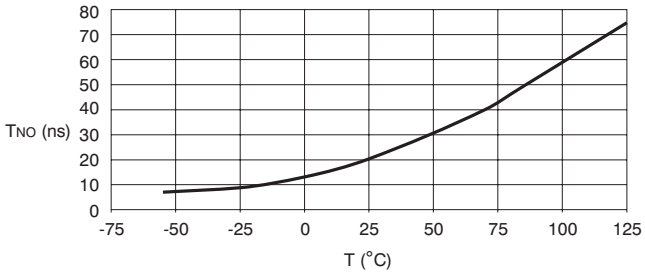
Timing Resistance vs Frequency



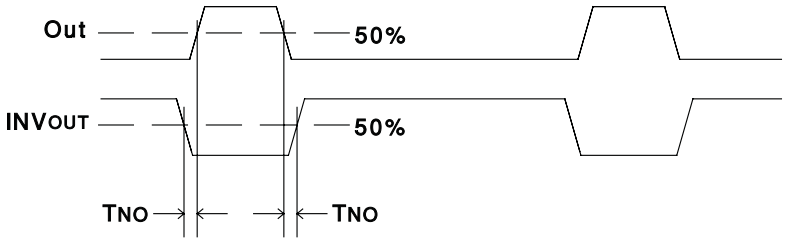
Primary Output Deadtime vs Frequency



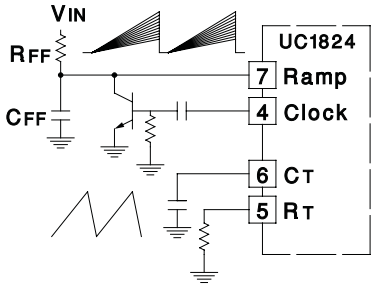
Typical Non-Overlap Time (T_{NO}) Over Temperature



Non-Overlap Time (T_{NO})

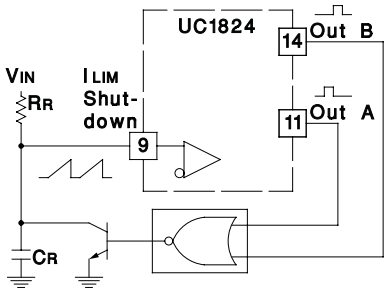


Forward Technique for Off-Line Voltage Mode Application



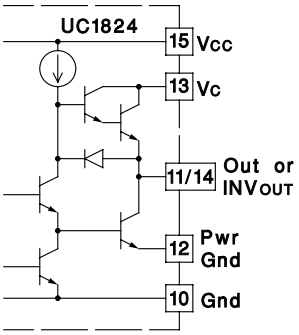
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

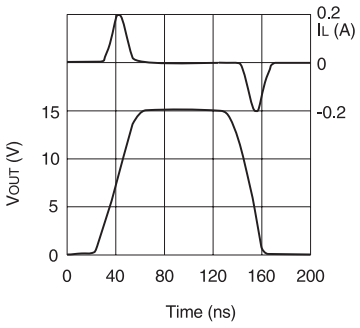


Output Section

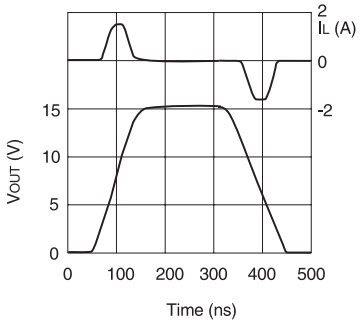
Simplified Schematic



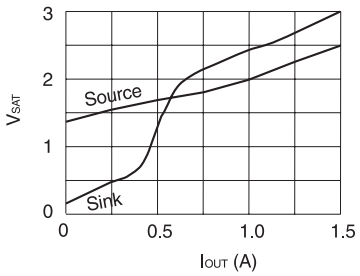
Rise/Fall Time (C_L=1 nF)



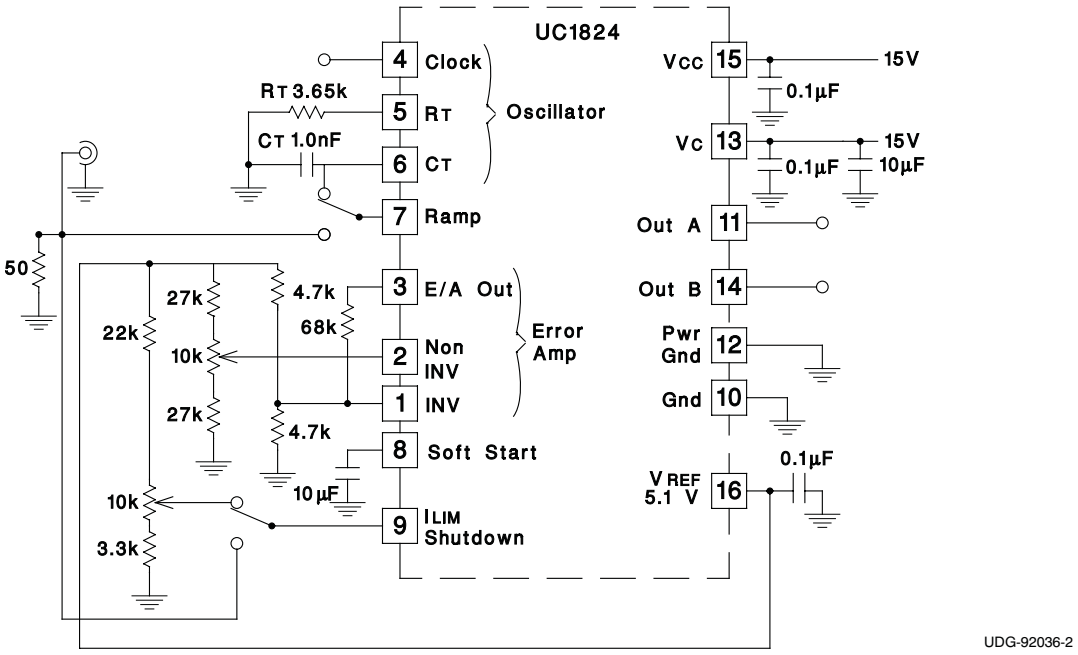
Rise/Fall Time (C_L=10 nF)



Saturation Curves



Open-Loop Laboratory Test Fixture



This test fixture is useful for exercising many of the UC1824's functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2824DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2824DW	Samples
UC2824DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2824DW	Samples
UC2824N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2824N	Samples
UC3824DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3824DW	Samples
UC3824DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3824DW	Samples
UC3824DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3824DW	Samples
UC3824N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3824N	Samples
UC3824NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3824N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

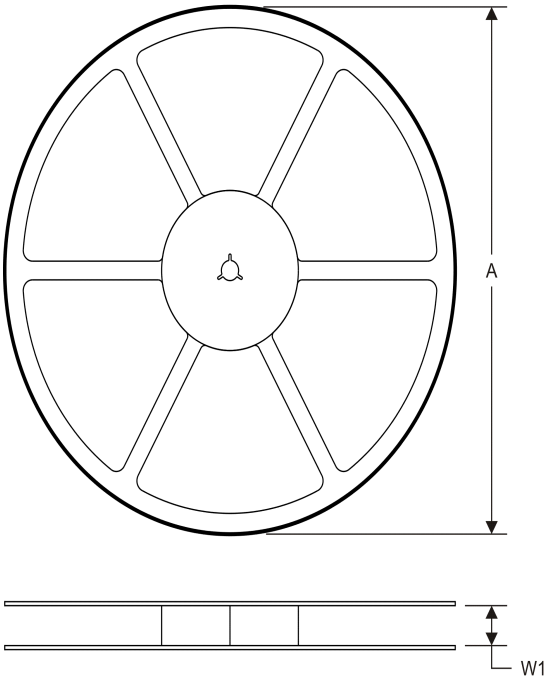
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

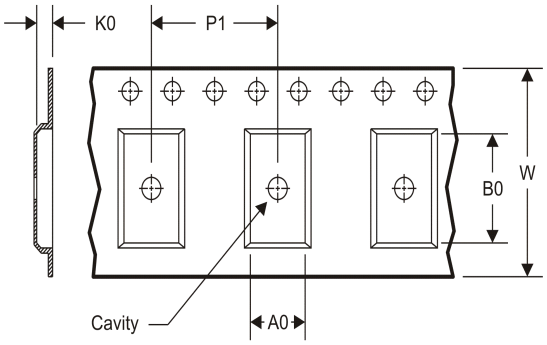
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



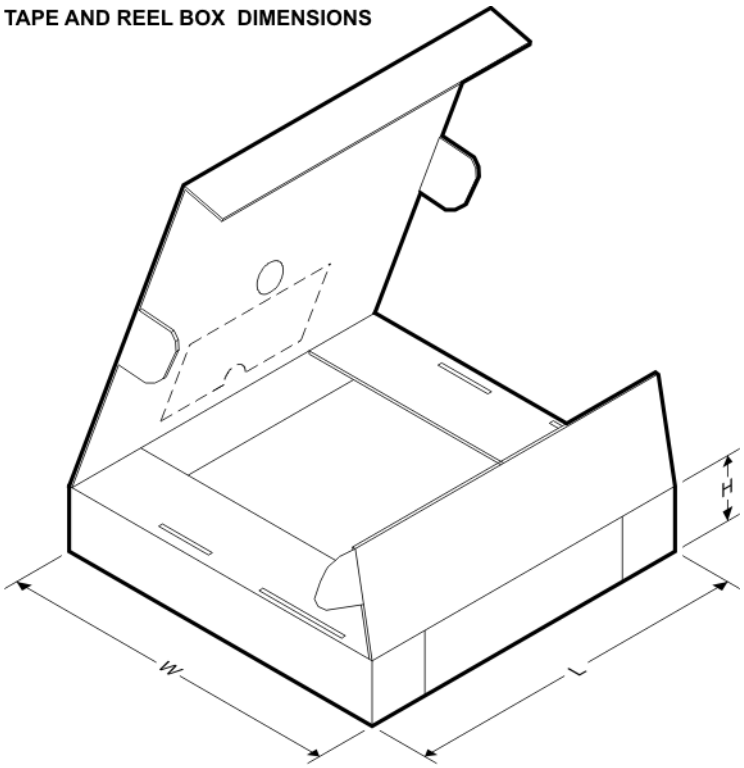
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3824DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3824DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

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