

## MICROCIRCUIT DATA SHEET

Original Creation Date: 03/25/97 Last Update Date: 04/27/99

Last Major Revision Date: 04/13/99

## LMD18200 3A, 55V H-BRIDGE

MNLMD18200-2-X REV 1A1

## General Description

The LMD18200 is a 3A H-Bridge designed for motion control applications. The device is built using a multi-technology process which combines bipolar and CMOS control circuitry with DMOS power devices on the same monolithic structure. Ideal for driving DC and stepper motors; the LMD18200 accommodates peak output currents up to 6A. An innovative circuit which facilitates low-loss sensing of the output current has been implemented.

#### Industry Part Number

NS Part Numbers

LMD18200

LMD18200-2D-QV LMD18200-2D/883

Prime Die

LM18200

## Controlling Document

SEE FEATURES SECTION

Subgrp	Description	Temp ( $^{\circ}$ C)
1	Static tests at	+25
		+125
-		-55
		+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
	1 2 3 4 5 6 7 8A 8B 9	2 Static tests at 3 Static tests at 4 Dynamic tests at 5 Dynamic tests at 6 Dynamic tests at 7 Functional tests at 8A Functional tests at 8B Functional tests at 9 Switching tests at 10 Switching tests at

#### **Features**

- Delivers up to 3A continuous output
- Operates at supply voltages up to 55V
- Low Rds(ON) typically 0.3 Ohms per switch
- TTL and CMOS compatible inputs
- No "shoot-through" current
- Thermal warning flag output at 145  $\ensuremath{\text{C}}$
- Thermal shutdown (outputs off) at 170 C
- Internal clamp diodes
- Shorted load protection
- Internal charge pump with external bootstrap capability
- CONTROLLING DOCUMENTS:

LMD18200-2D-QV 5962-9232501VXA LMD18200-2D/883 5962-9232501MXA

## Applications

- DC and stepper motor drives
- Position and velocity servomechanisms
- Factory automation robots
- Numerically controlled machinery
- Computer printers and plotters

## (Absolute Maximum Ratings)

(Note 1)

```
Total Supply Voltage at Vs Pin
    Vs, Pins 6 & 7
                                                          607
Voltage at Pins
    Pins 3, 4, 5, 9, 10, 15, 16, 17, 21 & 22
                                                          12V
Voltage at Bootstrap Pins
                                                          Vout. + 16V
    Pins 1, 12, 13, & 24
Peak Output Current (200ms)
                                                          бΑ
Continuous Output Current
(Note 4)
                                                          3A
Power Dissipation
(Note 2, 3)
                                                          25W
Power Dissipation (Ta = 25 C, Free Air)
                                                          3W
Junction Temperature, Ti(max)
                                                          150 C
Thermal Resistance
    ThetaJA
      (Still Air)
                                                          40.5 C/W
      (500LF/Min Air flow)
                                                              C/W
    ThetaJC
                                                          1.4 C/W
     (Note 3)
ESD Susceptibility
(Note 5)
                                                          15007
Storage Temperature, Tstg
                                                          -65 C to +150 C
Lead Temperature (Soldering, 10 Sec.)
                                                          300 C
```

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- The maximum power dissipation must be derated at elevated temperatures and is Note 2: dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.
- The package material for these devices allows much improved heat transfer over our Note 3: standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the pacakge, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal reisstance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.
- Note 4:
- See Application Information for details regarding current limiting.
  Human-body model, 100pF discharged through a 1.5K Ohm resistor. Except Bootstrap pins Note 5: (pins 1, 12, 13, and 24) which are protected to 1000V of ESD.

## Recommended Operating Conditions

(Note 1)

Junction Temperature, Tj

-55 C to +125 C

Vs Supply Voltage

+12V to +55V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

## Electrical Characteristics

## DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.) DC: Vs = 42V.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN- NAME	MIN	MAX	UNIT	SUB- GROUPS
Rds (ON)	Switch ON Resistance	Output current = 2.4A	1			0.6	Ohms	1
	Resiseance		1			0.7	Ohms	2, 3
Vclamp	Clamp Diode Forward Drop	Clamp current = 2.4A	1			1.70	V	1, 2,
Vil	Logic Low Input Voltage			3,4,5, 15,16, 17	-0.1	0.8	V	1, 2,
Iil	Logic Low Input Current	Vin = -0.1V		3,4,5, 15,16, 17		-10	uA	1, 2,
Vih	Logic High Input Voltage			3,4,5, 15,16, 17	2	12	V	1, 2,
Iih	Logic High Input Current	Vin = 12V		3,4,5, 15,16, 17		10	uA	1, 2,
Iout Sense	Current Sense Output	Iout = 1A			250	500	uA	1
	Caspac				225	525	uA	2, 3
Ilin Sense	Current Sense Linearity	1A < Iout < 2.4A	2		-20	20	olo	1, 2,
	Undervoltage Lockout	Outputs turn OFF			9	15	V	1, 2,
If(OFF)	Flag Output Leakage	Vf = 12V				10	uA	1, 2,
Is	Quiescent Supply Current	All Logic Inputs Low				25	mA	1, 2,

#### DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.) DC: Vs = 42V. "Delta calculations performed on Jan S and QV devices at Group B, Subgroup 5 ONLY."

Iout Sense	Current Sense Output	Iout = 1A		-25	+25	uA	1
Is	Quiescent Supply Current	All Logic Inputs Low		-5	+5	mA	1

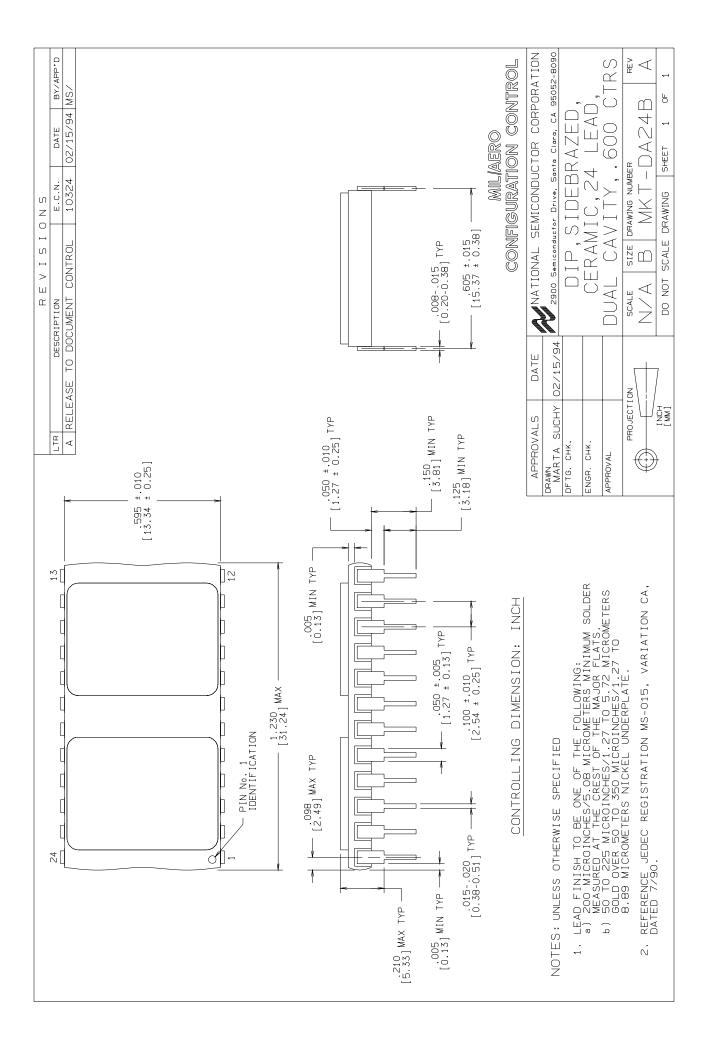
Note 1: Output currents are pulsed (duty cycle <5%).

Note 2: Linearity is calculated relative to the current sense output value with 1A load.

## Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06257HRD3	DIP, S/B, CERAMIC,24LD DUAL CAV .600CTRS(B/I CKT)
DA24BRA	DIP, S/B, CERAMIC,24LD DUAL CAV .600CTRS(P/P DWG)
P000001C	DIP, S/B, CERAMIC,24LD DUAL CAV .600CTRS(PINOUT)

See attached graphics following this page.



BOOTSTRAP 1A	1	24	BOOTSTRAP 2A
V <sub>OUT</sub> 1A —	2	23	V <sub>OUT</sub> 2A
DIRECTION A ——	3	22	Thermal Flag A
BRAKE A ——	4	21	Current Sense A
PWM A	5	20	Signal GND A
V <sub>S</sub> A ———	6	19	Power GND A
V <sub>S</sub> B ——	7	18	Power GND B
Signal GND B ——	8	17	PWM B
Current Sense B ———	9	16	BRAKE B
Thermal Flag B ———	10	15	DIRECTION B
V <sub>OUT</sub> 2B ——	11	14	V <sub>OUT</sub> 1B
BOOTSTRAP 2B ——	12	13	BOOTSTRAP 1B

# LMD18200-2D 24 - LEAD DIP CONNECTION DIAGRAM TOP VIEW P000001C



## Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A1	M0003382	04/27/99		Update MDS: MNLMD18200-2-X, Rev. 0B1 to MNLMD18200-2-X, Rev. 1A1. Updated NSID, moved Controlling Document reference to Features Section, update notes and not link in Absolute Section, and is Recommend Section. Added QV device, and Drift Table. Changed B/I ckt from 6257HRD2 to 06257HRD3.