ispLSI® 2128

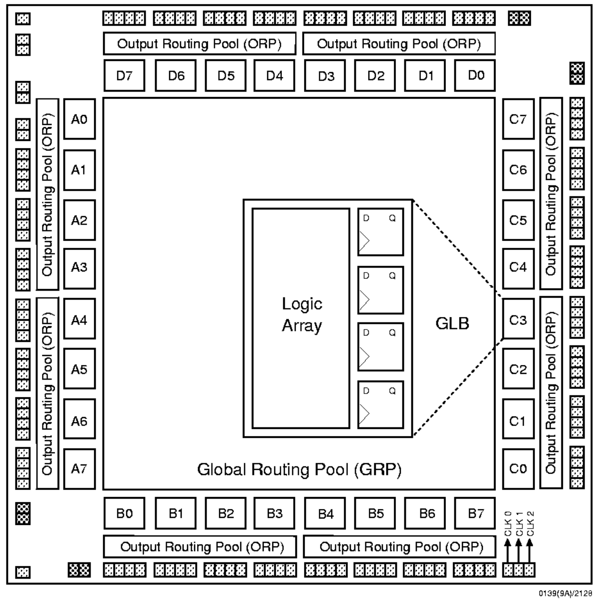
In-System Programmable High Density PLD

Lattice Semiconductor Corporation

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - — 6000 PLD Gates
  - — 128 I/O Pins, Eight Dedicated Inputs
  - — 128 Registers
  - — High Speed Global Interconnect
  - — Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - — Small Logic Block Size for Random Logic
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — f_{max} = 100 MHz Maximum Operating Frequency
  - — t_{pd} = 10 ns Propagation Delay
  - — TTL Compatible Inputs and Outputs
  - — Electrically Erasable and Reprogrammable
  - — Non-Volatile
  - — 100% Tested at Time of Manufacture
  - — Unused Product Term Shutdown Saves Power
- **IN-SYSTEM PROGRAMMABLE**
  - — In-System Programmable (ISP™) 5V Only
  - — Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - — Reprogram Soldered Devices for Faster Prototyping
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - — Complete Programmable Device Can Combine Glue Logic and Structured Designs
  - — Enhanced Pin Locking Capability
  - — Three Dedicated Clock Input Pins
  - — Synchronous and Asynchronous Clocks
  - — Programmable Output Slew Rate Control to Minimize Switching Noise
  - — Flexible Pin Placement
  - — Optimized Global Routing Pool Provides Global Interconnectivity
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - — Superior Quality of Results
  - — Tightly Integrated with Leading CAE Vendor Tools
  - — Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™
  - — PC and UNIX Platforms

Functional Block Diagram



Description

The ispLSI 2128 is a High Density Programmable Logic Device. The device contains 128 Registers, 128 Universal I/O pins, eight Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2128 features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 2128 offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2128 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see Figure 1). There are a total of 32 GLBs in the ispLSI 2128 device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

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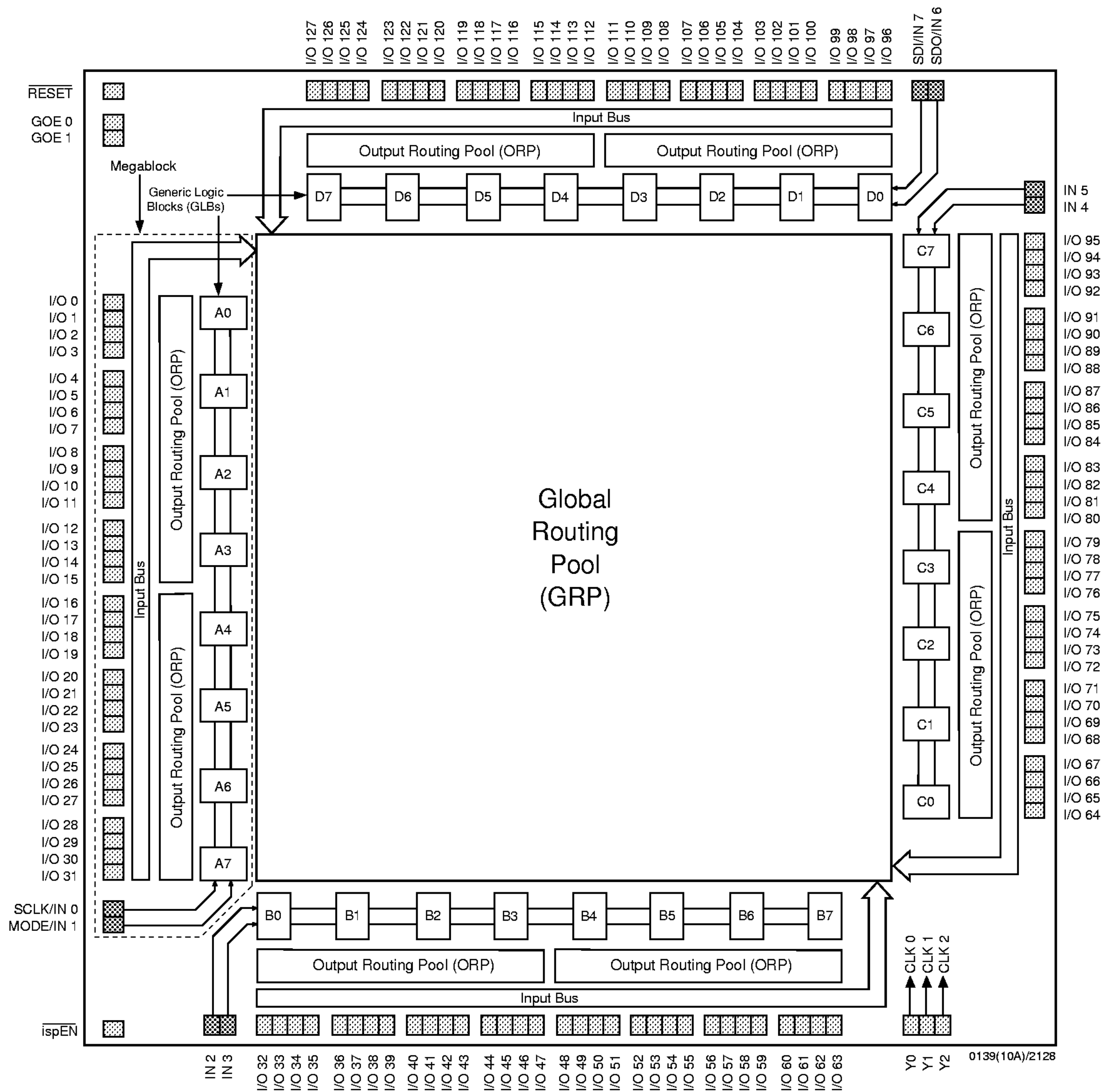
Functional Block Diagram

Figure 1. ispLSI 2128 Functional Block Diagram



The device also has 128 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the two ORPs. Each ispLSI 2128 device contains four Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2128 device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ....-0.5 to +7.0V

Input Voltage Applied........................ -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature .... -65 to 150°C

Case Temp. with Power Applied .... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{cc}+1	V

Table 2 - 0005/2128

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O and Dedicated Input Capacitance	8	pf	V_{CC} = 5.0V, $V_{I/O,\ IN}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006/2128

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
Erase/Reprogram Cycles	1000	–	Cycles

Table 2-0008/2128

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

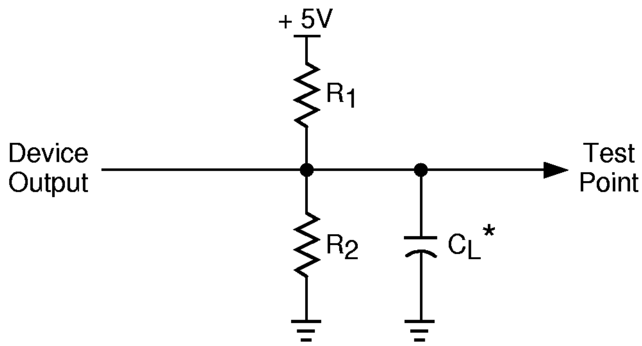
Table 2 - 0003/2000

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A/2000

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		–	–	10	µA
$I_{IL\text{-}isp}$	$\overline{\text{ispEN}}$ Input Low Leakage Current	$0V \le V_{IN} \le V_{IL}$		–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	$0V \le V_{IN} \le V_{IL}$		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V, f_{CLOCK} = 1 MHz	Commercial	–	165	325	mA
			Industrial	–	165	–	mA

Table 2-0007/2128

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-100		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	100	–	81.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	77.0	–	57.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	100	–	83.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	6.5	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	5.0	–	6.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	8.0	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	6.0	–	8.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	17.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Product Term OE, Enable	–	15.0	–	18.0	ns
$t_{ptoedis}$	C	15	Product Term OE, Disable	–	15.0	–	18.0	ns
t_{goeen}	B	16	Global OE, Enable	–	9.0	–	12.0	ns
t_{goedis}	C	17	Global OE, Disable	–	9.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	5.0	–	6.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	5.0	–	6.0	–	ns

Table 2-0030B/2128-100

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

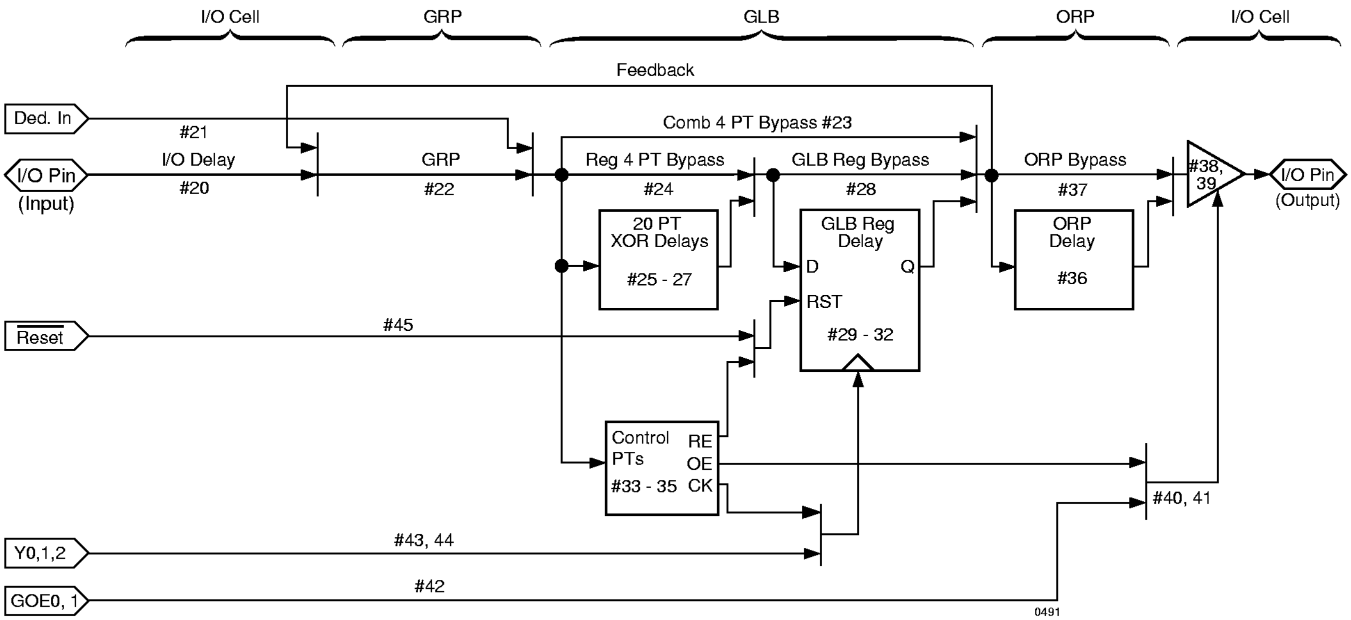
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100 MIN.	-100 MAX.	-80 MIN.	-80 MAX.	UNITS
Inputs							
t_{io}	20	Input Buffer Delay	–	0.5	–	1.8	ns
t_{din}	21	Dedicated Input Delay	–	2.2	–	4.4	ns
GRP							
t_{grp}	22	GRP Delay	–	1.7	–	2.6	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay	–	5.8	–	8.1	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay	–	5.8	–	6.8	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	6.8	–	8.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	7.3	–	8.8	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	8.0	–	9.8	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.5	–	1.3	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	1.2	–	1.4	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.3	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.3	–	1.6	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	6.1	–	8.6	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	8.6	–	9.0	ns
t_{ptck}	35	GLB Product Term Clock Delay	4.1	7.1	5.6	10.2	ns
ORP							
t_{orp}	36	ORP Delay	–	1.4	–	2.0	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.4	–	0.5	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	1.6	–	2.0	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	4.2	–	4.6	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	4.2	–	4.6	ns
t_{goe}	42	Global Output Enable	–	4.8	–	7.4	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.7	2.7	3.6	3.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.7	2.7	3.6	3.6	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	9.2	–	11.4	ns

Table 2- 0036C/2128-100

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI 2128 Timing Model



Derivations of tsu, th and tco from the Product Term Clock

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
	=	(#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
4.4 ns	=	(0.5 + 1.7 + 7.3) + (1.2) + (0.5 + 1.7 + 4.1)
th	=	Clock (max) + Reg h - Logic
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
	=	(#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
3.8 ns	=	(0.5 + 1.7 + 7.1) + (4.0) + (0.5 + 1.7 + 7.3)
tco	=	Clock (max) + Reg co + Output
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#20+ #22+ #35) + (#31) + (#36 + #38)
12.6 ns	=	(0.5 + 1.7 + 7.1) + (0.3) + (1.4 + 1.6)

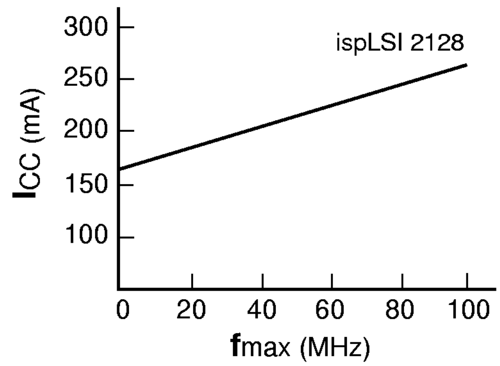
Table 2-0042/2128

Note: Calculations are based upon timing specifications for the ispLSI 2128-100L.

Power Consumption

Power consumption in the ispLSI 2128 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of eight 16-bit counters
Typical current at 5V, 25° C

I_{CC} can be estimated for the ispLSI 2128 using the following equation:

I_{CC} (mA) = 20 + (# of PTs * 0.48) + (# of nets * Max freq * 0.009)

Where:
- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127B-16-80-isp/2128

Pin Description

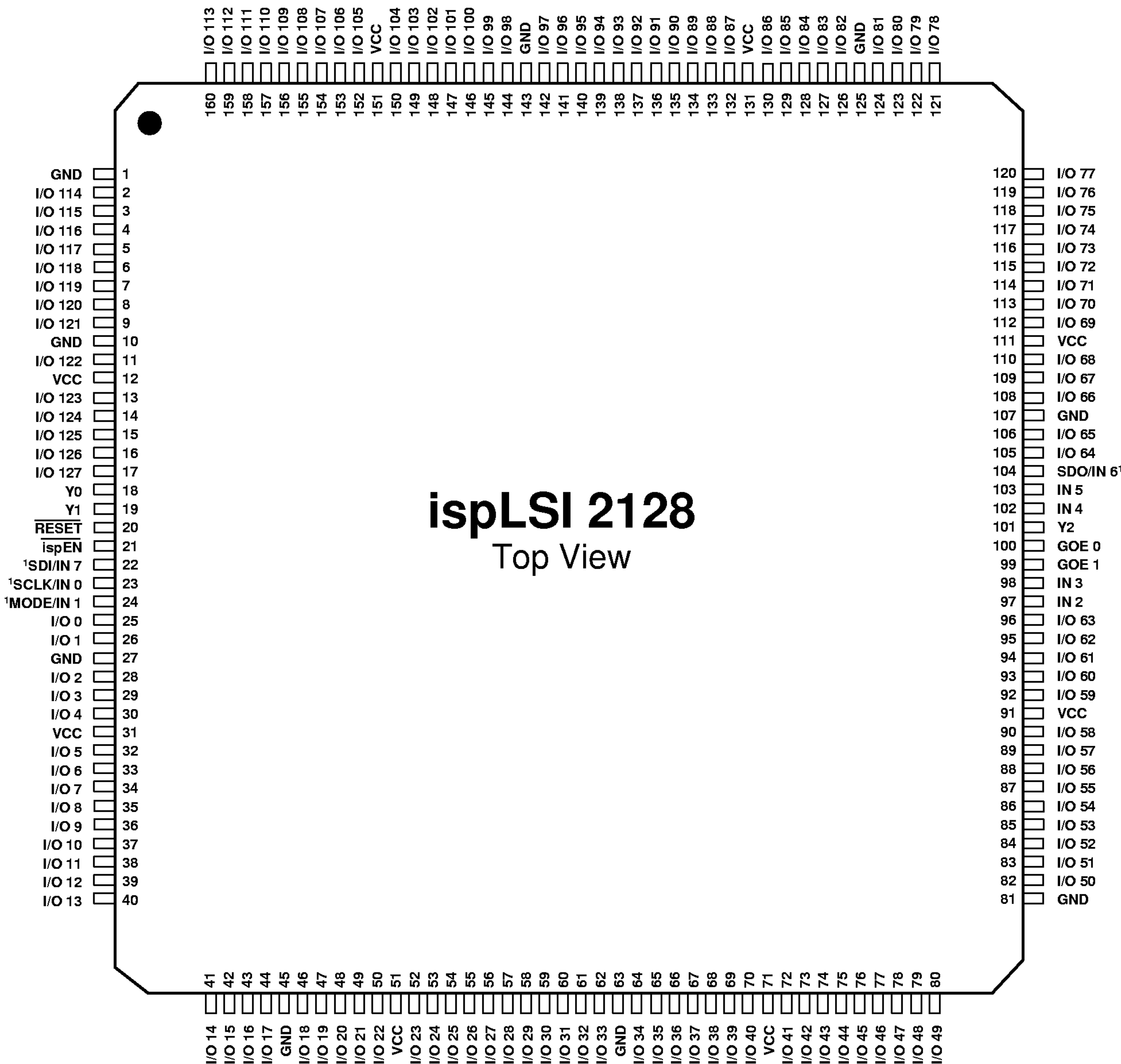
NAME	PQFP/MQFP PIN NUMBERS	TQFP PIN NUMBERS*	DESCRIPTION
I/O 0 - I/O 4	25, 26, 28, 29, 30,	27, 28, 31, 32, 33,	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
I/O 5 - I/O 9	32, 33, 34, 35, 36,	35, 36, 37, 38, 39,	
I/O 10 - I/O 14	37, 38, 39, 40, 41,	41, 42, 43, 44, 45,	
I/O 15 - I/O 19	42, 43, 44, 46, 47,	46, 47, 48, 50, 51,	
I/O 20 - I/O 24	48, 49, 50, 52, 53,	52, 53, 55, 57, 58,	
I/O 25 - I/O 29	54, 55, 56, 57, 58,	59, 60, 61, 62, 63,	
I/O 30 - I/O 34	59, 60, 61, 62, 64,	65, 66, 67, 68, 70,	
I/O 35 - I/O 39	65, 66, 67, 68, 69,	71, 72, 73, 75, 76,	
I/O 40 - I/O 44	70, 72, 73, 74, 75,	77, 79, 80, 81, 82,	
I/O 45 - I/O 49	76, 77, 78, 79, 80,	83, 85, 86, 87, 88,	
I/O 50 - I/O 54	82, 83, 84, 85, 86,	90, 91, 92, 93, 94,	
I/O 55 - I/O 59	87, 88, 89, 90, 92,	95, 96, 97, 99, 101,	
I/O 60 - I/O 64	93, 94, 95, 96, 105,	102, 103, 104, 105, 115,	
I/O 65 - I/O 69	106, 108, 109, 110, 112,	116, 119, 120, 121, 123,	
I/O 70 - I/O 74	113, 114, 115, 116, 117,	124, 125, 126, 127, 129,	
I/O 75 - I/O 79	118, 119, 120, 121, 122,	130, 131, 132, 133, 134,	
I/O 80 - I/O 84	123, 124, 126, 127, 128,	135, 136, 138, 139, 140,	
I/O 85 - I/O 89	129, 130, 132, 133, 134,	141, 143, 145, 146, 147,	
I/O 90 - I/O 94	135, 136, 137, 138, 139,	148, 149, 150, 151, 153,	
I/O 95 - I/O 99	140, 141, 142, 144, 145,	154, 155, 156, 158, 159,	
I/O 100 - I/O 104	146, 147, 148, 149, 150,	160, 161, 163, 164, 165,	
I/O 105 - I/O 109	152, 153, 154, 155, 156,	167, 168, 169, 170, 171,	
I/O 110 - I/O 114	157, 158, 159, 160, 2,	173, 174, 175, 176, 2,	
I/O 115 - I/O 119	3, 4, 5, 6, 7,	3, 4, 5, 6, 7,	
I/O 120 - I/O 124	8, 9, 11, 13, 14,	8, 9, 12, 14, 15,	
I/O 125 - I/O 127	15, 16, 17	16, 17, 18	
IN 2 - IN 5	97, 98, 102, 103	106, 107, 112, 113	Dedicated input pins to the device.
GOE 0, GOE 1	100, 99,	110, 109,	Global Output Enable input pins.
$\overline{\text{RESET}}$	20	22	Active Low (0) Reset pin which resets all of the GLB registers in the device.
Y0, Y1, Y2	18, 19, 101	19, 21, 111	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
$\overline{\text{ispEN}}$	21	23	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
*SDI/IN 7[2]	22	24	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SCLK/IN 0[2]	23	25	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE/IN 1[2]	24	26	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SDO/IN 6[2]	104	114	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
GND	1, 10, 27, 45, 63, 81, 107, 125, 143	1, 11, 29, 49, 69, 89, 117, 137, 157	Ground (GND)
VCC	12, 31, 51, 71, 91, 111, 131, 151	13, 34, 56, 78, 100, 122, 144, 166	V_{CC} (+5V)
NC[1]		20, 30, 40, 54, 64, 74, 84, 98, 108, 118 128, 142, 152, 162, 172	No Connect.

Table 2-0002/2128

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.

Pin Configuration

ispLSI 2128 160-Pin PQFP Pinout Diagram

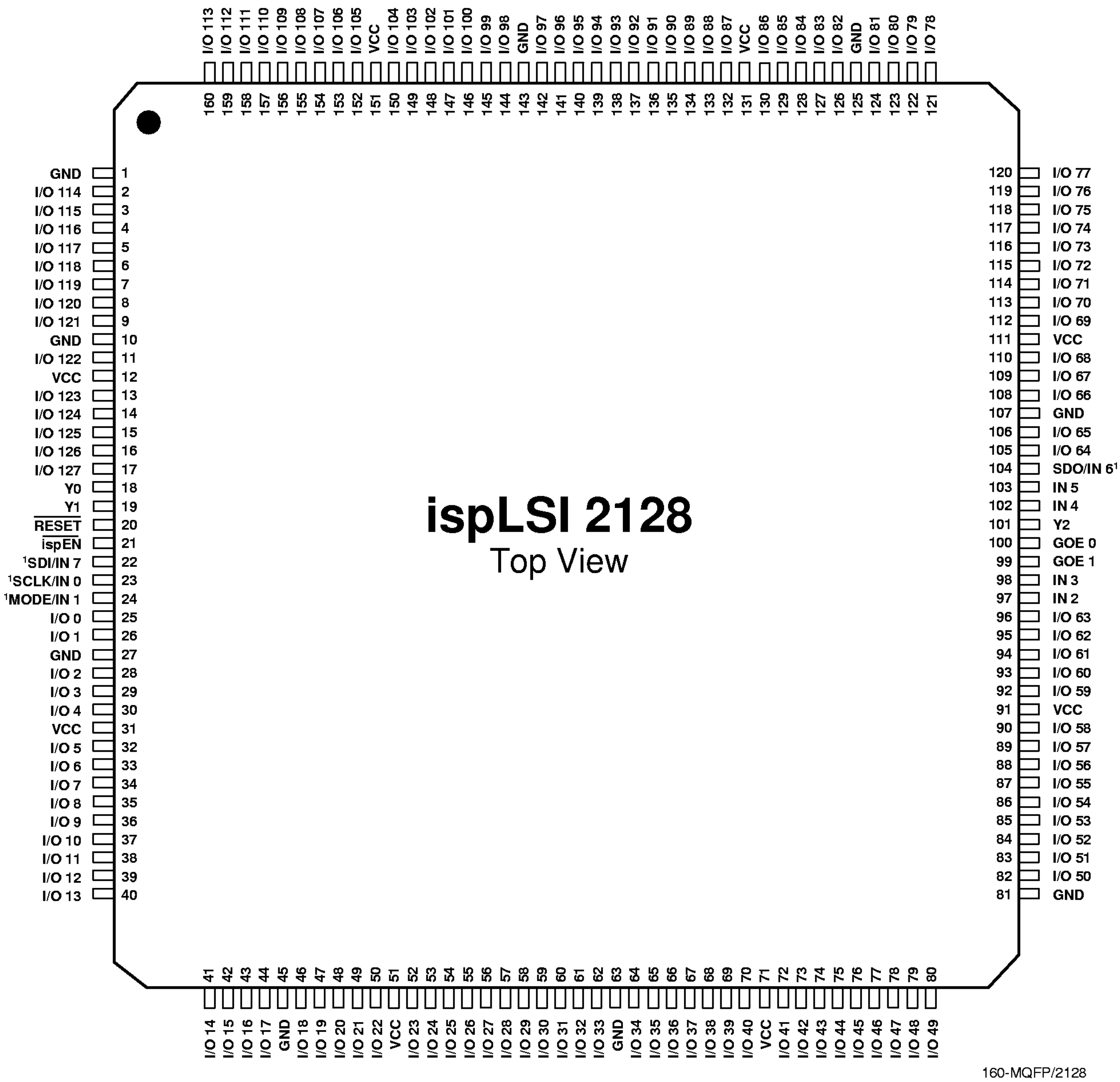


1. Pins have dual function capability.

160-PQFP/2128

Pin Configuration

ispLSI 2128 160-Pin MQFP Pinout Diagram

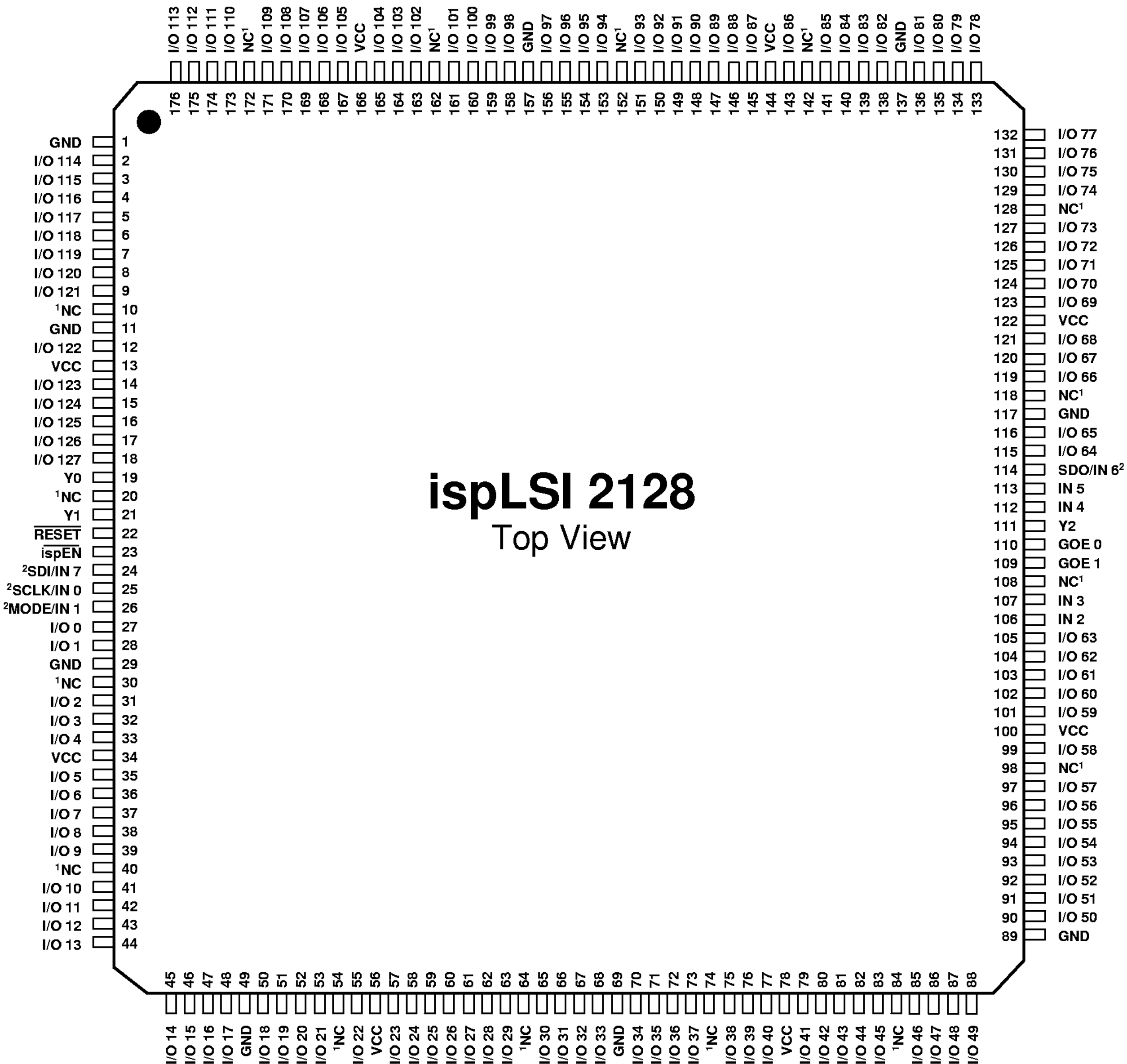


1. Pins have dual function capability.

Note: 160-Pin PQFP recommended for new designs.

Pin Configuration

ispLSI 2128 176-Pin TQFP Pinout Diagram



176-TQFP/2128

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.

Part Number Description

ispLSI 2128 – XXX X X X

Device Family

Device Number

Speed
100 = 100 MHz fmax
80 = 81 MHz fmax

Grade
Blank = Commercial
I = Industrial

Package
Q = PQFP
M = MQFP
T = TQFP

Power
L = Low

0212/2128

ispLSI 2128 Ordering Information

COMMERCIAL

FAMILY	Fmax (MHz)	Tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	100	10	ispLSI 2128-100LQ	160-Pin PQFP
	100	10	ispLSI 2128-100LM*	160-Pin MQFP
	100	10	ispLSI 2128-100LT	176-Pin TQFP
	81	15	ispLSI 2128-80LQ	160-Pin PQFP
	81	15	ispLSI 2128-80LM*	160-Pin MQFP
	81	15	ispLSI 2128-80LT	176-Pin TQFP

*Use 160-Pin PQFP for all new designs.

Table 2-0041A/2128

INDUSTRIAL

FAMILY	Fmax (MHz)	Tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	81	15	ispLSI 2128-80LTI	176-Pin TQFP

Table 2-0041B/2128