OHCI-Lynx™ PCI-Based IEEE 1394 Host Controller

FEATURES

- **3.3-V and 5-V PCI bus signaling**
- **3.3-V supply (core voltage is internally regulated to 1.8 V)**
- **Serial bus data rates of 100M bits/s, 200M bits/s, and 400M bits/s**
- **Physical write posting of up to three outstanding transactions**
- **Serial ROM interface supports 2-wire devices**
- **External cycle timer control for customized synchronization**
- **PCI burst transfers and deep FIFOs to tolerate large host latency**
- **Two general-purpose I/Os**
- **Fabricated in advanced low-power CMOS process**
- **Packaged in 100-terminal LQFP (PZT)**
- **$\overline{\text{PCI\_CLKRUN}}$ protocol**

DESCRIPTION

The Texas Instruments TSB12LV26 device is a PCI-to-1394 host controller compliant with the *PCI Local Bus Specification*, *PCI Bus Power Management Interface Specification*, IEEE Std 1394-1995, and *1394 Open Host Controller Interface Specification*. The chip provides the IEEE 1394 link function and is compatible with 100M bits/s, 200M bits/s, and 400M bits/s serial bus data rates.

As required by the *1394 Open Host Controller Interface Specification* (OHCI) and IEEE Std 1394a-2000, internal control registers are memory-mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles specified by PCI and provides plug-and-play (PnP) compatibility. Furthermore, the TSB12LV26 device is compliant with the *PCI Bus Power Management Interface Specification*, per the *PC 99 Design Guide* requirements. TSB12LV26 device supports the D0, D2, and D3 power states.

The TSB12LV26 design provides PCI bus master bursting and is capable of transferring a cacheline of data at 132M bytes/s after connection to the memory controller. Since PCI latency can be large, deep FIFOs are provided to buffer 1394 data.

The TSB12LV26 device provides physical write posting buffers and a highly-tuned physical data path for SBP-2 performance. The TSB12LV26 device also provides multiple isochronous contexts, multiple cacheline burst transfers, advanced internal arbitration, and bus-holding buffers on the PHY/link interface.

An advanced CMOS process achieves low power consumption and allows the TSB12LV26 device to operate at PCI clock rates up to 33 MHz.

NOTE:

This product is for high-volume PC applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSB12LV26PZT	Active	Production	TQFP (PZT) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	0 to 70	TSB12LV26 F731652A
TSB12LV26PZT.A	Active	Production	TQFP (PZT) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	0 to 70	TSB12LV26 F731652A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

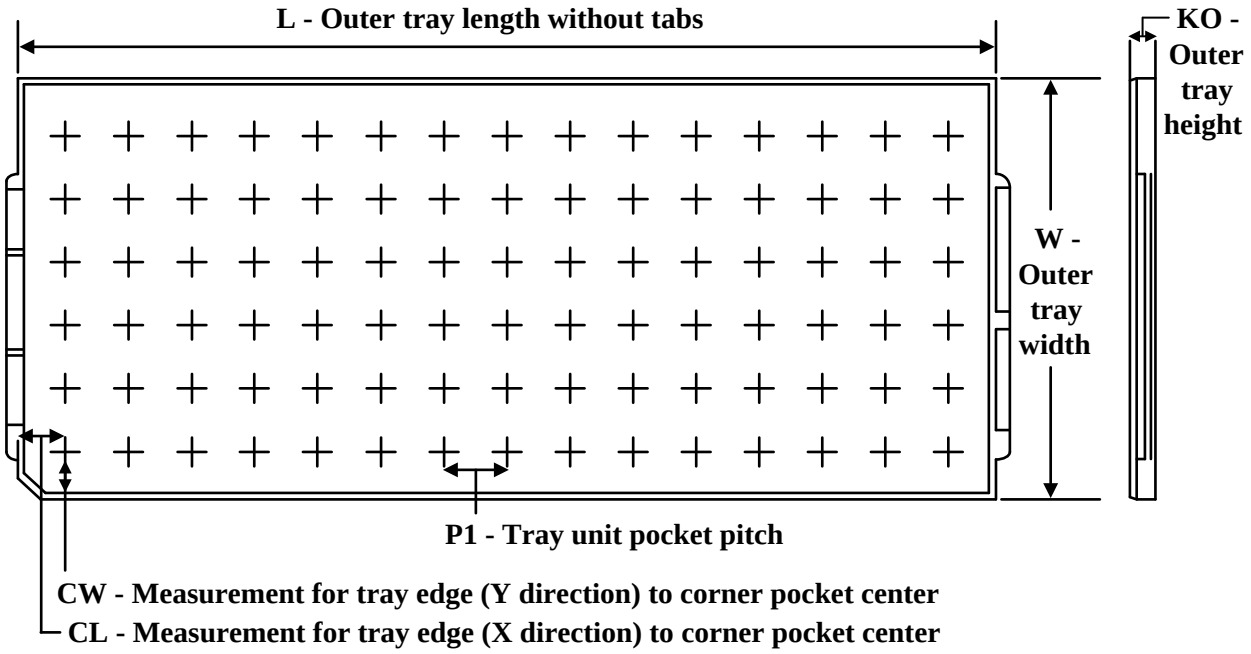
OTHER QUALIFIED VERSIONS OF TSB12LV26 :

- Enhanced Product : TSB12LV26-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TSB12LV26PZT	PZT	TQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TSB12LV26PZT.A	PZT	TQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21

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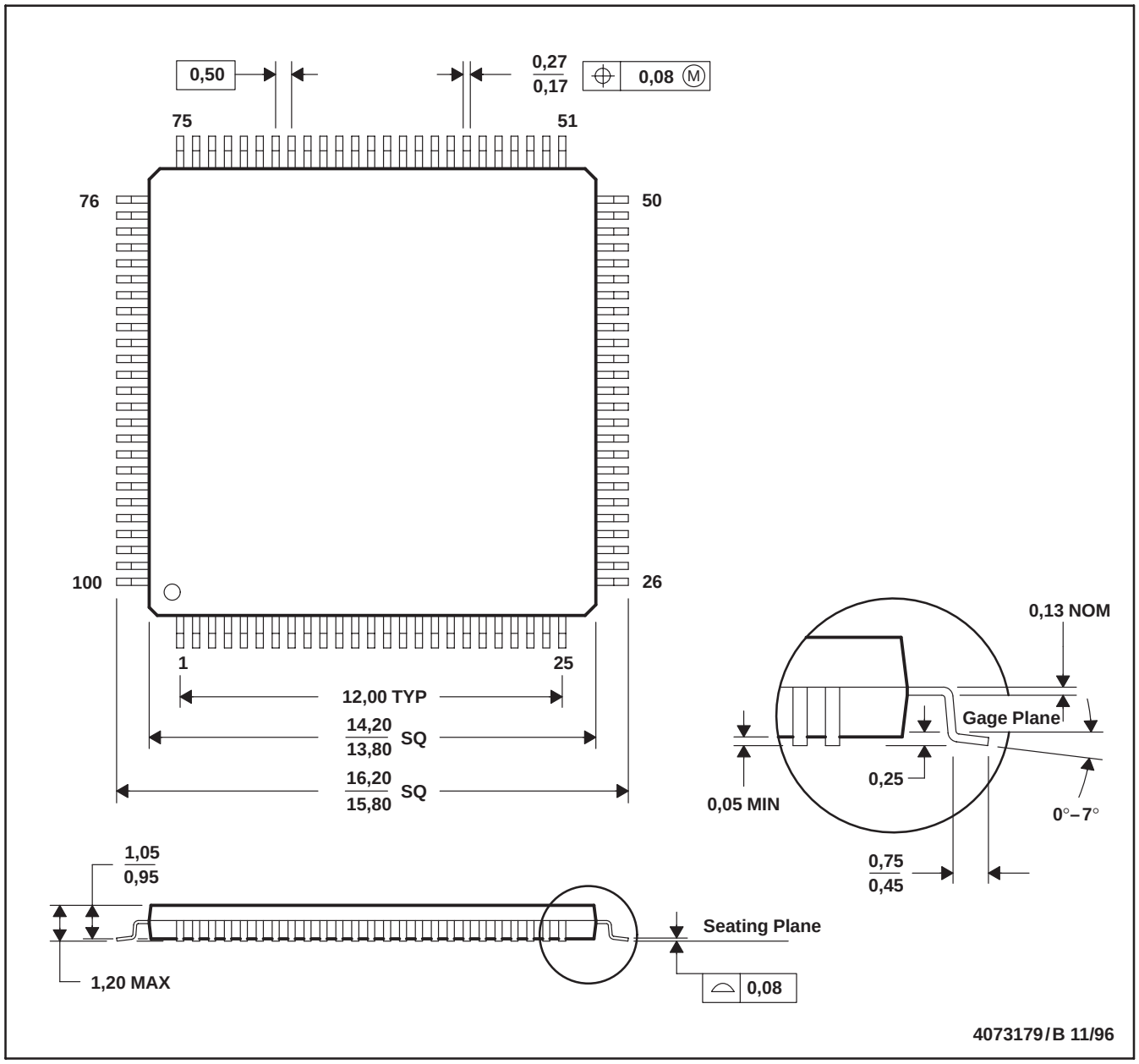
PZT (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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