- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Clocked FIFO Buffering Data From Port A to Port B**
- **Memory Size: 1024 × 36**
- **Synchronous Read-Retransmit Capability**
- **Mailbox Register in Each Direction**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **Input-Ready and Almost-Full Flags Synchronized by CLKA**
- **Output-Ready and Almost-Empty Flags Synchronized by CLKB**
- **Low-Power 0.8 μm Advanced CMOS Technology**
- **Supports Clock Frequencies up to 50 MHz**
- **Fast Access Times of 15 ns**
- **Released as DSCC SMD (Standard Microcircuit Drawing) 5962-9560801QYA and 5962-9560801NXD**
- **Package Options include 132-Pin Ceramic Quad Flat (HFP) and 120-Pin Plastic Quad Flat (PCB) Packages**

## description

The SN54ACT3641 is a high-speed, low-power, CMOS clocked FIFO memory. It supports clock frequencies up to 50 MHz and has read access times as fast as 15 ns. The 1024 × 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO memory has retransmit capability, which allows previously read data to be accessed again. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port can take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider datapaths. Expansion is also possible in word depth.

The SN54ACT3641 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses with synchronous control.

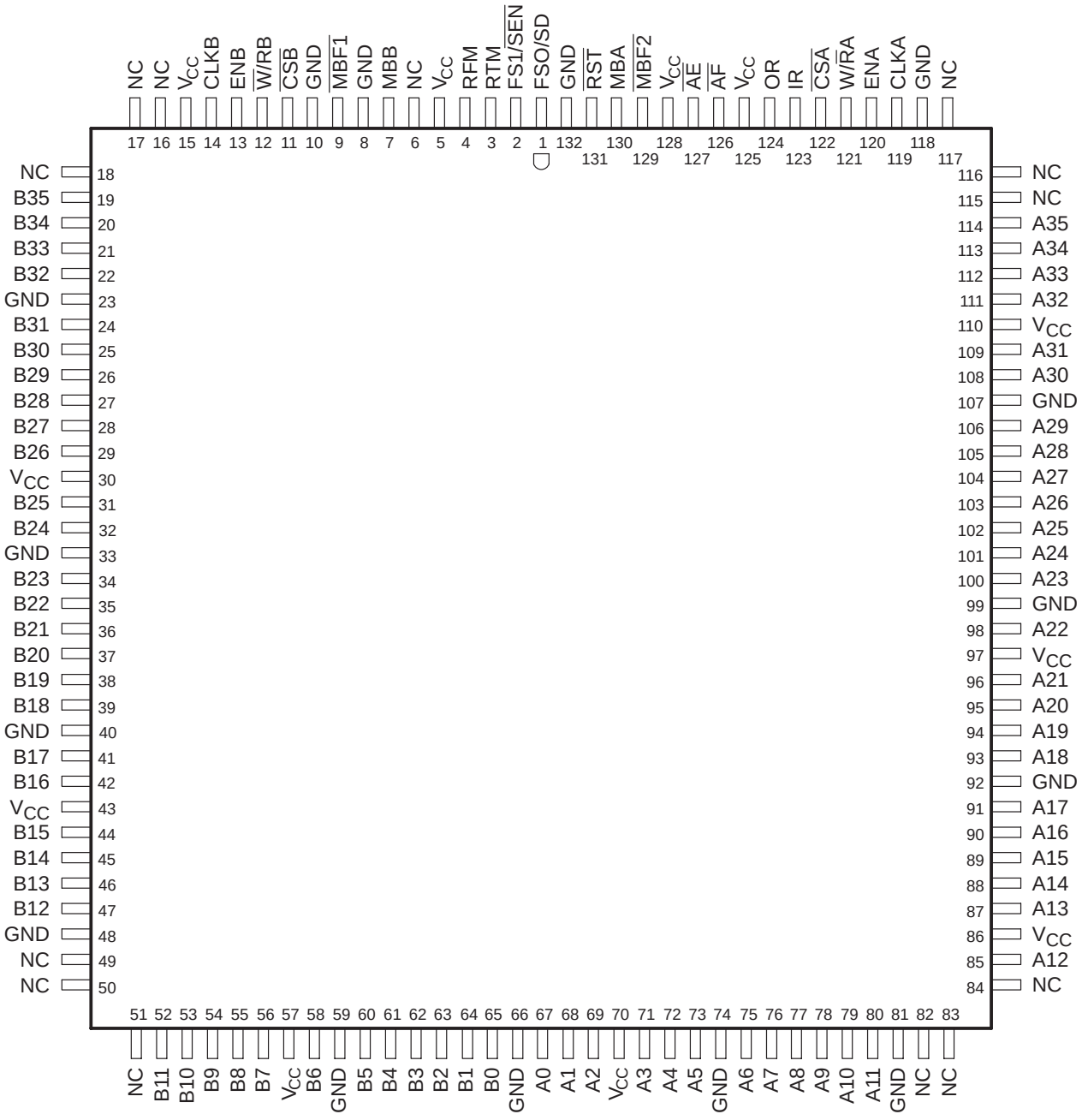
The input-ready (IR) flag and almost-full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to CLKA. The output-ready (OR) flag and almost-empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to CLKB. Offset values for the $\overline{AF}$ and $\overline{AE}$ flags of the FIFO can be programmed from port A or through a serial input.

The SN54ACT3641 is characterized for operation over the full military temperature range of – 55°C to 125°C.

For more information on this device family, see the following application reports:

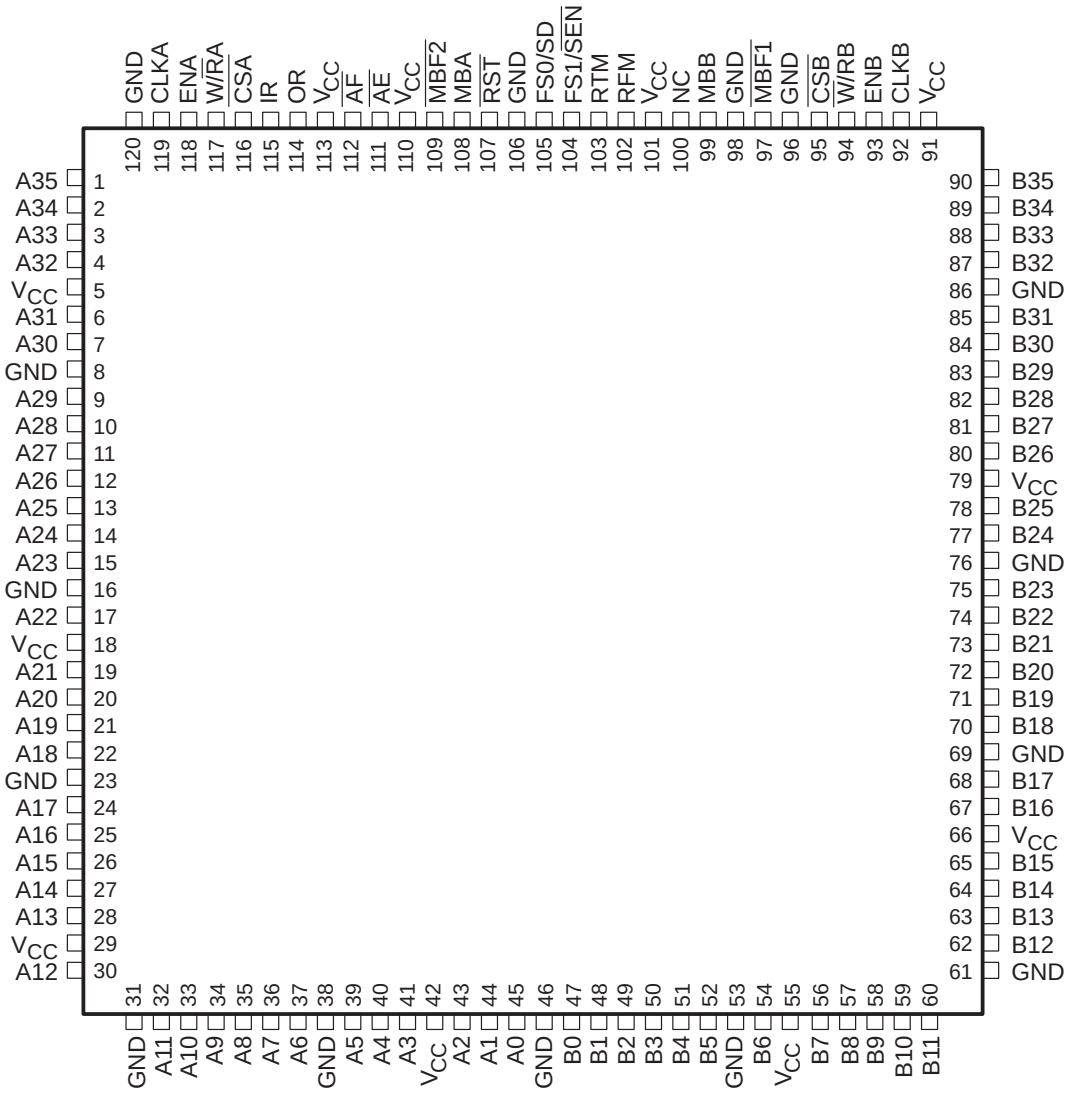
- *FIFO Patented Synchronous Retransmit: Programmable DSP-Interface Application for FIR Filtering* (literature number SCAA009)
- *FIFO Mailbox-Bypass Registers: Using Bypass Registers to Initialize DMA Control* (literature number SCAA007)
- *Metastability Performance of Clocked FIFOs* (literature number SCZA004)

**HFP PACKAGE**
**(TOP VIEW)**



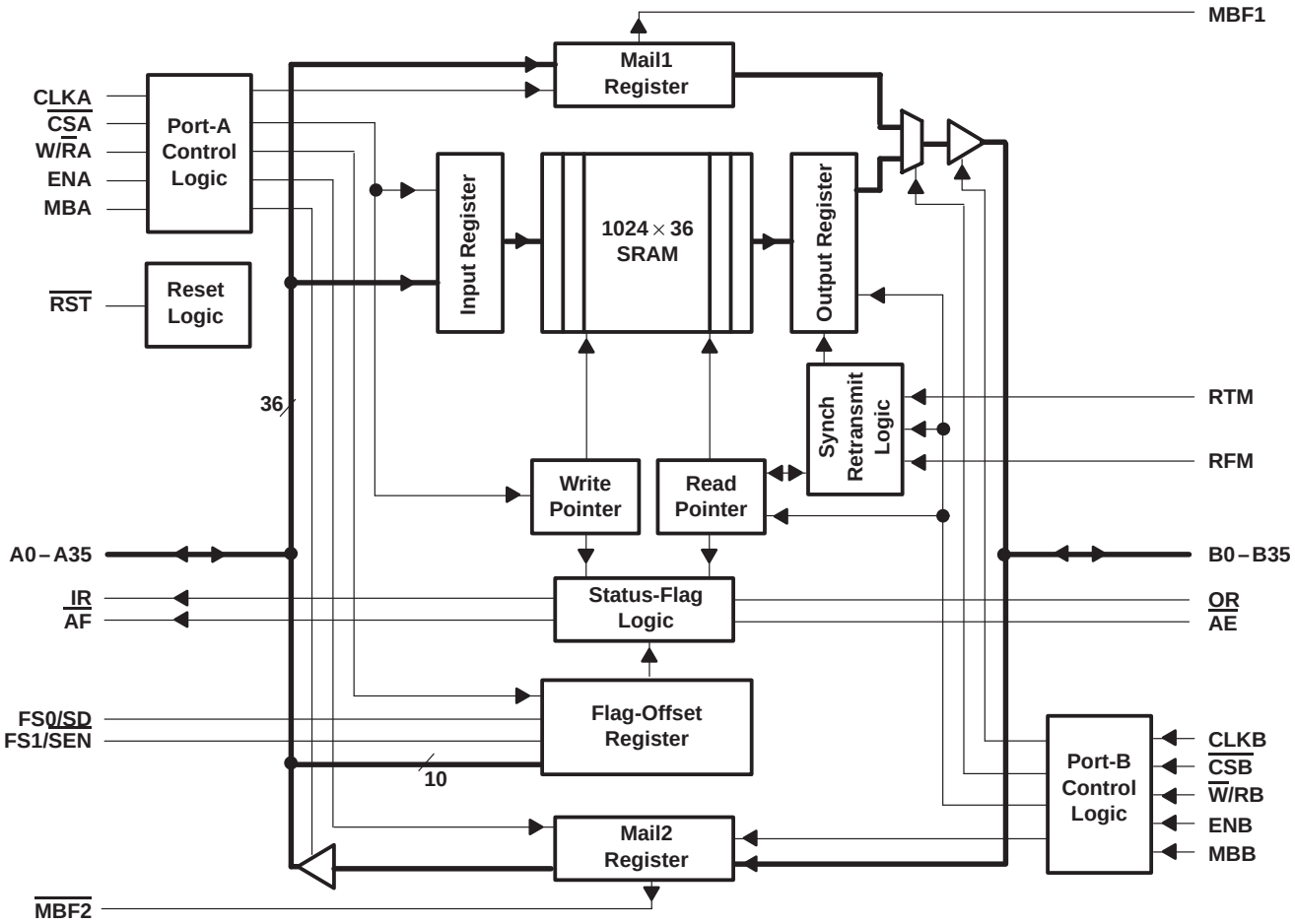

NC – No internal connection

**PCB PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## functional block diagram



## Terminal Functions

| TERMINAL NAME | I/O | DESCRIPTION |
|---|---|---|
| A0–A35 | I/O | Port-A data. The 36-bit bidirectional data port for side A. |
| $\overline{AE}$ | O | Almost-empty flag. Programmable flag synchronized to CLKB. $\overline{AE}$ is low when the number of words in the FIFO is less than or equal to the value in the almost-empty offset register (X). |
| $\overline{AF}$ | O | Almost-full flag. Programmable flag synchronized to CLKA. $\overline{AF}$ is low when the number of empty locations in the FIFO is less than or equal to the value in the almost-full offset register (Y). |
| B0–B35 | I/O | Port-B data. The 36-bit bidirectional data port for side B. |
| CLKA | I | Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IR and $\overline{AF}$ are synchronous to the low-to-high transition of CLKA. |
| CLKB | I | Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. OR and $\overline{AE}$ are synchronous to the low-to-high transition of CLKB. |
| $\overline{CSA}$ | I | Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high. |
| $\overline{CSB}$ | I | Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high. |
| ENA | I | Port-A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A. |
| ENB | I | Port-B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B. |
| FS1/$\overline{SEN}$, FS0/SD | I | Flag offset select 1/serial enable, flag offset select 0/serial data. FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag offset-register programming. During a device reset, FS1/$\overline{SEN}$ and FS0/SD select the flag offset-programming method. Three offset-register programming methods are available: automatically load one of two preset values, parallel load from port A, and serial load.<br>When serial load is selected for flag offset-register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the low-to-high transition of CLKA. When FS1/$\overline{SEN}$ is low, a rising edge on CLKA loads the bit present on FS0/SD into the X-and Y-offset registers. The number of bit writes required to program the offset registers is 20. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB. |
| IR | O | Input-ready flag. IR is synchronized to the low-to-high transition of CLKA. When IR is low, the FIFO is full and writes to its array are disabled. When the FIFO is in retransmit mode, IR indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IR is set low during reset and is set high after reset. |
| MBA | I | Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. |
| MBB | I | Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO data for output. |
| $\overline{MBF1}$ | O | Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{MBF1}$ is set high by a reset. |
| $\overline{MBF2}$ | O | Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is set high by a reset. |
| OR | O | Output-ready flag. OR is synchronized to the low-to-high transition of CLKB. When OR is low, the FIFO is empty and reads are disabled. Ready data is present in the output register of the FIFO when OR is high. OR is forced low during the reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory. |
| RFM | I | Read from mark. When the FIFO is in retransmit mode, a high on RFM enables a low-to-high transition of CLKB to reset the read pointer to the beginning retransmit location and output the first selected retransmit data. |
| $\overline{RST}$ | I | Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST}$ is low. The low-to-high transition of $\overline{RST}$ latches the status of FS0 and FS1 for $\overline{AF}$ and $\overline{AE}$ offset selection. |
| RTM | I | Retransmit mode. When RTM is high and valid data is present in the FIFO output register (OR is high), a low-to-high transition of CLKB selects the data for the beginning of a retransmit and puts the FIFO in retransmit mode. The selected word remains the initial retransmit point until a low-to-high transition of CLKB occurs while RTM is low, taking the FIFO out of retransmit mode. |

**Terminal Functions (Continued)**

| TERMINAL NAME | I/O | DESCRIPTION |
|---|---|---|
| W/$\overline{R}$A | I | Port-A write/read select. A high on W/$\overline{R}$A selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{R}$A is high. |
| $\overline{W}$/RB | I | Port-B write/read select. A low on $\overline{W}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{W}$/RB is low. |

## detailed description

### reset

The SN54ACT3641 is reset by taking the reset ($\overline{RST}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A reset initializes the memory read and write pointers and forces the IR flag low, the OR flag low, the $\overline{AE}$ flag low, and the $\overline{AF}$ flag high. Resetting the device also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) high. After a FIFO is reset, its IR flag is set high after at least two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

### almost-empty flag and almost-full flag offset programming

Two registers in the SN54ACT3641 are used to hold the offset values for the $\overline{AE}$ and $\overline{AF}$ flags. The $\overline{AE}$ flag offset register is labeled X, and the $\overline{AF}$ flag offset register is labeled Y. The offset registers can be loaded with a value in three ways: one of two preset values are loaded into the offset registers, parallel load from port A, or serial load. The offset register programming mode is chosen by the flag select (FS1, FS0) inputs during a low-to-high transition on $\overline{RST}$ (see Table 1).

**Table 1. Flag Programming**

| FS1 | FS0 | $\overline{RST}$ | X AND Y REGISTERS† |
|---|---|---|---|
| H | H | ↑ | Serial load |
| H | L | ↑ | 64 |
| L | H | ↑ | 8 |
| L | L | ↑ | Parallel load from port A |

† X register holds the offset for $\overline{AE}$; Y register holds the offset for $\overline{AF}$.

#### *preset values*

If a preset value of 8 or 64 is chosen by FS1 and FS0 at the time of an $\overline{RST}$ low-to-high transition according to Table 1, the preset value is automatically loaded into the X and Y registers. No other device initialization is necessary to begin normal operation, and the IR flag is set high after two low-to-high transitions on CLKA.

#### *parallel load from port A*

To program the X and Y registers from port A, the device is reset with FS0 and FS1 low during the low-to-high transition of $\overline{RST}$. After this reset is complete, IR is set high after two low-to-high transitions on CLKA. The first two writes to the FIFO do not store data in its memory but load the offset registers in the order Y, X. Each offset register of the SN54ACT3641 uses port-A inputs (A9–A0). Data input A9 is used as the most-significant bit of the binary number. Each register value can be programmed from 1 to 1020. After both offset registers are programmed from port A, subsequent FIFO writes store data in the SRAM.

***serial load***

To program the X and Y registers serially, the device is reset with FS0/SD and FS1/$\overline{SEN}$ high during the low-to-high transition of $\overline{RST}$. After this reset is complete, the X-and Y-register values are loaded bitwise through FS0/SD on each low-to-high transition of CLKA that FS1/$\overline{SEN}$ is low. Twenty-bit writes are needed to complete the programming. The first bit write stores the most-significant bit of the Y register, and the last bit write stores the least-significant bit of the the X register. Each register value can be programmed from 1 to 1020.

When the option is chosen to program the offset registers serially, IR remains low until all 20 bits are written. IR is set high by the low-to-high transition of CLKA after the last bit is loaded to allow normal FIFO operation.

**FIFO write/read operation**

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0–A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. The A0–A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are low.

Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{CSA}$ and the port-A mailbox select (MBA) are low, W/$\overline{RA}$, the port-A enable (ENA), and the IR flag are high (see Table 2). Writes to the FIFO are independent of any concurrent FIFO reads.

**Table 2. Port-A Enable Function Table**

| $\overline{CSA}$ | W/$\overline{RA}$ | ENA | MBA | CLKA | A0 – A35 OUTPUTS | PORT FUNCTION |
|---|---|---|---|---|---|---|
| H | X | X | X | X | In high-impedance state | None |
| L | H | L | X | X | In high-impedance state | None |
| L | H | H | L | ↑ | In high-impedance state | FIFO write |
| L | H | H | H | ↑ | In high-impedance state | Mail1 write |
| L | L | L | L | X | Active, mail2 register | None |
| L | L | H | L | ↑ | Active, mail2 register | None |
| L | L | L | H | X | Active, mail2 register | None |
| L | L | H | H | ↑ | Active, mail2 register | Mail2 read (set $\overline{MBF2}$ high) |

The port-B control signals are identical to those of port A with the exception that the port-B write/read select ($\overline{W}$/RB) is the inverse of the port-A write/read select (W/$\overline{RA}$). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select ($\overline{W}$/RB). The B0–B35 outputs are in the high-impedance state when either $\overline{CSB}$ is high or $\overline{W}$/RB is low. The B0–B35 outputs are active when $\overline{CSB}$ is low and $\overline{W}$/RB is high.

Data is read from the FIFO to its output register on a low-to-high transition of CLKB when $\overline{CSB}$ and the port-B mailbox select (MBB) are low, $\overline{W}$/RB, the port-B enable (ENB), and the OR flag are high (see Table 3). Reads from the FIFO are independent of any concurrent FIFO writes.

**FIFO write/read operation (continued)**

**Table 3. Port-B Enable Function Table**

| $\overline{CSB}$ | $\overline{W}$/RB | ENB | MBB | CLKB | B0 – B35 OUTPUTS | PORT FUNCTION |
|---|---|---|---|---|---|---|
| H | X | X | X | X | In high-impedance state | None |
| L | L | L | X | X | In high-impedance state | None |
| L | L | H | L | ↑ | In high-impedance state | None |
| L | L | H | H | ↑ | In high-impedance state | Mail2 write |
| L | H | L | L | X | Active, FIFO output register | None |
| L | H | H | L | ↑ | Active, FIFO output register | FIFO read |
| L | H | L | H | X | Active, mail1 register | None |
| L | H | H | H | ↑ | Active, mail1 register | Mail1 read (set $\overline{MBF1}$ high) |

The setup- and hold-time constraints to the port clocks for the port-chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port-chip select and write/read select can change states during the setup- and hold-time window of the cycle.

When OR is low, the next data word is sent to the FIFO output register automatically by the CLKB low-to-high transition that sets the flag high. When OR is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port-B chip select ($\overline{CSB}$), write/read select ($\overline{W}$/RB), enable (ENB), and mailbox select (MBB).

**synchronized FIFO flags**

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another. OR and $\overline{AE}$ are synchronized to CLKB. IR and $\overline{AF}$ are synchronized to CLKA. Table 4 shows the relationship of each flag to the number of words stored in memory.

**Table 4. FIFO Flag Operation**

| NUMBER OF WORDS IN FIFO†‡ | SYNCHRONIZED TO CLKB | | SYNCHRONIZED TO CLKA | |
|---|---|---|---|---|
| | OR | $\overline{AE}$ | $\overline{AF}$ | IR |
| 0 | L | L | H | H |
| 1 to X | H | L | H | H |
| (X + 1) to [1024 – (Y + 1)] | H | H | H | H |
| (1024 – Y) to 1023 | H | H | L | H |
| 1024 | H | H | L | L |

† X is the almost-empty offset for $\overline{AE}$. Y is the almost-full offset for $\overline{AF}$.
‡ When a word is present in the FIFO output register, its previous memory location is free.

***output-ready flag (OR)***

The OR flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). When the OR flag is high, new data is present in the FIFO output register. When OR is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an OR flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of CLKB; therefore, an OR flag is low if a word in memory is the next data to be sent to the FIFO output register and three CLKB cycles have not elapsed since the time the word was written. The OR flag of the FIFO remains low until the third low-to-high transition of CLKB occurs, simultaneously forcing OR high and shifting the word to the FIFO output register.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time $t_{sk(1)}$, or greater, after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 6).

***input-ready flag (IR)***

The IR flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). When IR is high, a memory location is free in the SRAM to write new data. No memory locations are free when the IR flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an IR flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of three cycles of CLKA. Therefore, IR is low if less than two cycles of CLKA have elapsed since the next memory write location has been read. The second low-to-high transition on CLKA after the read sets IR high, and data can be written in the following cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time $t_{sk(1)}$, or greater, after the read. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 7).

***almost-empty flag ($\overline{AE}$)***

The $\overline{AE}$ flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an $\overline{AE}$ flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). $\overline{AE}$ is low when the FIFO contains X or fewer words and is high when the FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKB are required after a FIFO write for the $\overline{AE}$ flag to reflect the new level of fill. Therefore, the $\overline{AE}$ flag of a FIFO containing (X + 1) or more words remains low if two cycles of CLKB have not elapsed since the write that filled the memory to the (X + 1) level. $\overline{AE}$ is set high by the second low-to-high transition of CLKB after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of CLKB begins the first synchronization cycle if it occurs at time $t_{sk(2)}$, or greater, after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 8).

***almost-full flag ($\overline{AF}$)***

The $\overline{AF}$ flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an $\overline{AF}$ flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). $\overline{AF}$ is low when the number of words in the FIFO is greater than or equal to (1024 – Y). $\overline{AF}$ is high when the number of words in the FIFO is less than or equal to [1024 – (Y + 1)]. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKA are required after a FIFO read for its $\overline{AF}$ flag to reflect the new level of fill. Therefore, the $\overline{AF}$ flag of a FIFO containing [1024 – (Y + 1)] or fewer words remains low if two cycles of CLKA have not elapsed since the read that reduced the number of words in memory to [1024 – (Y + 1)]. $\overline{AF}$ is set high by the second low-to-high transition of CLKA after the FIFO read that reduces the number of words in memory to [1024 – (Y + 1)]. A low-to-high transition of CLKA begins the first synchronization cycle if it occurs at time $t_{sk(2)}$, or greater, after the read that reduces the number of words in memory to [1024 – (Y + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 9).

**synchronous retransmit**

The synchronous-retransmit feature of the SN54ACT3641 allows FIFO data to be read repeatedly, starting at a user-selected position. First the FIFO is put into retransmit mode to select a beginning word and prevent ongoing FIFO write operations from destroying retransmit data. Data vectors with a minimum length of three words can retransmit repeatedly starting at the selected word. The FIFO can be taken out of retransmit mode at any time and allow normal device operation.

The FIFO is put in retransmit mode by a low-to-high transition on CLKB when the retransmit-mode (RTM) input is high and OR is high. This rising CLKB edge marks the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a low-to-high transition occurs while RTM is low.

When two or more reads have been done, past the initial retransmit word, a retransmit is initiated by a low-to-high transition on CLKB when the read-from-mark (RFM) input is high. This rising CLKB edge shifts the first retransmit word to the FIFO output register and subsequent reads can begin immediately. Retransmit loops can be done endlessly while the FIFO is in retransmit mode. RFM must be low during the CLKB rising edge that takes the FIFO out of retransmit mode.

When the FIFO is put into retransmit mode, it operates with two read pointers. The current read pointer operates normally, incrementing each time a new word is shifted to the FIFO output register and used by the OR and $\overline{AE}$ flags. The shadow read pointer stores the SRAM location at the time the device is put into retransmit mode and does not change until the device is taken out of retransmit mode. The shadow read pointer is used by the IR and $\overline{AF}$ flags. Data writes can proceed while the FIFO is in retransmit mode, but $\overline{AF}$ is set low by the write that stores (102 – Y) words after the first retransmit word. The IR flag is set low by the 1024th write after the first retransmit word.

When the FIFO is in retransmit mode and RFM is high, a rising CLKB edge loads the current read pointer with the shadow read-pointer value and the OR flag reflects the new level of fill immediately. If the retransmit changes the FIFO status out of the almost-empty range, up to two CLKB rising edges after the retransmit cycle are needed to switch $\overline{AE}$ high (see Figure 11). The rising CLKB edge that takes the FIFO out of retransmit mode shifts the read pointer used by the IR and $\overline{AF}$ flags from the shadow to the current read pointer. If the change of read pointer used by IR and $\overline{AF}$ should cause one or both flags to transition high, at least two CLKA synchronizing cycles are needed before the flags reflect the change. A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of IR if it occurs at time $t_{sk(1)}$, or greater, after the rising CLKB edge (see Figure 12). A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of $\overline{AF}$ if it occurs at time $t_{sk(2)}$, or greater, after the rising CLKB edge (see Figure 14).

### mailbox registers

Two 36-bit bypass registers are on the SN54ACT3641 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while its mail flag is low.

When the port-B data (B0–B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B mailbox select (MBB) input is low and from the mail1 register when MBB is high. Mail2 data is always present on the port-A data (A0–A35) outputs when they are active. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

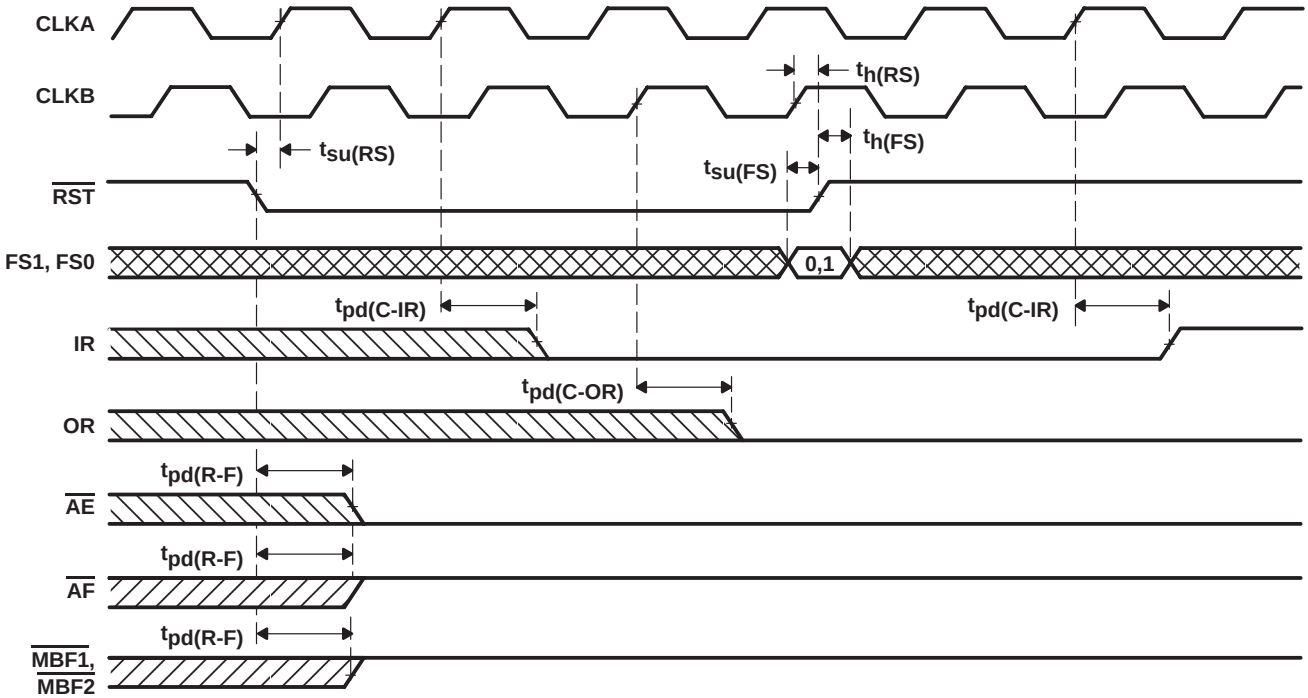
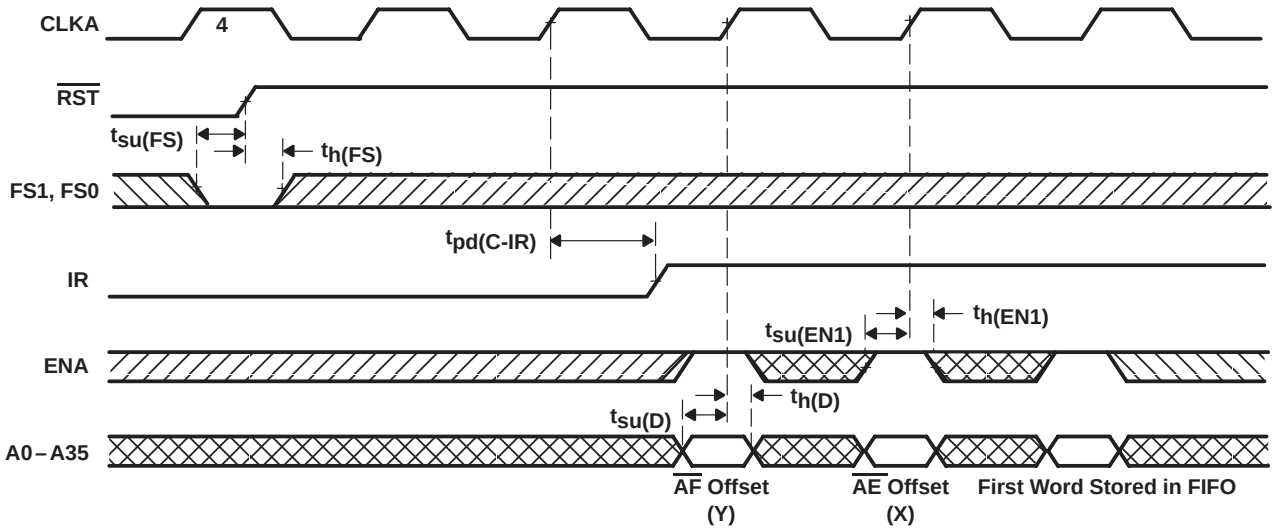
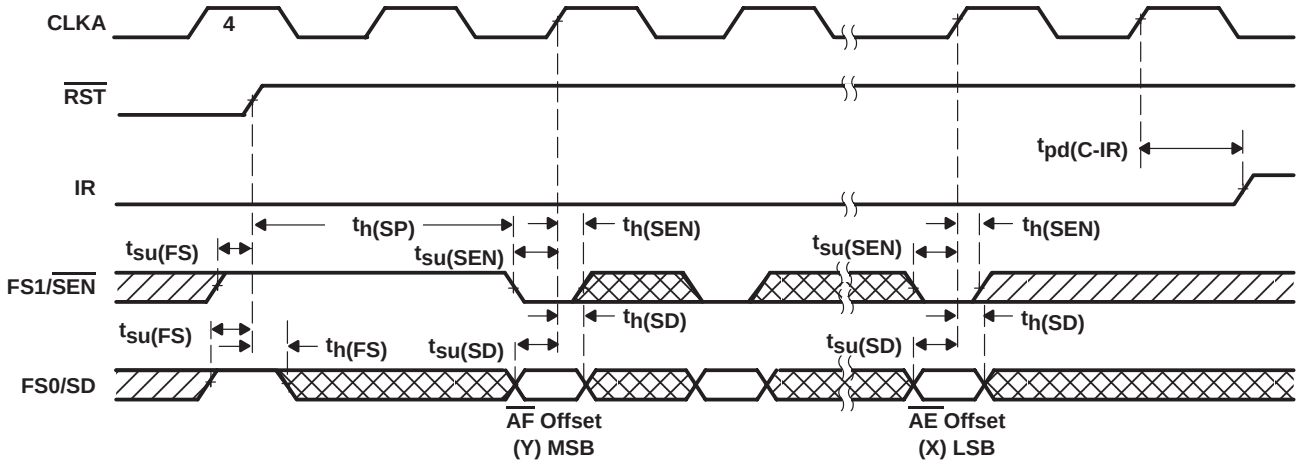



**Figure 1. FIFO Reset Loading X and Y With a Preset Value of Eight**




NOTE A: $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

**Figure 2. Programming the $\overline{AF}$ Flag and $\overline{AE}$ Flag Offset Values From Port A**




NOTE B: It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until IR is set high.

**Figure 3. Programming the $\overline{AF}$ Flag and $\overline{AE}$ Flag Offset Values Serially**

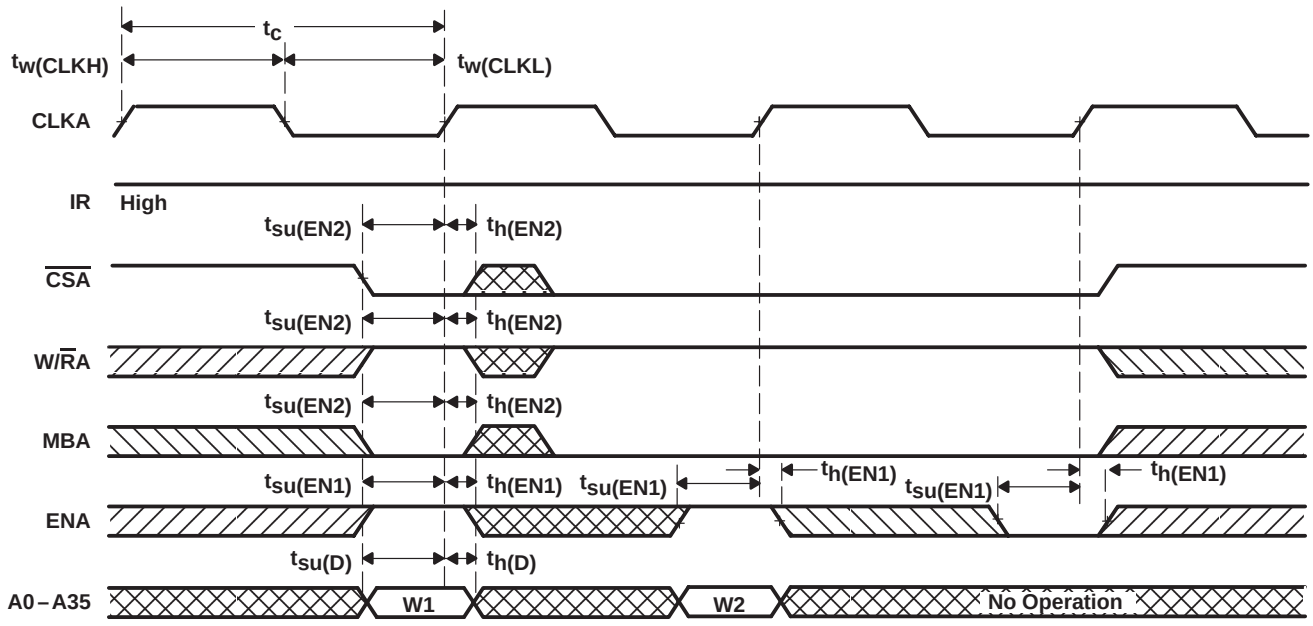



**Figure 4. FIFO Write-Cycle Timing**

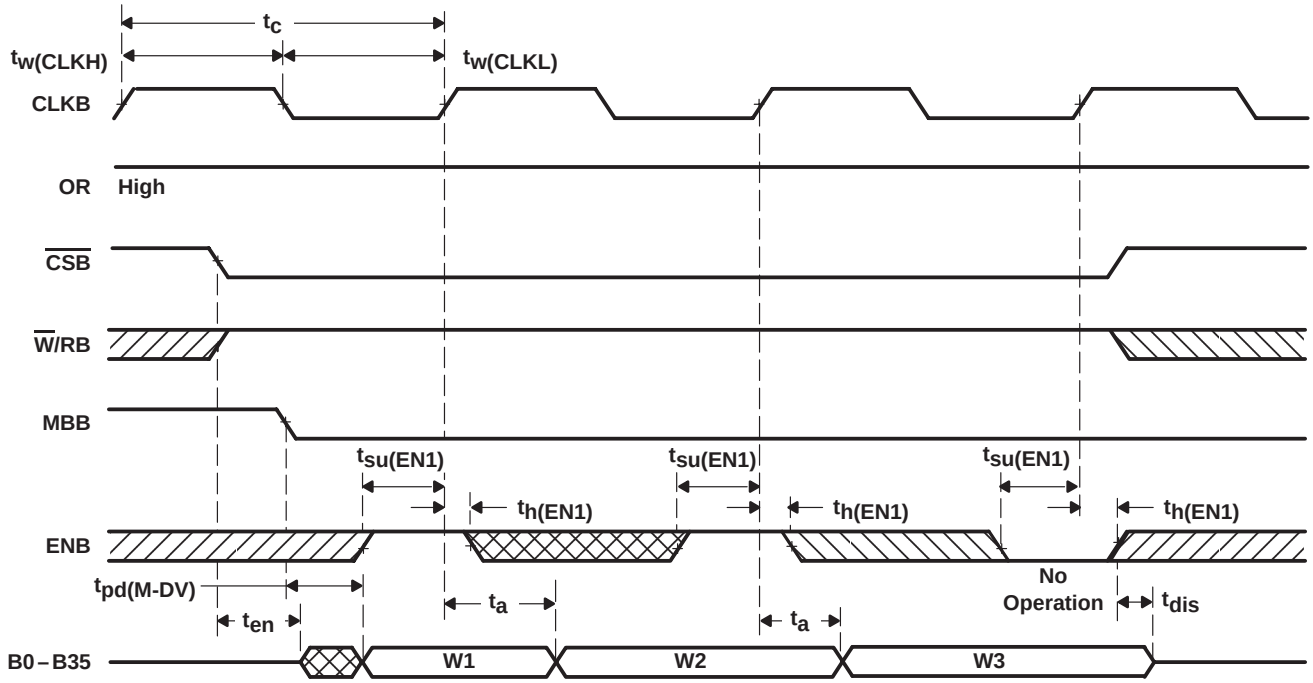
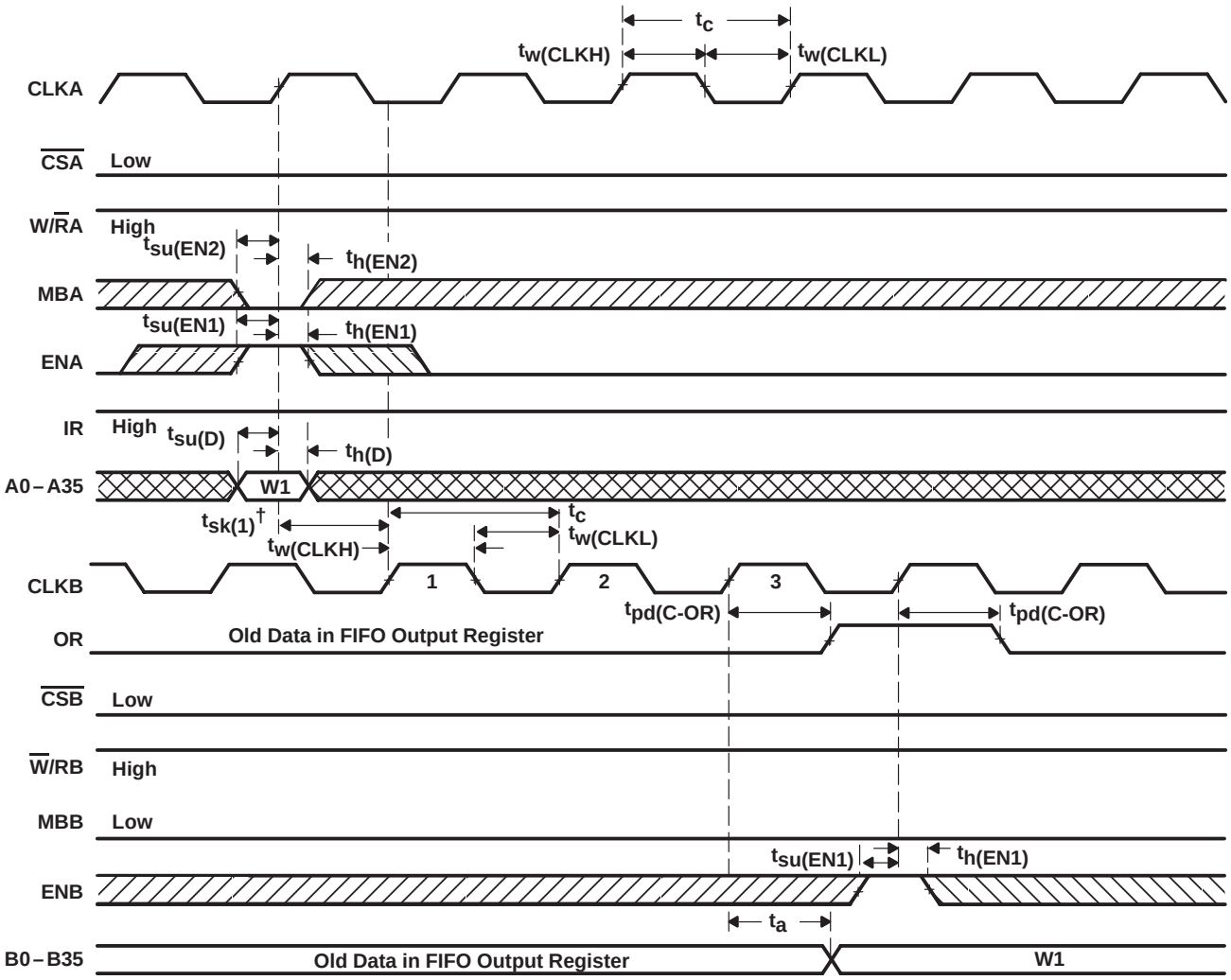
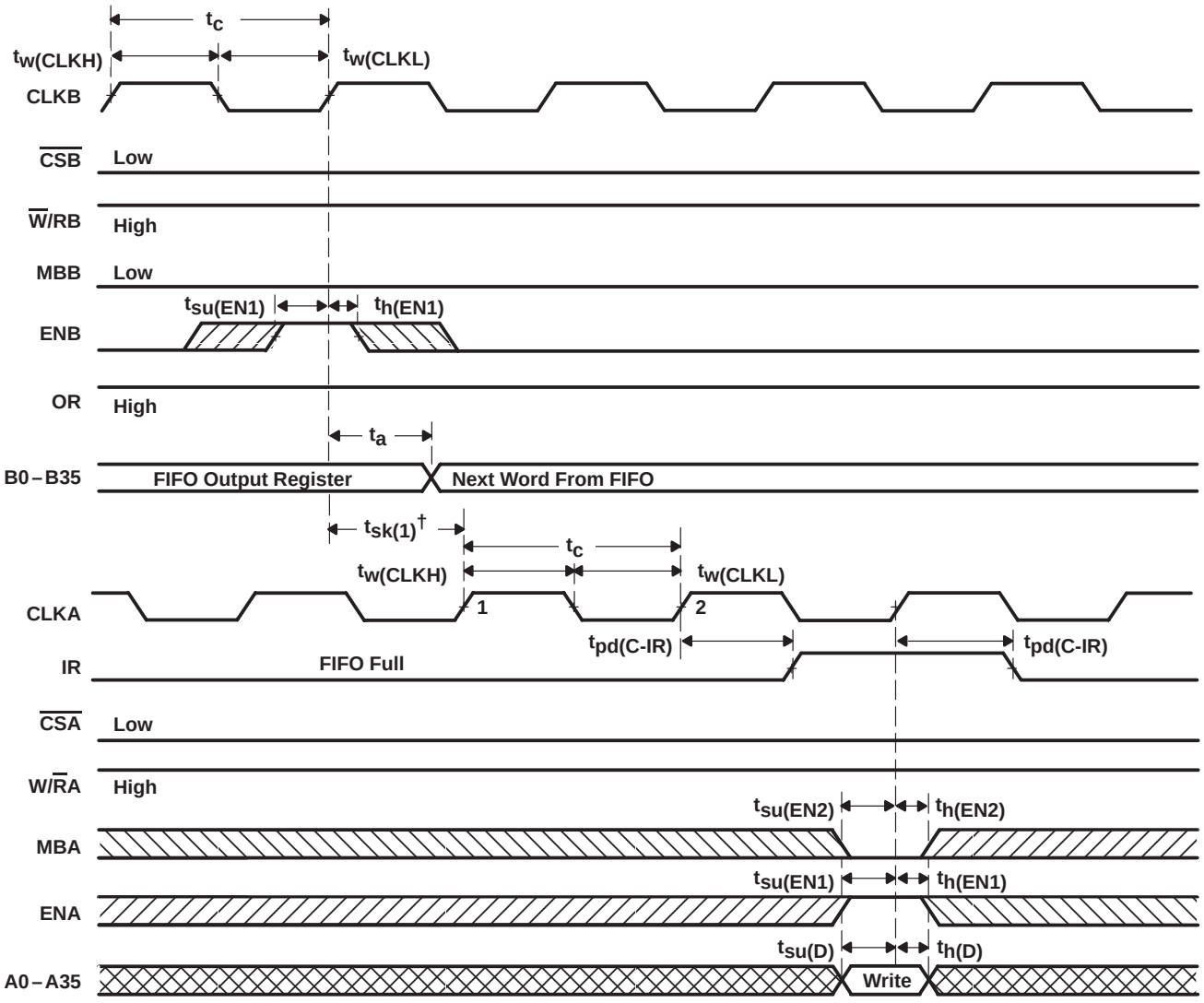



**Figure 5. FIFO Read-Cycle Timing**



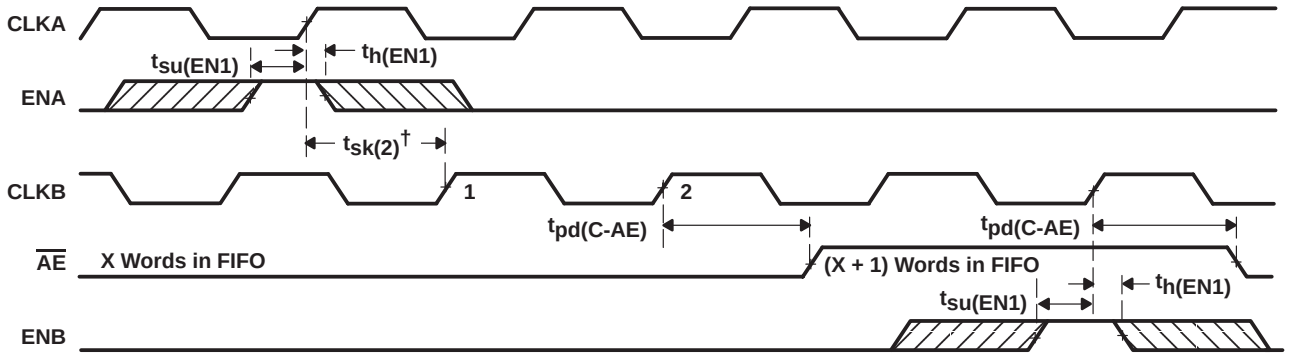

† $t_{sk(1)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition high and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(1)}$, the transition of OR high and the first word load to the output register can occur one CLKB cycle later than shown.

**Figure 6. OR-Flag Timing and First Data-Word Fall Through When the FIFO Is Empty**



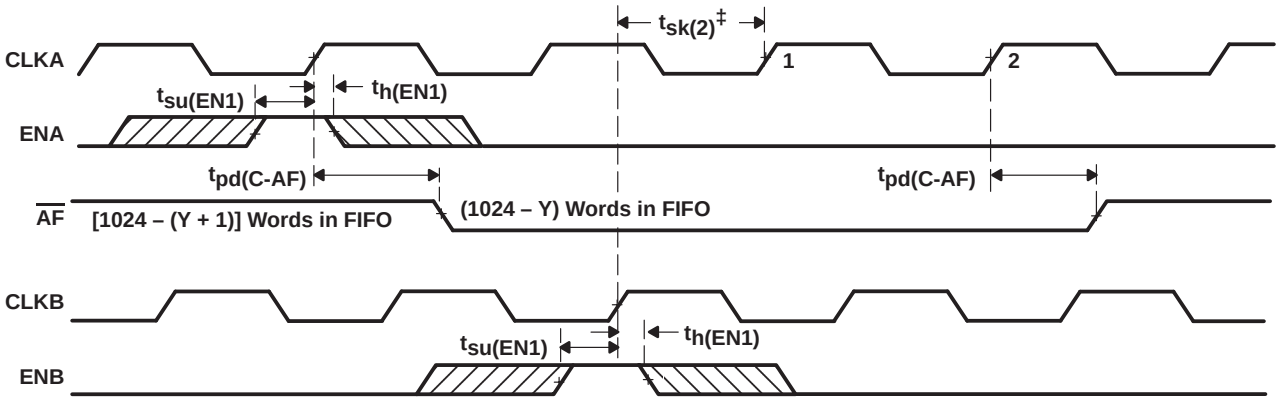

† $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, IR can transition high one CLKA cycle later than shown.

**Figure 7. IR-Flag Timing and First Available Write When the FIFO Is Full**



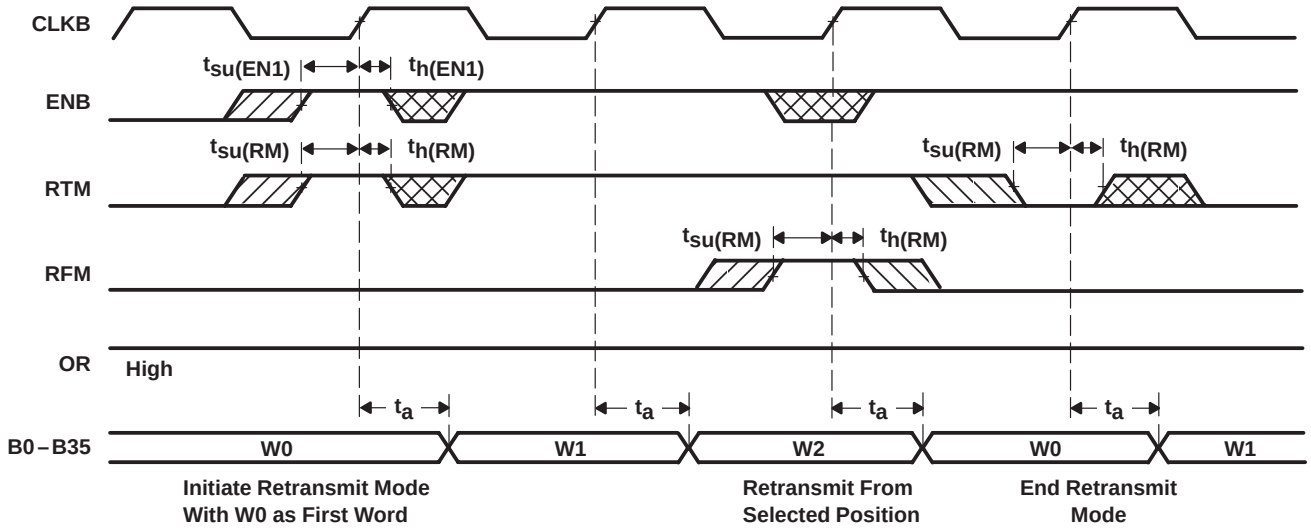

† $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(2)}$, $\overline{AE}$ can transition high one CLKB cycle later than shown.
NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L)

**Figure 8. Timing for $\overline{AE}$ When FIFO Is Almost Empty**



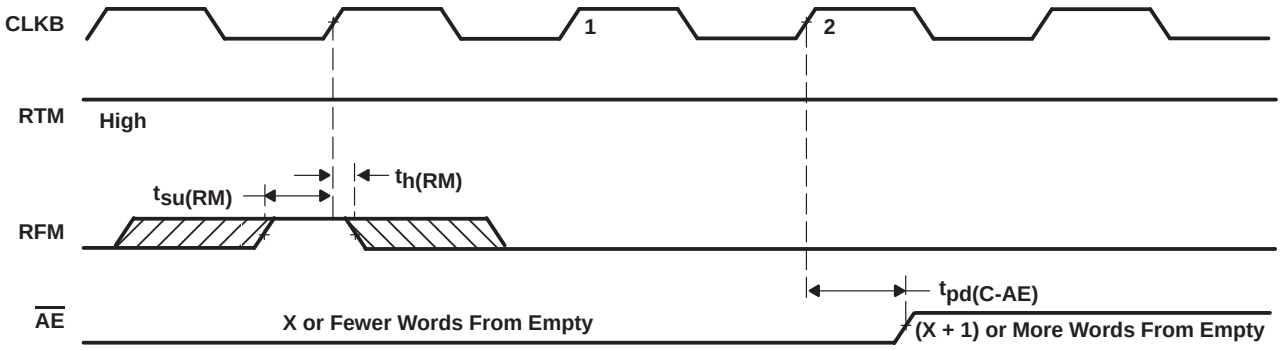

‡ $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, $\overline{AF}$ can transition high one CLKA cycle later than shown.
NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L)

**Figure 9. Timing for $\overline{AF}$ When FIFO Is Almost Full**



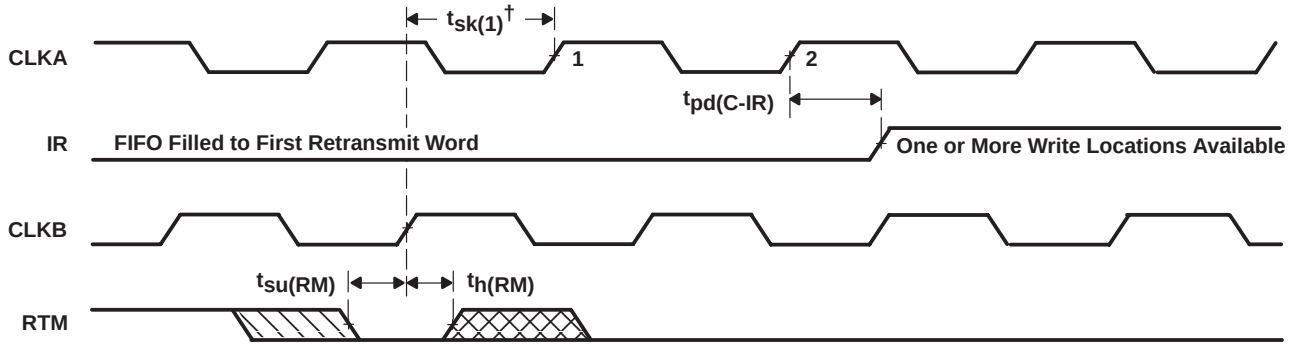

NOTE A: $\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L. No input enables other than RTM and RFM are needed to control retransmit mode or begin a retransmit. Other enables are shown only to relate retransmit operations to the FIFO output register.

**Figure 10. Retransmit Timing Showing Minimum Retransmit Length**



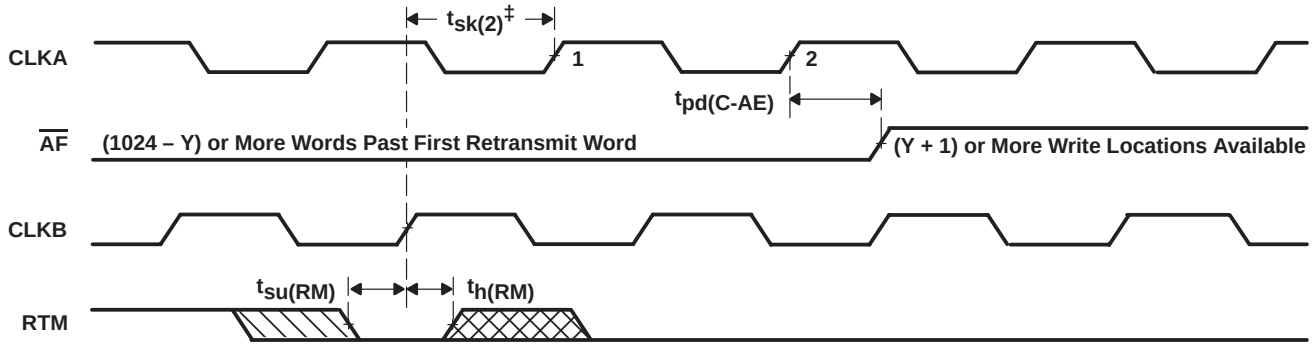

NOTE A: X is the value loaded in the $\overline{AE}$ flag offset register.

**Figure 11. $\overline{AE}$ Maximum Latency When Retransmit Increases the Number of Stored Words Above X**




† $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, IR can transition high one CLKA cycle later than shown.

**Figure 12. IR Timing From the End of Retransmit Mode When One or More Write Locations Are Available**




‡ $t_{sk(2)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, $\overline{AF}$ can transition high one CLKA cycle later than shown.

NOTE A: Y is the value loaded in the $\overline{AF}$ flag offset register.

**Figure 13. $\overline{AF}$ Timing From the End of Retransmit Mode When (Y + 1) or More Write Locations Are Available**

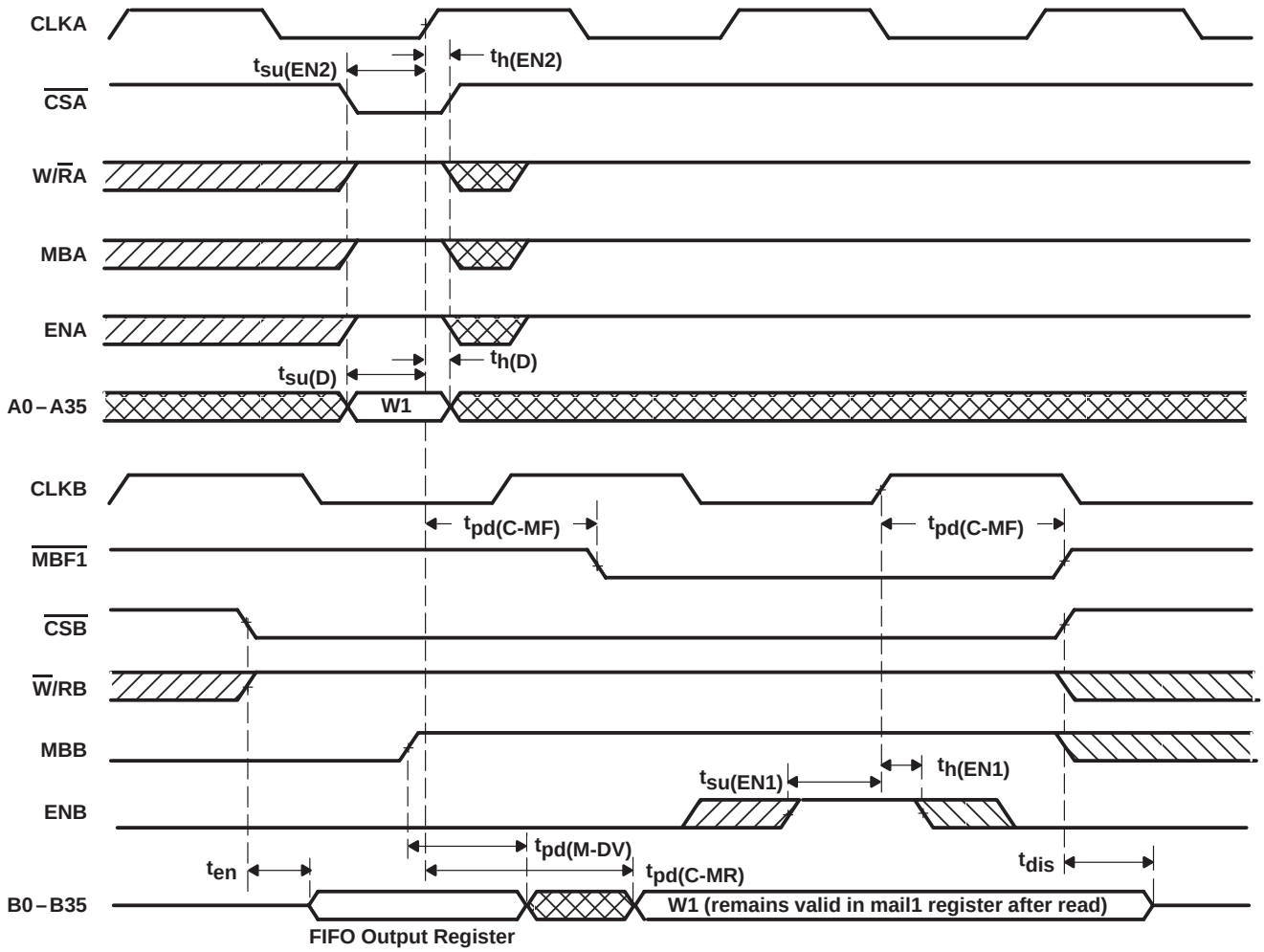



**Figure 14. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag**

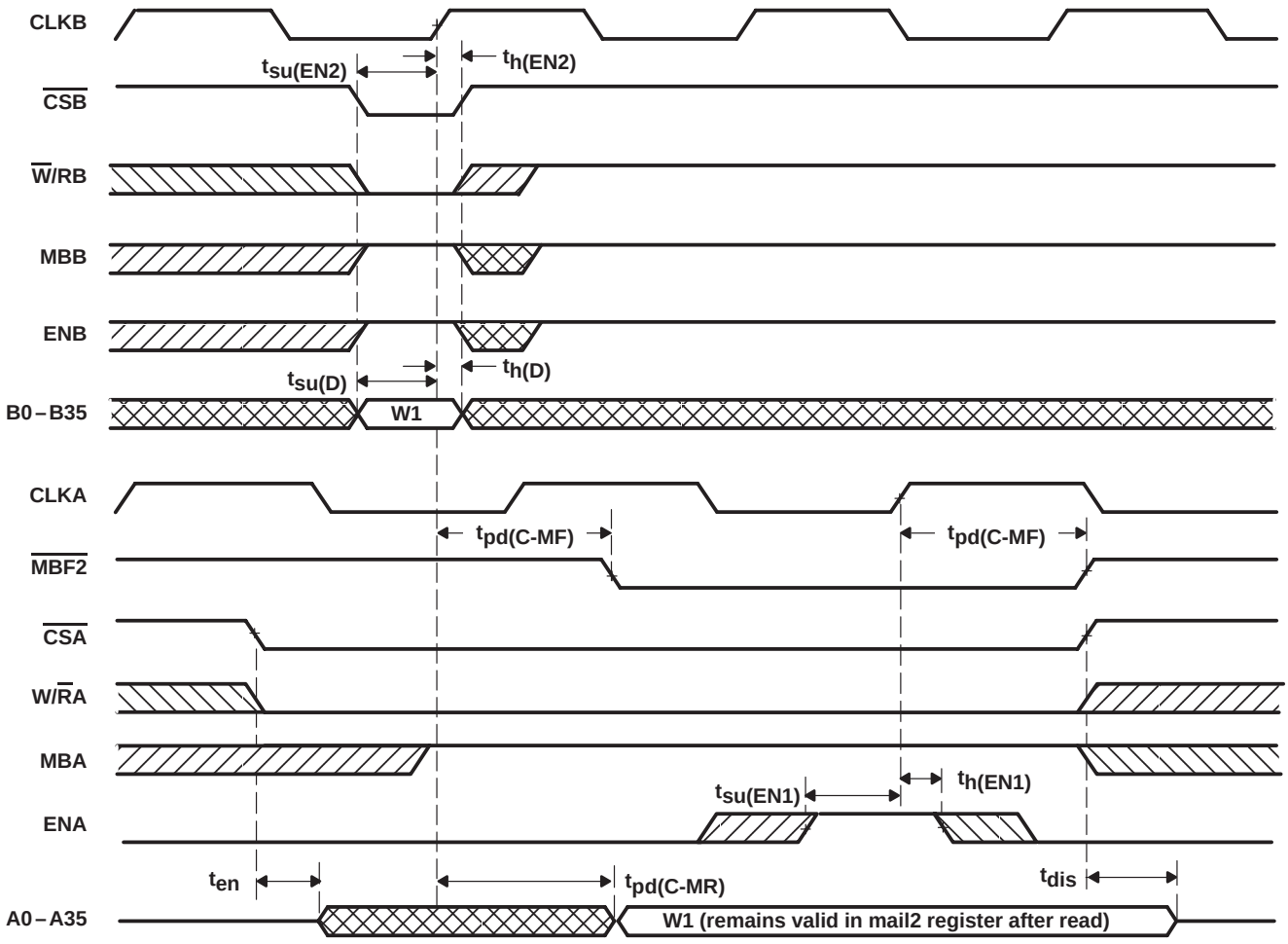



**Figure 15. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±400 mA
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

### recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | –4 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $T_A$ | Operating free-air temperature | –55 | 125 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CC}$ = 4.5 V, $I_{OH}$ = –4 mA | | | 2.4 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, $I_{OL}$ = 8 mA | | | | | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ or 0 | | | | | ±5 | µA |
| $I_{OZ}$ | $V_{CC}$ = 5.5 V, $V_O$ = $V_{CC}$ or 0 | | | | | ±5 | µA |
| $I_{CC}$§ | $V_{CC}$ = 5.5 V, $V_I$ = $V_{CC}$ – 0.2 V or 0 | | | | | 400 | µA |
| $\Delta I_{CC}$¶ | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | $\overline{CSA}$ = $V_{IH}$ | A0–A35 | | 0 | | mA |
| | | $\overline{CSB}$ = $V_{IH}$ | B0–B35 | | 0 | | |
| | | $\overline{CSA}$ = $V_{IL}$ | A0–A35 | | | 1 | |
| | | $\overline{CSB}$ = $V_{IL}$ | B0–B35 | | | 1 | |
| | | All other inputs | | | | 1 | |
| $C_i$ | $V_I$ = 0, f = 1 MHz | | | | 4 | | pF |
| $C_o$ | $V_O$ = 0, f = 1 MHz | | | | 8 | | pF |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ $I_{CC}$ is measured in the A to B direction.
¶ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 16)**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{clock}$ | Clock frequency, CLKA or CLKB | | 50 | MHz |
| $t_c$ | Clock cycle time, CLKA or CLKB | 20 | | ns |
| $t_{w(CH)}$ | Pulse duration, CLKA and CLKB high | 8 | | ns |
| $t_{w(CL)}$ | Pulse duration, CLKA and CLKB low | 8 | | ns |
| $t_{su(D)}$ | Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑ | 6 | | ns |
| $t_{su(EN1)}$ | Setup time, ENA to CLKA↑; ENB to CLKB↑ | 6 | | ns |
| $t_{su(EN2)}$ | Setup time, $\overline{CSA}$, W/$\overline{RA}$, and MBA to CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, and MBB to CLKB↑ | 7.5 | | ns |
| | W/$\overline{RA}$ to CLKA↑ | 9 | | |
| $t_{su(RM)}$ | Setup time, RTM and RFM to CLKB↑ | 6.5 | | ns |
| $t_{su(RS)}$ | Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑† | 6 | | ns |
| $t_{su(FS)}$ | Setup time, FS0 and FS1 before $\overline{RST}$ high | 10 | | ns |
| $t_{su(SD)}$‡ | Setup time, FS0/SD before CLKA↑ | 6 | | ns |
| $t_{su(SEN)}$‡ | Setup time, FS1/$\overline{SEN}$ before CLKA↑ | 6 | | ns |
| $t_{h(D)}$ | Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑ | 0 | | ns |
| $t_{n(EN1)}$ | Hold time, ENA after CLKA↑; ENB after CLKB↑ | 0 | | ns |
| $t_{n(EN2)}$ | Hold time, $\overline{CSA}$, W/$\overline{RA}$, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, and MBB after CLKB↑ | 0 | | ns |
| $t_{n(RM)}$ | Hold time, RTM and RFM after CLKB↑ | 0 | | ns |
| $t_{h(RS)}$ | Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑ † | 6 | | ns |
| $t_{h(FS)}$ | Hold time, FS0 and FS1 after $\overline{RST}$ high | 0 | | ns |
| $t_{h(SP)}$‡ | Hold time, FS1/$\overline{SEN}$ high after $\overline{RST}$ high | 0 | | ns |
| $t_{h(SD)}$‡ | Hold time, FS0/SD after CLKA↑ | 0 | | ns |
| $t_{h(SEN)}$‡ | Hold time, FS1/$\overline{SEN}$ after CLKA↑ | 0 | | ns |
| $t_{sk(1)}$§ | Skew time between CLKA↑ and CLKB↑ for OR and IR | 11 | | ns |
| $t_{sk(2)}$§ | Skew time between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$ | 16 | | ns |

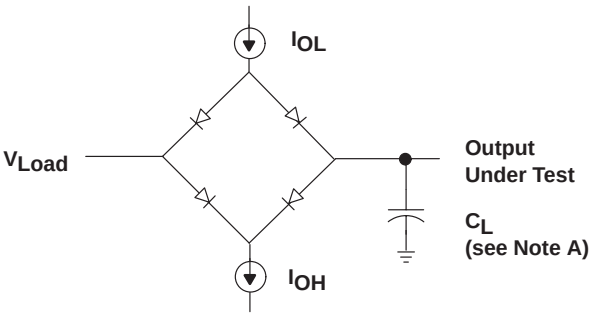
† Requirement to count the clock edge as one of at least four needed to reset a FIFO
‡ Applies only when serial load method is used to program flag offset registers
§ Skew time is not a timing constraint for proper device operation and is included only to illustrate the timing relationship between CLKA cycle and CLKB cycle.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 30 pF (see Figures 1 through 16)**

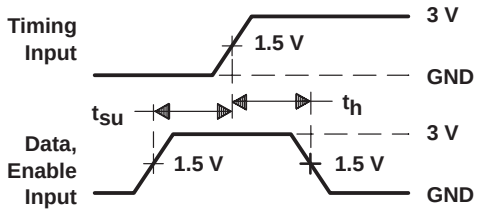
| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{max}$ | | 50 | | MHz |
| $t_a$ | Access time, CLKB↑ to B0–B35 | 3 | 15 | ns |
| $t_{pd(C-IR)}$ | Propagation delay time, CLKA↑ to IR | 1 | 10 | ns |
| $t_{pd(C-OR)}$ | Propagation delay time, CLKB↑ to OR | 1 | 10 | ns |
| $t_{pd(C-AE)}$ | Propagation delay time, CLKB↑ to $\overline{AE}$ | 1 | 10 | ns |
| $t_{pd(C-AF)}$ | Propagation delay time, CLKA↑ to $\overline{AF}$ | 1 | 10 | ns |
| $t_{pd(C-MF)}$ | Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high | 0 | 10 | ns |
| $t_{pd(C-MR)}$ | Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡ | 3 | 15 | ns |
| $t_{pd(M-DV)}$ | Propagation delay time, MBB to B0–B35 valid | 3 | 15 | ns |
| $t_{pd(R-F)}$ | Propagation delay time, $\overline{RST}$ low to $\overline{AE}$ low and $\overline{AF}$ high | 1 | 20 | ns |
| $t_{en}$ | Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active | 2 | 13 | ns |
| $t_{dis}$ | Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance | 1 | 10 | ns |

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high

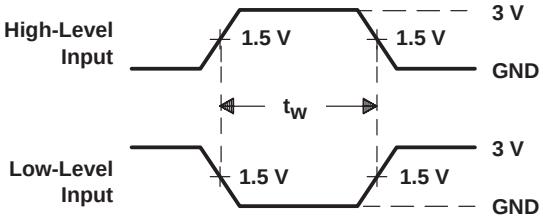
## PARAMETER MEASUREMENT INFORMATION



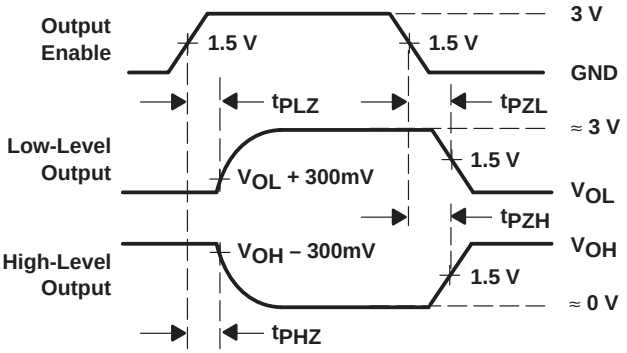

LOAD CIRCUIT



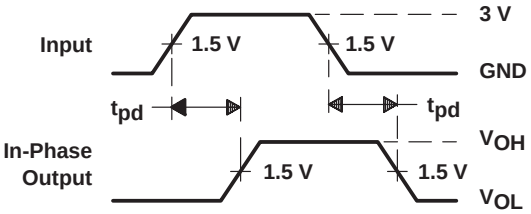

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. Includes probe and jig capacitance
B. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
C. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

| CONDITIONS FOR LOAD CIRCUIT | | | | |
|---|---|---|---|---|
| PARAMETER | $I_{OL}$ | $I_{OH}$ | $V_{Load}$ | $C_L$† (typical) |
| $t_{PZH}$ | 4 mA | 8 mA | 0 V | 20 pF |
| $t_{PZL}$ | 4 mA | 8 mA | 3 V | 20 pF |
| $t_{PHZ}$ | 4 mA | 8 mA | 0 V | 20 pF |
| $t_{PLZ}$ | 4 mA | 8 mA | 3 V | 20 pF |
| $t_{PD}$ | 8 mA | 4 mA | 1.5 V | 20 pF |

† Includes probe and test-fixture capacitance

**Figure 16. Load Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

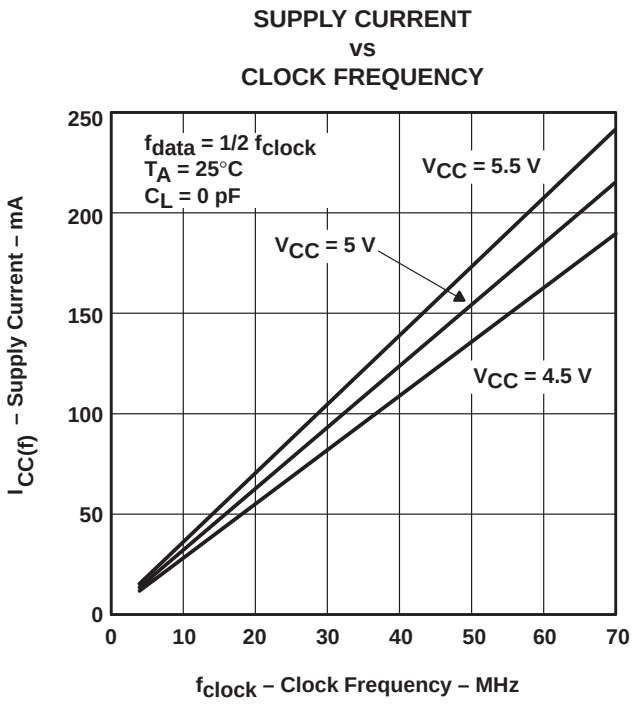



**Figure 17**

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